SDAS212A - DECEMBER 1983 - REVISED DECEMBER 1994

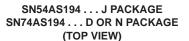
- Parallel-to-Serial, Serial-to-Parallel Conversions
- Left or Right Shifts
- Parallel Synchronous Loading
- Direct Overriding Clear
- Temporary Data-Latching Capability
- Package Options Include Plastic Small-Outline Packages (D), Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

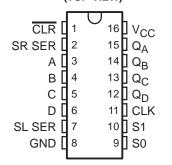
description

These 4-bit bidirectional universal shift registers feature parallel outputs, right-shift and left-shift serial (SR SER, SL SER) inputs, operating-mode-control (S0, S1) inputs, and a direct overriding clear (CLR) line. The registers have four distinct modes of operation:

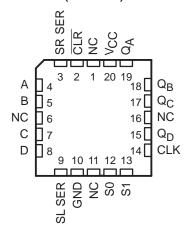
- Inhibit clock (temporary data latch/do nothing)
- Shift right (in the direction Q_A toward Q_D)
- Shift left (in the direction Q_D toward Q_A)
- Parallel (broadside) load

Parallel synchronous loading is accomplished by applying the four bits of data and taking both S0 and S1 high. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock (CLK) input. During loading, serial data flow is inhibited.





SN54AS194 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode-control inputs are low.

The SN54AS194 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AS194 is characterized for operation from 0°C to 70°C.

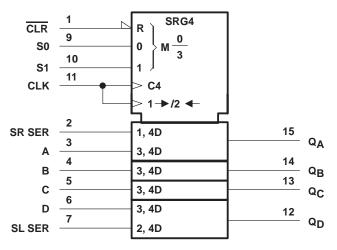
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FUNCTION TABLE

	INPUTS										OUTPUTS				
	MODE		01.17	SE	RIAL		PARA	LLEL			_	_	_		
CLR	S1	S0	CLK	LEFT	RIGHT	Α	В	С	D	Q_{A}	Q_{B}	σC	Q_D		
L	Х	Х	Χ	Х	Х	Х	Х	Х	Χ	L	L	L	L		
Н	Х	X	L	Х	Χ	Х	X	X	Χ	Q _{A0}	Q_{B0}	Q_{C0}	Q_{D0}		
Н	Н	Н	↑	Х	Χ	а	b	С	d	а	b	С	d		
Н	L	Н	↑	Х	Н	Х	X	X	Χ	Н	Q_{An}	Q_{Bn}	Q _{Cn}		
Н	L	Н	↑	Х	L	Х	X	X	Χ	L	Q_{An}	Q_{Bn}	Q_{Cn}		
Н	Н	L	↑	Н	Χ	Х	X	Χ	Χ	Q _{Bn}	Q_{Cn}	Q_{Dn}	Н		
Н	Н	L	↑	L	Х	Х	Χ	Χ	Χ	Q _{Bn}	Q_{Cn}	Q_{Dn}	L		
Н	L	L	Χ	Х	Χ	Х	X	Χ	Χ	Q _{A0}	Q_{B0}	Q_{C0}	Q_{D0}		

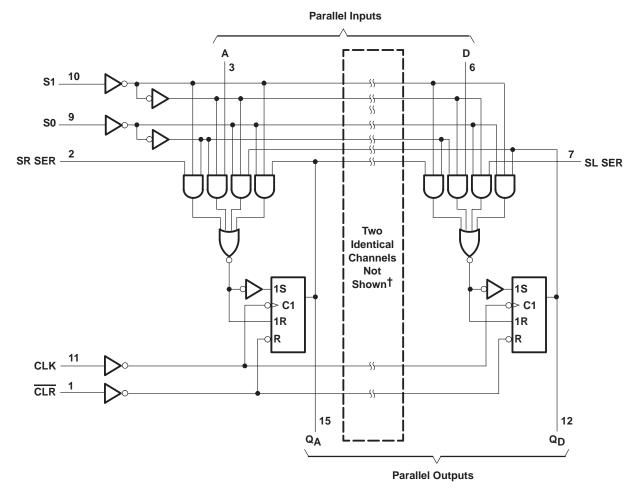
 $H=\text{high level (steady state)}; \ L=\text{low level (steady state)}; \ X=\text{irrelevant (any input, including transitions)}; \ \uparrow=\text{transition from low to high level}; \ a, b, c, d=\text{the level of steady-state input at inputs A, B, C, or D, respectively; } Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}=\text{the level of } Q_A, Q_B, Q_C, \text{ or } Q_D, \text{ respectively, before the indicated steady-state input conditions were established; } Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}=\text{the level of } Q_A, Q_B, Q_C, \text{ respectively, before the most recent } \uparrow \text{ transition of the clock.}$

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



 \dagger I/O ports not shown: QB (14) and QC (13) Pin numbers shown are for the D, J, and N packages.

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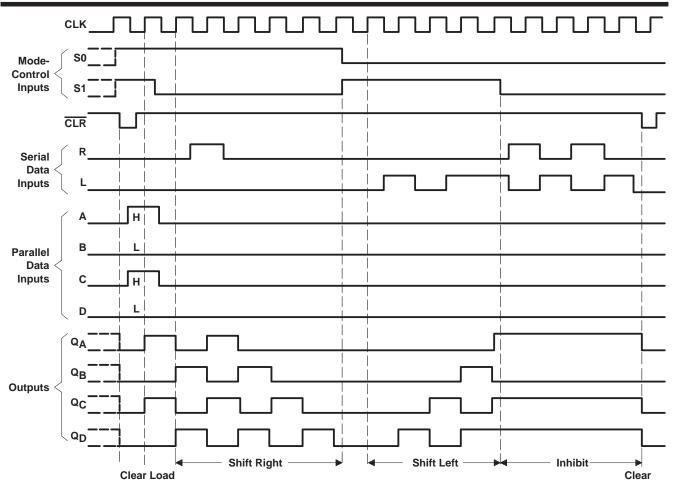


Figure 1. Typical Clear, Load, Right-Shift, and Clear Sequences

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC}		7 V
Input voltage, V _I		7 V
Operating free-air temperature range, TA: SN54AS194	·	-55°C to 125°C
SN74AS194	1	0°C to 70°C
Storage temperature range		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SI	N54AS19)4	SN74AS194			LINUT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			8.0	V
lOH	High-level output current				-2			-2	mA
l _{OL}	Low-level output current				20			20	mA
fclock*	Clock frequency		0		75	0		80	MHz
		CLR	4			4.5			
tw*	Pulse duration	CLK high	4			4			ns
		CLK low	6			7			
		Select	9			9.5			
t _{su} *	Setup time before CLK↑	Data	3.5			4			ns
		Clear inactive state	6			6			
th*	Hold time, data after CLK↑		0.5			0.5			ns
TA	Operating free-air temperature		-55		125	0		70	°C

^{*} On products compliant to MIL-STD-883, Class B, these parameters are based on characterization data, but are not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEOT 0011	DITIONS	SI	N54AS19)4	SN	174AS19	4		
	PARAMETER	TEST CON	TEST CONDITIONS			MAX	MIN	TYP†	MAX	UNIT	
٧ıK		V _{CC} = 4.5 V,	$I_{I} = -18 \text{ mA}$			-1.2			-1.2	V	
VOH		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2			V _{CC} -2			V	
VOL		$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 20 \text{ mA}$		0.35	0.5		0.35	0.5	V	
	Data, CLK, CLR	V 55V	7./			0.1			0.1	4	
I _I	Mode, SL, SR	$V_{CC} = 5.5 \text{ V},$	$V_I = 7 V$			0.2			0.2	mA	
	Data, CLK, CLR		V 07V			20			20		
ΊΗ	Mode, SL, SR	$V_{CC} = 5.5 \text{ V},$	$V_{ } = 2.7 \text{ V}$	40			40		μΑ		
	Data, CLK, CLR	V 55V				-0.5			-0.5	•	
ΊL	Mode, SL, SR	$V_{CC} = 5.5 \text{ V},$	$V_{I} = 0.4 V$	-1				-1	mA		
IO [‡]		V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	-30		-112	mA	
la a		Vac 55V	Outputs high		30	49		30	43	A	
ICC		V _{CC} = 5.5 V	Outputs low		38	60		38	53	53 mA	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54AS194, SN74AS194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

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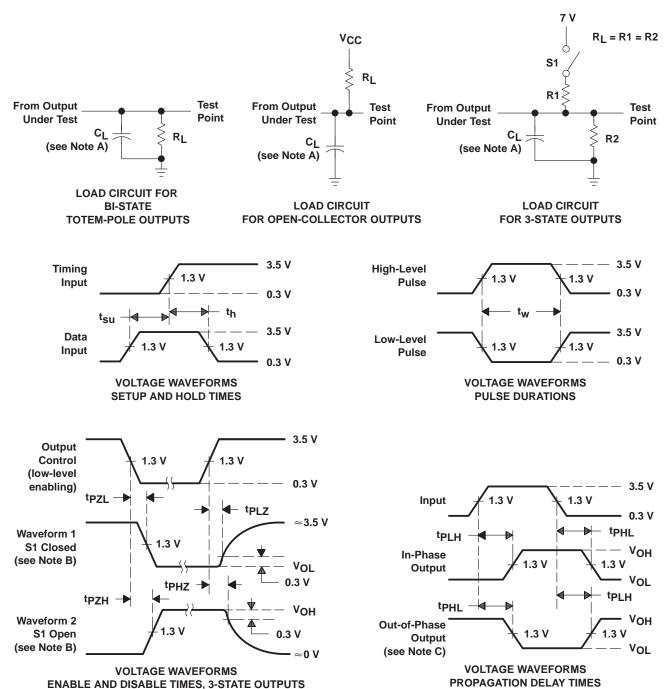
switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _C C _L R _L T _A	V,	UNIT		
	, ,	(22 2)	SN54A	\S194	SN74AS194		
			MIN	MAX	MIN	MAX	
fmax*			75		80		MHz
^t PLH	CLIK	A O	2.5	8	3	7	
t _{PHL}	CLK	Any Q	2.5	8	3	7	ns
^t PHL	CLR	Any Q	3.5	13	4	12	ns

^{*} On products compliant to MIL-STD-883, Class B, these parameters are based on characterization data, but are not production tested.

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, $t_f = t_f = 2$ ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms





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PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AS194D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	AS194	
SN74AS194DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS194	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

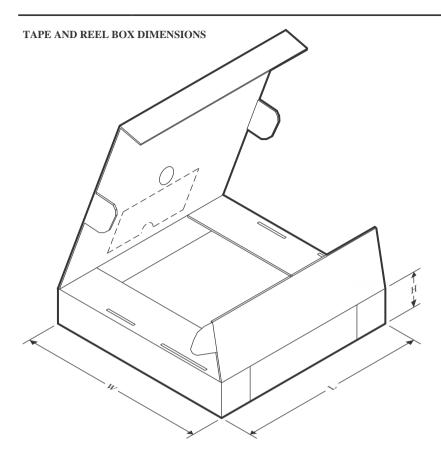
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AS194DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

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*All dimensions are nominal

Ì	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ı	SN74AS194DR	SOIC	D	16	2500	340.5	336.1	32.0

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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