SN74AVC4T774-Q1 Automotive 4-Bit Dual-Supply Bus Transceiver With Configurable Voltage-Level Shifting and 3-State Outputs With Independent Direction Control Inputs

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level H3B (JES-001)
  - Device CDM ESD classification level C5 (JESD 22 C101)
- Function safety capable
- Control input V_{IH} and V_{IL} levels are referenced to V_{CCA} voltage
- Fully configurable dual-rail design allows each port to operate over the full 1.08V to 3.6V power-supply range
- I/Os are 4.6V tolerant
- I_{off} supports partial power-down-mode operation
- Maximum data rates:
  - 500Mbps (1.08V to 3.6V translation)
- Latch-up performance exceeds 100mA per JESD 78, Class II

2 Applications

- Telematics
- Cluster
- Head unit
- Navigation systems

3 Description

This 4-bit non-inverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.08V to 3.6V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.08V to 3.6V. This allows for universal low-voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The SN74AVC4T774-Q1 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The SN74AVC4T774-Q1 is designed so that the control pins (DIR1, DIR2, DIR3, DIR4 and $\overline{OE}$) are supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

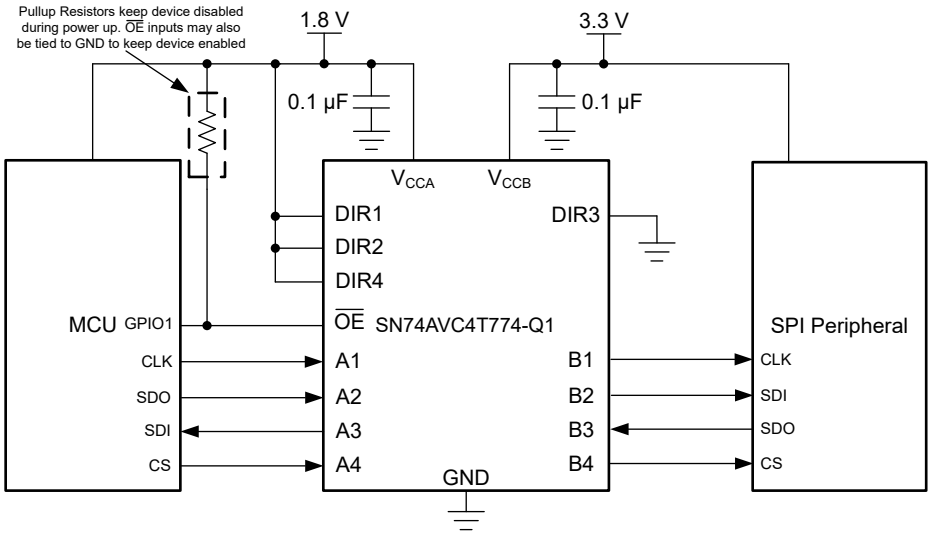
The design of the V_{CC} isolation feature places both ports in the high-impedance state if either V_{CC} input is at GND.

To place the device in the high-impedance state during power up or power down, tie $\overline{OE}$ to V_{CC} through a pullup resistor; the current-sinking capability of the driver determines the minimum value of the resistor.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN74AVC4T774-Q1	PW (TSSOP, 16)	5mm × 6.4mm
	BQB (WQFN, 16)	3.5mm × 2.5mm
	DYY (SOT, 16)	4.2mm × 2mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic SN74AVC4T774-Q1

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4 Pin Configuration and Functions

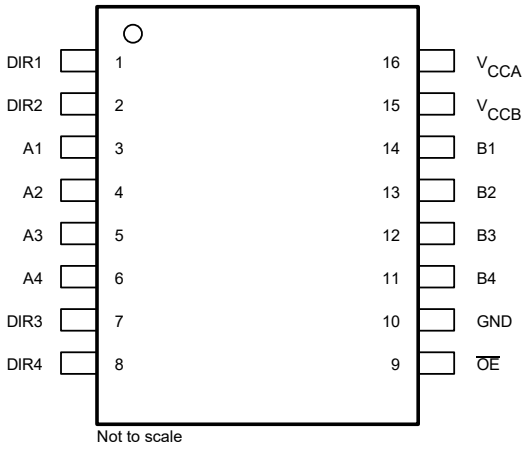


Figure 4-1. PW Package, 16-Pin TSSOP (Top View)

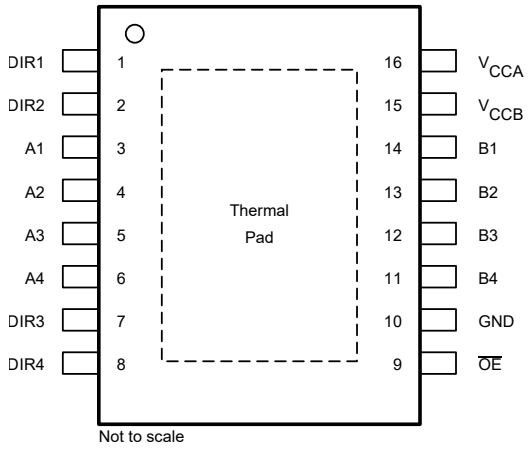


Figure 4-2. DYY Package, 16-Pin SOT (Top View)

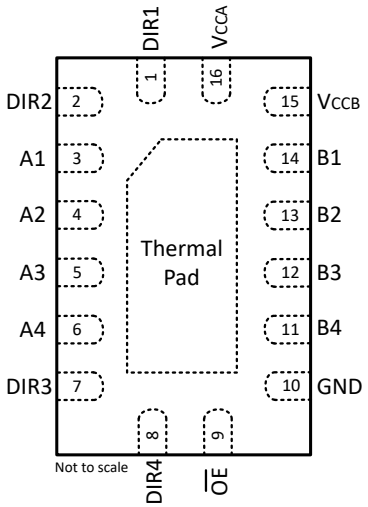


Figure 4-3. BQB Package, 16-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DIR1	1	I	Controls signal flow for the first (A1/B1) I/O channels. Direction-control input referenced to V_{CCA}
DIR2	2	I	Controls signal flow for the second (A2/B2) I/O channels. Direction-control input referenced to V_{CCA}
A1	3	I/O	Input/output A1. Referenced to V_{CCA}
A2	4	I/O	Input/output A2. Referenced to V_{CCA}.
A3	5	I/O	Input/output A3. Referenced to V_{CCA}.
A4	6	I/O	Input/output A4. Referenced to V_{CCA}.
DIR3	7	I	Controls signal flow for the third (A3/B3) I/O channels. Direction-control input referenced to V_{CCA}
DIR4	8	I	Controls signal flow for the fourth (A4/B4) I/O channels. Direction-control input referenced to V_{CCA}
$\overline{OE}$	9	I	3-state output-mode enables. Pull $\overline{OE}$ high to place all outputs in 3-state mode. Referenced to V_{CCA}.
GND	10	G	Ground
B4	11	I/O	Input/output B4. Referenced to V_{CCB}.
B3	12	I/O	Input/output B3. Referenced to V_{CCB}.
B2	13	I/O	Input/output B2. Referenced to V_{CCB}.
B1	14	I/O	Input/output B1. Referenced to V_{CCB}.
V_{CCB}	15	P	B-port supply voltage. 1.08V ≤ V_{CCB} ≤ 3.6V
V_{CCA}	16	P	A-port supply voltage. 1.08V ≤ V_{CCA} ≤ 3.6V
Thermal pad		—	The exposed thermal pad must be connected as a secondary GND or be left electrically open.

(1) I = input, O = output, P = Power, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±1000	
		Machine model (C101)	±150	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.08	3.6	V
V_{CCB}	Supply voltage				1.08	3.6	V
V_{IH}	High-level input voltage	Data inputs(1)	1.08V		V_{CCI} × 0.7		V
			1.2V to 1.95V		V_{CCI} × 0.65		
			2V to 2.7V		1		
			2.8V to 3.6V		1.4		
V_{IL}	Low-level input voltage	Data inputs(1)	1.08V			V_{CCI} × 0.3	V
			1.1V to 1.95V			V_{CCI} × 0.35	
			2V to 2.7V			1.5	
			3V to 3.6V			1.9	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})(2)	1.08V to 1.95V		V_{CCA} × 0.65		V
			2V to 2.7V		1		
			3V to 3.6V		1.3		

5.3 Recommended Operating Conditions (continued)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})(2)	1.08V to 1.95V			V_{CCA} × 0.35	V
			2V to 2.7V			1.3	
			3V to 3.6V			1.7	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.08V to 1.32V		–3	mA
				1.4V to 1.6V		–6	
				1.65V to 1.95V		–8	
				2.3V to 2.7V		–9	
				3V to 3.6V		–12	
I_{OL}	Low-level output current			1.08V to 1.32V		3	mA
				1.4V to 1.6V		6	
				1.65V to 1.95V		8	
				2.3V to 2.7V		9	
				3V to 3.6V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating ambient temperature				–40	125	°C

(1) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7V, V_{IL} max = V_{CCI} × 0.3V
(2) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7V, V_{IL} max = V_{CCA} × 0.3V

5.4 Thermal Information

THERMAL METRIC(1)		SN74AVC4T774-Q1			UNIT
		PW (TSSOP)	BQB (WQFN)	DYY (SOT)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123.8	79.9	163.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.3	77.5	90.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81.7	49.0	93.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.7	7.3	10.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.9	49.0	92.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	26.4	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 125°C (unless otherwise noted).(1) (2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –100µA; V_{CCA} = 1.08V to 3.6V; V_{CCB} = 1.08V to 3.6V; V_I = V_{IH}	V_{CCO} – 0.2			V
	I_{OH} = –3mA; V_{CCA} = 1.1V; V_{CCB} = 1.1V; V_I = V_{IH}	0.8			
	I_{OH} = –6mA; V_{CCA} = 1.4V; V_{CCB} = 1.4V; V_I = V_{IH}	1			
	I_{OH} = –8mA; V_{CCA} = 1.65V; V_{CCB} = 1.65V; V_I = V_{IH}	1.2			
	I_{OH} = –9mA; V_{CCA} = 2.3V; V_{CCB} = 2.3V; V_I = V_{IH}	1.8			
	I_{OH} = –12mA; V_{CCA} = 3V; V_{CCB} = 3V; V_I = V_{IH}	2.3			

5.5 Electrical Characteristics (continued)

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 125°C (unless otherwise noted).(1) (2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL}		I_{OL} = 100µA; V_{CCA} = 1.08V to 3.6V; V_{CCB} = 1.08V to 3.6V; $V_I = V_{IL}$				0.2	V
		I_{OL} = 3mA; V_{CCA} = 1.1V; V_{CCB} = 1.1V; $V_I = V_{IL}$				0.2	
		I_{OL} = 6mA; V_{CCA} = 1.4V; V_{CCB} = 1.4V; $V_I = V_{IL}$				0.31	
		I_{OL} = 8mA; V_{CCA} = 1.65V; V_{CCB} = 1.65V; $V_I = V_{IL}$				0.35	
		I_{OL} = 9mA; V_{CCA} = 2.3V; V_{CCB} = 2.3V; $V_I = V_{IL}$				0.33	
		I_{OL} = 12mA; V_{CCA} = 3V; V_{CCB} = 3V; $V_I = V_{IL}$				0.40	
I_I	DIR input	$V_I = V_{CCA}$ or GND; V_{CCA} = 1.08V to 3.6V; V_{CCB} = 1.08V to 3.6V	T_A = 25°C	-0.25		0.25	µA
			T_A = –40°C to 125°C	-1		1.5	
I_{off}	A port	V_I or V_O = 0 to 3.6V; V_{CCA} = 0V; V_{CCB} = 0V to 3.6V	T_A = 25°C		±0.1	±1	µA
			T_A = –40°C to 125°C			±5	
	B port	V_I or V_O = 0 to 3.6V; V_{CCA} = 0V to 3.6V; V_{CCB} = 0V	T_A = 25°C		±0.1	±1	
			T_A = –40°C to 125°C			±5	
I_{OZ} (3)	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND; $\overline{OE} = V_{IH}$; V_{CCA} = 3.6V; V_{CCB} = 3.6V	T_A = 25°C		±0.5	±2.5	µA
			T_A = –40°C to 125°C			±5	
	B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND; $\overline{OE}$ = don't care; V_{CCA} = 0V; V_{CCB} = 3.6V				±5	
	A port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND; $\overline{OE}$ = don't care; V_{CCA} = 3.6V; V_{CCB} = 0V				±5	
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0	V_{CCA} = 1.08V to 3.6V V_{CCB} = 1.08V to 3.6V			9	µA
			V_{CCA} = 0V; V_{CCB} = 3.6V			–2	
			V_{CCA} = 3.6V; V_{CCB} = 0V			5	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0	V_{CCA} = 1.08V to 3.6V V_{CCB} = 1.08V to 3.6V			7	µA
			V_{CCA} = 0V; V_{CCB} = 3.6V			4.5	
			V_{CCA} = 3.6V; V_{CCB} = 0V			–2	
I_{CCA} + I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0; V_{CCA} = 1.08V to 3.6V; V_{CCB} = 1.08V to 3.6V				16	µA
C_i	Control inputs	V_I = 3.3V or GND; V_{CCA} = 3.3V; V_{CCB} = 3.3V				4.5	pF
C_{io}	A or B port	V_O = 3.3V or GND; V_{CCA} = 3.3V; V_{CCB} = 3.3V				5.1	pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

5.6 Switching Characteristics: VCCA = 1.2V ± 0.12V

over recommended operating free-air temperature range (for parameter descriptions, see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	TYP	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2V ± 0.12V	3.1	ns
			V_{CCB} = 1.5V ± 0.1V	2.6	
			V_{CCB} = 1.8V ± 0.15V	2.5	
			V_{CCB} = 2.5V ± 0.2V3	3	
			V_{CCB} = 3.3V ± 0.3V	3.5	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2V ± 0.12V	3.1	ns
			V_{CCB} = 1.5V ± 0.1V	2.7	
			V_{CCB} = 1.8V ± 0.15V	2.5	
			V_{CCB} = 2.5V ± 0.2V	2.4	
			V_{CCB} = 3.3V ± 0.3V	2.3	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2V ± 0.12V	5.3	ns
			V_{CCB} = 1.5V ± 0.1V	5.3	
			V_{CCB} = 1.8V ± 0.15V	5.3	
			V_{CCB} = 2.5V ± 0.2V	5.3	
			V_{CCB} = 3.3V ± 0.3V	5.3	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V ± 0.12V	5.1	ns
			V_{CCB} = 1.5V ± 0.1V	4	
			V_{CCB} = 1.8V ± 0.15V	3.5	
			V_{CCB} = 2.5V ± 0.2V	3.2	
			V_{CCB} = 3.3V ± 0.3V	3.1	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2V ± 0.12V	4.8	ns
			V_{CCB} = 1.5V ± 0.1V	4.8	
			V_{CCB} = 1.8V ± 0.15V	4.8	
			V_{CCB} = 2.5V ± 0.2V	4.8	
			V_{CCB} = 3.3V ± 0.3V	4.8	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2V ± 0.12V	4.7	ns
			V_{CCB} = 1.5V ± 0.1V	4	
			V_{CCB} = 1.8V ± 0.15V	4.1	
			V_{CCB} = 2.5V ± 0.2V	4.3	
			V_{CCB} = 3.3V ± 0.3V	5.1	

5.7 Switching Characteristics, V_{CCA} = 1.5V ± 0.1V

over temperature range -40 °C to +125 °C (for parameter descriptions, see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PHL}, t_{PLH}	A	B	V_{CCB} = 1.2V ± 0.12V		4.2		ns
			V_{CCB} = 1.5V ± 0.1V	2.2		5.7	
			V_{CCB} = 1.8V ± 0.15V	2.0		4.7	
			V_{CCB} = 2.5V ± 0.2V	1.7		3.8	
			V_{CCB} = 3.3V ± 0.3V	1.5		3.4	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2V ± 0.12V		4.6		ns
			V_{CCB} = 1.5V ± 0.1V	2.1		5.7	
			V_{CCB} = 1.8V ± 0.15V	1.9		5.1	
			V_{CCB} = 2.5V ± 0.2V	1.7		4.2	
			V_{CCB} = 3.3V ± 0.3V	1.6		3.8	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2V ± 0.12V		5.8		ns
			V_{CCB} = 1.5V ± 0.1V	3.8		10.6	
			V_{CCB} = 1.8V ± 0.15V	3.8		10.7	
			V_{CCB} = 2.5V ± 0.2V	3.7		10.6	
			V_{CCB} = 3.3V ± 0.3V	3.7		10.5	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V ± 0.12V		8.7		ns
			V_{CCB} = 1.5V ± 0.1V	3.9		10.8	
			V_{CCB} = 1.8V ± 0.15V	3.5		9.5	
			V_{CCB} = 2.5V ± 0.2V	3.2		8.3	
			V_{CCB} = 3.3V ± 0.3V	3.1		8.0	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2V ± 0.12V		5.6		ns
			V_{CCB} = 1.5V ± 0.1V	3.9		9.4	
			V_{CCB} = 1.8V ± 0.15V	3.9		9.4	
			V_{CCB} = 2.5V ± 0.2V	3.9		9.4	
			V_{CCB} = 3.3V ± 0.3V	3.9		9.4	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2V ± 0.12V		8.6		ns
			V_{CCB} = 1.5V ± 0.1V	4.6		11.0	
			V_{CCB} = 1.8V ± 0.15V	4.6		10.6	
			V_{CCB} = 2.5V ± 0.2V	3.7		8.9	
			V_{CCB} = 3.3V ± 0.3V	4.2		9.4	

5.8 Switching Characteristics: V_{CCA} = 1.8V ± 0.15V

over temperature range -40 °C to +125 °C (for parameter descriptions, see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2V ± 0.12V		3.8		ns
			V_{CCB} = 1.5V ± 0.1V	2.1		5.1	
			V_{CCB} = 1.8V ± 0.15V	2.0		4.2	
			V_{CCB} = 2.5V ± 0.2V	1.6		3.1	
			V_{CCB} = 3.3V ± 0.3V	1.4		2.9	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2V ± 0.12V		4.2		ns
			V_{CCB} = 1.5V ± 0.1V	2.2		4.7	
			V_{CCB} = 1.8V ± 0.15V	2.0		4.2	
			V_{CCB} = 2.5V ± 0.2V	1.8		3.7	
			V_{CCB} = 3.3V ± 0.3V	1.7		3.3	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2V ± 0.12V		4.5		ns
			V_{CCB} = 1.5V ± 0.1V	3.4		7.7	
			V_{CCB} = 1.8V ± 0.15V	3.4		7.7	
			V_{CCB} = 2.5V ± 0.2V	3.3		7.7	
			V_{CCB} = 3.3V ± 0.3V	3.4		7.6	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V ± 0.12V		8.0		ns
			V_{CCB} = 1.5V ± 0.1V	3.9		9.1	
			V_{CCB} = 1.8V ± 0.15V	3.4		7.9	
			V_{CCB} = 2.5V ± 0.2V	3.0		6.6	
			V_{CCB} = 3.3V ± 0.3V	2.9		6.2	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2V ± 0.12V		5.3		ns
			V_{CCB} = 1.5V ± 0.1V	4.1		7.9	
			V_{CCB} = 1.8V ± 0.15V	4.1		8.0	
			V_{CCB} = 2.5V ± 0.2V	4.1		8.0	
			V_{CCB} = 3.3V ± 0.3V	4.1		8.0	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2V ± 0.12V		7.7		ns
			V_{CCB} = 1.5V ± 0.1V	4.5		9.4	
			V_{CCB} = 1.8V ± 0.15V	4.6		9.1	
			V_{CCB} = 2.5V ± 0.2V	3.9		7.6	
			V_{CCB} = 3.3V ± 0.3V	4.3		8.1	

Switching Characteristics, VCCA = 2.5V ± 0.2V

5.9 Switching Characteristics: V_{CCA} = 2.5V ± 0.2V

over temperature range -40 °C to +125 °C (for parameter descriptions, see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2V ± 0.12V		3.3		ns
			V_{CCB} = 1.5V ± 0.1V	1.9		4.2	
			V_{CCB} = 1.8V ± 0.15V	1.8		3.7	
			V_{CCB} = 2.5V ± 0.2V	1.5		2.6	
			V_{CCB} = 3.3V ± 0.3V	1.3		2.3	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2V ± 0.12V		3.6		ns
			V_{CCB} = 1.5V ± 0.1V	1.8		3.8	
			V_{CCB} = 1.8V ± 0.15V	1.6		3.1	
			V_{CCB} = 2.5V ± 0.2V	1.5		2.6	
			V_{CCB} = 3.3V ± 0.3V	1.5		2.5	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2V ± 0.12V		3.0		ns
			V_{CCB} = 1.5V ± 0.1V	2.5		4.8	
			V_{CCB} = 1.8V ± 0.15V	2.5		4.8	
			V_{CCB} = 2.5V ± 0.2V	2.5		4.8	
			V_{CCB} = 3.3V ± 0.3V	2.5		4.8	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V ± 0.12V		7.0		ns
			V_{CCB} = 1.5V ± 0.1V	3.5		7.4	
			V_{CCB} = 1.8V ± 0.15V	3.1		6.1	
			V_{CCB} = 2.5V ± 0.2V	2.6		4.9	
			V_{CCB} = 3.3V ± 0.3V	2.4		4.4	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2V ± 0.12V		3.7		ns
			V_{CCB} = 1.5V ± 0.1V	3.1		5.3	
			V_{CCB} = 1.8V ± 0.15V	3.2		5.4	
			V_{CCB} = 2.5V ± 0.2V	3.1		5.4	
			V_{CCB} = 3.3V ± 0.3V	3.1		5.4	
t_{PHZ}	$\overline{OE}$	B	V_{CCB} = 1.2V ± 0.12V		4.5		ns
			V_{CCB} = 1.5V ± 0.1V	1.5		9.4	
			V_{CCB} = 1.8V ± 0.15V	1.3		8.2	
			V_{CCB} = 2.5V ± 0.2V	1.1		6.2	
			V_{CCB} = 3.3V ± 0.3V	0.9		5.2	
t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2V ± 0.12V		6.6		ns
			V_{CCB} = 1.5V ± 0.1V	4.1		7.4	
			V_{CCB} = 1.8V ± 0.15V	4.2		7.3	
			V_{CCB} = 2.5V ± 0.2V	3.5		6.0	
			V_{CCB} = 3.3V ± 0.3V	4.0		6.6	

5.10 Switching Characteristics: V_{CCA} = 3.3V ± 0.3V

over temperature range -40 °C to +125 °C (for parameter descriptions, see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2V ± 0.12V		3.2		ns
			V_{CCB} = 1.5V ± 0.1V	1.8		3.8	
			V_{CCB} = 1.8V ± 0.15V	1.7		3.3	
			V_{CCB} = 2.5V ± 0.2V	1.5		2.5	
			V_{CCB} = 3.3V ± 0.3V	1.2		2.0	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2V ± 0.12V		3.4		ns
			V_{CCB} = 1.5V ± 0.1V	1.7		3.4	
			V_{CCB} = 1.8V ± 0.15V	1.5		2.9	
			V_{CCB} = 2.5V ± 0.2V	1.3		2.9	
			V_{CCB} = 3.3V ± 0.3V	1.2		2.0	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2V ± 0.12V		2.4		ns
			V_{CCB} = 1.5V ± 0.1V	2.2		3.6	
			V_{CCB} = 1.8V ± 0.15V	2.2		3.6	
			V_{CCB} = 2.5V ± 0.2V	2.2		3.6	
			V_{CCB} = 3.3V ± 0.3V	2.2		3.6	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V ± 0.12V		6.7		ns
			V_{CCB} = 1.5V ± 0.1V	3.2		6.7	
			V_{CCB} = 1.8V ± 0.15V	2.8		5.4	
			V_{CCB} = 2.5V ± 0.2V	2.4		4.2	
			V_{CCB} = 3.3V ± 0.3V	2.2		3.7	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2V ± 0.12V		4.0		ns
			V_{CCB} = 1.5V ± 0.1V	3.5		5.5	
			V_{CCB} = 1.8V ± 0.15V	3.5		5.5	
			V_{CCB} = 2.5V ± 0.2V	3.4		5.4	
			V_{CCB} = 3.3V ± 0.3V	3.5		5.4	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2V ± 0.12V		6.3		ns
			V_{CCB} = 1.5V ± 0.1V	4.0		6.6	
			V_{CCB} = 1.8V ± 0.15V	4.0		6.5	
			V_{CCB} = 2.5V ± 0.2V	3.3		5.3	
			V_{CCB} = 3.3V ± 0.3V	3.7		5.9	

5.11 Operating Characteristics

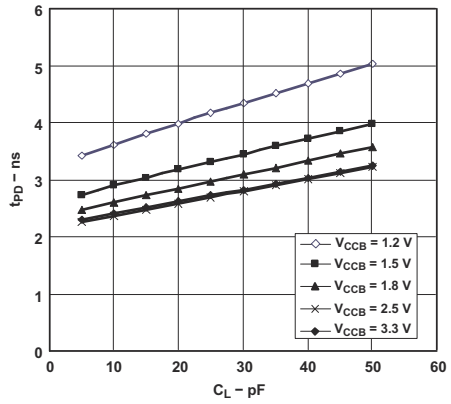
T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCA}	TYP	UNIT
C_{pdA} (1)	A to B	Outputs enabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	1	pF
				$V_{CCA} = V_{CCB}$ = 1.5V	1	
				$V_{CCA} = V_{CCB}$ = 1.8V	1	
				$V_{CCA} = V_{CCB}$ = 2.5V	1.5	
				$V_{CCA} = V_{CCB}$ = 3.3V	2	
		Outputs disabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	1	
				$V_{CCA} = V_{CCB}$ = 1.5V		
				$V_{CCA} = V_{CCB}$ = 1.8V		
				$V_{CCA} = V_{CCB}$ = 2.5V		
				$V_{CCA} = V_{CCB}$ = 3.3V		
	B to A	Outputs enabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	12	
				$V_{CCA} = V_{CCB}$ = 1.5V	12.5	
				$V_{CCA} = V_{CCB}$ = 1.8V	13	
				$V_{CCA} = V_{CCB}$ = 2.5V	14	
				$V_{CCA} = V_{CCB}$ = 3.3V	15	
		Outputs disabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	1	
				$V_{CCA} = V_{CCB}$ = 1.5V		
				$V_{CCA} = V_{CCB}$ = 1.8V		
				$V_{CCA} = V_{CCB}$ = 2.5V		
				$V_{CCA} = V_{CCB}$ = 3.3V		
C_{pdB} (1)	A to B	Outputs enabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	12	pF
				$V_{CCA} = V_{CCB}$ = 1.5V	12.5	
				$V_{CCA} = V_{CCB}$ = 1.8V	13	
				$V_{CCA} = V_{CCB}$ = 2.5V	14	
				$V_{CCA} = V_{CCB}$ = 3.3V	15	
		Outputs disabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	1	
				$V_{CCA} = V_{CCB}$ = 1.5V		
				$V_{CCA} = V_{CCB}$ = 1.8V		
				$V_{CCA} = V_{CCB}$ = 2.5V		
				$V_{CCA} = V_{CCB}$ = 3.3V		
	B to A	Outputs enabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	1	
				$V_{CCA} = V_{CCB}$ = 1.5V	1	
				$V_{CCA} = V_{CCB}$ = 1.8V	1	
				$V_{CCA} = V_{CCB}$ = 2.5V	1	
				$V_{CCA} = V_{CCB}$ = 3.3V	2	
		Outputs disabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	1	
				$V_{CCA} = V_{CCB}$ = 1.5V		
				$V_{CCA} = V_{CCB}$ = 1.8V		
				$V_{CCA} = V_{CCB}$ = 2.5V		
				$V_{CCA} = V_{CCB}$ = 3.3V		

(1) Power dissipation capacitance per transceiver

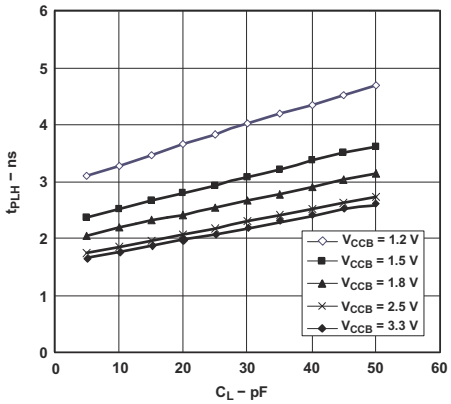
5.12 Typical Characteristics

T_A = 25°C



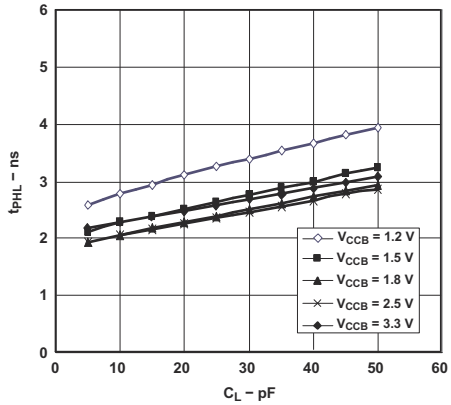
V_{CCA} = 1.2V

Figure 5-1. Typical Propagation Delay (A to B) vs Load Capacitance



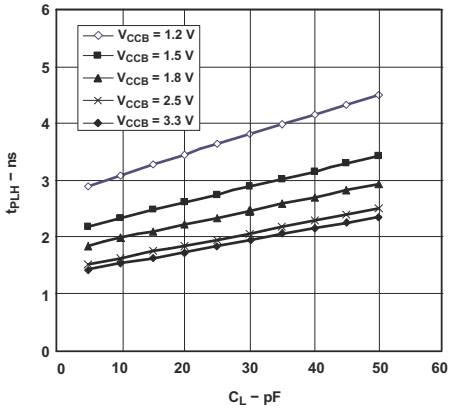
V_{CCA} = 1.5V

Figure 5-2. Typical Propagation Delay (A to B) vs Load Capacitance



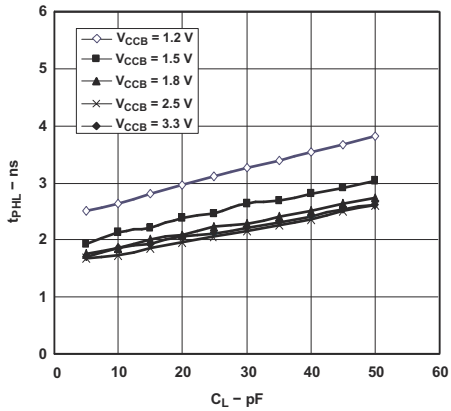
V_{CCA} = 1.5V

Figure 5-3. Typical Propagation Delay (A to B) vs Load Capacitance



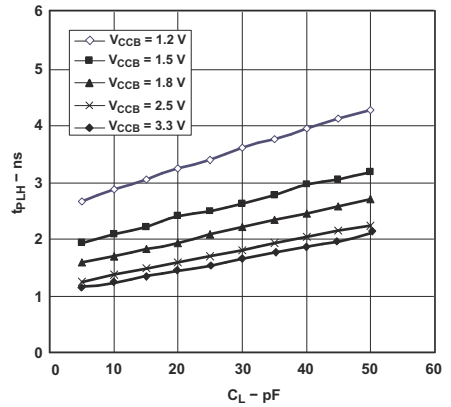
V_{CCA} = 1.8V

Figure 5-4. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 1.8V

Figure 5-5. Typical Propagation Delay (A to B) vs Load Capacitance

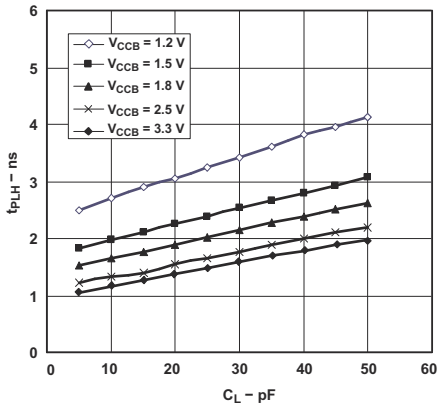


V_{CCA} = 2.5V

Figure 5-6. Typical Propagation Delay (A to B) vs Load Capacitance

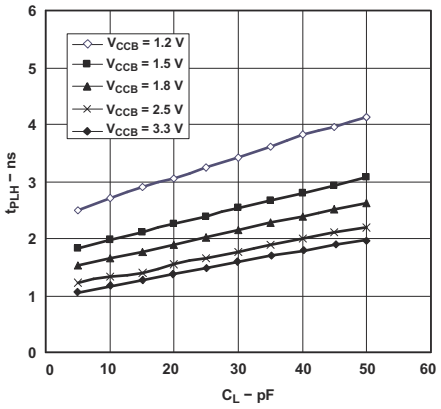
5.12 Typical Characteristics (continued)

T_A = 25°C



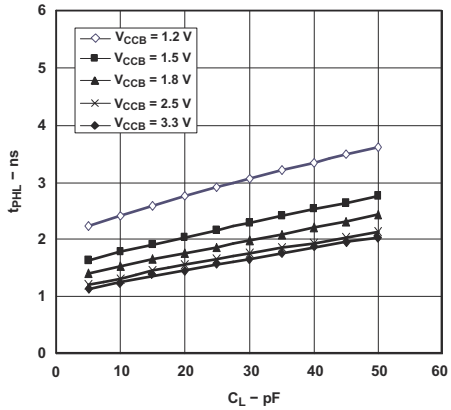
V_{CCA} = 2.5V

Figure 5-7. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 3.3V

Figure 5-8. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 3.3V

Figure 5-9. Typical Propagation Delay (A to B) vs Load Capacitance

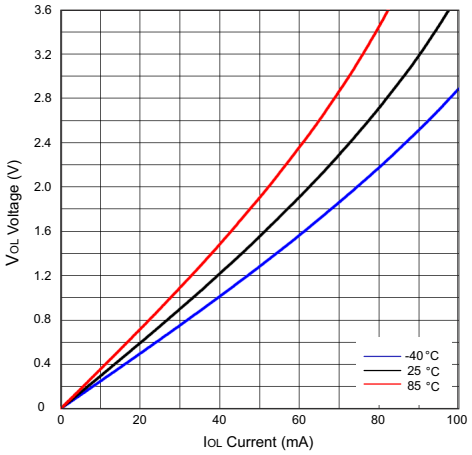


Figure 5-10. Low-Level Output Voltage (V_{OL}) vs Low-Level Current (I_{OL})

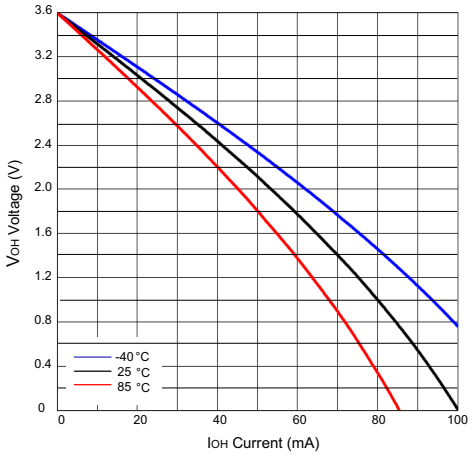
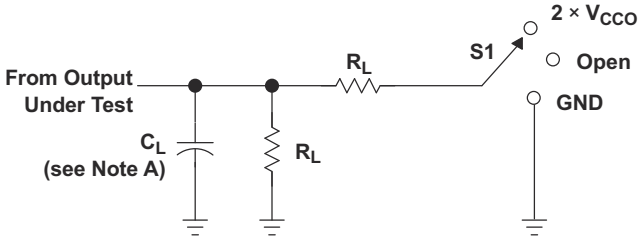


Figure 5-11. High-Level Output Voltage (V_{OH}) vs High-Level Current (I_{OH})

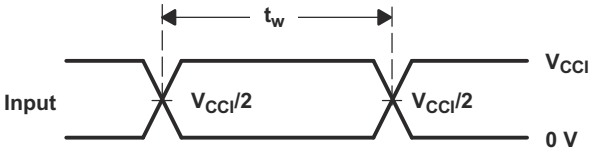
6 Parameter Measurement Information



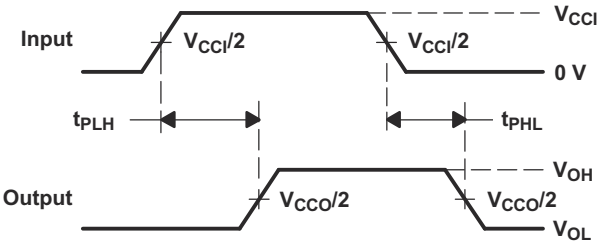
LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CCO} GND

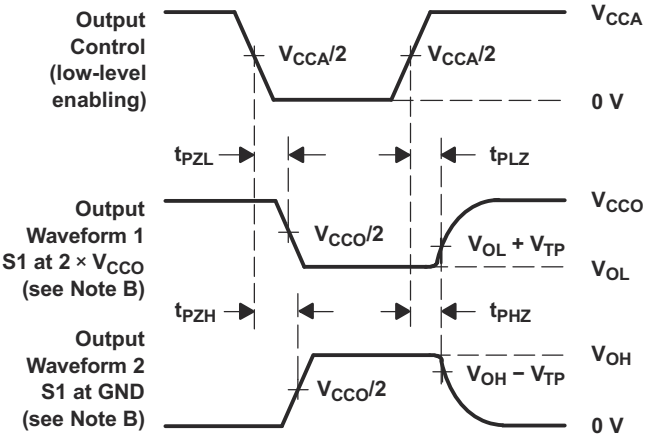
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

Figure 6-1. Load and Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74AVC4T774-Q1 is a 4-bit, dual-supply noninverting bidirectional voltage level translation device. Ax pins and control pins (DIR1, DIR2, DIR3, DIR4 and $\overline{OE}$) are supported by V_{CCA}, and Bx pins are supported by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.08V to 3.6V, while the B port can accept I/O voltages from 1.08V to 3.6V. A high on DIR allows data transmission from Ax to Bx and a low on DIR allows data transmission from Bx to Ax when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both Ax and Bx pins are in the high-impedance state.

7.2 Functional Block Diagram

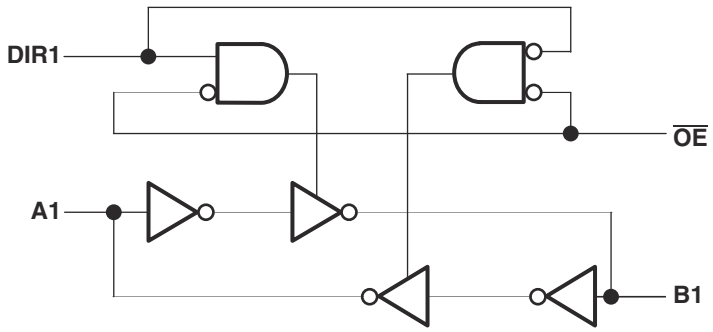


Figure 7-1. Logic Diagram (Positive Logic) of SN74AVC4T774-Q1

7.3 Feature Description

7.3.1 Fully Configurable Dual-Rail Design

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.08V and 3.6V; thus, making the device suitable for translating between any of the low voltage nodes (1.2V, 1.8V, 2.5V, and 3.3V).

7.3.2 Supports High Speed Translation

The SN74AVC4T774-Q1 device can support high data rate applications. The translated signal data rate can be up to 500Mbps when the signal is translated from 1.8V to 3.3V.

7.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} prevents backflow current by disabling I/O output circuits when the device is in partial-power-down mode.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74AVC4T774-Q1 device.

Table 7-1. Function Table (Each Bit)

CONTROL INPUTS		OUTPUT CIRCUITS(1)		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AVC4T774-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVC4T774-Q1 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The maximum data rate can be up to 500Mbps when the device translates a signal from 1.8V to 3.3V.

8.2 Typical Application

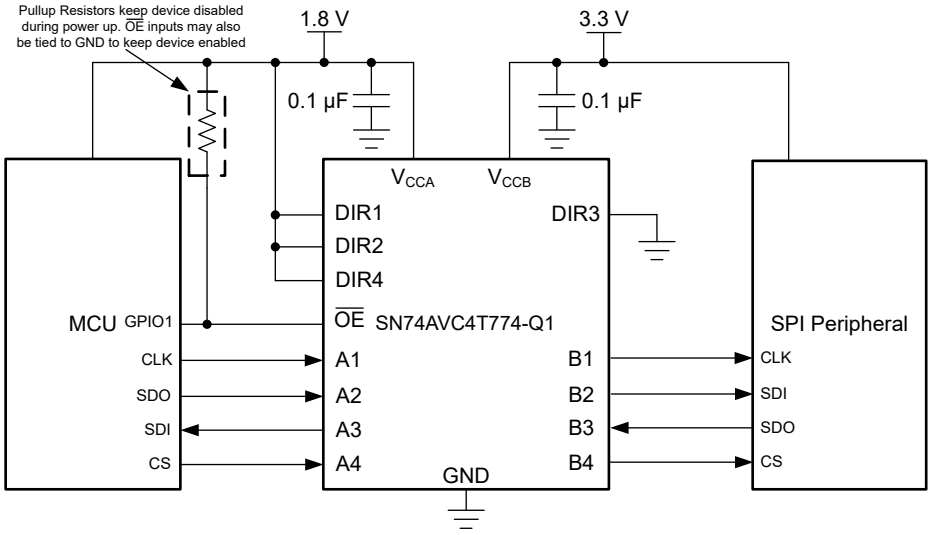


Figure 8-1. Typical Application Diagram

8.2.1 Design Requirements

Table 8-1 lists the parameters for this design example.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2V
Output voltage range	3.3V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVC4T774-Q1 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port. For this example, the input voltage is 1.2V.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVC4T774-Q1 device is driving to determine the output voltage range. For this example, the output voltage is 3.3V.

8.2.3 Application Curve

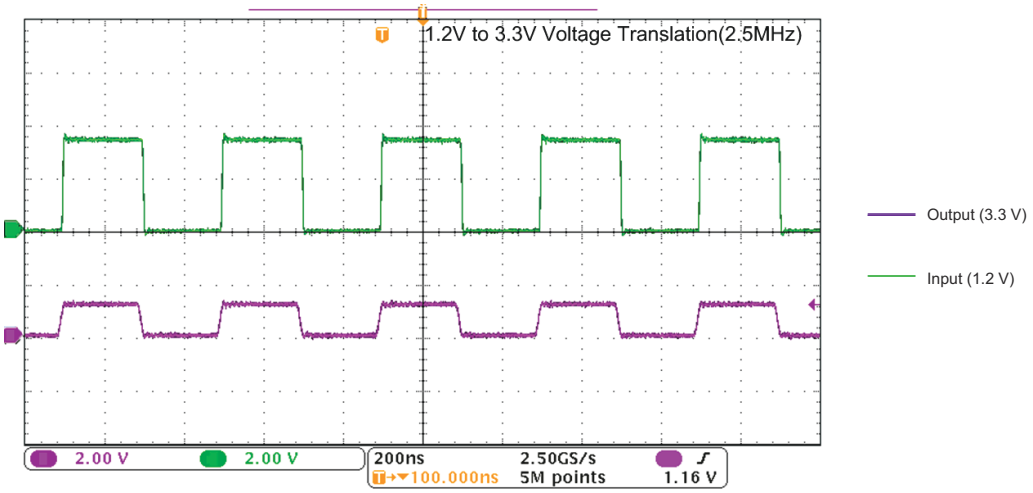


Figure 8-2. Translation Up (1.2V to 3.3V) at 2.5MHz

8.3 Power Supply Recommendations

The SN74AVC4T774-Q1 device uses two separate configurable power-supply rails: V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.08V to 3.6V, and V_{CCB} accepts any supply voltage from 1.08V to 3.6V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively, allowing for low-voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The output-enable ($\overline{OE}$) input circuit is designed so that it is supplied by V_{CCA}; when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To place the outputs in the high-impedance state during power up or power down, tie the $\overline{OE}$ input pin to V_{CCA} through a pullup resistor and do not enable it until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

8.4 Layout

8.4.1 Layout Guidelines

For device reliability, the recommendation is to follow common printed-circuit board layout guidelines such as:

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals, depending on the system requirements.

8.4.2 Layout Example

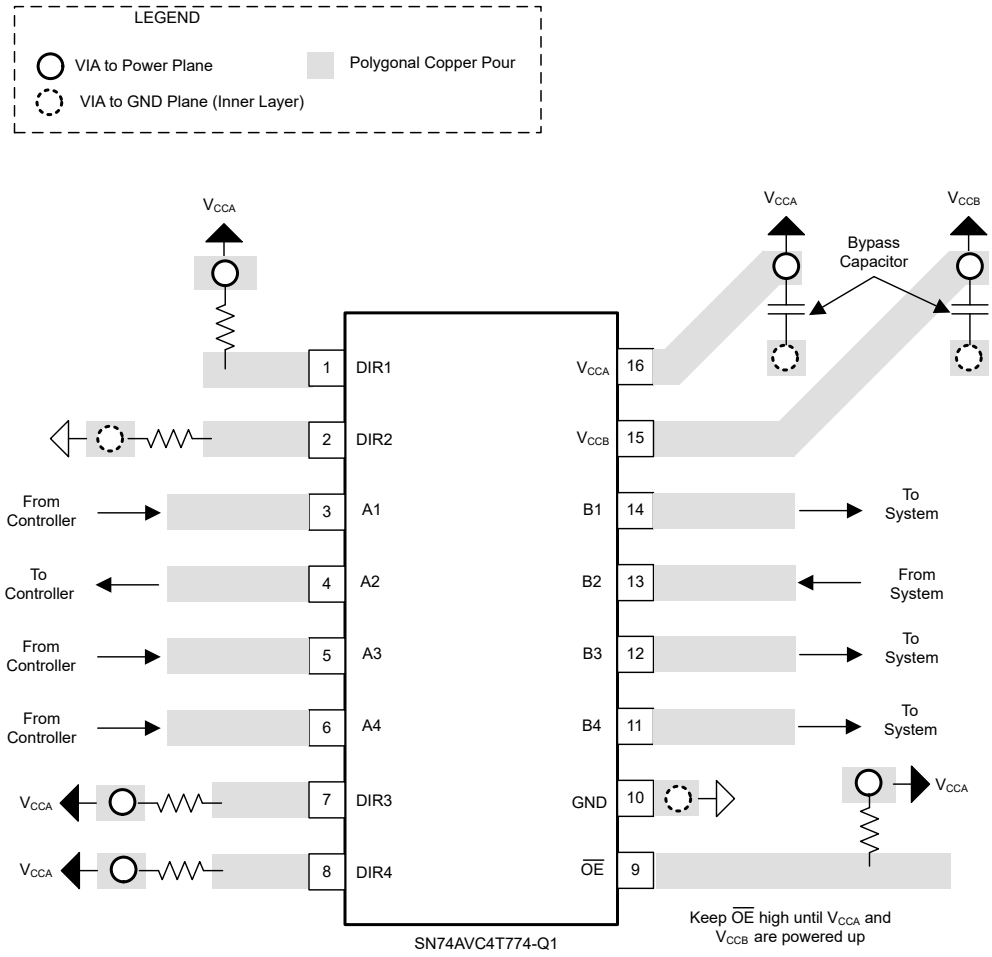


Figure 8-3. SN74AVC4T774-Q1 PW Package Layout Diagram

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *IC Package Thermal Metrics*
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2024) to Revision B (December 2024)	Page
• Updated Description	1
• Updated Pinout Diagrams	4
• Updated Pin Description	4
• Updated Overview	18
• Updated Figure 7-1	18
• Updated Figure 8-1	19
• Updated Figure 8-3	21

Changes from Revision * (March 2024) to Revision A (September 2024)	Page
• Changed status from Advanced Information to Production Data	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AVC4T774QDYYRQ1	ACTIVE	SOT-23-THIN	DYY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT774Q	Samples
74AVC4T774QPWRQ1	ACTIVE	TSSOP	PW	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT774Q	Samples
74AVC4T774QWBQBRQ1	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT774Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AVC4T774-Q1 :

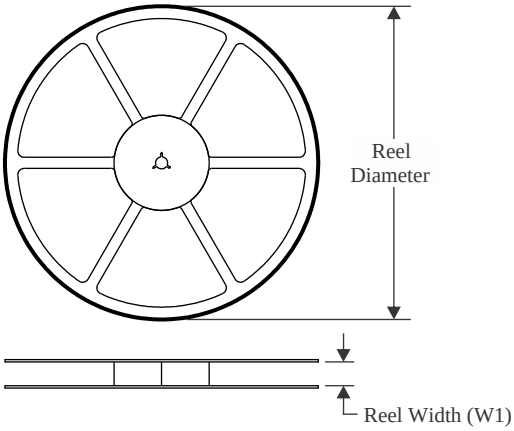
- Catalog : SN74AVC4T774

NOTE: Qualified Version Definitions:

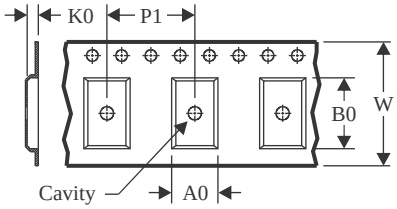
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

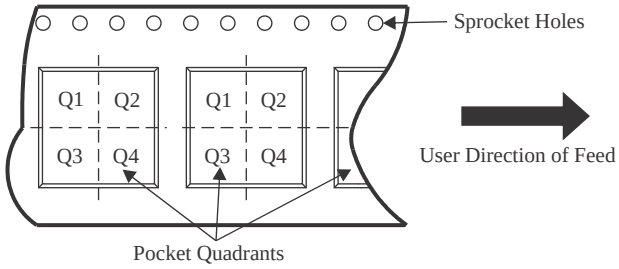


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

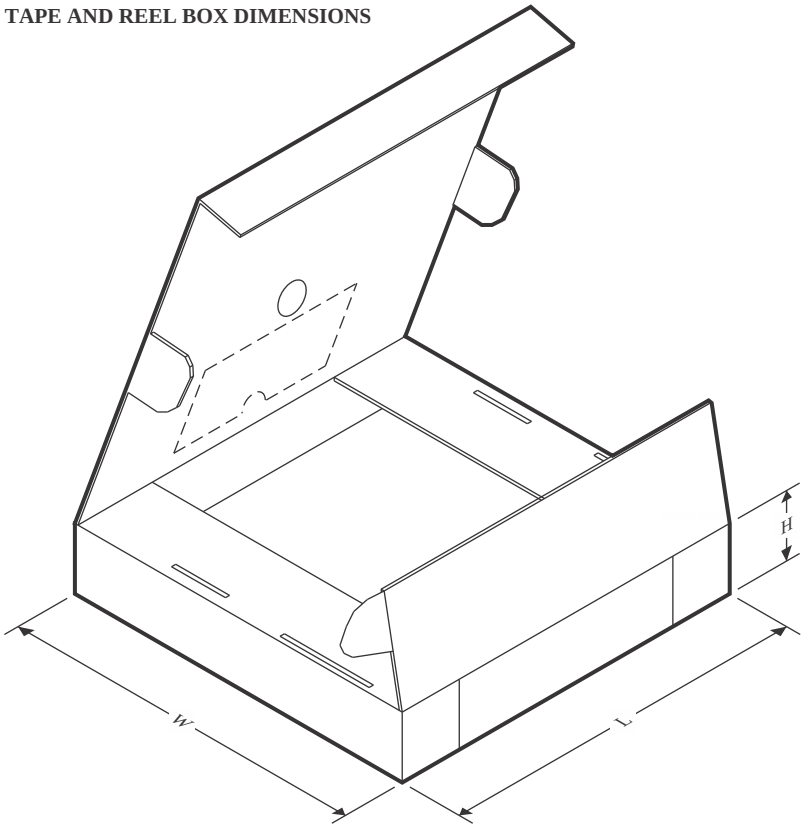
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AVC4T774QDYYRQ1	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
74AVC4T774QPWRQ1	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
74AVC4T774QWBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

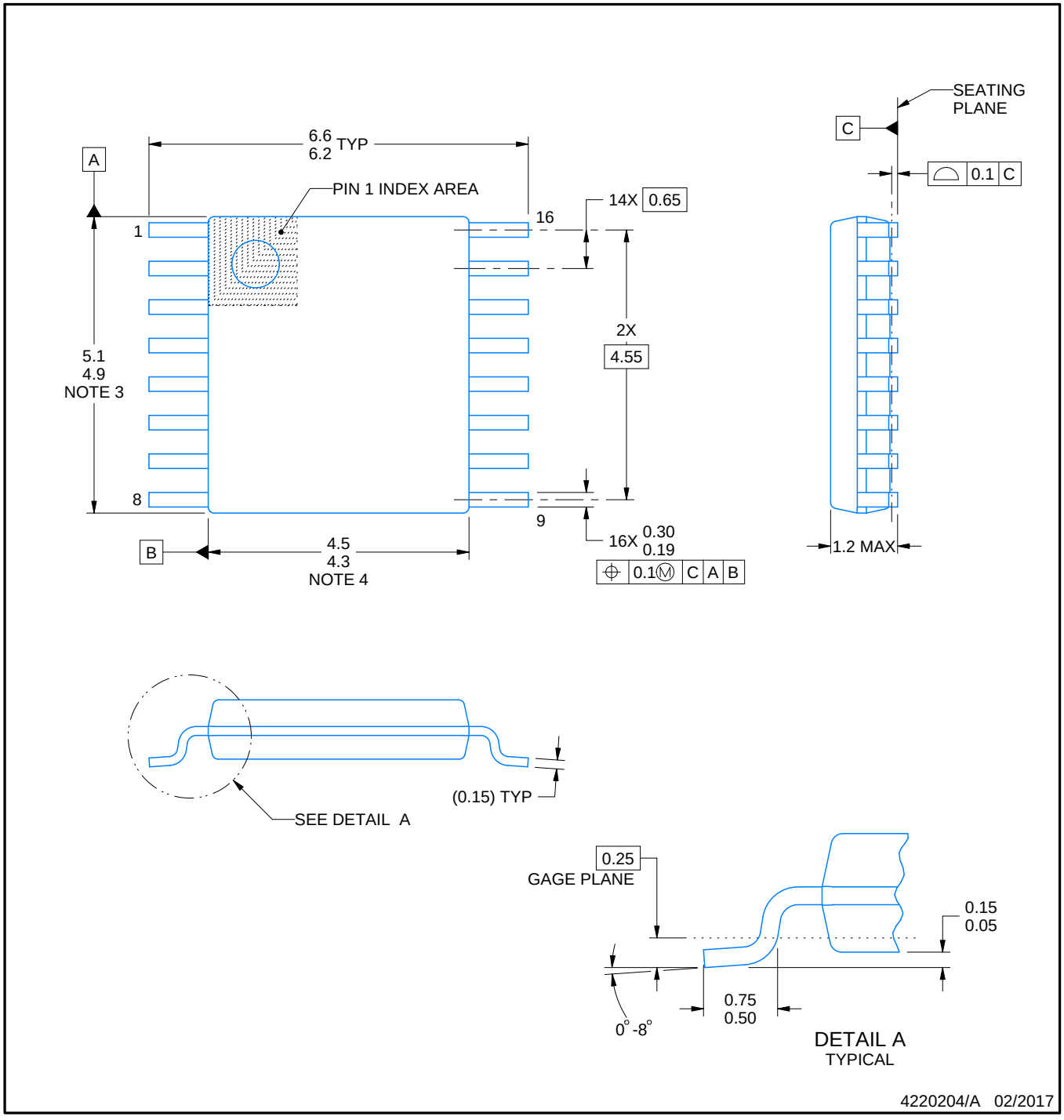
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AVC4T774QDYYRQ1	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
74AVC4T774QPWRQ1	TSSOP	PW	16	3000	356.0	356.0	35.0
74AVC4T774QWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0

PACKAGE OUTLINE

PW0016A

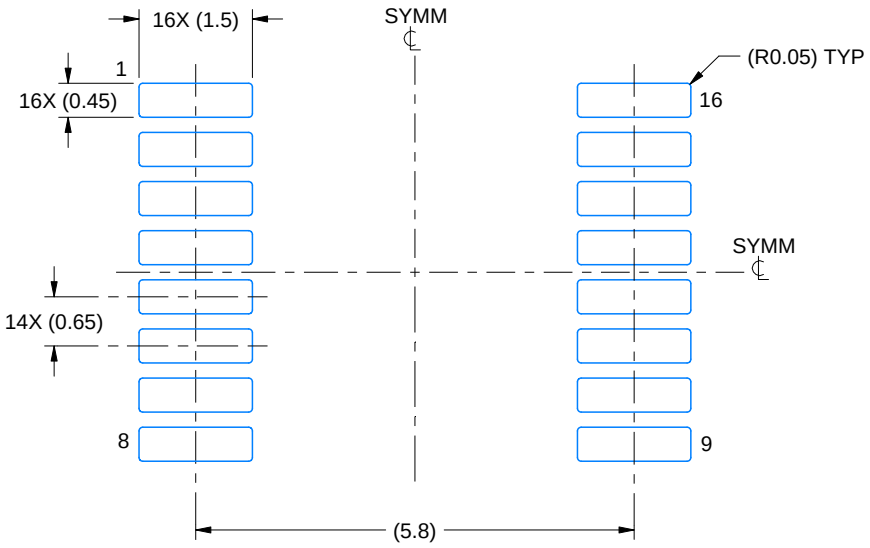
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

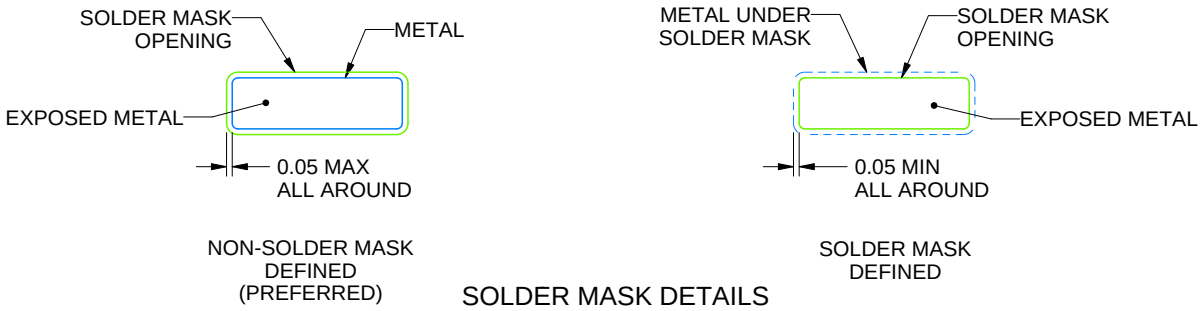


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

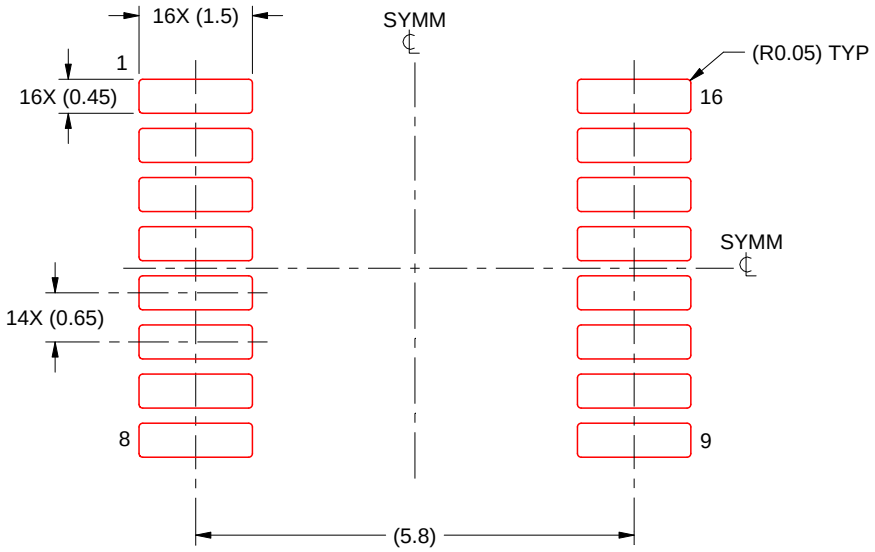


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

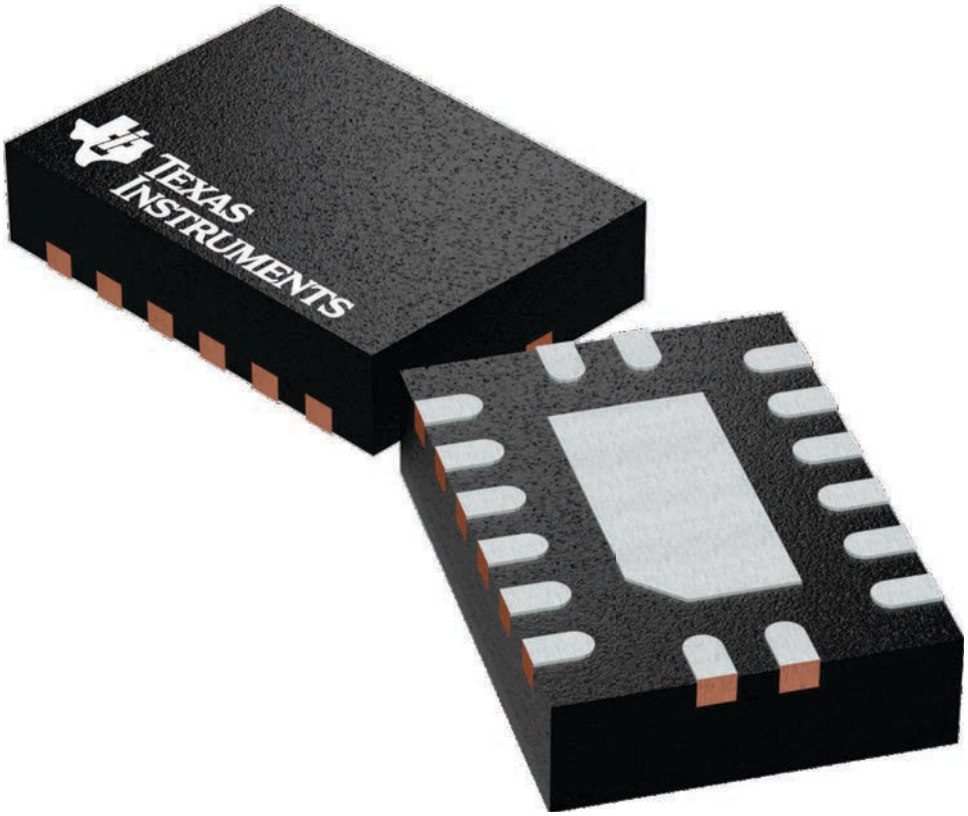
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



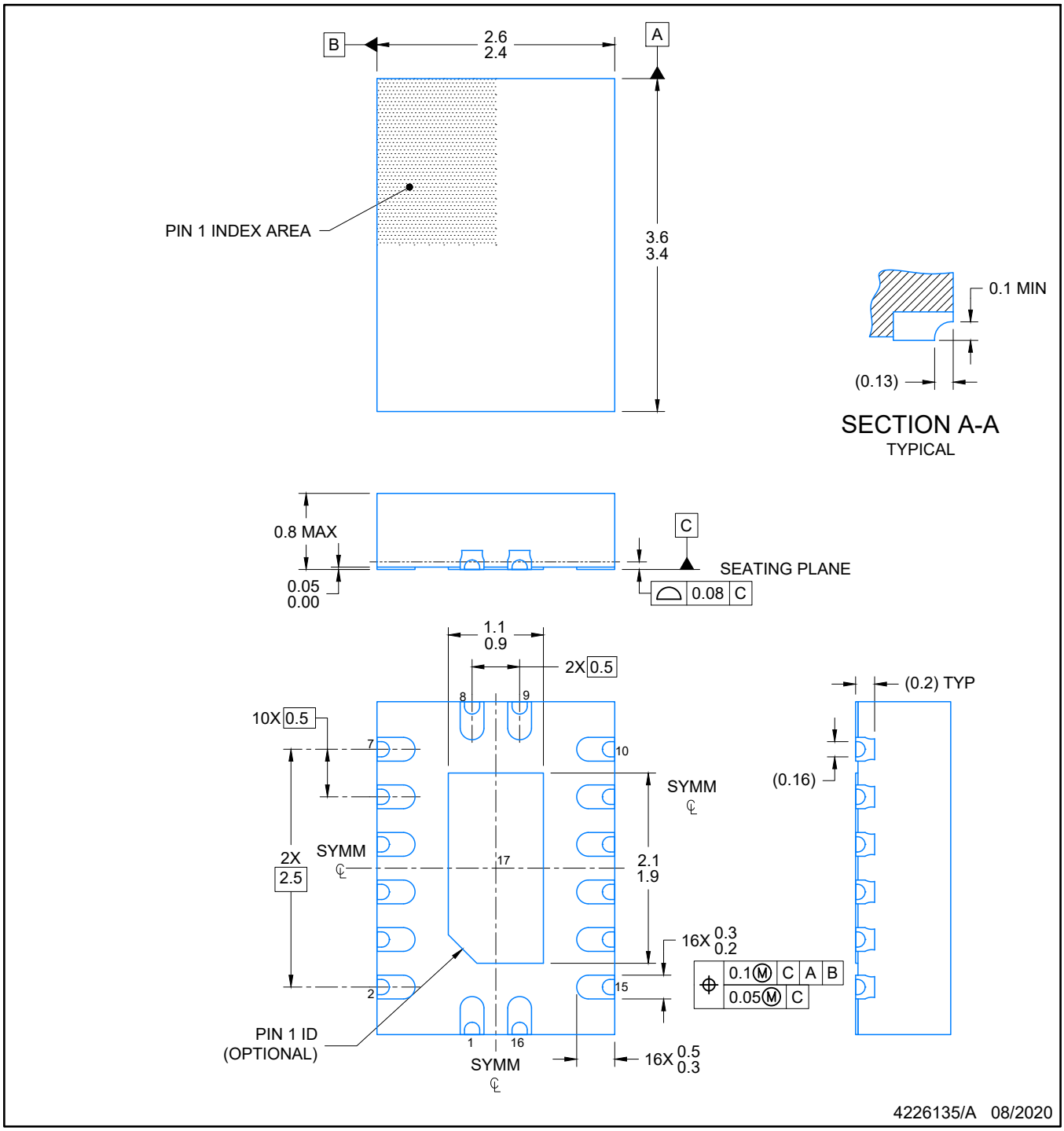
4226161/A

PACKAGE OUTLINE

BQB0016B

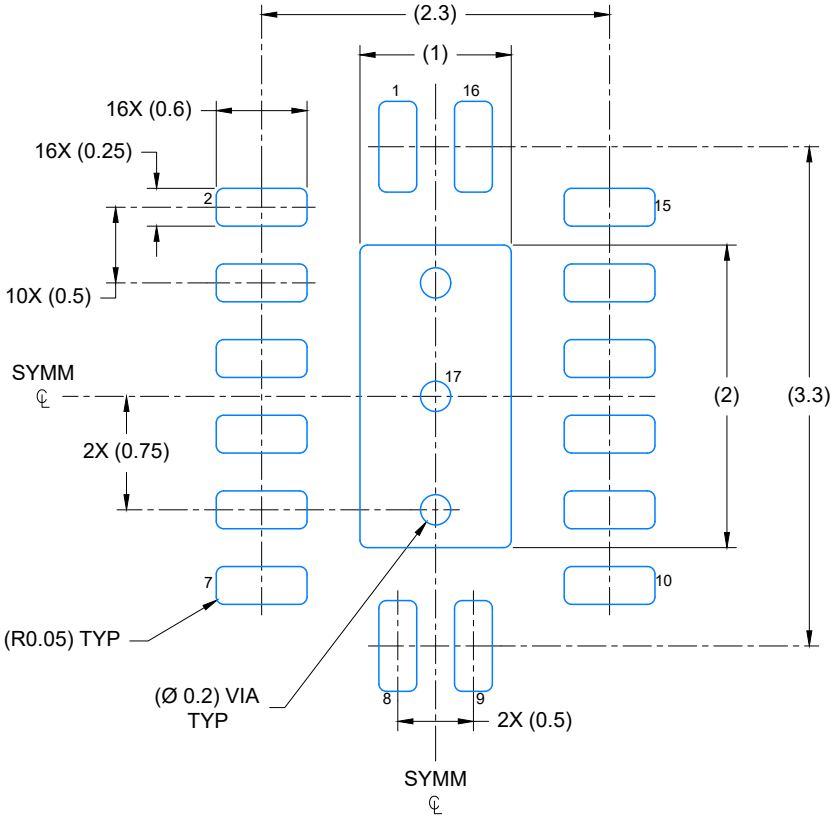
WQFN - 0.8 mm max height

INDSTNAME



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

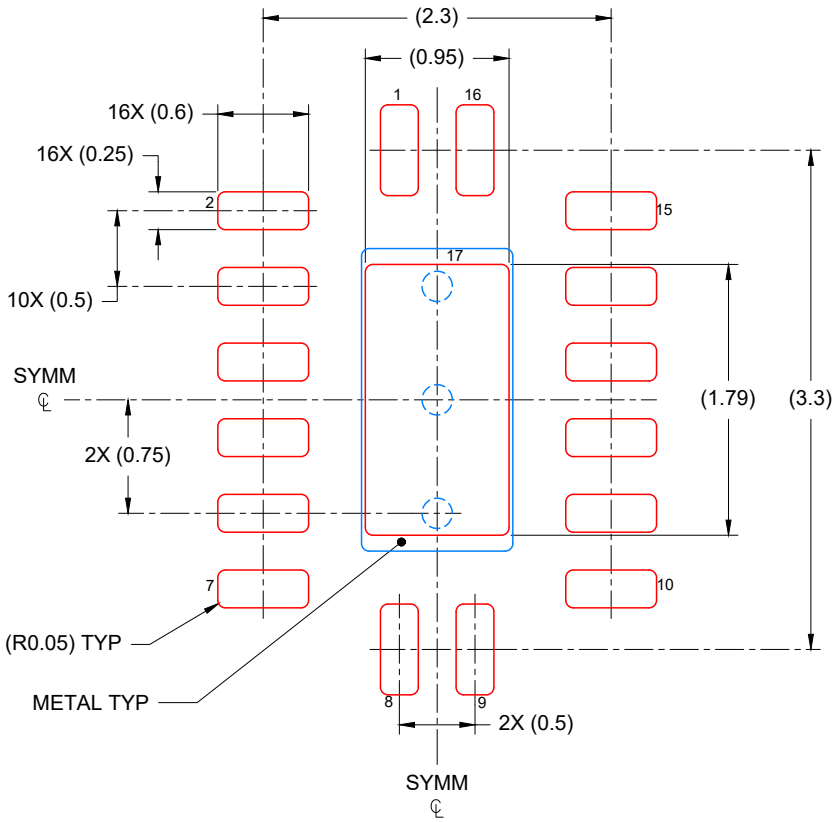


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

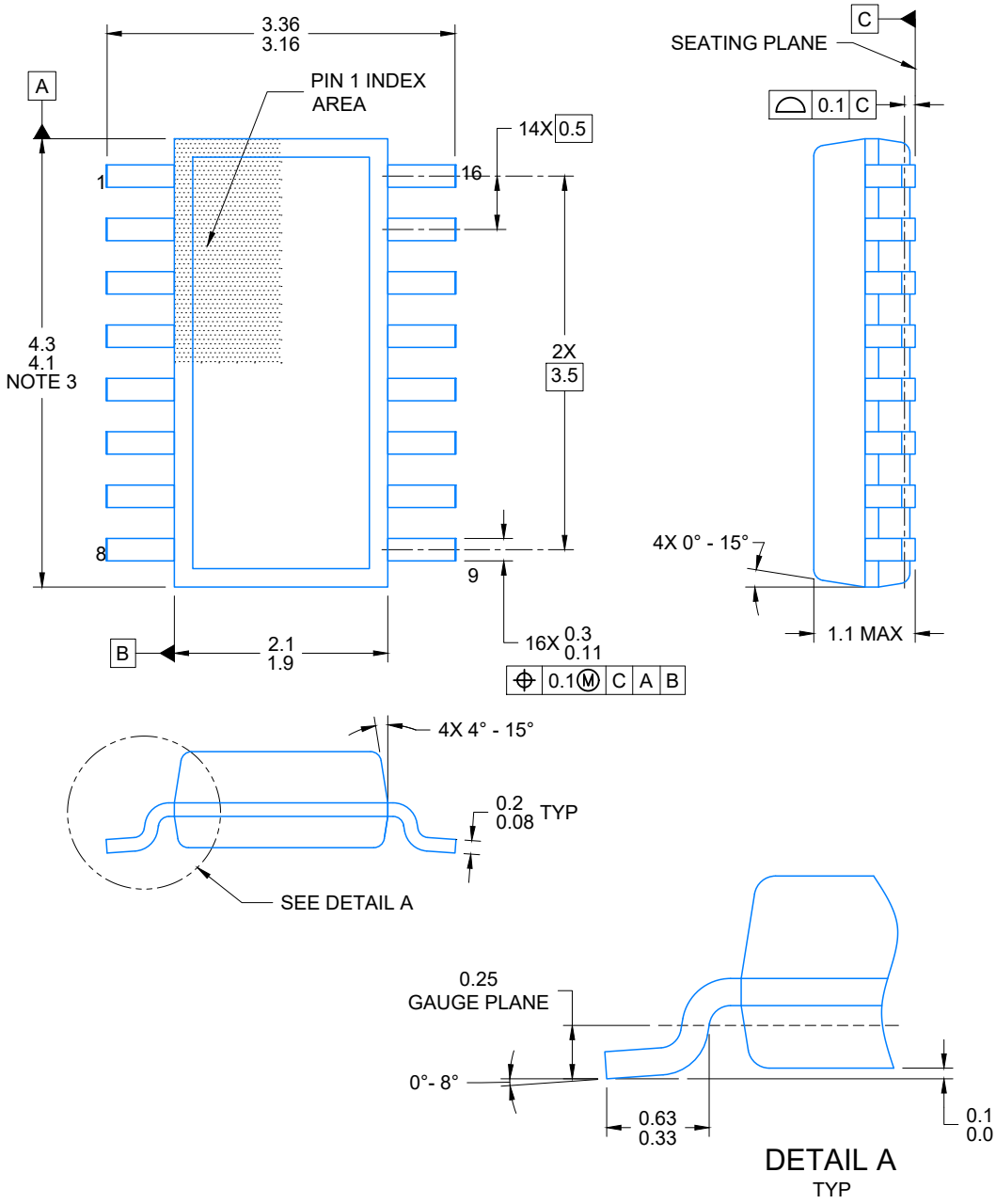
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYY0016A

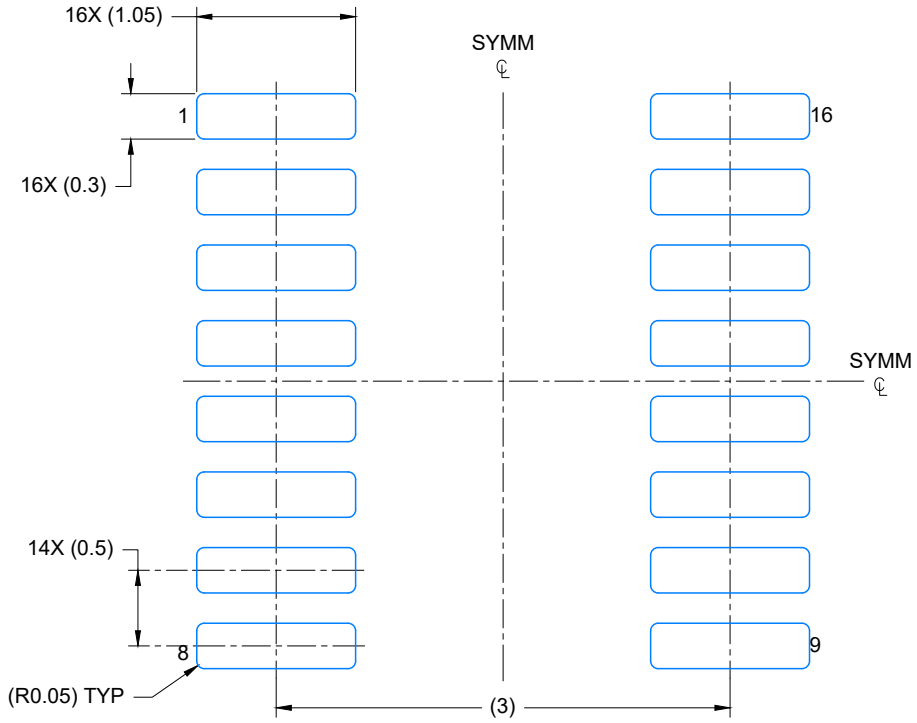
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

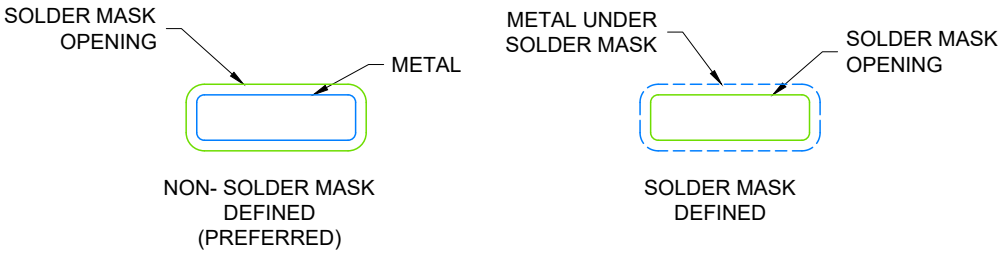


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

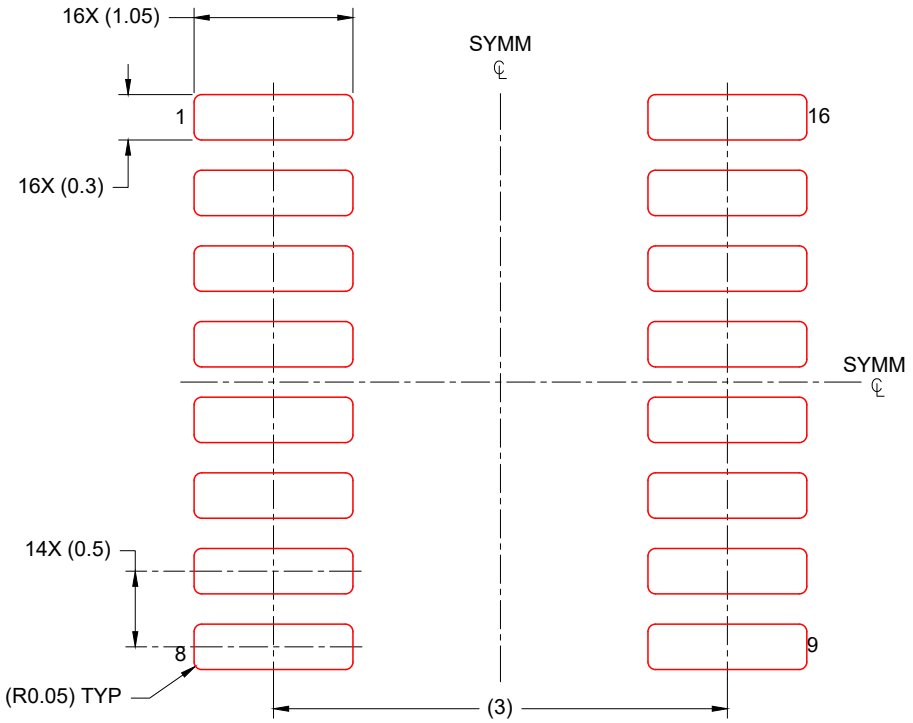
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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