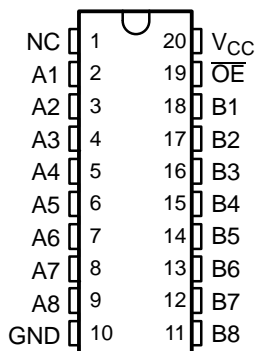


## FEATURES

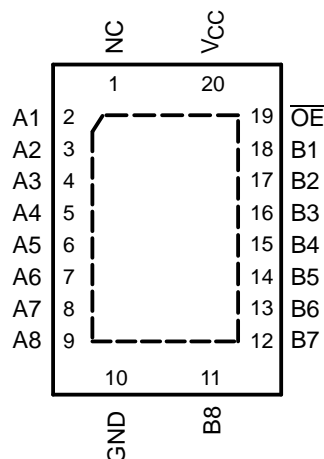
- Standard '245-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



NC - No internal connection

RGY PACKAGE  
(TOP VIEW)



NC - No internal connection

## DESCRIPTION/ORDERING INFORMATION

The SN74CBTLV3245A provides eight bits of high-speed bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 8-bit switch. When output enable ( $\overline{OE}$ ) is low, the 8-bit bus switch is on, and port A is connected to port B. When  $\overline{OE}$  is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

| $T_A$         | PACKAGE <sup>(1)</sup> |                    | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|--------------------|-----------------------|------------------|
| –40°C to 85°C | QFN – RGY              | Tape and reel      | SN74CBTLV3245ARGYR    | CL245A           |
|               | SOIC – DW              | Tube               | SN74CBTLV3245ADW      | CBTLV3245A       |
|               |                        | Tape and reel      | SN74CBTLV3245ADWR     |                  |
|               | SSOP (QSOP) – DBQ      | Tape and reel      | SN74CBTLV3245ADBQR    | CBTLV3245A       |
|               | TSSOP – PW             | Tape and reel      | SN74CBTLV3245APWR     | CL245A           |
|               | TVSOP – DGV            | Tape and reel      | SN74CBTLV3245ADGVR    | CL245A           |
|               | VFBGA – GQN            | Tape and reel      | SN74CBTLV3245AGQNR    | CL245A           |
| VFBGA – ZQN   | Tape and reel          | SN74CBTLV3245AZQNR | CL245A                |                  |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

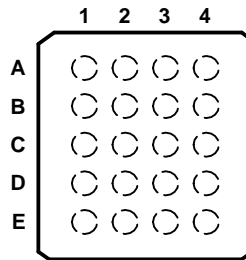


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN74CBTLV3245A LOW-VOLTAGE OCTAL FET BUS SWITCH

SCDS034M—JULY 1997—REVISED AUGUST 2005

**GQN OR ZQN PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS<sup>(1)</sup>**

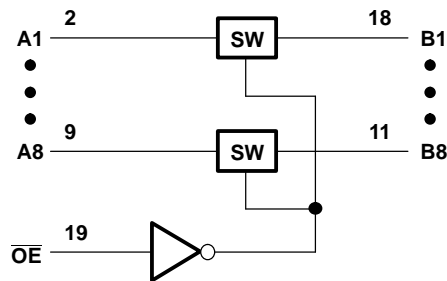
|          | 1   | 2  | 3               | 4               |
|----------|-----|----|-----------------|-----------------|
| <b>A</b> | A1  | NC | V <sub>CC</sub> | $\overline{OE}$ |
| <b>B</b> | A3  | B2 | A2              | B1              |
| <b>C</b> | A5  | A4 | B4              | B3              |
| <b>D</b> | A7  | B6 | A6              | B5              |
| <b>E</b> | GND | A8 | B8              | B7              |

(1) NC - No internal connection

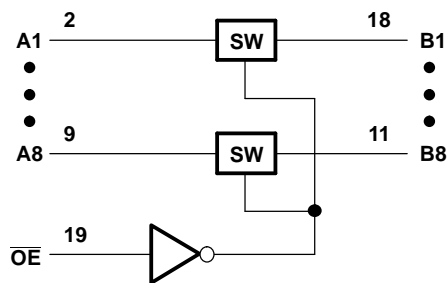
**FUNCTION TABLE**

| INPUT<br>$\overline{OE}$ | FUNCTION        |
|--------------------------|-----------------|
| L                        | A port = B port |
| H                        | Disconnect      |

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**SIMPLIFIED SCHEMATIC, EACH FET SWITCH**



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|               |                                    | MIN                        | MAX | UNIT   |
|---------------|------------------------------------|----------------------------|-----|--------|
| $V_{CC}$      | Supply voltage range               | –0.5                       | 4.6 | V      |
| $V_I$         | Input voltage range <sup>(2)</sup> | –0.5                       | 4.6 | V      |
|               | Continuous channel current         |                            | 128 | mA     |
| $I_{IK}$      | Input clamp current                | $V_{I/O} < 0$              |     | –50 mA |
| $\theta_{JA}$ | Package thermal impedance          | DBQ package <sup>(3)</sup> |     | 68     |
|               |                                    | DGV package <sup>(3)</sup> |     | 92     |
|               |                                    | DW package <sup>(3)</sup>  |     | 58     |
|               |                                    | PW package <sup>(3)</sup>  |     | 83     |
|               |                                    | RGY package <sup>(4)</sup> |     | 37     |
| $T_{stg}$     | Storage temperature range          | –65                        | 150 | °C     |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) The package thermal impedance is calculated in accordance with JESD 51-5.

### Recommended Operating Conditions<sup>(1)</sup>

|          |                                  | MIN  | MAX | UNIT |
|----------|----------------------------------|--|-----|------|
| $V_{CC}$ | Supply voltage                   | 2.3  | 3.6 | V    |
| $V_{IH}$ | High-level control input voltage | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.7 | V    |
|          |                                  | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 2   |      |
| $V_{IL}$ | Low-level control input voltage  | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 0.7 | V    |
|          |                                  | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 0.8 |      |
| $T_A$    | Operating free-air temperature   | –40  | 85  | °C   |

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74CBTLV3245A LOW-VOLTAGE OCTAL FET BUS SWITCH

SCDS034M–JULY 1997–REVISED AUGUST 2005

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                       |  | TEST CONDITIONS            |   | MIN                    | TYP <sup>(1)</sup> | MAX  | UNIT |   |
|---------------------------------|--|----------------------------|---|------------------------|--------------------|------|------|---|
| V <sub>IK</sub>                 | Control inputs   | V <sub>CC</sub> = 3 V,     | I <sub>I</sub> = –18 mA                                     |                        |                    | –1.2 | V    |   |
|                                 | Data inputs  |                            |   |                        |                    | –0.8 |      |   |
| I <sub>I</sub>                  |  | V <sub>CC</sub> = 3.6 V,   | V <sub>I</sub> = V <sub>CC</sub> or GND                     |                        |                    | ±60  | μA   |   |
| I <sub>off</sub>                |  | V <sub>CC</sub> = 0,       | V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V               |                        |                    | 40   | μA   |   |
| I <sub>CC</sub>                 |  | V <sub>CC</sub> = 3.6 V,   | I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND |                        |                    | 20   | μA   |   |
| ΔI <sub>CC</sub> <sup>(2)</sup> | Control inputs   | V <sub>CC</sub> = 3.6 V,   | One input at 3 V, Other inputs at V <sub>CC</sub> or GND    |                        |                    | 300  | μA   |   |
| C <sub>i</sub>                  | Control inputs   | V <sub>I</sub> = 3 V or 0  |   |                        |                    | 4    | pF   |   |
| C <sub>io(OFF)</sub>            |  | V <sub>O</sub> = 3 V or 0, | $\overline{OE}$ = V <sub>CC</sub>                           |                        |                    | 9    | pF   |   |
| r <sub>on</sub> <sup>(3)</sup>  | V <sub>CC</sub> = 2.3 V,<br>TYP at V <sub>CC</sub> = 2.5 V | V <sub>I</sub> = 0         | I <sub>O</sub> = 64 mA                                      |                        |                    | 5    | 8    | Ω |
|                                 |  |                            | I <sub>O</sub> = 24 mA                                      |                        |                    | 5    | 8    |   |
|                                 | V <sub>CC</sub> = 3 V                                      | V <sub>I</sub> = 1.7 V,    | I <sub>O</sub> = 15 mA                                      |                        |                    | 27   | 40   |   |
|                                 |  |                            | V <sub>I</sub> = 0  | I <sub>O</sub> = 64 mA |                    |      | 5    |   |
|                                 | V <sub>I</sub> = 2.4 V,                                    | I <sub>O</sub> = 24 mA     |   |                        |                    | 5    | 7    |   |
|                                 |  | I <sub>O</sub> = 15 mA     |   |                        | 10                 | 15   |      |   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V (unless otherwise noted), T<sub>A</sub> = 25°C.

(2) This is the increase in supply current for each input that is at the specified voltage level, rather than V<sub>CC</sub> or GND.

(3) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

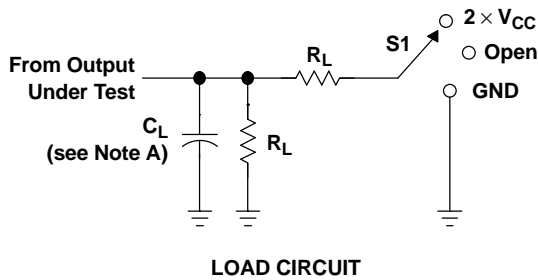
## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

| PARAMETER                      | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |      | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |      | UNIT |
|--------------------------------|-----------------|----------------|------------------------------------|------|------------------------------------|------|------|
|                                |                 |                | MIN                                | MAX  | MIN                                | MAX  |      |
| t <sub>pd</sub> <sup>(1)</sup> | A or B          | B or A         |                                    | 0.15 |                                    | 0.25 | ns   |
| t <sub>en</sub>                | $\overline{OE}$ | A or B         | 1                                  | 6    | 1                                  | 4.7  | ns   |
| t <sub>dis</sub>               | $\overline{OE}$ | A or B         | 1                                  | 6.1  | 1                                  | 6.4  | ns   |

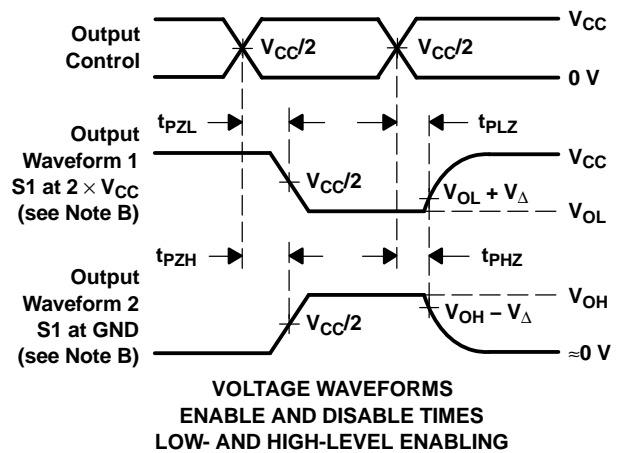
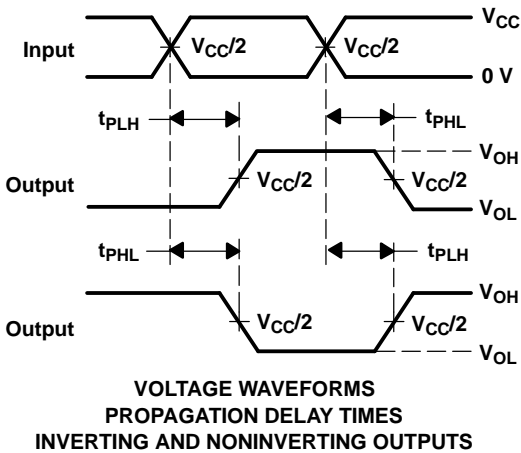
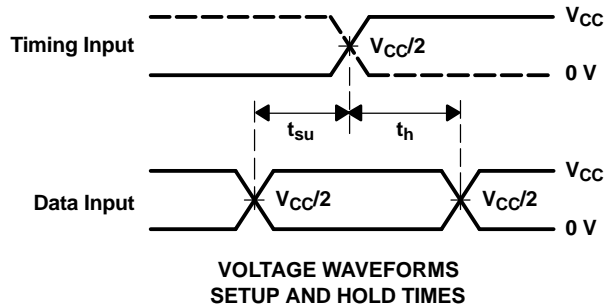
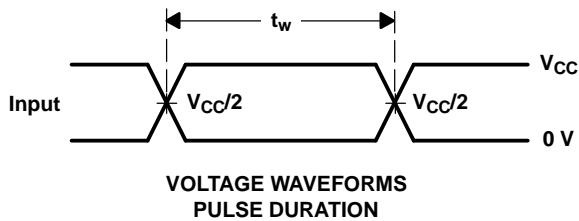
(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



| TEST              | S1                |
|-------------------|-------------------|
| $t_{PLH}/t_{PHL}$ | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |

| $V_{CC}$                          | $C_L$ | $R_L$        | $V_{\Delta}$ |
|-----------------------------------|-------|--------------|--------------|
| $2.5 \text{ V} \pm 0.2 \text{ V}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| $3.3 \text{ V} \pm 0.3 \text{ V}$ | 50 pF | 500 $\Omega$ | 0.3 V        |



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2$  ns,  $t_f \leq 2$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device   | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|--------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| 74CBTLV3245ADWG4   | ACTIVE        | SOIC         | DW              | 20   | 25          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CBTLV3245A              | <a href="#">Samples</a> |
| 74CBTLV3245APWRG4  | ACTIVE        | TSSOP        | PW              | 20   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CL245A                  | <a href="#">Samples</a> |
| SN74CBTLV3245ADBQR | ACTIVE        | SSOP         | DBQ             | 20   | 2500        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | CBTLV3245A              | <a href="#">Samples</a> |
| SN74CBTLV3245ADGVR | ACTIVE        | TVSOP        | DGV             | 20   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CL245A                  | <a href="#">Samples</a> |
| SN74CBTLV3245ADW   | ACTIVE        | SOIC         | DW              | 20   | 25          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CBTLV3245A              | <a href="#">Samples</a> |
| SN74CBTLV3245ADWE4 | ACTIVE        | SOIC         | DW              | 20   | 25          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CBTLV3245A              | <a href="#">Samples</a> |
| SN74CBTLV3245ADWR  | ACTIVE        | SOIC         | DW              | 20   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CBTLV3245A              | <a href="#">Samples</a> |
| SN74CBTLV3245APW   | OBSOLETE      | TSSOP        | PW              | 20   |             | TBD             | Call TI                              | Call TI              | -40 to 85    | CL245A                  |                         |
| SN74CBTLV3245APWR  | ACTIVE        | TSSOP        | PW              | 20   | 2000        | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 85    | CL245A                  | <a href="#">Samples</a> |
| SN74CBTLV3245ARGYR | ACTIVE        | VQFN         | RGY             | 20   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | CL245A                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74CBTLV3245APWRG4  | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74CBTLV3245ADBQR | SSOP         | DBQ             | 20   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74CBTLV3245ADGVR | TVSOP        | DGV             | 20   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CBTLV3245ADWR  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74CBTLV3245APWR  | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74CBTLV3245ARGYR | VQFN         | RGY             | 20   | 3000 | 330.0              | 12.4               | 3.8     | 4.8     | 1.6     | 8.0     | 12.0   | Q1            |



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74CBTLV3245APWRG4  | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74CBTLV3245ADBQR | SSOP         | DBQ             | 20   | 2500 | 356.0       | 356.0      | 35.0        |
| SN74CBTLV3245ADGVR | TVSOP        | DGV             | 20   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74CBTLV3245ADWR  | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74CBTLV3245APWR  | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74CBTLV3245ARGYR | VQFN         | RGY             | 20   | 3000 | 367.0       | 367.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device             | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 74CBTLV3245ADWG4   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74CBTLV3245ADW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74CBTLV3245ADWE4 | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

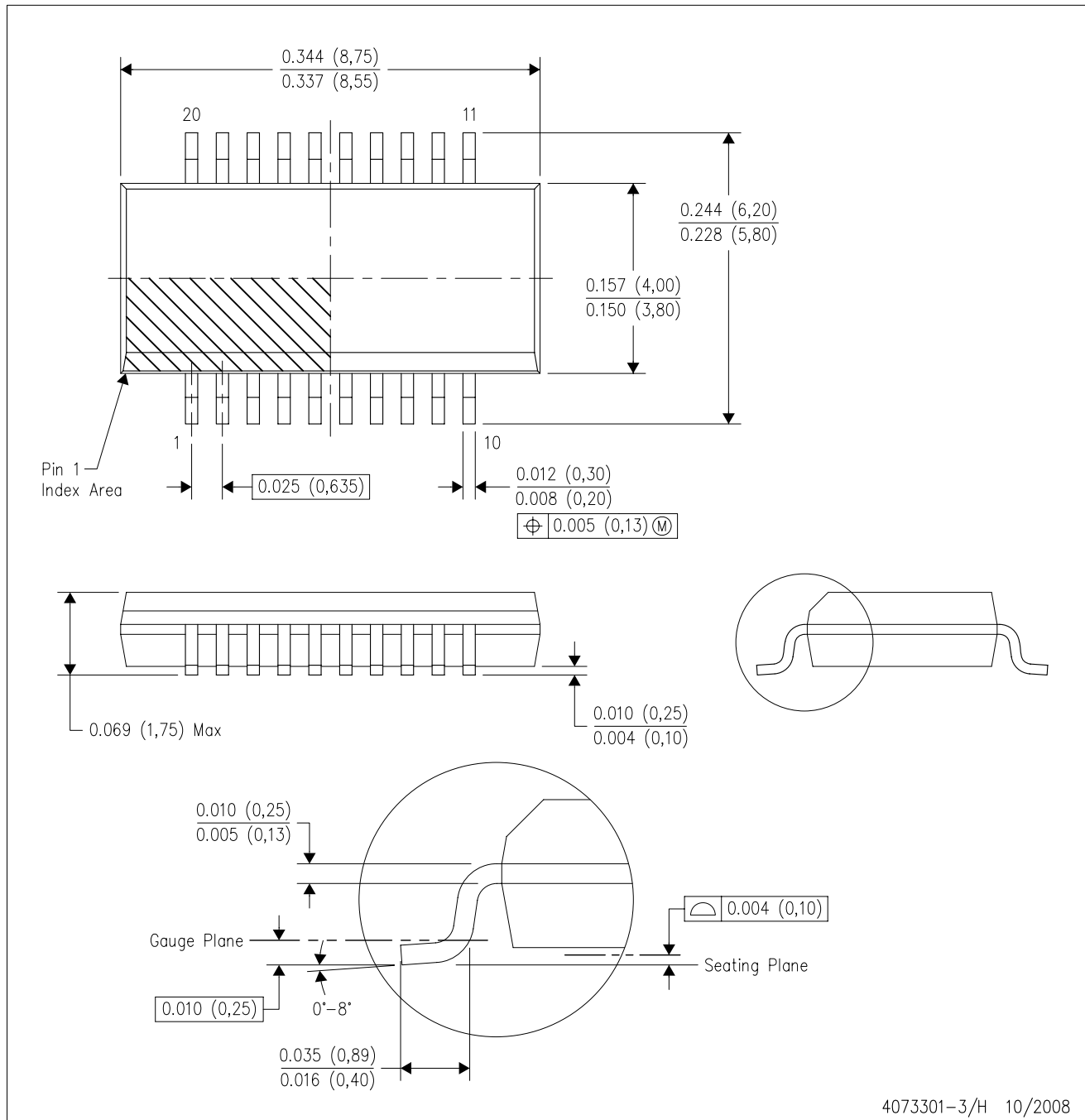
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



DBQ (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AD.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## GENERIC PACKAGE VIEW

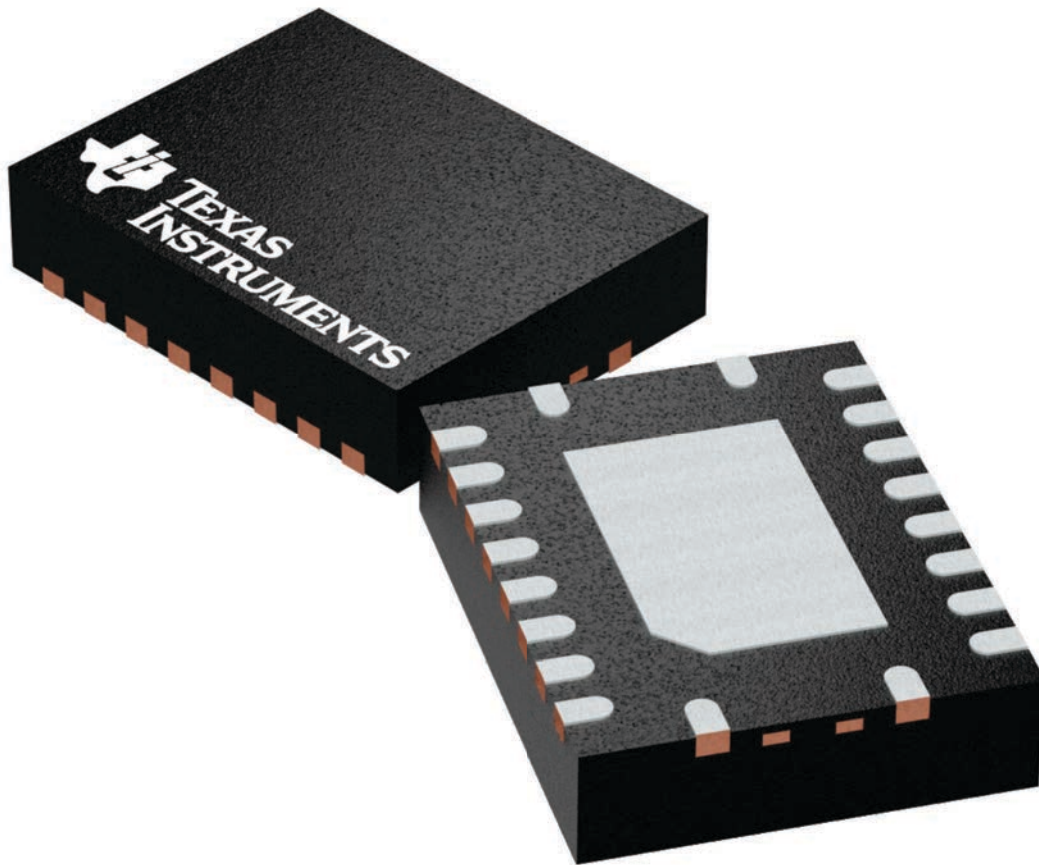
**RGY 20**

**VQFN - 1 mm max height**

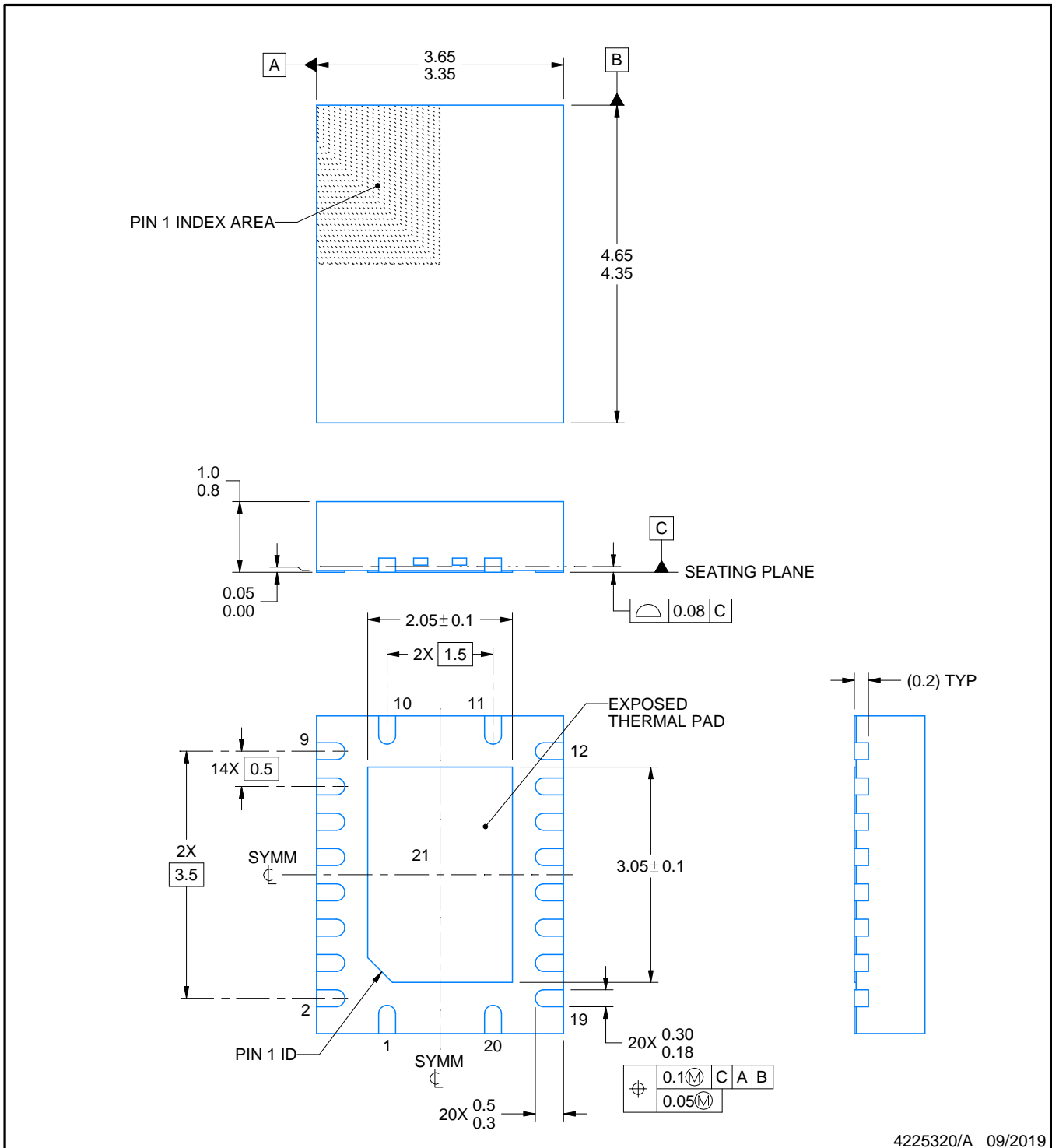
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



4225320/A 09/2019

NOTES: (continued)

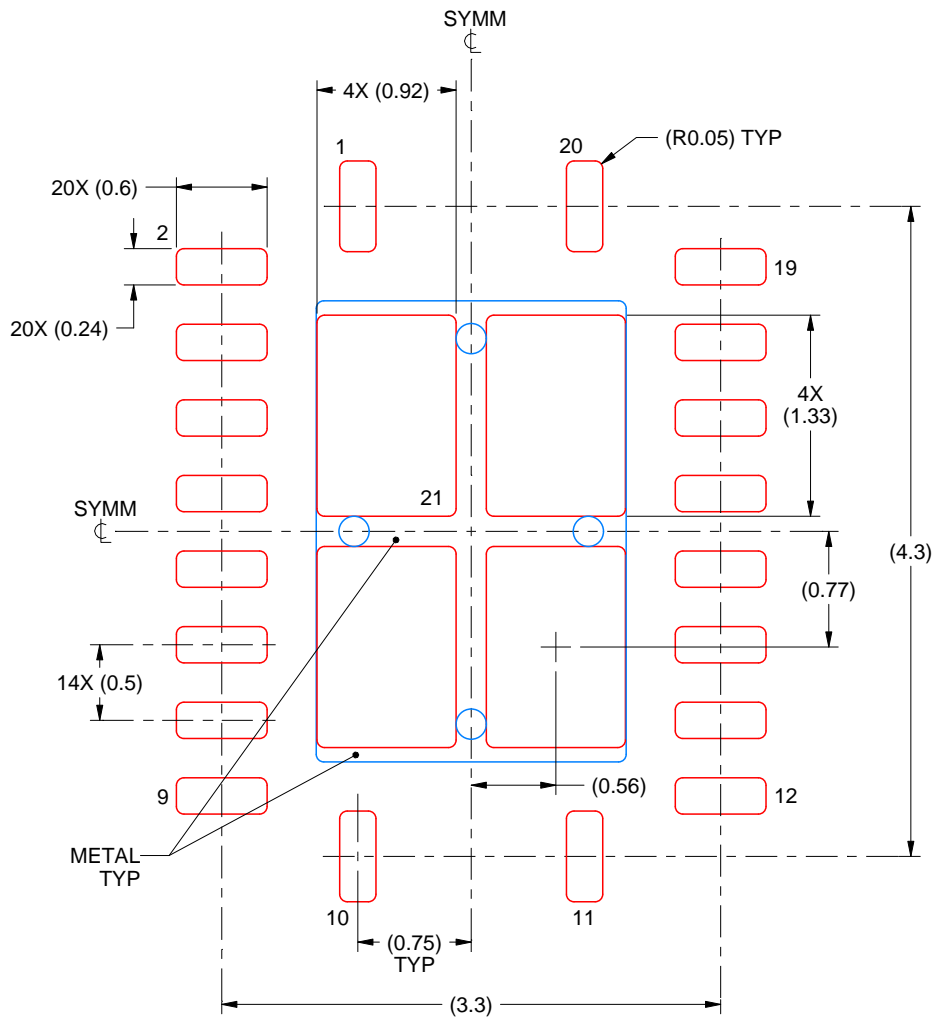
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21  
 78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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