SN74HC373A OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS
SCLS458 – MARCH 2001

- Eight High-Current Latches in a Single Package
- High-Current 3-State True Outputs Can Drive up to 15 LSTTL Loads
- Full Parallel Access for Loading

description

This 8-bit latch features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

DB, N, OR PW PACKAGE (TOP VIEW)								
OE [1	U ₂₀	Vcc					
1Q [2	19	8Q					
1D [3	18	BD					
2D [4	17	[] 7D					
2Q [5	16] 7Q					
3Q [6	15] 6Q					
3D [7	14] 6D					
4D [8	13] 5D					
4Q [9	12] 5Q					
GND [10	11	LE					

The eight latches of the SN74HC373A are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

An output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

TA	PACK	AGE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING								
	PDIP – N	Tube	SN74HC373AN	SN74HC373AN								
–40°C to 85°C	SSOP – DB	Tape and reel	SN74HC373ADBR	HC373A								
	TSSOP – PW	Tape and reel	SN74HC373APWR	HC373A								

ORDERING INFORMATION

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each latch)

	INPUTS		OUTPUT
OE	LE	D	Q
L	Н	Н	Н
L	н	L	L
L	L	Х	Q ₀
н	Х	Х	Z



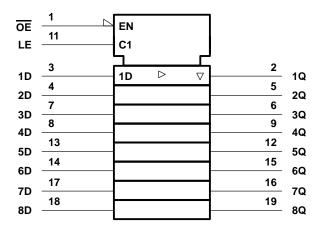
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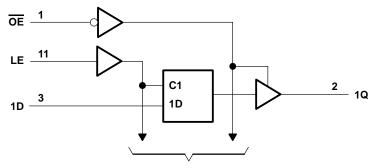
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logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range[‡]

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input clamp current, I_{IK} (V _I < 0 or V _I > V _{CC}) (see		
Output clamp current, I_{OK} (V _O < 0 or V _O > V _{CC})		
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$		
Continuous current through V _{CC} or GND		
Package thermal impedance, θ_{IA} (see Note 2):		
o	N package	
	PW package	83°C/W
Storage temperature range, T _{stg}		S5°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2	5	6	V
		$V_{CC} = 2 V$	1.5			
VIH	High-level input voltage	$V_{CC} = 4.5 V$	3.15			V
		V _{CC} = 6 V	4.2			
		$V_{CC} = 2 V$	0		0.5	
VIL	Low-level input voltage	$V_{CC} = 4.5 V$	0		1.35	V
		V _{CC} = 6 V	0		1.8	
٧I	Input voltage		0		VCC	V
VO	Output voltage		0		VCC	V
		$V_{CC} = 2 V$	0		1000	
tt	Input transition (rise and fall) time	V _{CC} = 4.5 V	0		500	ns
		V _{CC} = 6 V	0		400	
ТĄ	Operating free-air temperature		-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST	ONDITIONS	vcc	Т	A = 25°C	;	MIN	МАХ	UNIT
PARAMETER	TESTC			MIN	TYP	MAX	IVIIIN	IVIAA	UNIT
			2 V	1.9	1.998		1.9		
		I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		
VOH	$V_I = V_{IH} \text{ or } V_{IL}$		6 V	5.9	5.999		5.9		V
		I _{OH} = -6 mA	4.5 V	3.98	4.3		3.84		
		I _{OH} = -7.8 mA	6 V	5.48	5.8		5.34		
			2 V			0.1		0.1	
		I _{OL} = 20 μA	4.5 V			0.1		0.1	
VOL	VI = VIH or VIL		6 V			0.1		0.1	V
		I _{OL} = 6 mA	4.5 V			0.26		0.33	
		I _{OL} = 7.8 mA	6 V			0.26		0.33	
lı	VI = ACC or 0		6 V		±0.1	±100		±1000	nA
loz	AO = ACC or 0		6 V			±0.5		±5	μA
ICC	$V_I = V_{CC} \text{ or } 0,$	IO = 0	6 V			8		80	μA
Ci			2 V to 6 V		3	10		10	pF



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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		Vee	T _A = 1	25°C	MIN	МАХ	UNIT
		Vcc	MIN	MAX		IVIAA	UNIT
		2 V	75		95		
tw	t _w Pulse duration, LE high	4.5 V	15		19		ns
		6 V	13		16		
	Setup time, data before LE \downarrow	2 V	50		63		ns
t _{su}		4.5 V	10		13		
		6 V	9		11		
		2 V	20		24		ns
t _h	Hold time, data after LE \downarrow	4.5 V	10		12		
		6 V	10		12		

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	Vee	ТА	= 25°C	;	MIN MAX	UNIT
PARAMETER	(INPUT)	(OUTPUT)	Vcc	MIN	TYP	MAX		UNIT
			2 V		55	125	155	
	D	Q	4.5 V		15	25	31	
· .			6 V		12	21	26	-
^t pd			2 V		71	125	155	ns
	LE	Any Q	4.5 V		20	25	31	
			6 V		16	21	26	
			2 V		60	125	155	
ten	OE	Any Q	4.5 V		17	25	31	ns
			6 V		13	21	26	
			2 V		44	125	155	
^t dis	OE	Any Q	4.5 V		19	25	31	ns
			6 V		17	21	26	
			2 V		22	60	75	
tt		Any Q	4.5 V		7	12	15	ns
			6 V		5	10	13	



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switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	Vee	Тд	∖ = 25°C	;	MIN MAX	UNIT
FARAMETER	(INPUT)	(OUTPUT)	Vcc	MIN	TYP	MAX		UNIT
			2 V		73	175	220	
	D	Q	4.5 V		20	35	44	
· · ·			6 V		16	30	37	20
^t pd	LE	Any Q	2 V		90	175	220	ns
			4.5 V		25	35	44	
			6 V		20	30	37	
			2 V		78	175	220	
^t en	OE	Any Q	4.5 V		21	35	44	ns
			6 V		17	30	37	

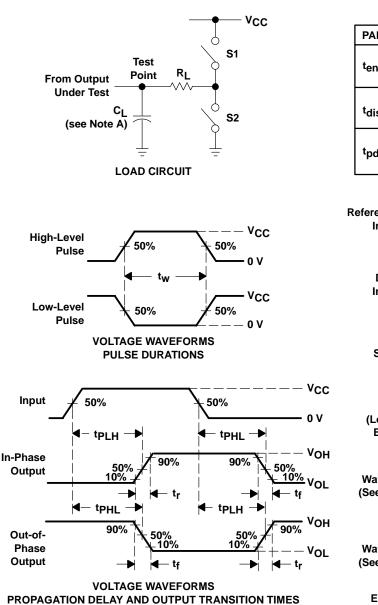
operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance	No load	100	pF

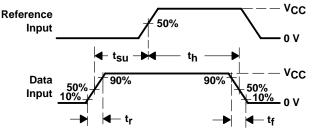


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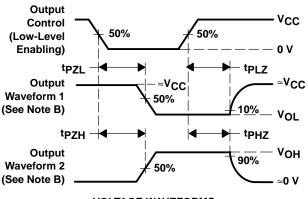
PARAMETER MEASUREMENT INFORMATION







VOLTAGE WAVEFORMS SETUP AND HOLD AND INPUT RISE AND FALL TIMES

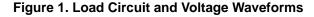


VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. CL includes probe and test-fixture capacitance.

 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following

- characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_f = 6 ns, t_f = 6 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tpLH and tpHL are the same as t_{pd} .







PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC373ANSR	ACTIVE	SOP	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		HC373A	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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