

# SN74LV1T08-Q1 Automotive 2-Input Positive-AND Gates With Integrated Translation

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Wide operating range of 1.8 V to 5.5 V
- Single-supply voltage translator (refer to *LVxT Enhanced Input Voltage*):
  - Up translation:
    - 1.2-V to 1.8-V
    - 1.5-V to 2.5-V
    - 1.8-V to 3.3-V
    - 3.3-V to 5.0-V
  - Down translation:
    - 5.0-V, 3.3-V, 2.5-V to 1.8-V
    - 5.0-V, 3.3-V to 2.5-V
    - 5.0-V to 3.3-V
- 5.5-V tolerant input pins
- Supports standard pinouts
- Up to 150Mbps with 5-V or 3.3-V  $V_{CC}$
- Latch-up performance exceeds 250 mA per JESD 17

## 2 Applications

- [Enable or disable a digital signal](#)
- [Controlling an indicator LED](#)
- [Translation between communication modules and system controllers](#)



**Simplified Logic Diagram (Positive Logic)**

## 3 Description

The SN74LV1T08-Q1 is a 2-input AND Gate. Each gate performs the Boolean function  $Y = A \times B$  in positive logic. The output level is referenced to the supply voltage ( $V_{CC}$ ) and supports 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

The input is designed with a lower threshold circuit to support up translation for lower voltage CMOS inputs (for example, 1.2-V input to 1.8-V output or 1.8-V input to 3.3-V output). In addition, the 5-V tolerant input pins enable down translation (for example, 3.3-V to 2.5-V output).

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE (NOM) <sup>(3)</sup>
SN74LV1T08-Q1	DCK (SC-70, 5)	2 mm × 2.1 mm	2 mm × 1.25 mm
	DBV (SOT-23, 5)	2.9 mm × 2.8 mm	2.9 mm × 1.6 mm

- (1) For more information, see [Section 11](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



## Table of Contents

<b>1 Features</b> .....	1	7.2 Functional Block Diagram.....	12
<b>2 Applications</b> .....	1	7.3 Feature Description.....	12
<b>3 Description</b> .....	1	7.4 Device Functional Modes.....	14
<b>4 Pin Configuration and Functions</b> .....	3	<b>8 Application and Implementation</b> .....	15
<b>5 Specifications</b> .....	4	8.1 Application Information.....	15
5.1 Absolute Maximum Ratings.....	4	8.2 Typical Application.....	15
5.2 ESD Ratings.....	4	8.3 Power Supply Recommendations.....	17
5.3 Recommended Operating Conditions.....	5	8.4 Layout.....	17
5.4 Thermal Information.....	6	<b>9 Device and Documentation Support</b> .....	19
5.5 Electrical Characteristics.....	7	9.1 Documentation Support.....	19
5.6 Switching Characteristics: 1.8-V $V_{CC}$ .....	8	9.2 Receiving Notification of Documentation Updates....	19
5.7 Switching Characteristics: 2.5-V $V_{CC}$ .....	8	9.3 Support Resources.....	19
5.8 Switching Characteristics: 3.3-V $V_{CC}$ .....	8	9.4 Trademarks.....	19
5.9 Switching Characteristics: 5.0-V $V_{CC}$ .....	8	9.5 Electrostatic Discharge Caution.....	19
5.10 Typical Characteristics.....	8	9.6 Glossary.....	19
<b>6 Parameter Measurement Information</b> .....	11	<b>10 Revision History</b> .....	19
<b>7 Detailed Description</b> .....	12	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	19
7.1 Overview.....	12		

## 4 Pin Configuration and Functions

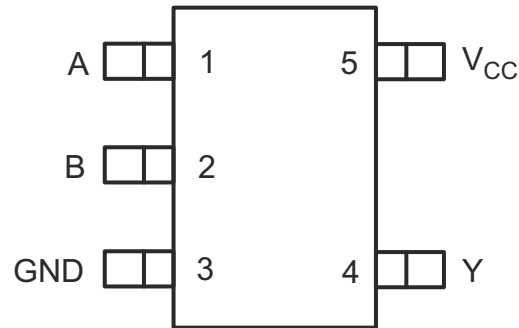


Figure 4-1. SN74LV1T08-Q1 DBV Package, 5-Pin SOT-23; DCK Package, 5-Pin SC-70 (Top View)

Table 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
A	1	I	Input A
B	2	I	Input B
GND	3	G	Ground
Y	4	O	Output Y
V <sub>CC</sub>	5	P	Positive Supply

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	-0.5	7	V
$V_I$	Input voltage range	-0.5	7	V
$V_O$	Output voltage range	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current <sup>(2)</sup>	$V_I < -0.5$ V	-20	mA
$I_{OK}$	Output clamp current <sup>(2)</sup>	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	±20	mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$	±25	mA
$I_O$	Continuous output current through $V_{CC}$ or GND		±50	mA
$T_{stg}$	Storage temperature	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD Classification Level 2	±2000
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC}$	Supply voltage		1.6	5.5	V
$V_I$	Input voltage		0	5.5	V
$V_O$	Output voltage		0	$V_{CC}$	V
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65\text{ V to }2\text{ V}$	1.1		V
		$V_{CC} = 2.25\text{ V to }2.75\text{ V}$	1.28		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	1.45		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.00		
$V_{IL}$	Low-Level input voltage	$V_{CC} = 1.65\text{ V to }2\text{ V}$		0.50	V
		$V_{CC} = 2.25\text{ V to }2.75\text{ V}$		0.65	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		0.75	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		0.85	
$I_O$	Output current	$V_{CC} = 1.65\text{ V to }2\text{ V}$		$\pm 3$	mA
		$V_{CC} = 2.25\text{ V to }2.75\text{ V}$		$\pm 7$	
		$V_{CC} = 3\text{ V to }5.5\text{ V}$		$\pm 15$	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.65\text{ V to }5.5\text{ V}$		20	ns/V
$T_A$	Operating free-air temperature		-40	125	$^{\circ}\text{C}$

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DBV (SOT-23)	DCK (SC-70)	UNIT
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278.0	293.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	180.5	208.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	184.4	180.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	115.4	120.6	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	183.4	179.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	1.65 V to 5.5 V	V <sub>CC</sub> -0.1			V <sub>CC</sub> -0.1			V
	I <sub>OH</sub> = -2 mA	1.65 V	1.28	1.7 <sup>(1)</sup>		1.21			
	I <sub>OH</sub> = -3 mA	2.25 V	2	2.4 <sup>(1)</sup>		1.93			
	I <sub>OH</sub> = -5.5 mA	3.0 V	2.6	3.08 <sup>(1)</sup>		2.49			
	I <sub>OH</sub> = -8 mA	4.5 V	4.1	4.65 <sup>(1)</sup>		3.95			
V <sub>OL</sub>	I <sub>OH</sub> = 50 μA	1.65 V to 5.5 V			0.1			0.1	V
	I <sub>OH</sub> = 2 mA	1.65 V		0.1 <sup>(1)</sup>	0.2			0.25	
	I <sub>OH</sub> = 3 mA	2.25 V		0.1 <sup>(1)</sup>	0.15			0.2	
	I <sub>OH</sub> = 5.5 mA	3.0 V		0.2 <sup>(1)</sup>	0.2			0.25	
	I <sub>OH</sub> = 8 mA	4.5 V		0.3 <sup>(1)</sup>	0.3			0.35	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5 V			0.12			±1	μA
		3.3 V			1			10	
		2.5 V			1			10	
		1.8 V			1			10	
ΔI <sub>CC</sub>	One input at 0.3 V or 3.4 V, other inputs at V <sub>CC</sub> or GND	5.5 V			1.35			1.5	mA
	One input at 0.3 V or 1.1 V, other inputs at V <sub>CC</sub> or GND	1.8 V			10			10	μA
I <sub>I</sub>	V <sub>I</sub> = 0 V to V <sub>CC</sub>				0.12			±1	μA
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		2	10		2	10	pF
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		2.5			2.5		pF
C <sub>PD</sub> <sup>(2) (3)</sup>	F = 1 MHz and 10 MHz	1.65 V to 5.5 V		14					pF

(1) Typical value at nearest nominal voltage (1.8 V; 2.5 V; 3.3 V; 5 V)

(2) C<sub>PD</sub> is used to determine the dynamic power consumption, per channel.

(3) P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> × F<sub>I</sub> × (C<sub>PD</sub> + C<sub>L</sub>) where F<sub>I</sub> = input frequency, C<sub>L</sub> = output load capacitance, V<sub>CC</sub> = supply voltage

### 5.6 Switching Characteristics: 1.8-V V<sub>CC</sub>

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PD</sub>	A or B	Y	CL = 15 pF	8.8	12.7		1	10.4	14.9	nS
			CL = 50 pF	10.8	15.7		1	12.7	18.3	

### 5.7 Switching Characteristics: 2.5-V V<sub>CC</sub>

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PD</sub>	A or B	Y	CL = 15 pF	6.3	7.9		7.4	9.5		nS
			CL = 50 pF	7.4	9.6		8.9	11.5		

### 5.8 Switching Characteristics: 3.3-V V<sub>CC</sub>

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PD</sub>	A or B	Y	CL = 15 pF	4.9	5.9		6	7.3		nS
			CL = 50 pF	5.9	7.2		7.1	8.8		

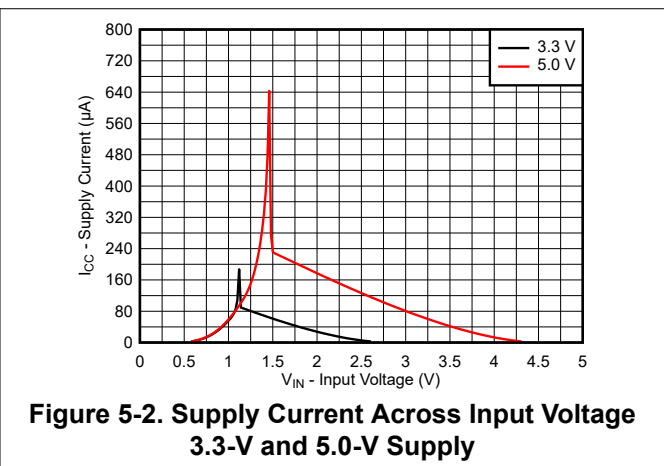
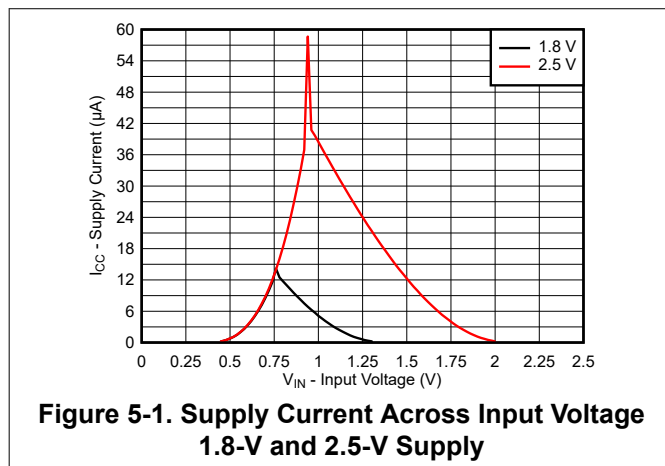
### 5.9 Switching Characteristics: 5.0-V V<sub>CC</sub>

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PD</sub>	A or B	Y	CL = 15 pF	3.4	4.1		4.1	4.7		nS
			CL = 50 pF	3.9	5.3		4.9	6.3		

### 5.10 Typical Characteristics

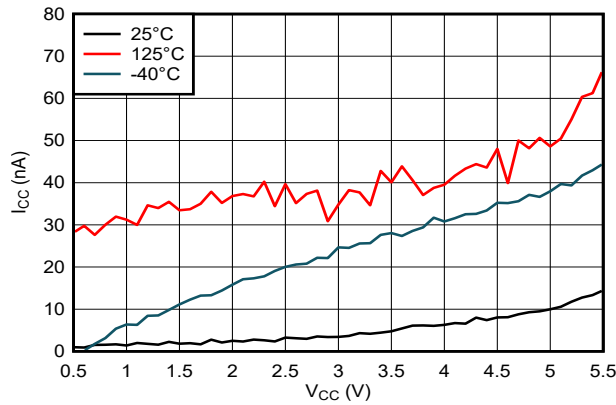
T<sub>A</sub> = 25°C (unless otherwise noted)



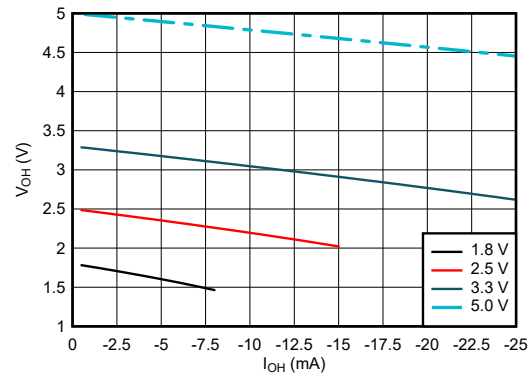


### 5.10 Typical Characteristics (continued)

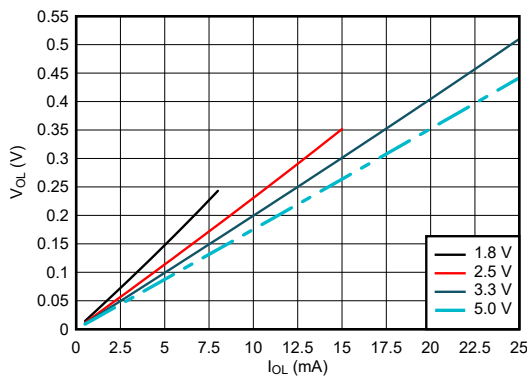
T<sub>A</sub> = 25°C (unless otherwise noted)



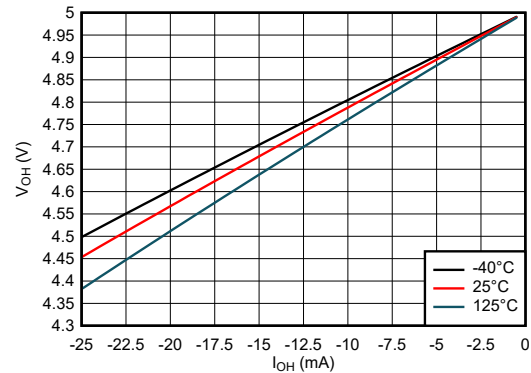
**Figure 5-3. Supply Current Across Supply Voltage**



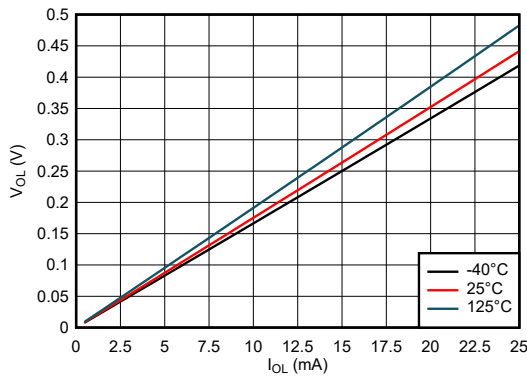
**Figure 5-4. Output Voltage vs Current in HIGH State**



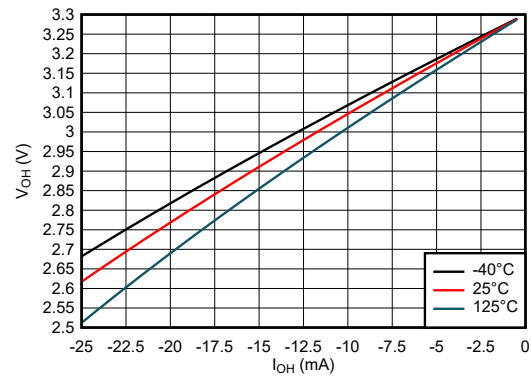
**Figure 5-5. Output Voltage vs Current in LOW State**



**Figure 5-6. Output Voltage vs Current in HIGH State; 5-V Supply**



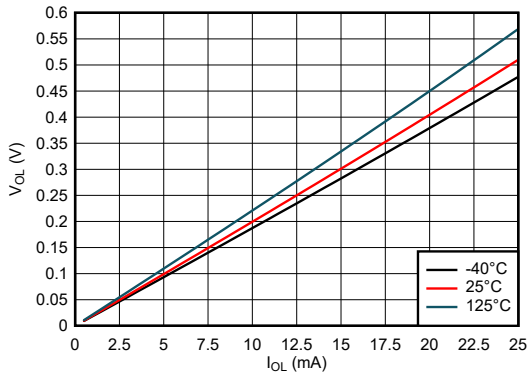
**Figure 5-7. Output Voltage vs Current in LOW State; 5-V Supply**



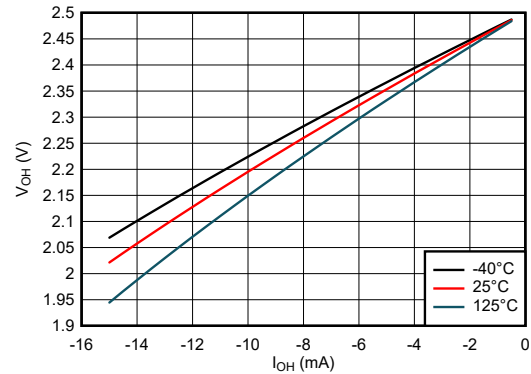
**Figure 5-8. Output Voltage vs Current in HIGH State; 3.3-V Supply**

### 5.10 Typical Characteristics (continued)

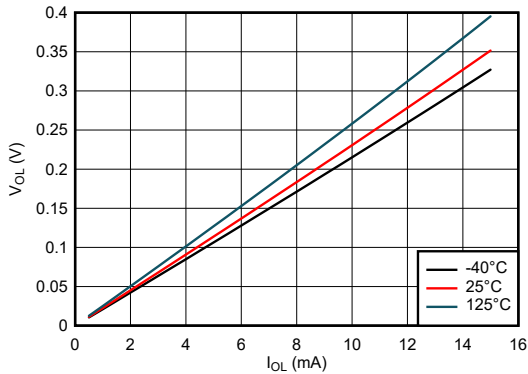
T<sub>A</sub> = 25°C (unless otherwise noted)



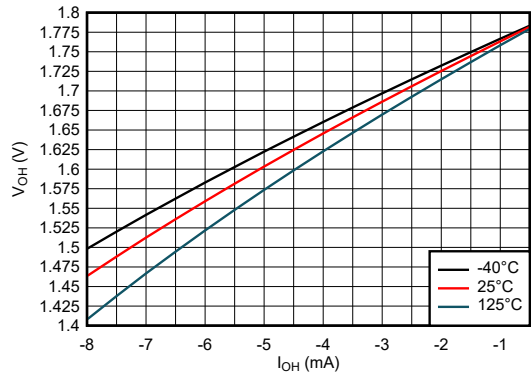
**Figure 5-9. Output Voltage vs Current in LOW State; 3.3-V Supply**



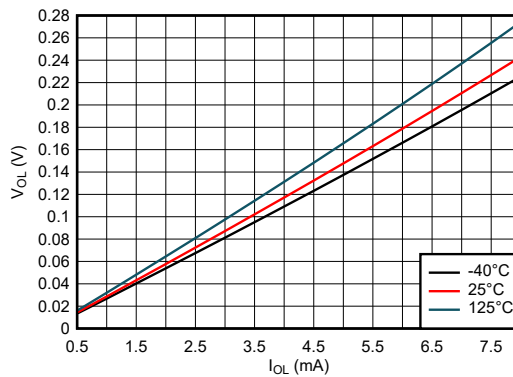
**Figure 5-10. Output Voltage vs Current in HIGH State; 2.5-V Supply**



**Figure 5-11. Output Voltage vs Current in LOW State; 2.5-V Supply**



**Figure 5-12. Output Voltage vs Current in HIGH State; 1.8-V Supply**



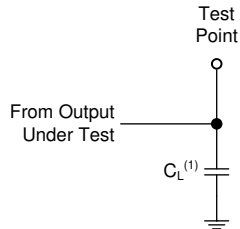
**Figure 5-13. Output Voltage vs Current in LOW State; 1.8-V Supply**

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \ \Omega$ ,  $t_t < 3 \text{ ns}$ .

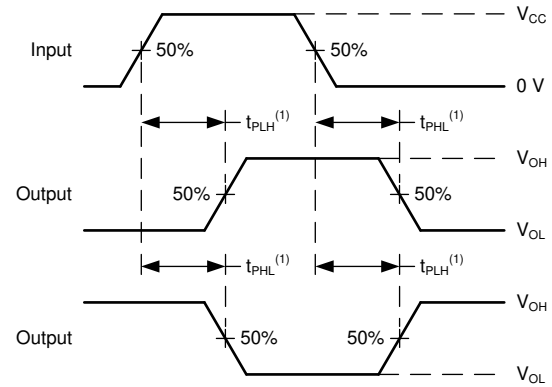
For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



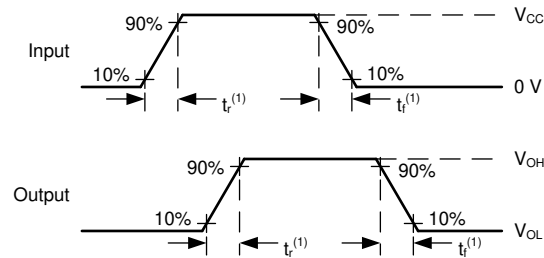
(1)  $C_L$  includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for Push-Pull Outputs**



(1) The greater between  $t_{pLH}$  and  $t_{pHL}$  is the same as  $t_{pd}$ .

**Figure 6-2. Voltage Waveforms Propagation Delays**



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

**Figure 6-3. Voltage Waveforms, Input and Output Transition Times**

## 7 Detailed Description

### 7.1 Overview

The SN74LV1T08-Q1 is a 2-input AND Gate. Each gate performs the Boolean function  $Y = A \times B$  in positive logic. The output level is referenced to the supply voltage ( $V_{CC}$ ) and supports 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

#### 7.3.2 LVxT Enhanced Input Voltage

The SN74LV1T08-Q1 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5 V levels to support down-translation. The output voltage will always be referenced to the supply voltage ( $V_{CC}$ ), as described in the *Electrical Characteristics* table. For proper functionality, input signals must remain at or below the specified  $V_{IH(MIN)}$  level for a HIGH input state, and at or below the specified  $V_{IL(MAX)}$  for a LOW input state. [Figure 7-1](#) shows the typical  $V_{IH}$  and  $V_{IL}$  levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the [Implications of Slow or Floating CMOS Inputs](#) application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at  $V_{CC}$  or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-k $\Omega$  resistor is recommended and will typically meet all requirements.

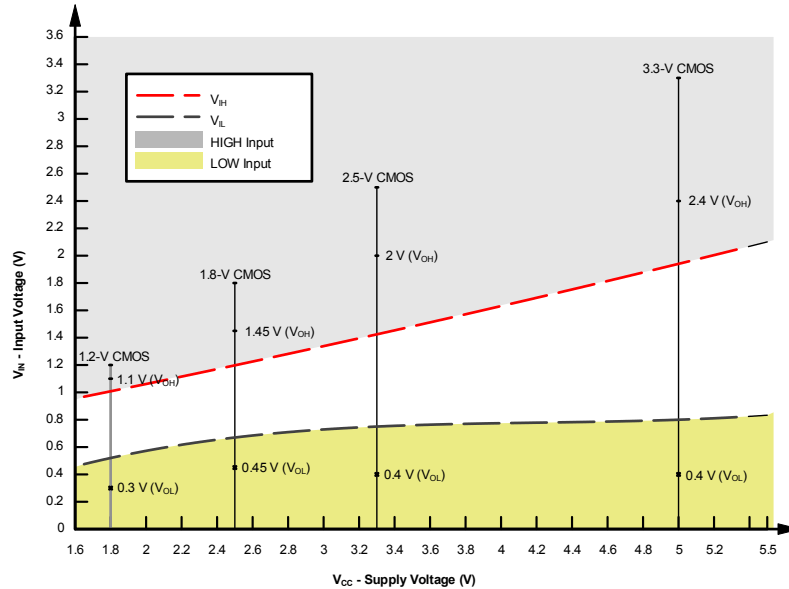


Figure 7-1. LVxT Input Voltage Levels

### 7.3.2.1 Down Translation

Signals can be translated down using the SN74LV1T08-Q1. The voltage applied at the  $V_{CC}$  will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately  $V_{CC}$  in the HIGH state, and 0 V in the LOW state. As shown in Figure 7-1, ensure that the input signals in the HIGH state are between  $V_{IH(MIN)}$  and 5.5 V, and input signals in the LOW state are lower than  $V_{IL(MAX)}$ .

As shown in Figure 7-2 for example, the standard CMOS inputs for devices operating at 5.0-V, 3.3-V or 2.5-V can be down-translated to match 1.8 V CMOS signals when operating from 1.8-V  $V_{CC}$ .

*Down Translation Combinations* are as follows:

- 1.8-V  $V_{CC}$  – Inputs from 2.5-V, 3.3-V, and 5.0-V
- 2.5-V  $V_{CC}$  – Inputs from 3.3-V and 5.0-V
- 3.3-V  $V_{CC}$  – Inputs from 5.0-V

### 7.3.2.2 Up Translation

Input signals can be up translated using the SN74LV1T08-Q1. The voltage applied at  $V_{CC}$  will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately  $V_{CC}$  in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5-V supply will have a  $V_{IH(MIN)}$  of 3.5 V. For the SN74LV1T08-Q1,  $V_{IH(MIN)}$  with a 5-V supply is only 2 V, which would allow for up-translation from a typical 2.5-V to 5-V signals.

As shown in Figure 7-2, ensure that the input signals in the HIGH state are above  $V_{IH(MIN)}$  and input signals in the LOW state are lower than  $V_{IL(MAX)}$ .

*Up Translation Combinations* are as follows:

- 1.8-V  $V_{CC}$  – Inputs from 1.2-V
- 2.5-V  $V_{CC}$  – Inputs from 1.8-V
- 3.3-V  $V_{CC}$  – Inputs from 1.8-V and 2.5-V

- 5.0-V  $V_{CC}$  – Inputs from 2.5-V and 3.3-V

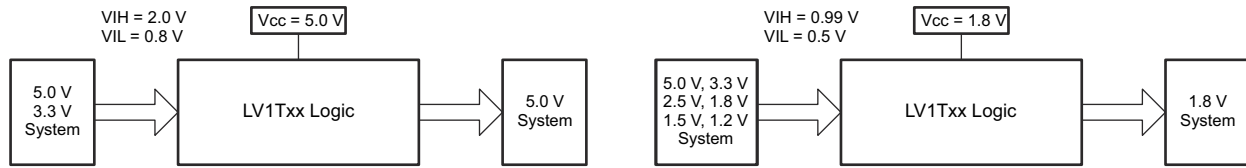


Figure 7-2. LVxT Up and Down Translation Example

### 7.3.3 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as shown in Figure 7-3.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

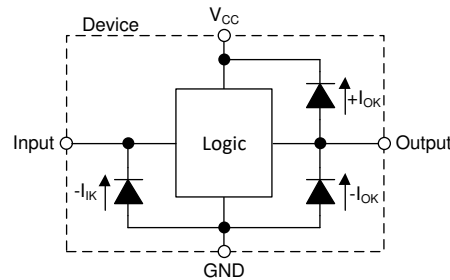


Figure 7-3. Electrical Placement of Clamping Diodes for Each Input and Output

### 7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74LV1T08-Q1.

Table 7-1. Function Table

INPUTS <sup>(1)</sup>		OUTPUT
A	B	Y
L	X	L
X	L	L
H	H	H

(1) H = high voltage level, L = low voltage level, X = do not care, Z = high impedance

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

In this application, three 2-input AND gates are combined to produce a 4-input AND gate function as shown in Figure 8-1. Multiple SN74LV1T08-Q1 are used to directly control the  $\overline{\text{RESET}}$  pin of a motor controller. The controller requires four input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 4-input AND gate function combines the four individual reset signals into a single active-low reset signal.

### 8.2 Typical Application

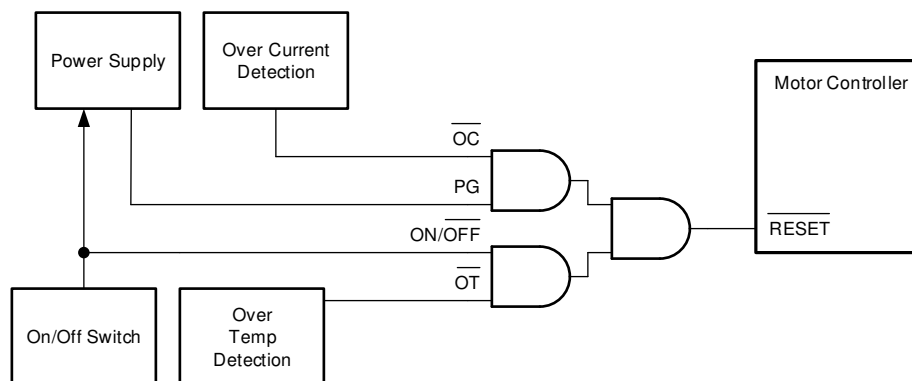


Figure 8-1. Typical Application Block Diagram

#### 8.2.1 Design Requirements

##### 8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV1T08-Q1 plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV1T08-Q1 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV1T08-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV1T08-Q1 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in the [CMOS Power Consumption and Cpd Calculation](#) application note.

Thermal increase can be calculated using the information provided in the [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#) application note.

#### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 8.2.1.2 Input Considerations

Input signals must cross  $V_{IL(max)}$  to be considered a logic LOW, and  $V_{IH(min)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV1T08-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k $\Omega$  resistor value is often used due to these factors.

The SN74LV1T08-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.



## 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50$  pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV1T08-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ , so that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in  $M\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

## 8.2.3 Application Curves

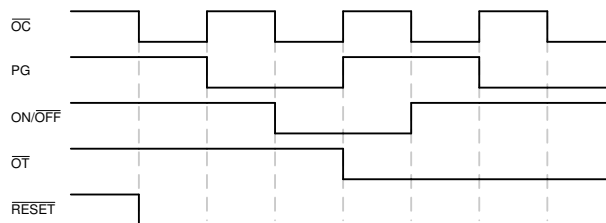


Figure 8-2. Application Timing Diagram

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 8.4.2 Layout Example

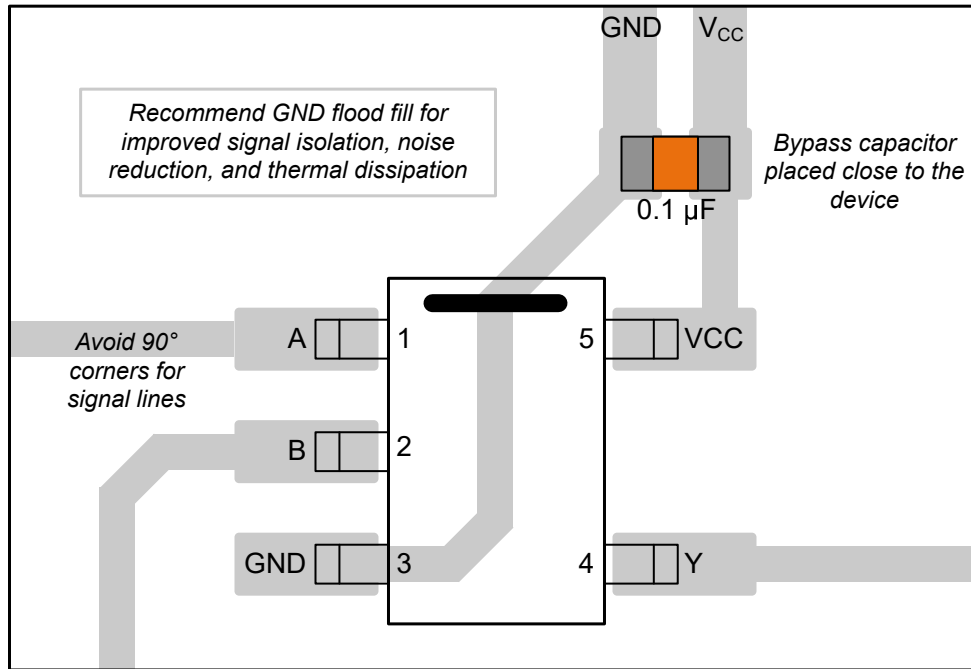


Figure 8-3. Example Layout for the SN74LV1T08-Q1

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.4 Trademarks

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### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

Changes from Revision * (July 2023) to Revision A (January 2024)	Page
• Added DBV package to <i>Package Information</i> table.....	1
• Added DBV package to <i>Pin Configuration and Functions</i> section.....	3
• Added thermal values for DBV package: R $\theta$ JA = 278.0, R $\theta$ JC(top) = 180.5, R $\theta$ JB = 184.4, $\Psi$ JT = 115.4, $\Psi$ JB = 183.4, R $\theta$ JC(bot) = N/A, all values in °C/W.....	6

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV1T08QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	39SH	<a href="#">Samples</a>
SN74LV1T08QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1PH	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LV1T08-Q1 :**

- Catalog : [SN74LV1T08](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV1T08QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LV1T08QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV1T08QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LV1T08QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0

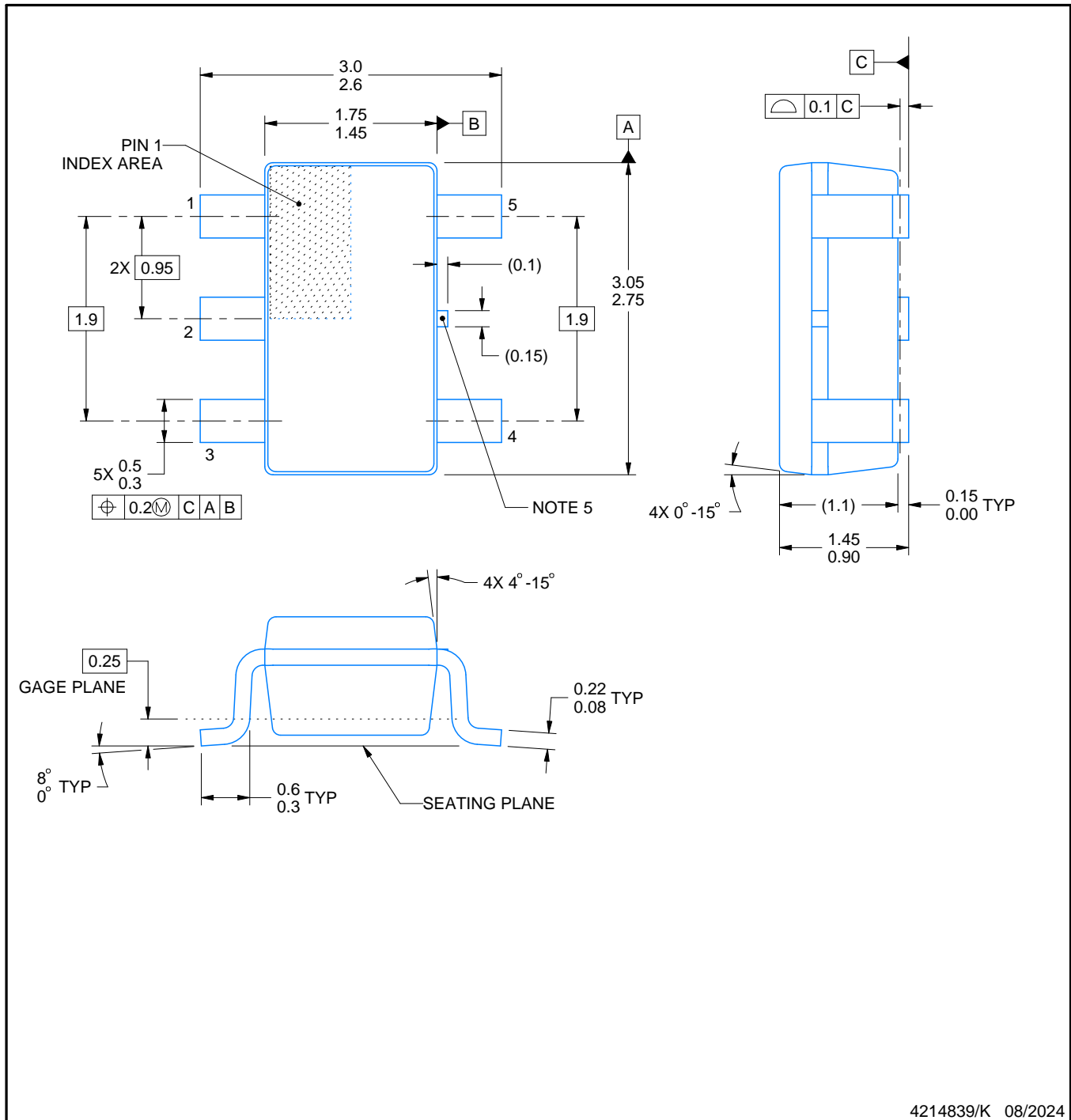
# DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

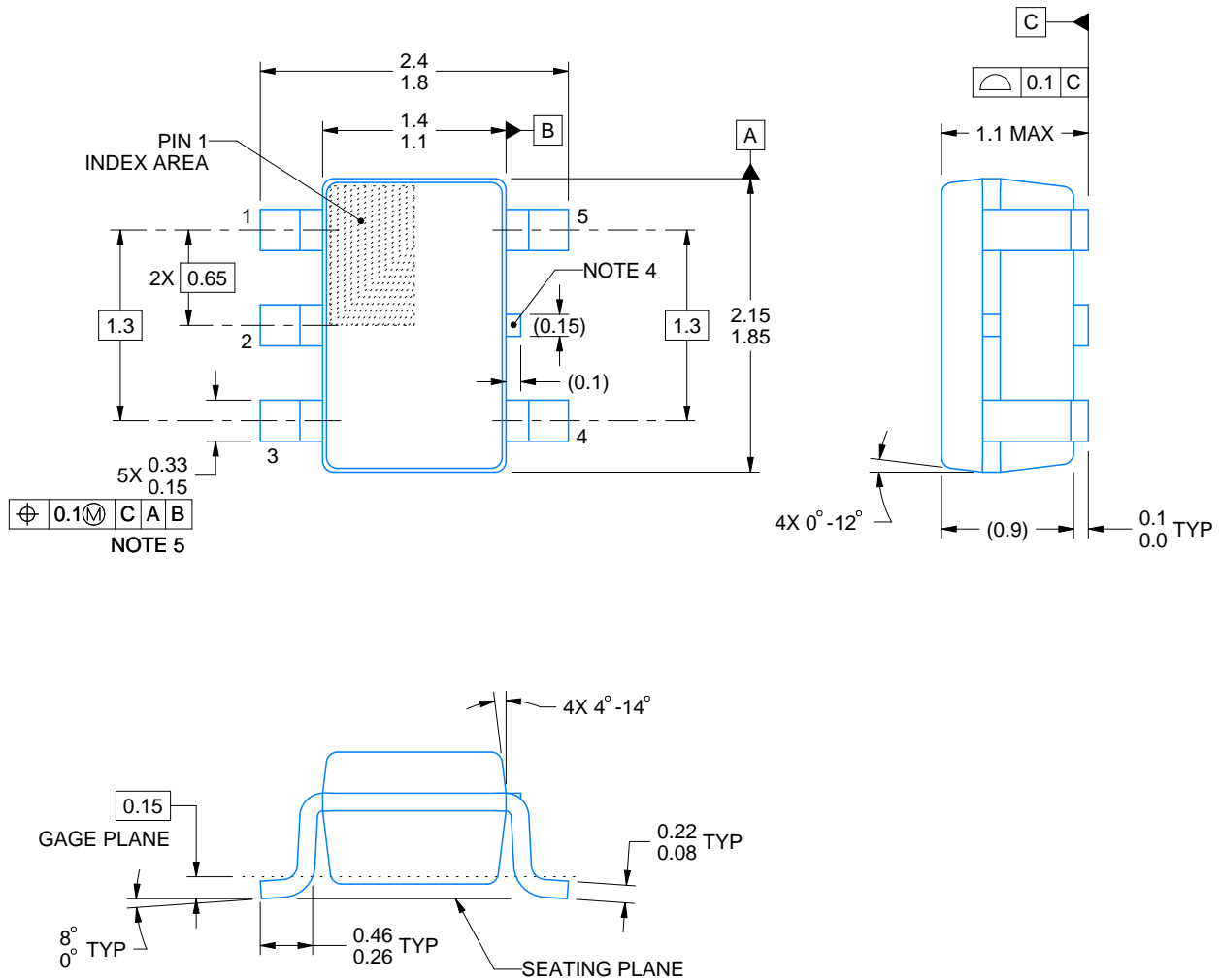
# DCK0005A



# PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/F 08/2024

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/F 08/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE: 18X

4214834/F 08/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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