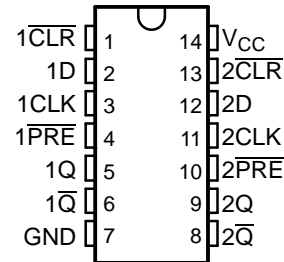


FEATURES

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of– 55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree ⁽¹⁾**
- **2-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 13 ns at 5 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3 V$, $T_A = 25^\circ C$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3 V$, $T_A = 25^\circ C$**
- **Supports Mixed-Mode Voltage Operation on All Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

These dual positive-edge-triggered D-type flip-flops are designed for 2-V to 5.5-V V_{CC} operation.

A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	TSSOP – PW	Reel of 2000	SN74LV74AMPWREP	LV74AEP

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	7	V
V_I	Input voltage range ⁽²⁾	-0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	7	V
V_O	Output voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-20	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}	± 25	mA
	Continuous current through V_{CC} or GND		± 50	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾		113	°C/W
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LV74A-EP DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

SCLS696–JANUARY 2006

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	μA
		V _{CC} = 2.3 V to 2.7 V	-2	mA
		V _{CC} = 3 V to 3.6 V	-6	
		V _{CC} = 4.5 V to 5.5 V	-12	
I _{OL}	Low-level output current	V _{CC} = 2 V	50	μA
		V _{CC} = 2.3 V to 2.7 V	2	mA
		V _{CC} = 3 V to 3.6 V	6	
		V _{CC} = 4.5 V to 5.5 V	12	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	200	ns/V
		V _{CC} = 3 V to 3.6 V	100	
		V _{CC} = 4.5 V to 5.5 V	20	
T _A	Operating free-air temperature	-55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} - 0.1		V	
	I _{OH} = -2 mA	2.3 V	2			
	I _{OH} = -6 mA	3 V	2.48			
	I _{OH} = -12 mA	4.5 V	3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1		V	
	I _{OL} = 2 mA	2.3 V	0.4			
	I _{OL} = 6 mA	3 V	0.44			
	I _{OL} = 12 mA	4.5 V	0.55			
I _I	V _I = 5.5 V or GND	0 to 5.5 V	±1		μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20		μA	
I _{off}	V _I or V _O = 0 to 5.5 V	0	5		μA	
C _i	V _I = V _{CC} or GND	3.3 V	2		pF	
		5 V	2			

Timing Requirements

over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER			$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	8		9		ns
		CLK	8		9		
t_{su}	Setup time before $\text{CLK}\uparrow$	Data	8		9		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	7		7		
t_h	Hold time, data after $\text{CLK}\uparrow$		0.5		0.5		ns

Timing Requirements

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER			$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	6		7		ns
		CLK	6		7		
t_{su}	Setup time before $\text{CLK}\uparrow$	Data	6		7		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	5		5		
t_h	Hold time, data after $\text{CLK}\uparrow$		1.45		2.15		ns

Timing Requirements

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER			$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	5		5		ns
		CLK	5		5		
t_{su}	Setup time before $\text{CLK}\uparrow$	Data	5		5		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	3		3		
t_h	Hold time, data after $\text{CLK}\uparrow$		1.45		2.15		ns

Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			$C_L = 50\text{ pF}$	30	70		25		MHz
t_{pd}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or \overline{Q}	$C_L = 50\text{ pF}$		13	17.4	1	20	ns
	CLK				14.2	20	1	23	

SN74LV74A-EP DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

SCLS696–JANUARY 2006

Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{\max}			$C_L = 50 \text{ pF}$	50	90		45		MHz
t_{pd}	PRE or CLR	Q or \bar{Q}	$C_L = 50 \text{ pF}$		9.2	15.8	1	18	ns
	CLK				10.2	15.4	1	18	

Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{\max}			$C_L = 50 \text{ pF}$	90	140		75		MHz
t_{pd}	PRE or CLR	Q or \bar{Q}	$C_L = 50 \text{ pF}$		6.6	9.7	1	12	ns
	CLK				7.2	9.9	1	13	

Noise Characteristics⁽¹⁾

$V_{CC} = 3.3 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.1	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		0	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.2		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

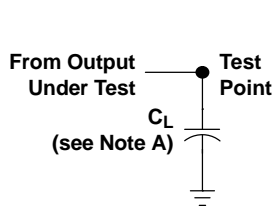
(1) Characteristics are for surface-mount packages only.

Operating Characteristics

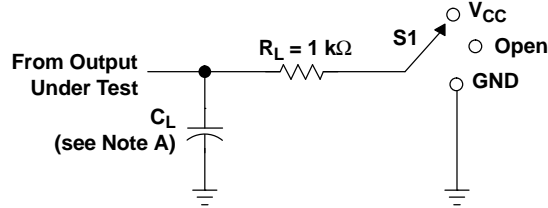
$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50 \text{ pF}$,	$f = 10 \text{ MHz}$	3.3 V	21	pF
				5 V	23	

PARAMETER MEASUREMENT INFORMATION

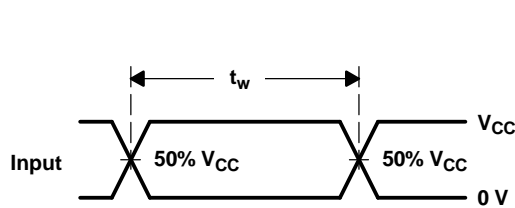


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

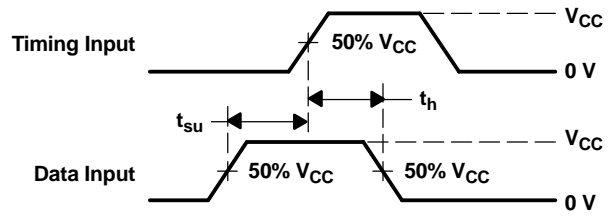


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

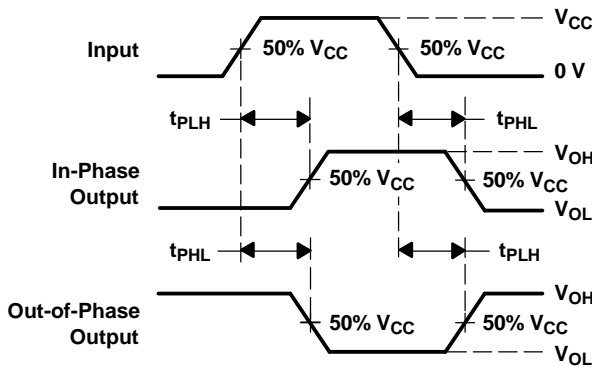
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



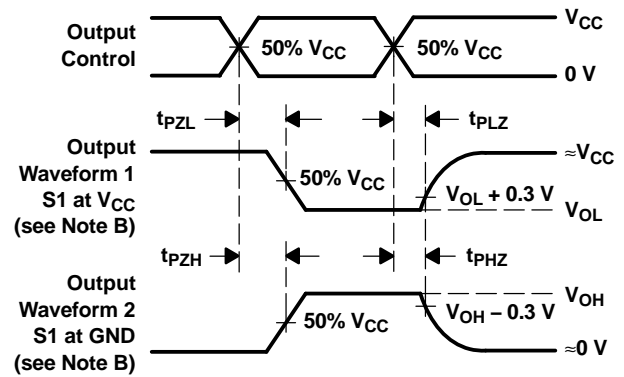
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 D. The outputs are measured one at a time, with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV74AMPWREP	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LV74AEP	Samples
V62/06605-01XE	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LV74AEP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LV74A-EP :

- Catalog: [SN74LV74A](#)
- Automotive: [SN74LV74A-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV74AMPWREP	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV74AMPWREP	TSSOP	PW	14	2000	356.0	356.0	35.0

PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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