- **2-V to 5.5-V V_{CC} Operation**
- **Unbuffered Outputs**
- **Max t_{pd} of 6.5 ns at 5 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C**

- **Support Mixed-Mode Voltage Operation on All Ports**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SN54LVU04A . . . J OR W PACKAGE
SN74LVU04A . . . D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)

1A	1	14	V_{CC}
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y
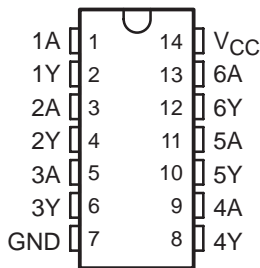
SN74LVU04A . . . RGY PACKAGE
(TOP VIEW)

1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A

Pin 1 = 1A, Pin 14 = V_{CC}, Pin 7 = GND, Pin 8 = 4Y

SN54LVU04A . . . FK PACKAGE
(TOP VIEW)

Top pins: 1Y (3), 1A (2), NC (1), V_{CC} (20), 6A (19)

2A	4	18	6Y
NC	5	17	NC
2Y	6	16	5A
NC	7	15	NC
3A	8	14	5Y

Bottom pins: 3Y (9), GND (10), NC (11), 4Y (12), 4A (13)

NC – No internal connection

description/ordering information

These hex inverters are designed for 2-V to 5.5-V V_{CC} operation.

The 'LVU04A devices contain six independent inverters with unbuffered outputs. These devices perform the Boolean function Y = $\overline{A}$.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVU04ARGYR	LVU04A
	SOIC – D	Tube of 50	SN74LVU04AD	LVU04A
		Reel of 2500	SN74LVU04ADR	
	SOP – NS	Reel of 2000	SN74LVU04ANSR	LVU04A
	SSOP – DB	Reel of 2000	SN74LVU04ADBR	LU04A
	TSSOP – PW	Tube of 90	SN74LVU04APW	LU04A
		Reel of 2000	SN74LVU04APWR	
		Reel of 250	SN74LVU04APWT	
	TVSOP – DGV	Reel of 2000	SN74LVU04ADGVR	LU04A
−55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVU04AJ	SNJ54LVU04AJ
	CFP – W	Tube of 150	SNJ54LVU04AW	SNJ54LVU04AW
	LCCC – FK	Tube of 85	SNJ54LVU04AFK	SNJ54LVU04AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
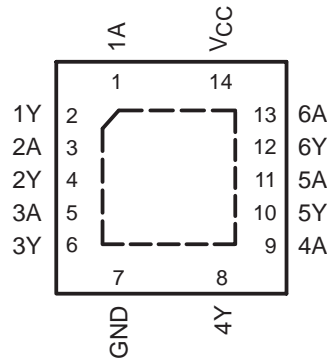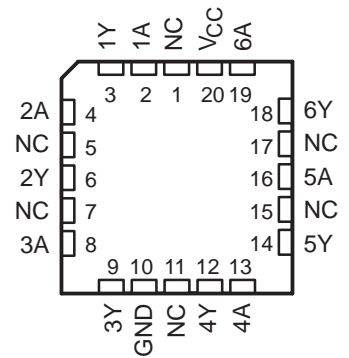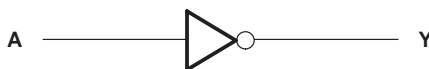
TEXAS INSTRUMENTS

SN54LVU04A, SN74LVU04A
HEX INVERTERS

SCES130L – MARCH 1998 – REVISED DECEMBER 2004

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram, each inverter (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2) . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) . . . . –20 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . –50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . 86°C/W
(see Note 3): DB package . . . . 96°C/W
(see Note 3): DGV package . . . . 127°C/W
(see Note 3): NS package . . . . 76°C/W
(see Note 3): PW package . . . . 113°C/W
(see Note 4): RGY package . . . . 47°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LVU04A		SN74LVU04A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.7		1.7		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.8$		$V_{CC} \times 0.8$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.8$		$V_{CC} \times 0.8$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.8$		$V_{CC} \times 0.8$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.3		0.3	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.2$		$V_{CC} \times 0.2$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.2$		$V_{CC} \times 0.2$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.2$		$V_{CC} \times 0.2$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	µA
		V_{CC} = 2.3 V to 2.7 V		−2		−2	mA
		V_{CC} = 3 V to 3.6 V		−6		−6	
		V_{CC} = 4.5 V to 5.5 V		−12		−12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		12		12	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LVU04A			SN74LVU04A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = −50 µA	2 V to 5.5 V	V_{CC}−0.1			V_{CC}−0.1			V
	I_{OH} = −2 mA	2.3 V	2			2			
	I_{OH} = −6 mA	3 V	2.48			2.48			
	I_{OH} = −12 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4	
	I_{OL} = 6 mA	3 V			0.44			0.44	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±1			±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	µA
C_i	V_I = V_{CC} or GND	3.3 V		4			4		pF

TEXAS INSTRUMENTS

SN54LVU04A, SN74LVU04A
HEX INVERTERS

switching characteristics over recommended operating free-air temperature range, V$_{CC}$ = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T$_A$ = 25°C			SN54LVU04A		SN74LVU04A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t$_{pd}$	A	Y	C$_L$ = 15 pF		3.2*	10.9*	1*	14*	1	14	ns
			C$_L$ = 50 pF		6.6	13.4	1	16	1	16	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V$_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T$_A$ = 25°C			SN54LVU04A		SN74LVU04A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t$_{pd}$	A	Y	C$_L$ = 15 pF		2.5*	8.9*	1*	10.5*	1	10.5	ns
			C$_L$ = 50 pF		4.7	11.4	1	13	1	13	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V$_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T$_A$ = 25°C			SN54LVU04A		SN74LVU04A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t$_{pd}$	A	Y	C$_L$ = 15 pF		2.2*	5.5*	1*	6.5*	1	6.5	ns
			C$_L$ = 50 pF		3.9	7	1	8	1	8	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V$_{CC}$ = 3.3 V, C$_L$ = 50 pF, T$_A$ = 25°C (see Note 6)

PARAMETER		SN74LVU04A			UNIT
		MIN	TYP	MAX	
V$_{OL(P)}$	Quiet output, maximum dynamic V$_{OL}$		0.5	0.8	V
V$_{OL(V)}$	Quiet output, minimum dynamic V$_{OL}$		−0.1	−0.8	V
V$_{OH(V)}$	Quiet output, minimum dynamic V$_{OH}$		3		V
V$_{IH(D)}$	High-level dynamic input voltage	2.31			V
V$_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics, T$_A$ = 25°C

PARAMETER		TEST CONDITIONS	V$_{CC}$	TYP	UNIT
C$_{pd}$	Power dissipation capacitance	C$_L$ = 50 pF, f = 10 MHz	3.3 V	5.6	pF
			5 V	6.7	

![Texas Instruments logo]

TEXAS INSTRUMENTS

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVU04AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	LVU04A	
SN74LVU04ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LU04A	Samples
SN74LVU04ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVU04A	Samples
SN74LVU04ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVU04A	Samples
SN74LVU04APW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	LU04A	
SN74LVU04APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LU04A	Samples
SN74LVU04APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LU04A	Samples
SN74LVU04APWT	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	LU04A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVU04A :

● Automotive : SN74LVU04A-Q1

NOTE: Qualified Version Definitions:

● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVU04ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVU04ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVU04ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVU04APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVU04ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LVU04ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LVU04ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LVU04APWR	TSSOP	PW	14	2000	356.0	356.0	35.0

SEATING PLANE

$\boxed{\triangle}$ $\boxed{0.1}$ $\boxed{C}$

$\boxed{C}$

$\frac{6.2}{5.8}$ TYP

PIN 1 ID
AREA

12X $\boxed{1.27}$

2X $\boxed{7.62}$

1

14

7

8

$\frac{8.75}{8.55}$
NOTE 3

A

B

$\frac{4.0}{3.8}$
NOTE 4

14X $\frac{0.51}{0.31}$

$\boxed{\oplus}$ $\boxed{0.25\text{\textcircled{M}}}$ $\boxed{C}$ $\boxed{A}$ $\boxed{B}$

1.75 MAX

SEE DETAIL A

$\frac{0.25}{0.13}$ TYP

$\boxed{0.25}$

GAGE PLANE

0° - 8°

$\frac{1.27}{0.40}$

$\frac{0.25}{0.10}$

DETAIL A
TYPICAL

4220718/A   09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

14X (1.55)

1

14X (0.6)

12X (1.27)

SYMM

14

8

SYMM

7

(R0.05)
TYP

(5.4)

LAND PATTERN EXAMPLE
SCALE:8X

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A   09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A   09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
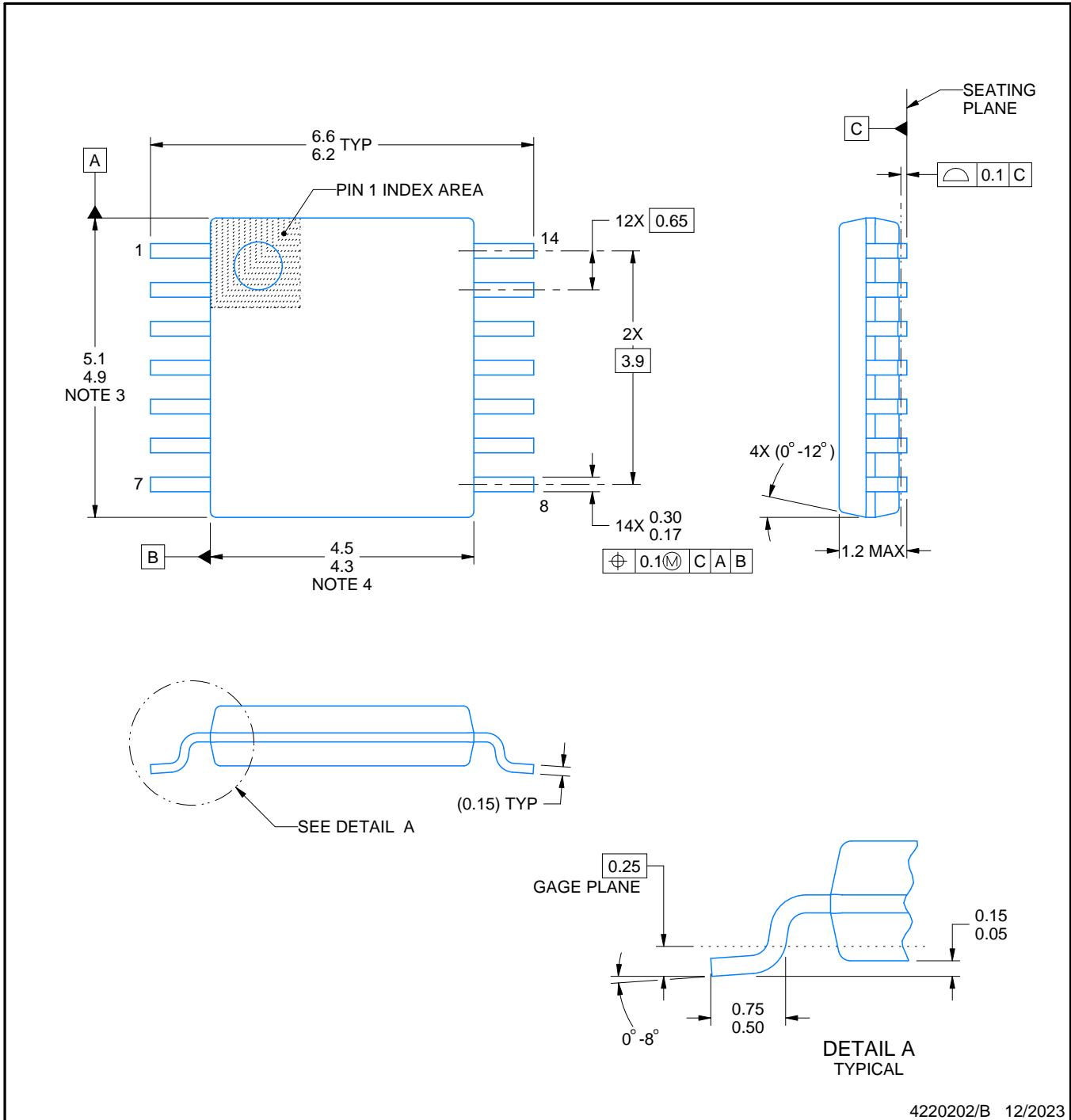
MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

8.2 / 7.4 TYP

A

PIN 1 INDEX AREA

1

6.5 / 5.9
NOTE 3

7

B

5.6 / 5.0
NOTE 4

14

12X 0.65

2X

3.9

8

14X 0.38 / 0.22

⊕ 0.15 Ⓜ C A B

C

◠ 0.1 C

SEATING PLANE

0.25 / 0.09

SEE DETAIL A

0.25

GAGE PLANE

0° -8°

0.95 / 0.55

2 MAX

0.05 MIN

DETAIL A
TYPICAL

4220762/A   05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

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14X (1.85)

1

14X (0.45)

12X (0.65)

7

SYMM

(R0.05) TYP

14

SYMM

8

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220762/A   05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

14X (1.85)

14X (0.45)

12X (0.65)

SYMM

SYMM

(R0.05) TYP

1

14

7

8

(7)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A   05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

6.6
6.2 TYP

A

PIN 1 INDEX AREA

1

5.1
4.9
NOTE 3

7

14

12X 0.65

2X

3.9

8

14X 0.30
0.17

⊕ 0.1 Ⓜ C A B

B

4.5
4.3
NOTE 4

SEATING
PLANE

C

⬜ 0.1 C

4X (0° -12°)

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0.15
0.05

0° -8°

0.75
0.50

DETAIL A
TYPICAL

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

TEXAS
INSTRUMENTS
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14X (1.5)

14X (0.45)

1

SYMM
℄

(R0.05) TYP

14

SYMM
℄

12X (0.65)

7

8

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

14X (1.5)

SYMM

(R0.05) TYP

1

14X (0.45)

14

SYMM

12X (0.65)

7

8

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.