

SN75476 THRU SN75478 DUAL PERIPHERAL DRIVERS

SLRS025A – DECEMBER 1976 – REVISED NOVEMBER 1995

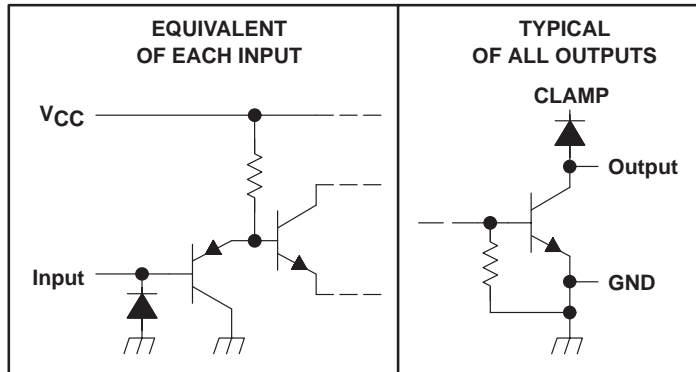
- Characterized for Use to 300 mA
- No Output Latch-Up at 55 V (After Conducting 300 mA)
- High-Voltage Outputs (100 V Typ)
- Output Clamp Diodes for Transient Suppression (300 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- pnp Transistor Inputs Reduce Input Current
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications
- Plastic DIP (P) With Copper-Lead Frame Provides Cooler Operation and Improved Reliability

description

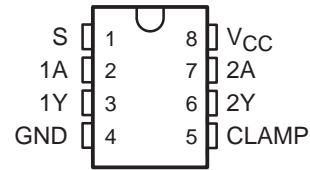
The SN75476 through SN75478 are dual peripheral drivers designed for use in systems that require high current, high voltage, and fast switching times. The SN75476, SN75477, and SN75478 provide AND, NAND, and OR drivers respectively. These devices have diode-clamped inputs as well as high-current, high-voltage clamp diodes on the outputs for inductive transient protection.

The SN75476, SN75477, and SN75478 drivers are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



D OR P PACKAGE
(TOP VIEW)



Function Tables

SN75476
(each AND driver)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | S | Y |
| H | H | H |
| L | X | L |
| X | L | L |

SN75477
(each NAND driver)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | S | Y |
| H | H | L |
| L | X | H |
| X | L | H |

SN75478
(each OR driver)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | S | Y |
| H | X | H |
| X | H | H |
| L | L | L |

H = high level, L = low level
X = irrelevant

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

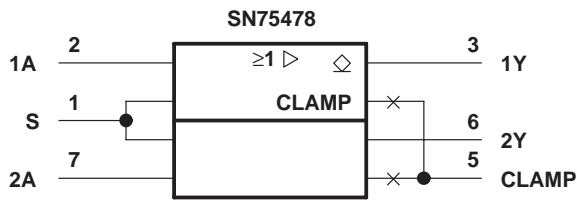
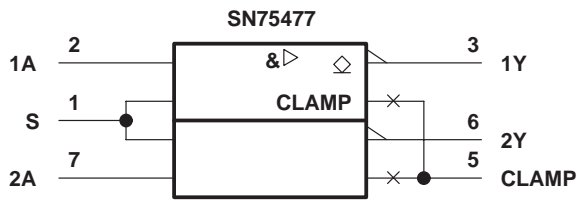
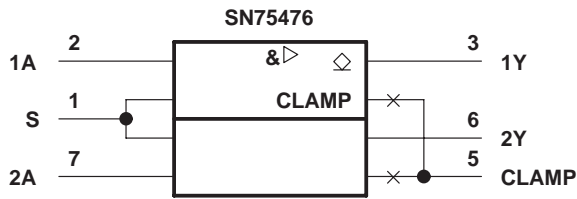


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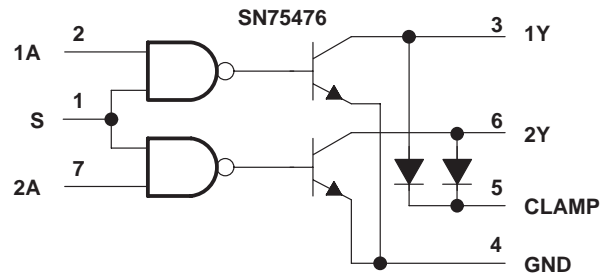
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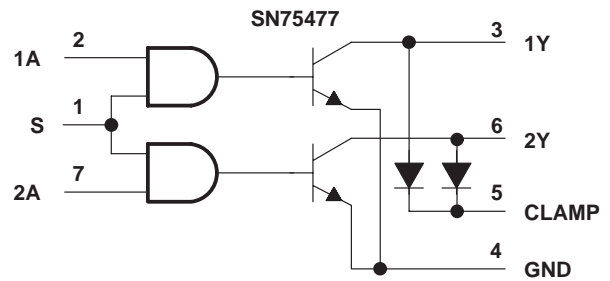
logic symbols†



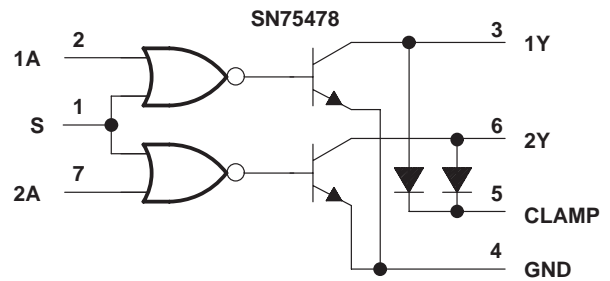
logic diagrams (positive logic)



Positive Logic: $Y = AS$ or $\overline{A+S}$



Positive Logic: $Y = \overline{AS}$ or $\overline{A+S}$



Positive Logic: $Y = A+S$ or $\overline{\overline{A} \overline{S}}$

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|------------------------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage, V_I | 5.5 V |
| Continuous output current (see Note 2) | 400 mA |
| Peak output current: $t_w \leq 10$ ms, duty cycle $\leq 50\%$ | 500 mA |
| $t_w \leq 30$ ns, duty cycle $\leq 0.002\%$ | 3 A |
| Output clamp current, I_{OK} | 400 mA |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A | 0°C to 70°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

- NOTES: 1. Voltage values are with respect to network GND.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous power dissipation ratings.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING |
|---------|---|---|--|
| D | 725 mW | 5.8 mW/°C | 464 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---------------------------------------|-----|-----|-----|------|
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | V |
| High-level input voltage, V_{IH} | 2 | | | V |
| Low-level input voltage, V_{IL} | | | 0.8 | V |
| Operating free-air temperature, T_A | 0 | | 70 | °C |



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electrical characteristics over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|--------------------|------------------------------|---|--|----------------------|------|------|------|
| V _{IK} | Input clamp voltage | I _I = -12 mA | | -0.95 | -1.5 | | V |
| V _{OL} | Low-level output voltage | V _{CC} = 4.5 V, V _{IH} = 2 V, V _{IL} = 0.8 V | I _{OL} = 100 mA | 0.16 | 0.3 | | V |
| | | | I _{OL} = 175 mA | 0.22 | 0.5 | | |
| | | | I _{OL} = 300 mA | 0.33 | 0.6 | | |
| V _{O(BR)} | Output breakdown voltage | V _{CC} = 4.5 V, | I _{OH} = 100 μA | 70 | 100 | | V |
| V _{R(K)} | Output clamp reverse voltage | V _{CC} = 4.5 V, | I _R = 100 μA | 70 | 100 | | V |
| V _{F(K)} | Output clamp forward voltage | V _{CC} = 4.5 V, | I _F = 300 mA | 0.8 | 1.15 | 1.6 | V |
| I _{OH} | High-level output current | V _{CC} = 4.5 V, V _{IL} = 0.8 V, | V _{IH} = 2 V, V _{OH} = 70 V | | 1 | 100 | μA |
| I _{IH} | High-level input current | V _{CC} = 5.5 V, | V _I = 5.5 V | | 0.01 | 10 | μA |
| I _{IL} | Low-level input current | A input | V _{CC} = 5.5 V, V _I = 0.8 V | | -80 | -110 | μA |
| | | S input | | | -160 | -220 | |
| I _{CCH} | Supply current, outputs high | SN75476 | V _{CC} = 5.5 V | V _I = 5 V | 10 | 17 | mA |
| | | SN75477 | | V _I = 0 | 10 | 17 | |
| | | SN75478 | | V _I = 5 V | 10 | 17 | |
| I _{CCL} | Supply current, outputs low | SN75476 | V _{CC} = 5.5 V | V _I = 0 | 54 | 75 | mA |
| | | SN75477 | | V _I = 5 V | 54 | 75 | |
| | | SN75478 | | V _I = 0 | 54 | 75 | |

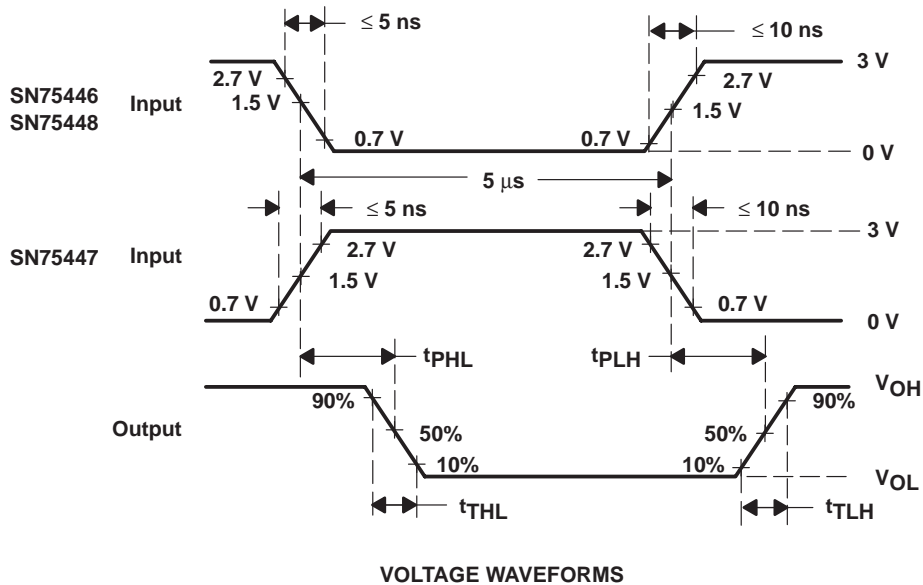
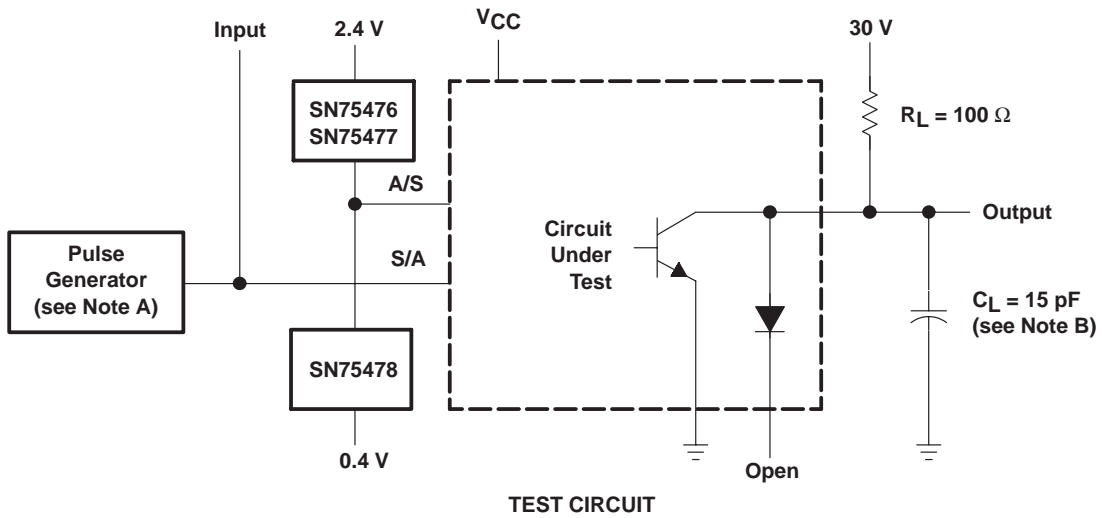
† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|--|--|--------------------------|--------------------|-----|-----|------|
| t _{PLH} | Propagation delay time, low-to-high-level output | C _L = 15 pF, R _L = 100 Ω, See Figure 1 | | | 200 | 350 | ns |
| t _{PHL} | Propagation delay time, high-to-low-level output | | | | 200 | 350 | ns |
| t _{TLH} | Transition time, low-to-high-level output | | | | 50 | 125 | ns |
| t _{THL} | Transition time, high-to-low-level output | | | | 90 | 125 | ns |
| V _{OH} | High-level output voltage after switching | V _S = 55 V, See Figure 2 | I _O ≈ 300 mA, | V _S -18 | | | mV |



PARAMETER MEASUREMENT INFORMATION



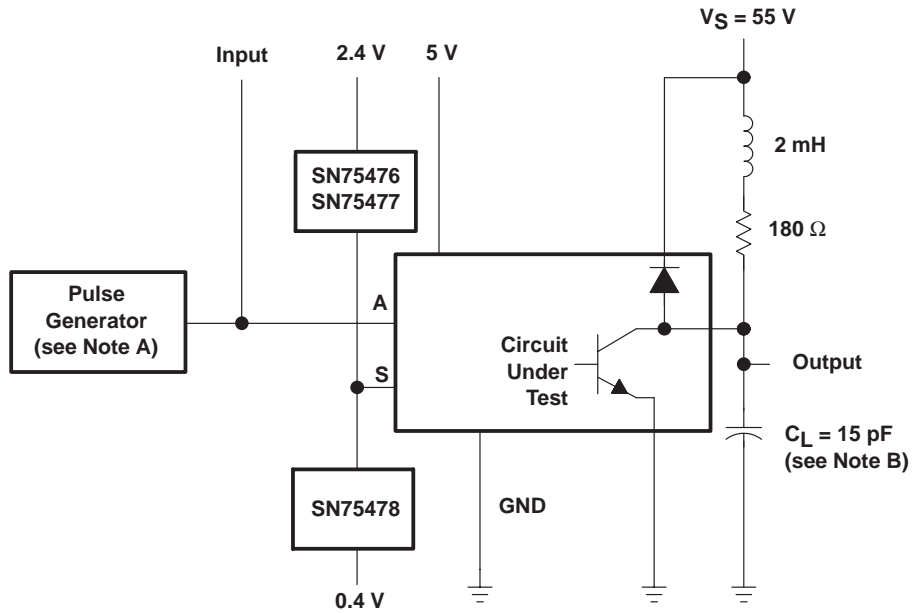
- NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Switching Characteristics

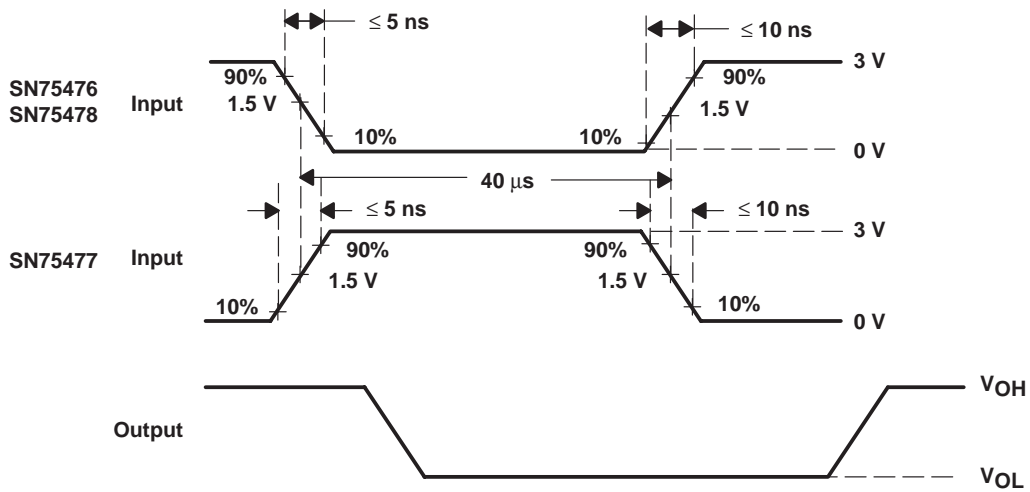
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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_0 = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 2. Latch-Up Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN75477D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75477 | Samples |
| SN75477DE4 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75477 | Samples |
| SN75477DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75477 | Samples |
| SN75477DRE4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75477 | Samples |
| SN75477P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN75477P | Samples |
| SN75477PE4 | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN75477P | Samples |
| SN75478P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN75478P | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75477DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75477DR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN75477D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN75477DE4 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN75477P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN75477PE4 | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN75478P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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