TEXAS INSTRUMENTS

TL1431, TL1431M

SLVS062N – DECEMBER 1991 – REVISED OCTOBER 2016

TL1431 Precision Programmable Reference

1 Features

- 0.4% Initial Voltage Tolerance
- 0.2-Ω Typical Output Impedance
- Fast Turnon (500 ns)
- Sink Current Capability (1 mA to 100 mA)
- Low Reference Current (REF)
- Adjustable Output Voltage ($V_{I(ref)}$ to 36 V)

2 Applications

- Adjustable Voltage and Current Referencing
- Secondary Side Regulation in Flyback SMPSs
- Zener Replacement
- Voltage Monitoring
- Comparator With Integrated Reference

3 Description

The TL1431 device is a precision programmable reference with specified thermal stability over automotive, commercial, and military temperature ranges. The output voltage can be set to any value between $V_{I(ref)}$ (approximately 2.5 V) and 36 V with two external resistors (see Figure 25). This device has a typical output impedance of 0.2 Ω. Active output circuitry provides a sharp turnon characteristic, making the device an excellent replacement for Zener diodes and other types of references in applications such as onboard regulation, adjustable power supplies, and switching power supplies.

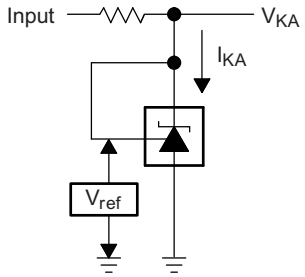
The TL1431C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TL1431Q is characterized for operation over the full automotive temperature range of –40°C to 125°C. The TL1431M is characterized for operation over the full military temperature range of –55°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL1431D	SOIC (8)	3.90 mm × 4.90 mm
TL1431PW	TSSOP (8)	4.40 mm × 3.00 mm
TL1431LP	TO-92 (3)	4.83 mm × 3.68 mm
TL1431MJG	CDIP (8)	9.58 mm x 6.67 mm
TL1431MFK	LCCC (20)	8.89 mm x 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

Changes from Revision M (April 2012) to Revision N **Page**

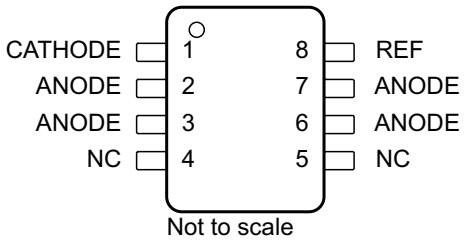
- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *ORDERING INFORMATION* table; see POA at the end of the data sheet ... 1
- Changed $R_{\theta JA}$ for D, LP and PW package from: 97 °C/W to 114.7 °C/W (D), 140 °C/W to 157 °C/W (LP) and 149 °C/W to 172.4 °C/W (PW) in the *Thermal Information* table. ... 4
- Changed $R_{\theta JC(bot)}$ for FK and JG package from: 5.61 °C/W to 9.5 °C/W (FK) and 14.5 °C/W to 9.5 °C/W (JG) in the *Thermal Information* table ... 4

Changes from Revision L (October 2007) to Revision M **Page**

- Added Ammo option to the LP package in the ORDERING INFORMATION table. ... 2

5 Pin Configuration and Functions

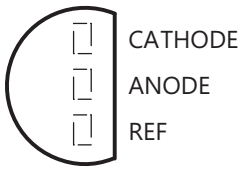
D Package
8-Pin SOIC
Top View



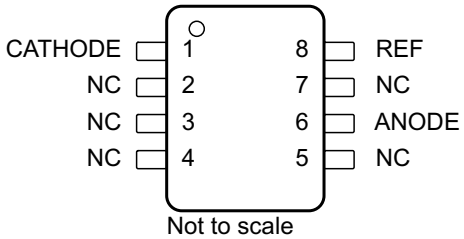
Not to scale

ANODE terminals are connected internally

LP Package
3-Pin TO-92
Top View



JG or PW Package
8-Pin CDIP or TSSOP
Top View



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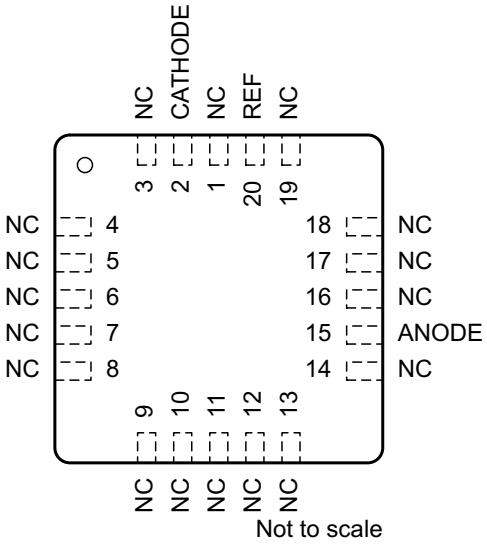
FK Package
20-Pin LCCC
Top View



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Pin Functions

PIN					I/O	DESCRIPTION
NAME	SOIC	CDIP, TSSOP	TO-92	LCCC		
ANODE	2, 3, 6, 7	6	2	15	O	Common pin, normally connected to ground
CATHODE	1	1	1	2	I/O	Shunt current/voltage input
REF	8	8	3	20	I	Threshold relative to common ground
NC	4, 5	2, 3, 4, 5, 7	—	1, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 16, 17, 18, 19	—	No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Cathode voltage, V_{KA}(2)		37	V
Continuous cathode current, I_{KA}	–100	150	mA
Reference input current, $I_{I(ref)}$	–0.05	10	mA
Lead temperature, 1.6 mm (1/16 in) from case for 10 s		260	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ANODE, unless otherwise noted.

6.2 ESD Ratings – TL1431C, TL1431Q

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{KA}	Cathode voltage		$V_{I(ref)}$	36	V
I_{KA}	Cathode current		1	100	mA
T_A	Operating free-air temperature	TL1431C	0	70	°C
		TL1431Q	–40	125	
		TL1431M	–55	125	

6.4 Thermal Information

THERMAL METRIC(1)		TL1431			TL1431M(2)		UNIT
		LP (TO-92)	D (SOIC)	PW (TSSOP)	JG (CDIP)	FK (LCCC)	
		3 PINS	8 PINS	8 PINS	8 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157	114.7	172.4	—	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.7	59	55.2	69.7	55.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	—	55.4	100.8	99	54.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.6	12	5	—	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	136.4	54.8	99	—	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	21	9.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) $R_{\theta JC}$ based on MIL-STD-883, and $R_{\theta JB}$ based on JESD51.

6.5 Electrical Characteristics – TL1431C

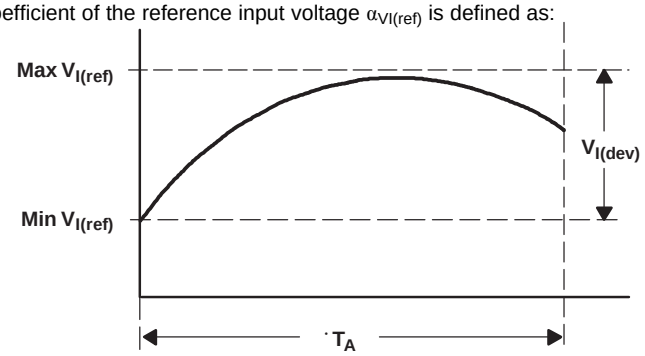
at specified free-air temperature and I_{KA} = 10 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(ref)}$	Reference input voltage	$V_{KA} = V_{I(ref)}$ (see Figure 13)	T_A = 25°C	2490	2500	2510	mV
			T_A = 0°C to 70°C	2480		2520	
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range(1)	$V_{KA} = V_{I(ref)}$, T_A = 0°C to 70°C (see Figure 13)			4	20	mV
$\frac{\Delta V_{I(ref)}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	ΔV_{KA} = 3 V to 36 V, T_A = 0°C to 70°C (see Figure 14)			–1.1	–2	mV/V
$I_{I(ref)}$	Reference input current	R1 = 10 kΩ, R2 = ∞ (see Figure 14)	T_A = 25°C		1.5	2.5	µA
			T_A = 0°C to 70°C			3	
$I_{I(dev)}$	Deviation of reference input current over full temperature range(1)	R1 = 10 kΩ, R2 = ∞, T_A = 0°C to 70°C (see Figure 14)			0.2	1.2	µA
I_{min}	Minimum cathode current for regulation	$V_{KA} = V_{I(ref)}$, T_A = 25°C (see Figure 13)			0.45	1	mA
I_{off}	Off-state cathode current	V_{KA} = 36 V, $V_{I(ref)}$ = 0 (see Figure 15)	T_A = 25°C		0.18	0.5	µA
			T_A = 0°C to 70°C			2	
$\lvert z_{KA} \rvert$	Output impedance(2)	$V_{KA} = V_{I(ref)}$, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA, T_A = 25°C (see Figure 13)			0.2	0.4	Ω

(1) The deviation parameters $V_{I(dev)}$ and $I_{I(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage $\alpha_{VI(ref)}$ is defined as:

$$\left|\alpha_{VI(ref)}\right| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{I(ref)\ at\ 25°C}}\right) \times 10^6}{T_A}$$

where:
ΔT_A is the rated operating temperature range of the device.



$\alpha_{VI(ref)}$ is positive or negative, depending on whether minimum $V_{I(ref)}$ or maximum $V_{I(ref)}$, respectively, occurs at the lower temperature.

(2) The output impedance is defined as: $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by: $|z'| = \frac{\Delta V}{\Delta I}$, which is approximately equal to $|z_{KA}|\left(1 + \frac{R1}{R2}\right)$.

6.6 Electrical Characteristics – TL1431Q

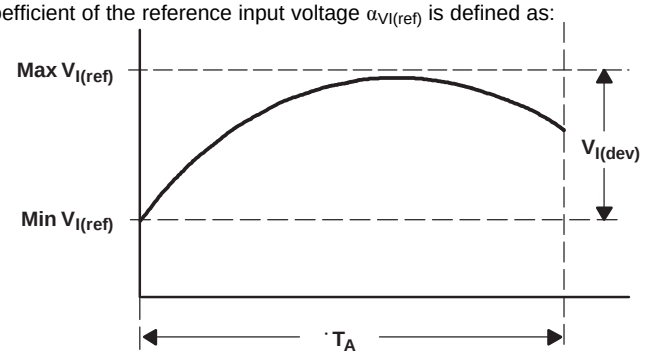
at specified free-air temperature and I_{KA} = 10 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(ref)}$	Reference input voltage	$V_{KA} = V_{I(ref)}$ (see Figure 13)	T_A = 25°C	2490	2500	2510	mV
			T_A = –40°C to 125°C	2470		2530	
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range(1)	$V_{KA} = V_{I(ref)}$, T_A = –40°C to 125°C (see Figure 13)			17	55	mV
$\frac{\Delta V_{I(ref)}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	ΔV_{KA} = 3 V to 36 V, T_A = –40°C to 125°C (see Figure 14)			–1.1	–2	mV/V
$I_{I(ref)}$	Reference input current	R1 = 10 kΩ, R2 = ∞ (see Figure 14)	T_A = 25°C		1.5	2.5	µA
			T_A = –40°C to 125°C			4	
$I_{I(dev)}$	Deviation of reference input current over full temperature range(1)	R1 = 10 kΩ, R2 = ∞, T_A = –40°C to 125°C (see Figure 14)			0.5	2	µA
I_{min}	Minimum cathode current for regulation	$V_{KA} = V_{I(ref)}$, T_A = 25°C (see Figure 13)			0.45	1	mA
I_{off}	Off-state cathode current	V_{KA} = 36 V, $V_{I(ref)}$ = 0 (see Figure 15)	T_A = 25°C		0.18	0.5	µA
			T_A = –40°C to 125°C			2	
$\lvert z_{KA} \rvert$	Output impedance(2)	$V_{KA} = V_{I(ref)}$, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA, T_A = 25°C (see Figure 13)			0.2	0.4	Ω

(1) The deviation parameters $V_{I(dev)}$ and $I_{I(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage $\alpha_{VI(ref)}$ is defined as:

$$\left|\alpha_{VI(ref)}\right| \left(\frac{ppm}{^{\circ}C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{I(ref)\ at\ 25^{\circ}C}}\right) \times 10^{6}}{T_A}$$

where:
ΔT_A is the rated operating temperature range of the device.



$\alpha_{VI(ref)}$ is positive or negative, depending on whether minimum $V_{I(ref)}$ or maximum $V_{I(ref)}$, respectively, occurs at the lower temperature.

(2) The output impedance is defined as: $\lvert z_{KA} \rvert = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by: $\lvert z' \rvert = \frac{\Delta V}{\Delta I}$, which is approximately equal to $\lvert z_{KA} \rvert \left(1 + \frac{R1}{R2}\right)$.

6.7 Electrical Characteristics – TL1431M

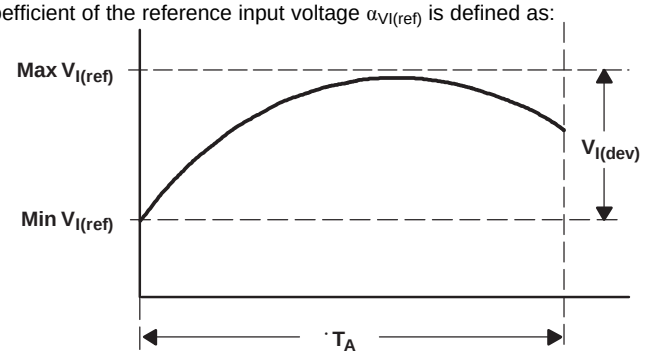
at specified free-air temperature and I_{KA} = 10 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(ref)}$	Reference input voltage	$V_{KA} = V_{I(ref)}$ (see Figure 13)	T_A = 25°C	2475	2500	2540	mV
			T_A = –55°C to 125°C	2460		2550	
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range(1)	$V_{KA} = V_{I(ref)}$, T_A = –55°C to 125°C (see Figure 13)			17	55(2)	mV
$\frac{\Delta V_{I(ref)}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	ΔV_{KA} = 3 V to 36 V, T_A = –55°C to 125°C (see Figure 14)			–1.1	–2	mV/V
$I_{I(ref)}$	Reference input current	R1 = 10 kΩ, R2 = ∞ (see Figure 14)	T_A = 25°C		1.5	2.5	μA
			T_A = –55°C to 125°C			5	
$I_{I(dev)}$	Deviation of reference input current over full temperature range(1)	R1 = 10 kΩ, R2 = ∞, T_A = –55°C to 125°C (see Figure 14)			0.5	3(2)	μA
I_{min}	Minimum cathode current for regulation	$V_{KA} = V_{I(ref)}$, T_A = 25°C (see Figure 13)			0.45	1	mA
I_{off}	Off-state cathode current	V_{KA} = 36 V, $V_{I(ref)}$ = 0 (see Figure 15)	T_A = 25°C		0.18	0.5	μA
			T_A = –55°C to 125°C			2	
$\lvert z_{KA} \rvert$	Output impedance(3)	$V_{KA} = V_{I(ref)}$, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA, T_A = 25°C (see Figure 13)			0.2	0.4	Ω

(1) The deviation parameters $V_{I(dev)}$ and $I_{I(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage $\alpha_{VI(ref)}$ is defined as:

$$\left|\alpha_{VI(ref)}\right| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{I(ref)\ at\ 25°C}}\right) \times 10^6}{T_A}$$

where:
ΔT_A is the rated operating temperature range of the device.



$\alpha_{VI(ref)}$ is positive or negative, depending on whether minimum $V_{I(ref)}$ or maximum $V_{I(ref)}$, respectively, occurs at the lower temperature.

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(3) The output impedance is defined as: $\lvert z_{KA} \rvert = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by: $\lvert z' \rvert = \frac{\Delta V}{\Delta I}$, which is approximately equal to $\lvert z_{KA} \rvert \left(1 + \frac{R1}{R2}\right)$.

6.8 Typical Characteristics

Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

Table 1. Table Of Graphs

GRAPH	FIGURE
Reference voltage vs Free-air temperature	Figure 1
Reference current vs Fire-air temperature	Figure 2
Cathode current vs Cathode voltage	Figure 3, Figure 4
Off-state cathode current vs Free-air temperature	Figure 5
Ratio of delta reference voltage to delta cathode voltage vs Free-air temperature	Figure 6
Equivalent input-noise voltage vs Frequency	Figure 7
Equivalent input-noise voltage over a 10-second period	Figure 8
Small-signal voltage amplification vs Frequency	Figure 9
Reference impedance vs Frequency	Figure 10
Pulse response	Figure 11
Stability boundary conditions	Figure 12

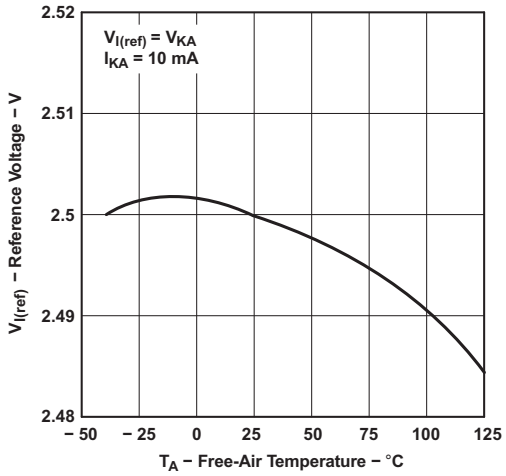


Figure 1. Reference Voltage vs Free-Air Temperature

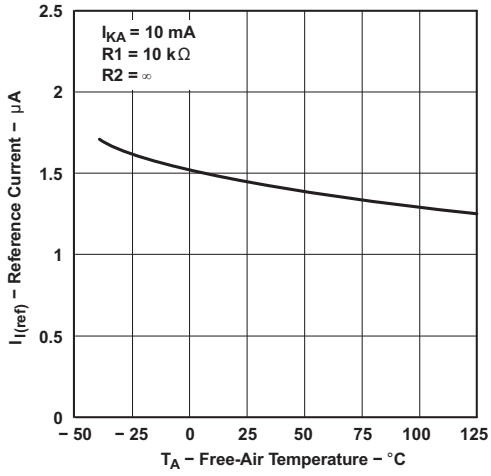


Figure 2. Reference Current vs Free-Air Temperature

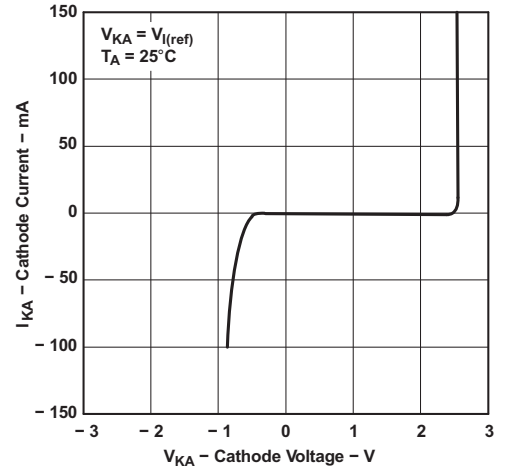


Figure 3. Cathode Current vs Cathode Voltage

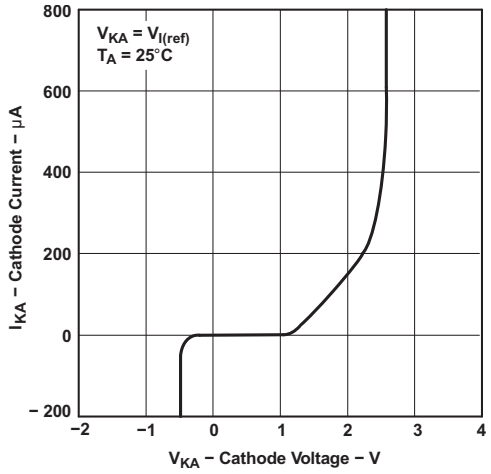


Figure 4. Cathode Current vs Cathode Voltage

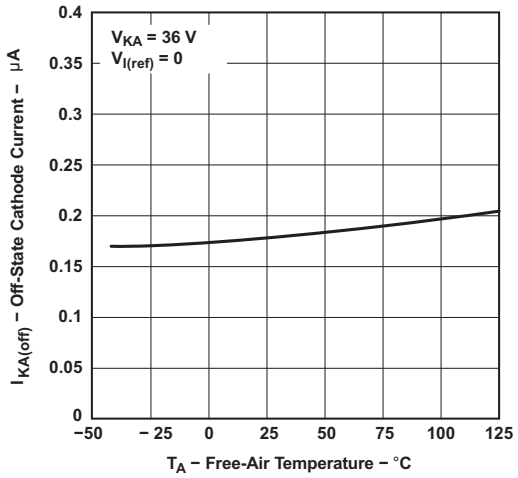


Figure 5. Off-State Cathode Current vs Free-Air Temperature

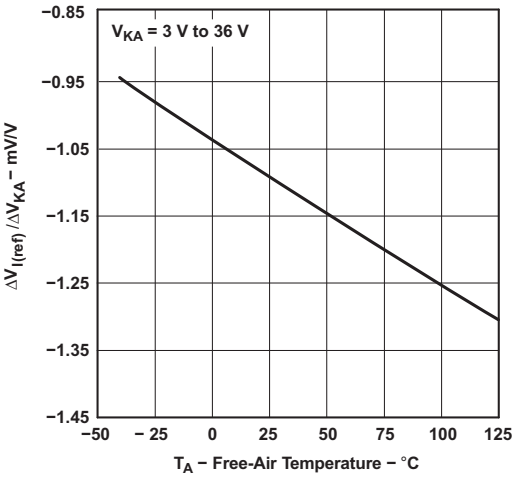


Figure 6. Ratio Of Delta Reference Voltage To Delta Cathode Voltage vs Free-Air Temperature

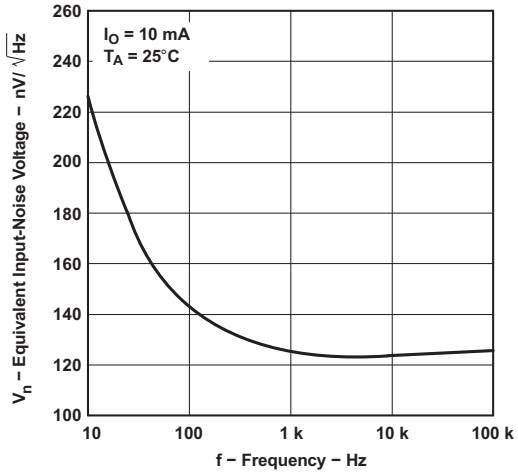


Figure 7. Equivalent Input-Noise Voltage vs Frequency

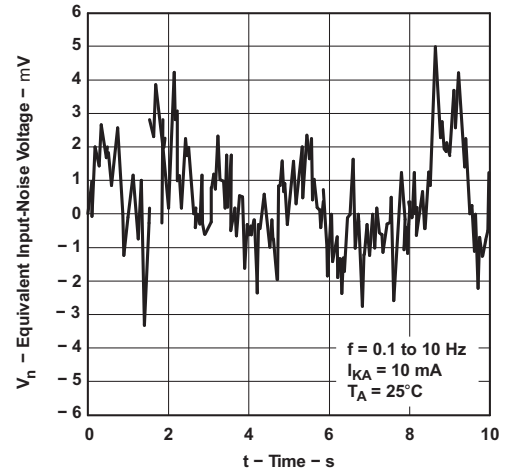


Figure 8. Equivalent Input-Noise Voltage Over A 10-S Period

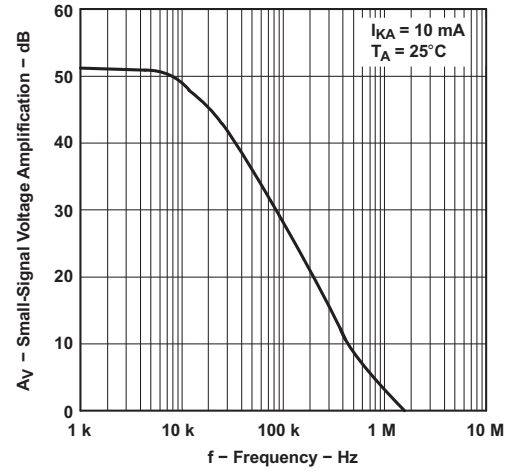


Figure 9. Small-Signal Voltage Amplification vs Frequency

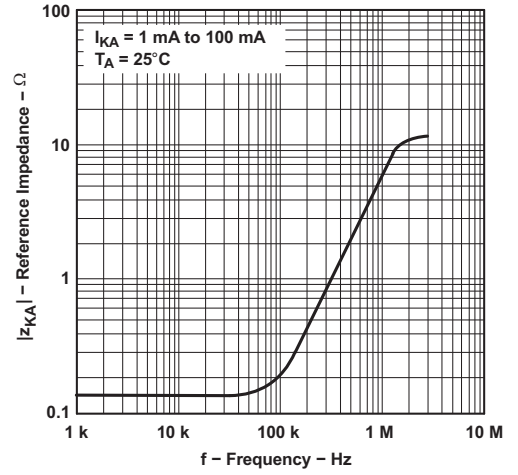


Figure 10. Reference Impedance vs Frequency

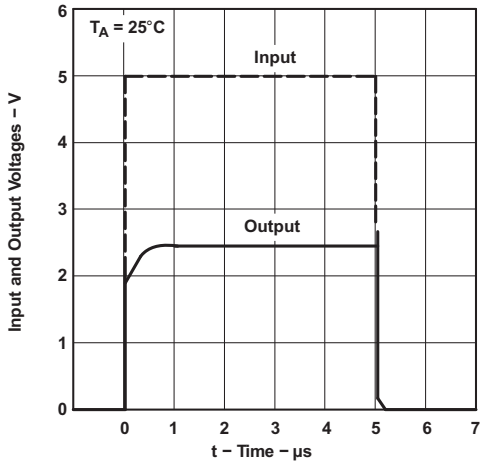
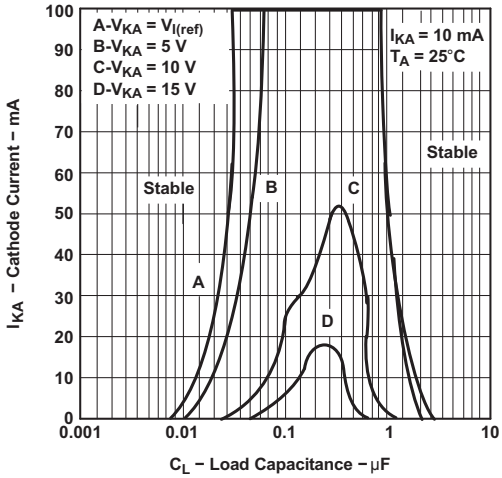


Figure 11. Pulse Response



The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V+ are adjusted to establish the initial V_{KA} and I_{KA} conditions, with C_L = 0. V_{BATT} and C_L then are adjusted to determine the ranges of stability.

Figure 12. Stability Boundary Conditions

7 Parameter Measurement Information

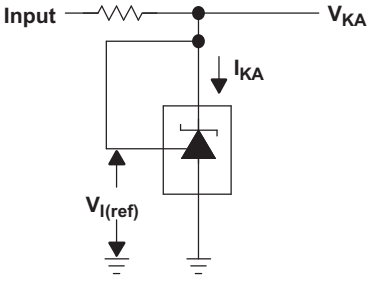


Figure 13. Test Circuit For $V_{(KA)} = V_{ref}$

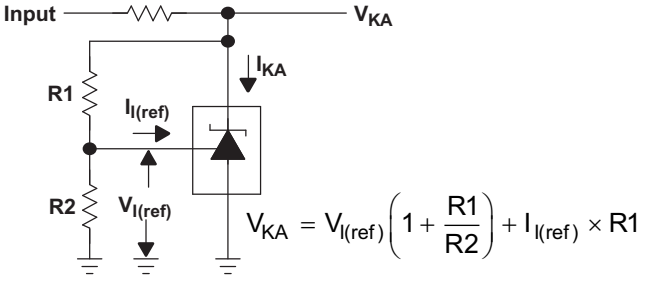


Figure 14. Test Circuit For $V_{(KA)} > V_{ref}$

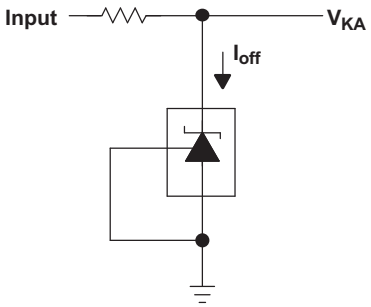


Figure 15. Test Circuit For I_{off}

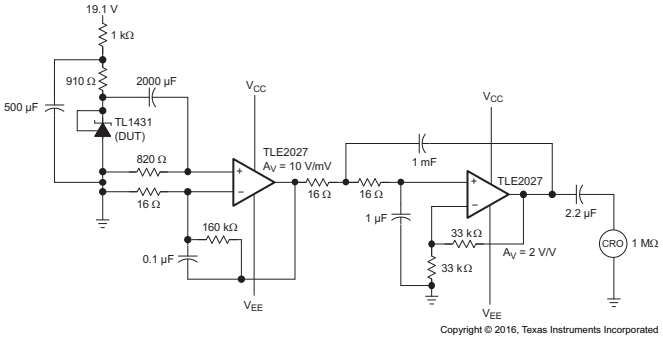


Figure 16. Test Circuit For 0.1-Hz To 10-Hz Equivalent Input-Noise Voltage

Parameter Measurement Information (continued)

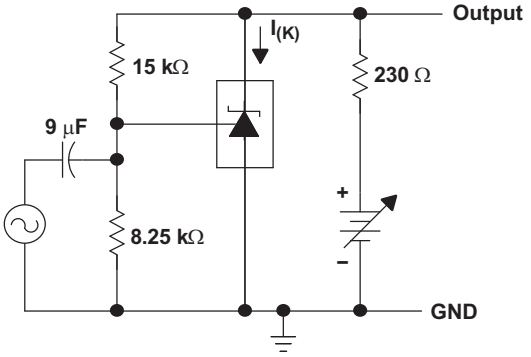


Figure 17. Test Circuit For Voltage Amplification

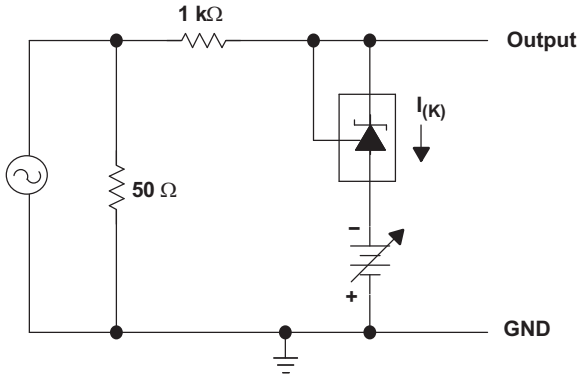


Figure 18. Test Circuit For Reference Impedance

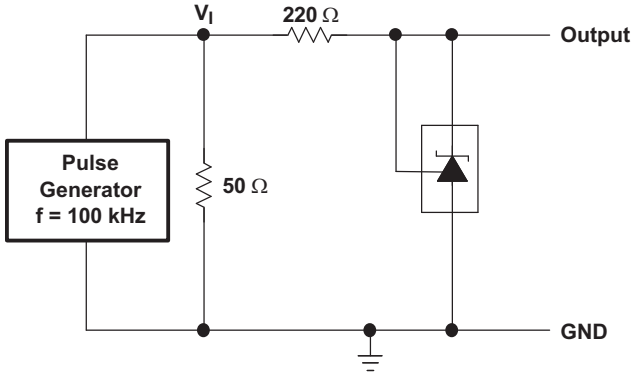


Figure 19. Test Circuit For Pulse Response

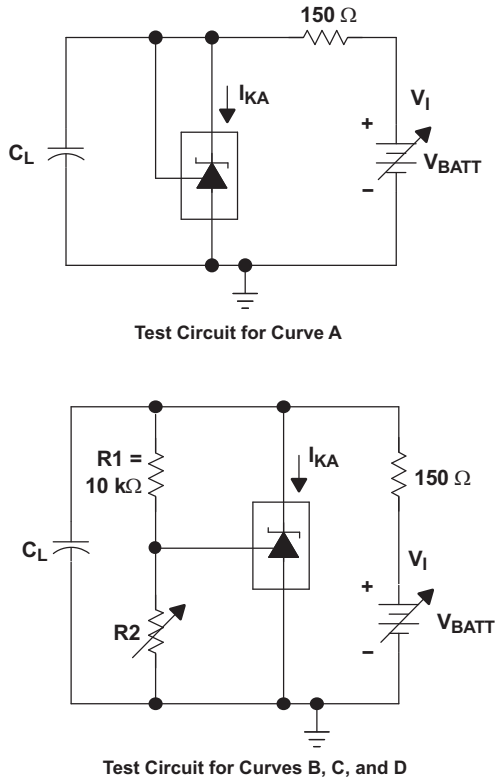


Figure 20. Test Circuits For Curves A Through D

8 Detailed Description

8.1 Overview

The TL1431 device has proven ubiquity and versatility across a wide range of applications, ranging from power to signal path. This is due to its key components containing an accurate voltage reference and op amp, which are very fundamental analog building blocks. TL1431 is used in conjunction with its key components to behave as a single voltage reference, error amplifier, voltage clamp, or comparator with integrated reference. TL1431 can be operated and adjusted to cathode voltages from 2.5 V to 36 V, making this part optimum for a wide range of end equipments in industrial, auto, telecom, and computing. In order for this device to behave as a shunt regulator or error amplifier, >1 mA (Imin(max)) must be supplied in to the cathode pin. Under this condition, feedback can be applied from the Cathode and Ref pins to create a replica of the internal reference voltage. Various reference voltage options can be purchased with initial tolerances (at 25°C) of 0.4% and 1%. The TL1431C devices are characterized for operation from 0°C to 70°C, the TL1431Q devices are characterized for operation from –40°C to 125°C, and the TL1431M devices are characterized for operation from –55°C to 125°C.

8.2 Functional Block Diagram

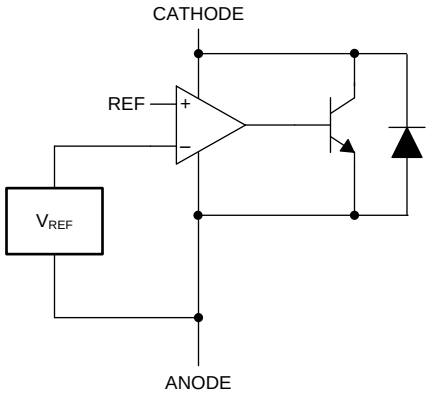
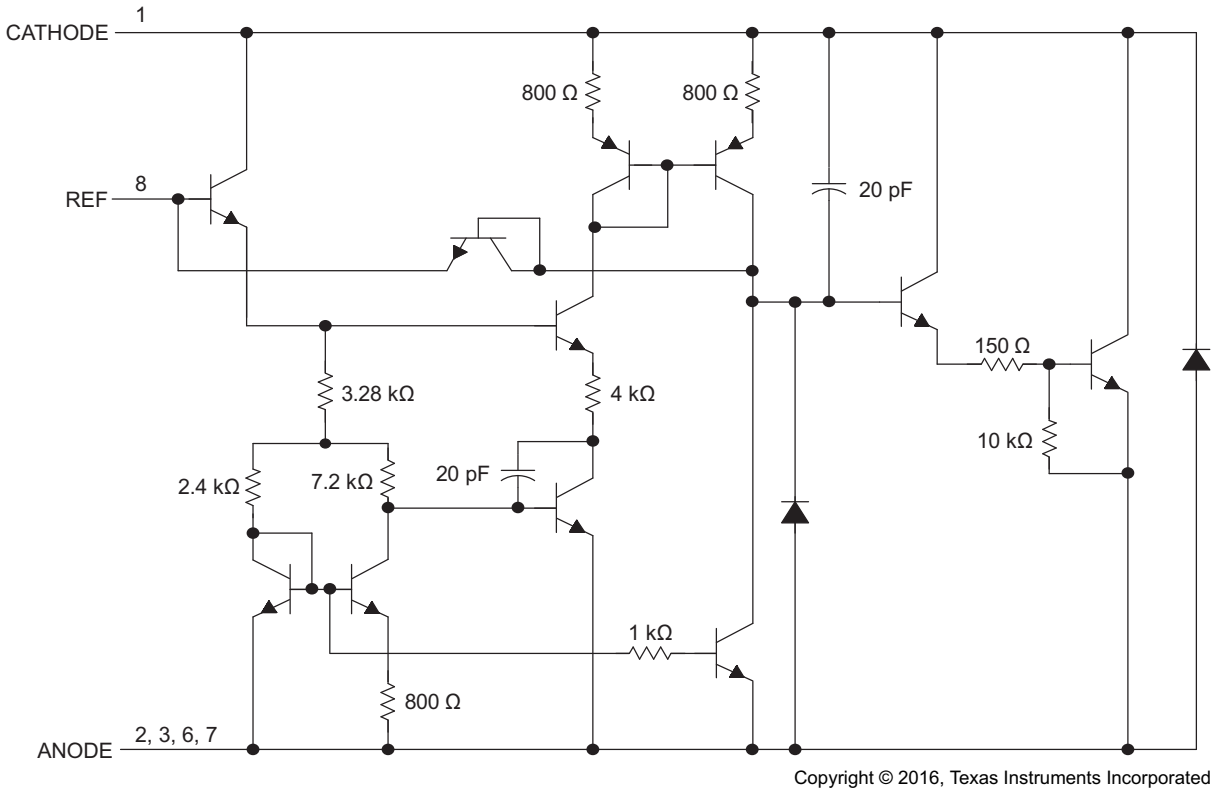


Figure 21. Equivalent Schematic

Functional Block Diagram (continued)



(1) All component values are nominal.

(2) Pin numbers shown are for the D package.

Figure 22. Detailed Schematic

8.3 Feature Description

TL1431 consists of an internal reference and amplifier that outputs a sink current base on the difference between the reference pin and the virtual internal pin. The sink current is produced by the internal Darlington pair, shown in Figure 22. A Darlington pair is used in order for this device to be able to sink a maximum current of 100 mA. When operated with enough voltage headroom (≥ 2.5 V) and cathode current (I_{KA}), TL1431 forces the reference pin to 2.5 V. However, the reference pin can not be left floating, as it needs I_{REF} ≥ 5 µA (see *Electrical Characteristics – TL1431M*). This is because the reference pin is driven into an npn, which needs base current to operate properly. When feedback is applied from the cathode and reference pins, TL1431 behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current needed in the above feedback situation must be applied to this device in open loop, servo, or error amplifying implementations in order for it to be in the proper linear region giving TL1431 enough gain. Unlike many linear regulators, TL1431 is internally compensated to be stable without an output capacitor between the cathode and anode. However, if desired an output capacitor can be used as a guide to assist in choosing the correct capacitor to maintain stability.

8.4 Device Functional Modes

8.4.1 Open Loop (Comparator)

When the cathode or output voltage or current of TL1431 is not being fed back to the reference or input pin in any form, this device is operating in open loop. With proper cathode current (I_{KA}) applied to this device, TL1431 has the characteristics shown in Figure 22. With such high gain in this configuration, TL1431 is typically used as a comparator. With the reference integrated makes TL1431 the preferred choice when users are trying to monitor a certain level of a single signal.

8.4.2 Closed Loop

When the cathode or output voltage or current of TL1431 is being fed back to the reference or input pin in any form, this device is operating in closed loop. The majority of applications involving TL1431 use it in this manner to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting it to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to make it equal to the internal reference voltage, which can be accomplished through resistive or direct feedback.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

As the TL1431 device has many applications and setups, there are many situations that this datasheet cannot characterize in detail. The linked application notes help the designer make the best choices when using this part. *Understanding Stability Boundary Conditions Charts in TL431, TL432 Data Sheet* (SLVA482) provides a deeper understanding of this devices stability characteristics and aid the user in making the right choices when choosing a load capacitor. *Setting the Shunt Voltage on an Adjustable Shunt Regulator* (SLVA445) assists designers in setting the shunt voltage to achieve optimum accuracy for this device.

9.2 Typical Application

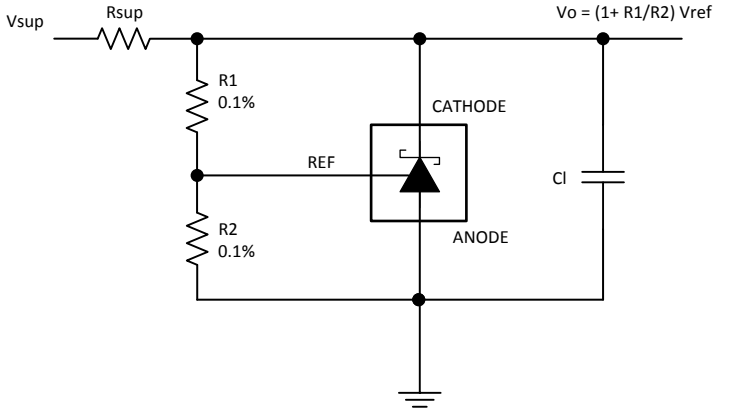


Figure 23. Comparator Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

PARAMETER	VALUE
Reference initial accuracy	0.4%
Supply voltage	48 V
Cathode current (I_K)	50 µA
Output voltage level	2.5 V to 36 V
Load capacitance	1 nF
Feedback resistor values and accuracy (R1 and R2)	10 kΩ

9.2.2 Detailed Design Procedure

When using TL1431 as a shunt regulator, determine the following:

- Input voltage range
- Temperature range
- Total accuracy
- Cathode current

- Reference initial accuracy
- Output capacitance

9.2.2.1 Programming Output/Cathode Voltage

To program the cathode voltage to a regulated voltage a resistive bridge must be shunted between the cathode and anode pins with the mid point tied to the reference pin. This can be seen in Figure 23, with R1 and R2 being the resistive bridge. The cathode/output voltage in the shunt regulator configuration can be approximated by the equation shown in Figure 23. The cathode voltage can be more accurately determined by taking in to account the cathode current with Equation 1.

$$Vo = (1 + R1 / R2) \times V_{REF} – I_{REF} \times R1 \quad (1)$$

For this equation to be valid, TL1431 must be fully biased so that it has enough open loop gain to mitigate any gain error. This can be done by meeting the Imin specification denoted in *Electrical Characteristics – TL1431M*.

9.2.2.2 Total Accuracy

When programming the output above unity gain (V_{KA}=V_{REF}), TL1431 is susceptible to other errors that may effect the overall accuracy beyond V_{REF}. These errors include:

- R1 and R2 accuracies
- $V_{I(dev)}$ – Change in reference voltage over temperature
- $\Delta V_{REF} / \Delta V_{KA}$ – Change in reference voltage to the change in cathode voltage
- $|z_{KA}|$ – Dynamic impedance, causing a change in cathode voltage with cathode current

Worst case cathode voltage can be determined taking all of the variables in to account.

9.2.2.3 Stability

Though TL1431 is stable with no capacitive load, the device that receives the shunt regulator's output voltage could present a capacitive load that is within the TL1431 region of stability, shown in Figure 12. Also, designers may use capacitive loads to improve the transient response or for power supply decoupling. When using additional capacitance between Cathode and Anode, refer to Figure 12.

9.2.2.4 Start-up Time

As shown in Figure 24, TL1431 has a fast response up to approximately 2 V and then slowly charges to its programmed value. This is due to the compensation capacitance the TL1431 has to meet its stability criteria. Despite the secondary delay, TL1431 still has a fast response suitable for many clamp applications.

9.2.3 Application Curve

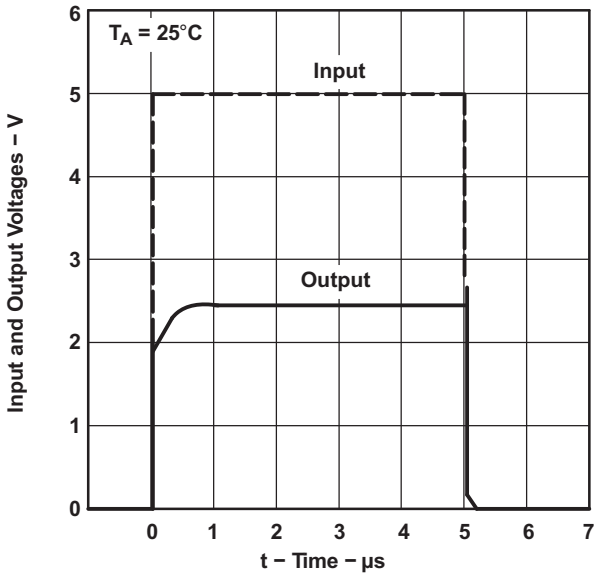


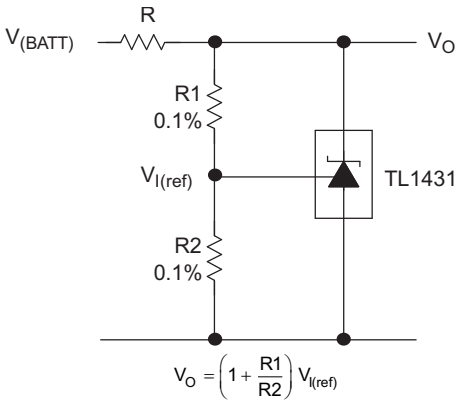
Figure 24. TL1431 Start-up Response

9.3 System Examples

Table 3 lists example circuits of the TL1431.

Table 3. Table Of Example Circuits

APPLICATION	FIGURE
Shunt regulator	Figure 25
Single-supply comparator with temperature-compensated threshold	Figure 26
Precision high-current series regulator	Figure 27
Output control of a three-terminal fixed regulator	Figure 28
Higher-current shunt regulator	Figure 29
Crowbar	Figure 30
Precision 5-V, 1.5-A, 0.5% regulator	Figure 31
5-V precision regulator	Figure 32
PWM converter with 0.5% reference	Figure 33
Voltage monitor	Figure 34
Delay timer	Figure 35
Precision current limiter	Figure 36
Precision constant-current sink	Figure 37



R must provide cathode current ≥1 mA to the TL1431 at minimum $V_{(BATT)}$.

Figure 25. Shunt Regulator

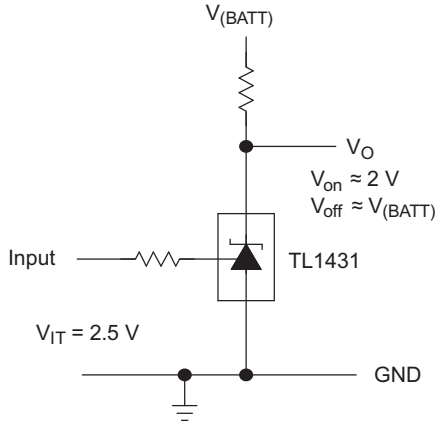
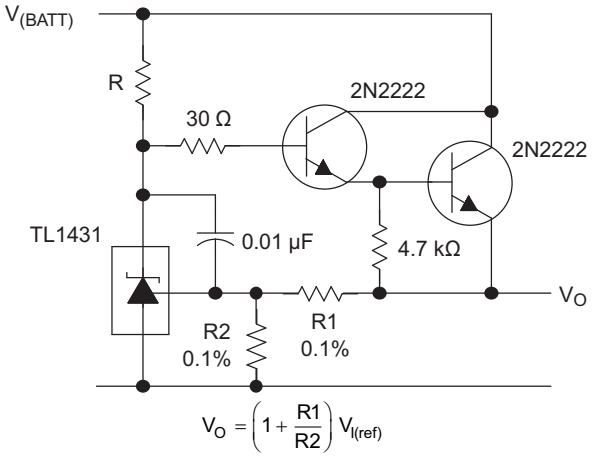


Figure 26. Single-Supply Comparator With Temperature-Compensated Threshold



R must provide cathode current ≥1 mA to the TL1431 at minimum $V_{(BATT)}$.

Figure 27. Precision High-Current Series Regulator

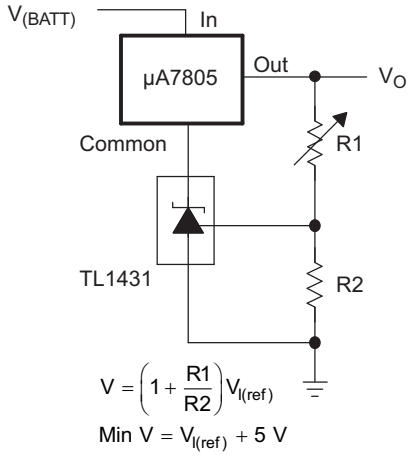


Figure 28. Output Control Of A Three-Terminal Fixed Regulator

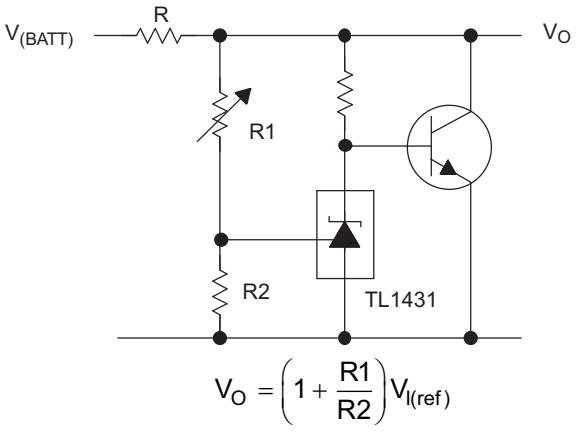
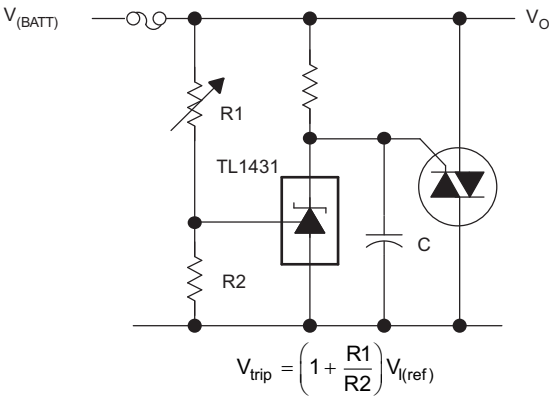


Figure 29. Higher-Current Shunt Regulator



See the stability boundary conditions in Figure 12 to determine allowable values for C.

Figure 30. Crowbar

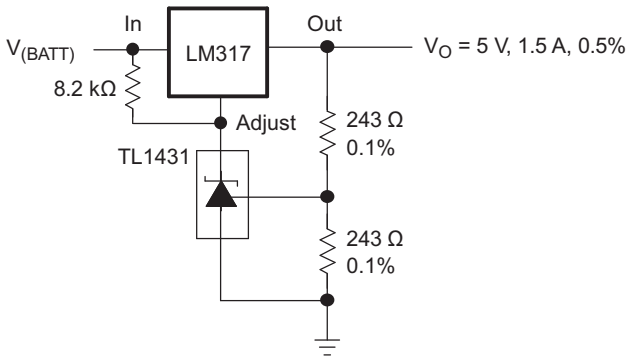
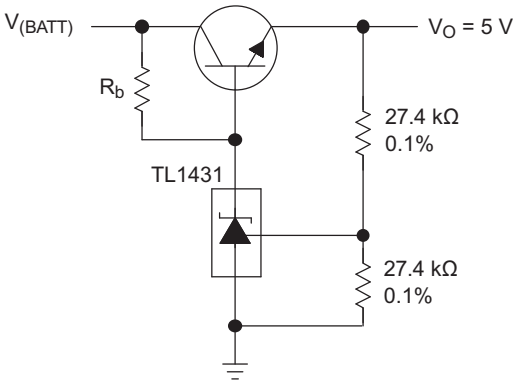


Figure 31. Precision 5-V, 1.5-A, 0.5% Regulator



R_b must provide cathode current ≥1 mA to the TL1431.

Figure 32. 5-V Precision Regulator

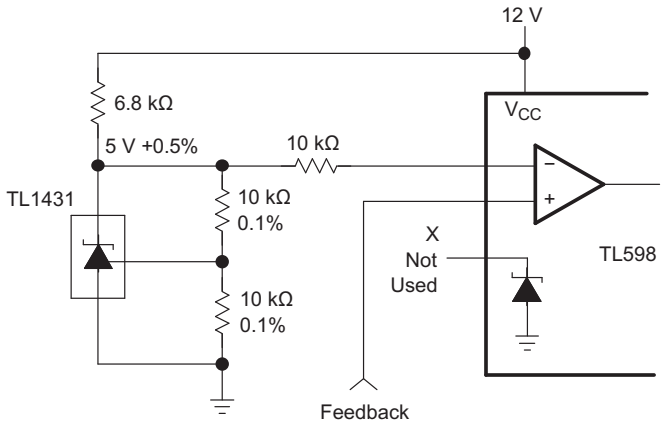
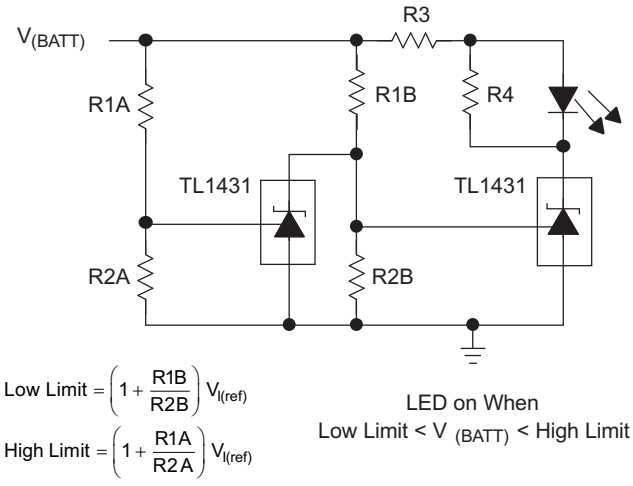
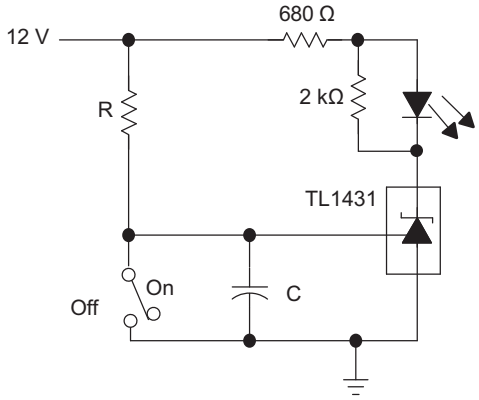


Figure 33. PWM Converter With 0.5% Reference



Select R3 and R4 to provide the desired LED intensity and cathode current ≥1 mA to the TL1431.

Figure 34. Voltage Monitor



$$\text{Delay} = R \times C \times I_I \frac{12\ V}{(12\ V) - V_{I(ref)}}$$

Figure 35. Delay Timer

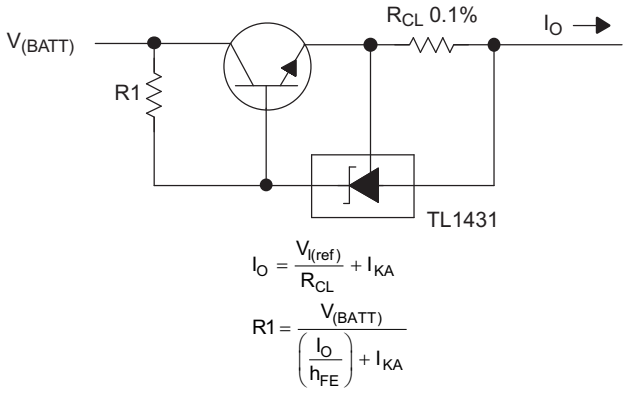


Figure 36. Precision Current Limiter

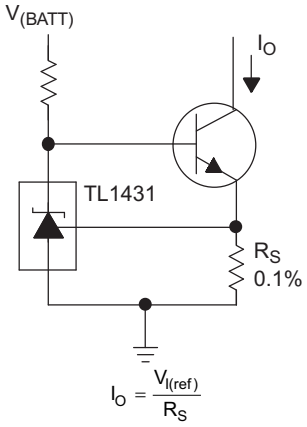


Figure 37. Precision Constant-Current Sink

10 Power Supply Recommendations

When using TL1431 as a linear regulator to supply a load, designers typically use a bypass capacitor on the output/cathode pin. When doing this, be sure that the capacitance is within the stability criteria shown in Figure 12. To not exceed the maximum cathode current, ensure the supply voltage is current limited. Also, be sure to limit the current being driven into the Ref pin, as not to exceed it's absolute maximum rating. For applications shunting high currents, pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have the proper current density.

11 Layout

11.1 Layout Guidelines

Bypass capacitors must be placed as close to the part as possible. Current-carrying traces need to have widths appropriate for the amount of current they are carrying; in the case of the TL1431, these currents are low.

11.2 Layout Example

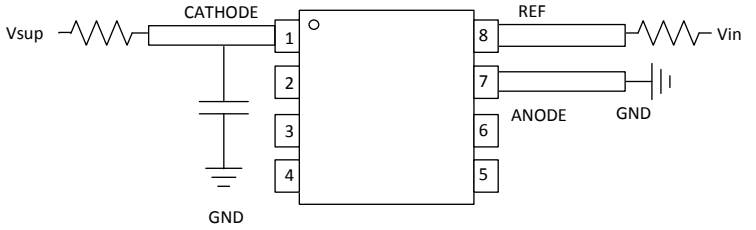


Figure 38. PW Package Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Understanding Stability Boundary Conditions Charts in TL431, TL432 Data Sheet* (SLVA482)
- *Setting the Shunt Voltage on an Adjustable Shunt Regulator* (SLVA445)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL1431	Click here	Click here	Click here	Click here	Click here
TL1431M	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9962001Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9962001Q2A TL1431MFKB	Samples
5962-9962001QPA	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9962001QPA TL1431M	Samples
TL1431CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	1431C	Samples
TL1431CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	1431C	Samples
TL1431CLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 70	TL1431C	Samples
TL1431CLPME3	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 70	TL1431C	Samples
TL1431CLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 70	TL1431C	Samples
TL1431CPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	T1431	Samples
TL1431MFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL1431MFK	Samples
TL1431MFKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9962001Q2A TL1431MFKB	Samples
TL1431MJG	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL1431MJG	Samples
TL1431MJGB	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9962001QPA TL1431M	Samples
TL1431QD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1431Q	Samples
TL1431QDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1431Q	Samples
TL1431QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1431Q	Samples
TL1431QDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1431Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TL1431, TL1431M :

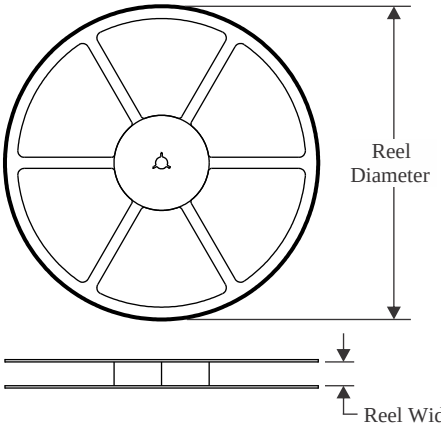
- Catalog : TL1431
- Automotive : TL1431-Q1, TL1431-Q1
- Enhanced Product : TL1431-EP, TL1431-EP
- Military : TL1431M
- Space : TL1431-SP, TL1431-SP

NOTE: Qualified Version Definitions:

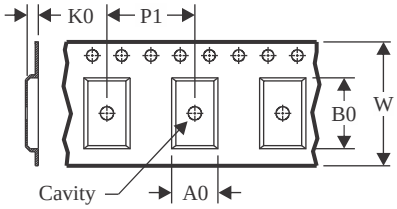
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

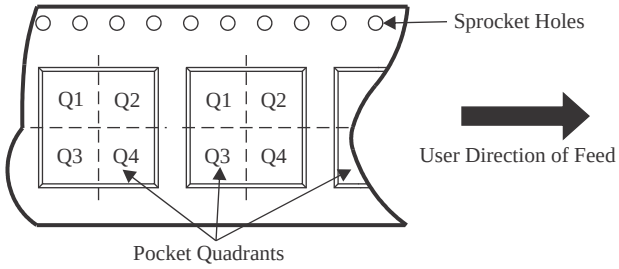


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

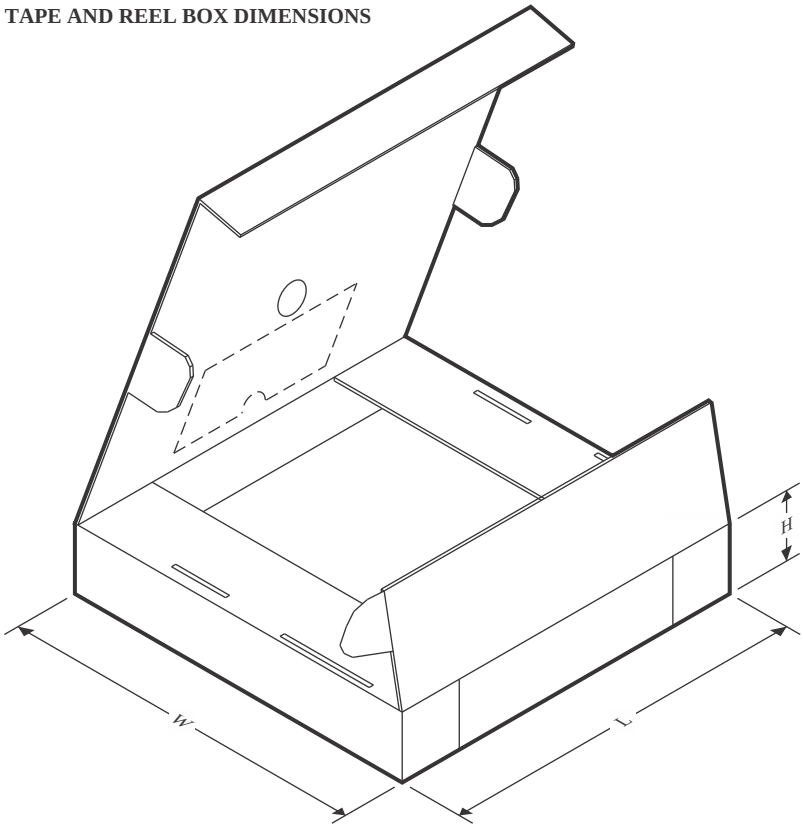
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL1431CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL1431CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL1431QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL1431QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

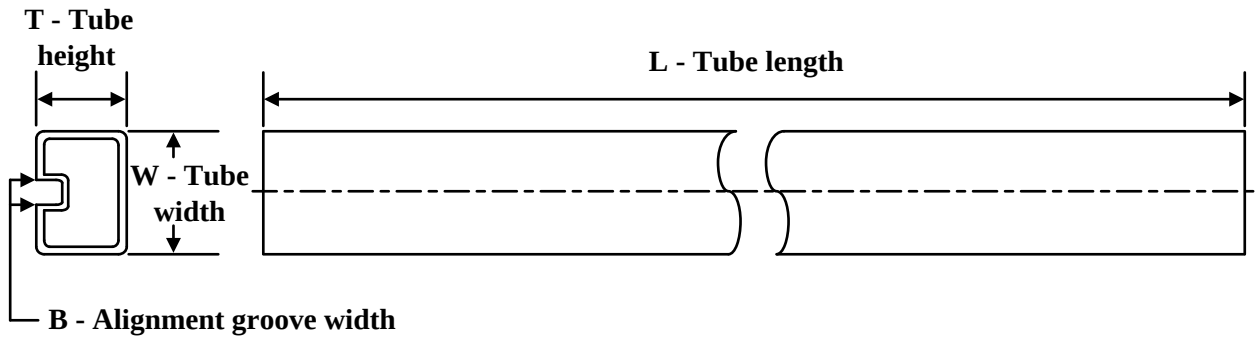
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL1431CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL1431CPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TL1431QDR	SOIC	D	8	2500	340.5	338.1	20.6
TL1431QDRG4	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9962001Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL1431CD	D	SOIC	8	75	507	8	3940	4.32
TL1431MFK	FK	LCCC	20	55	506.98	12.06	2030	NA
TL1431MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL1431QD	D	SOIC	8	75	505.46	6.76	3810	4
TL1431QDG4	D	SOIC	8	75	505.46	6.76	3810	4

GENERIC PACKAGE VIEW

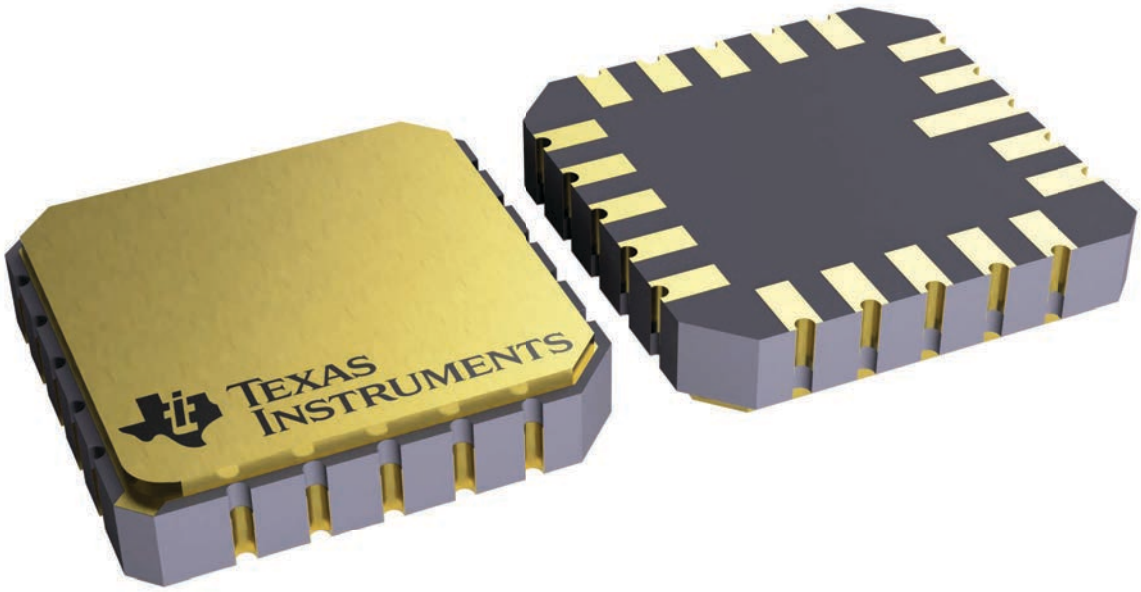
FK 20

LCCC - 2.03 mm max height

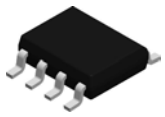
8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

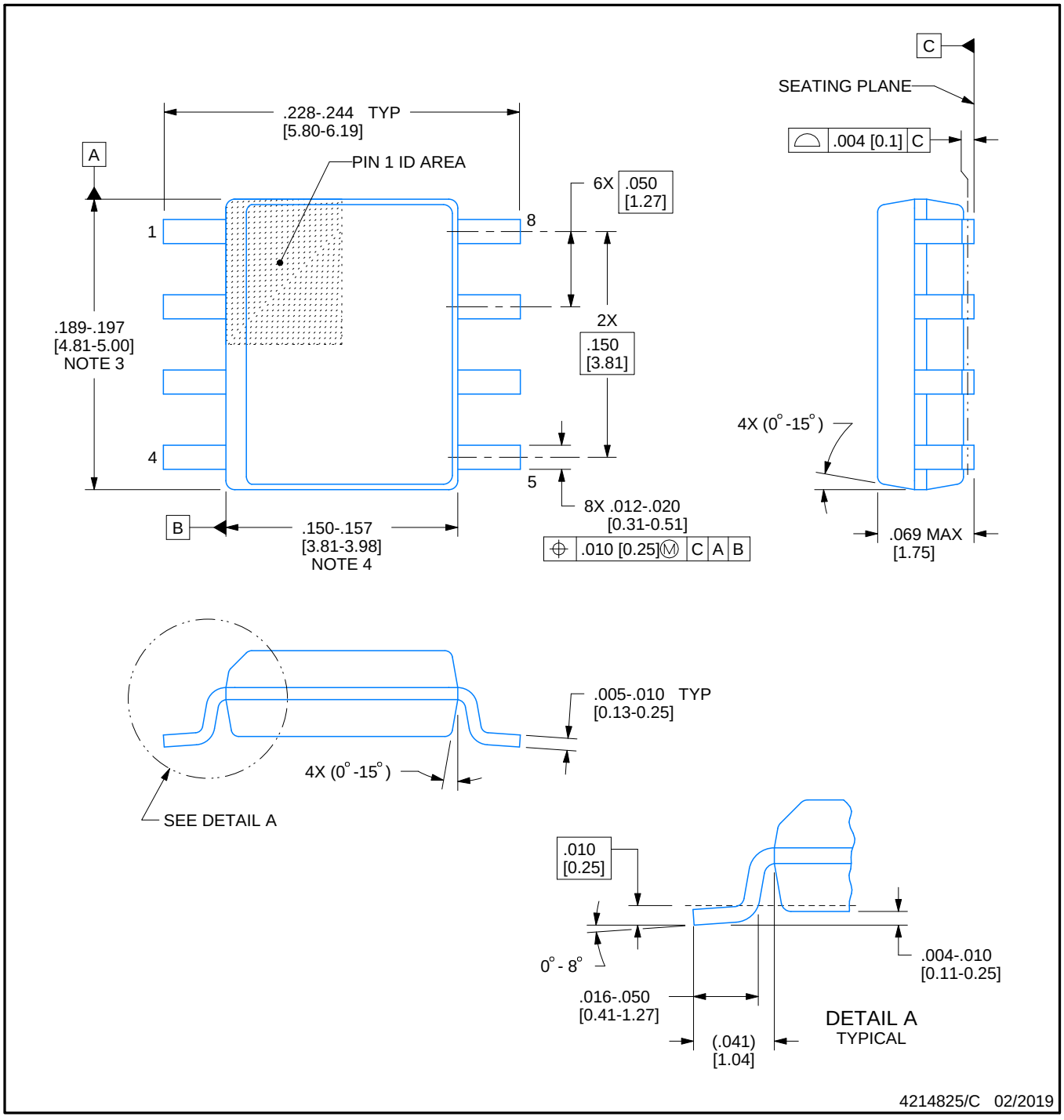


PACKAGE OUTLINE

D0008A

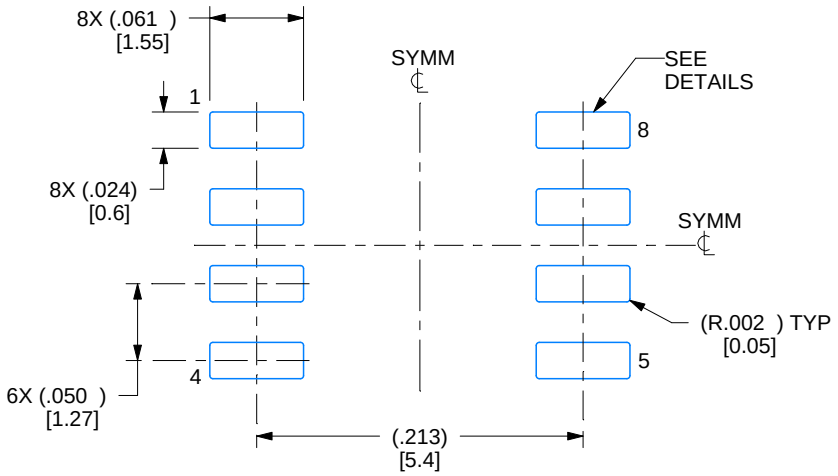
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

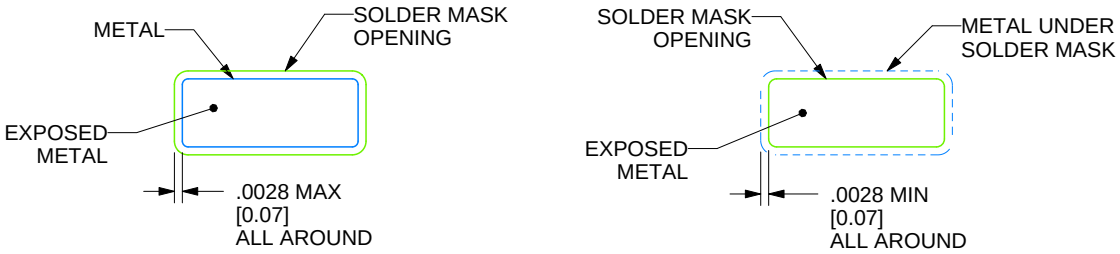


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

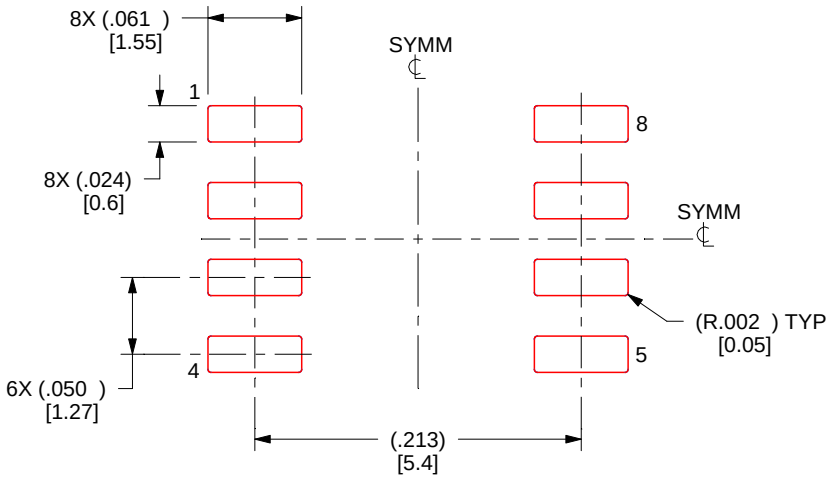
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

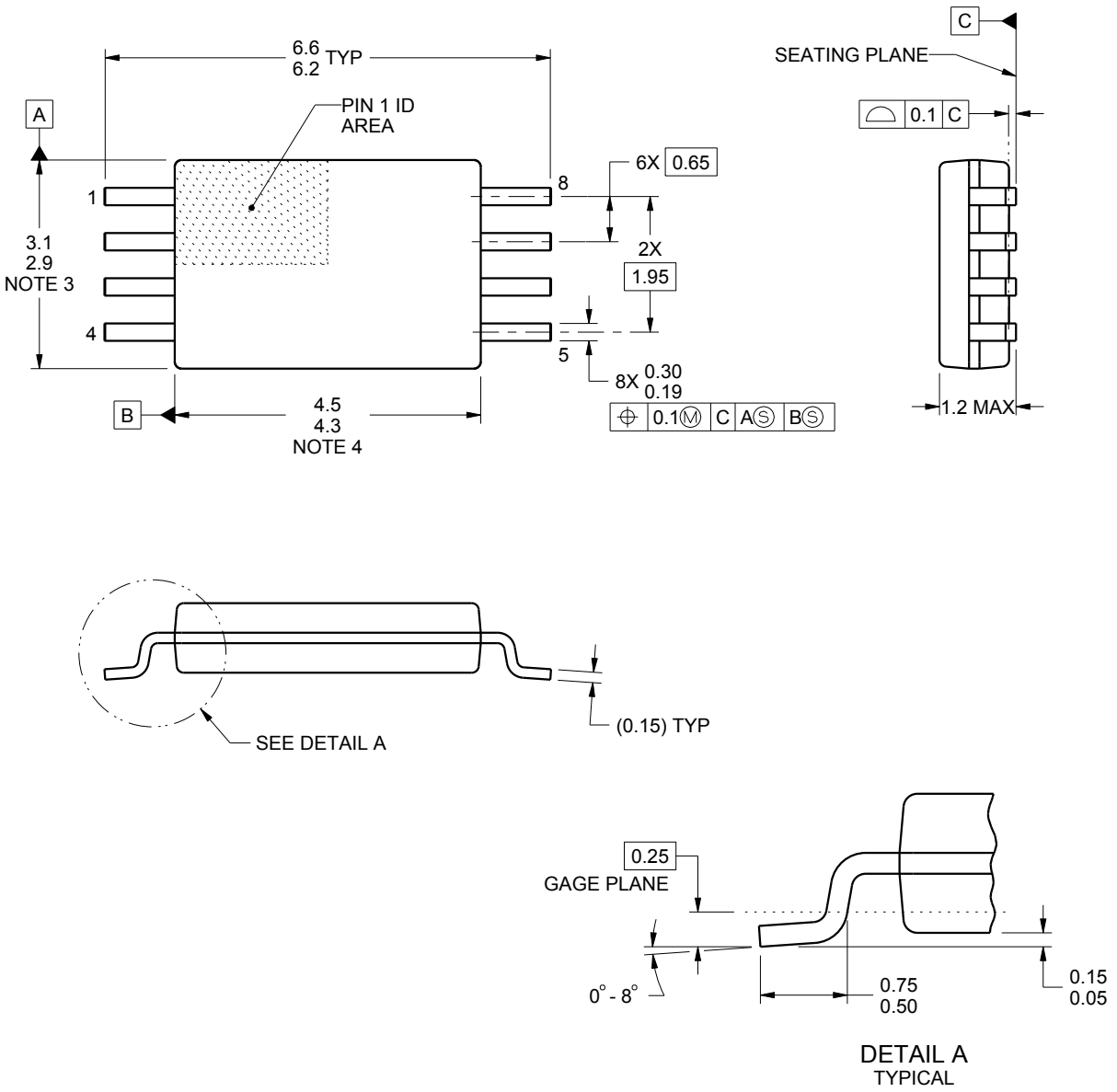
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

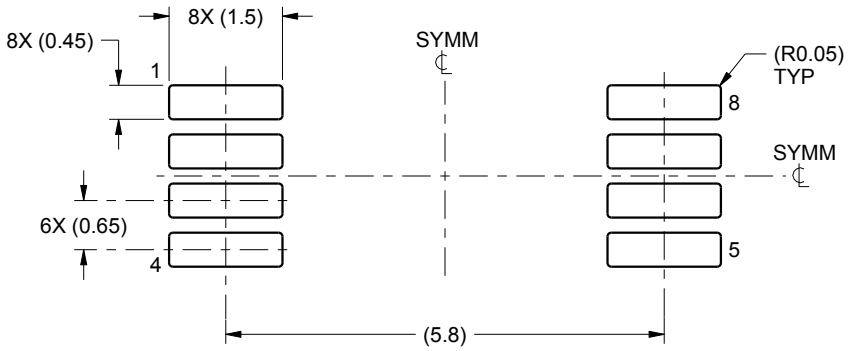
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

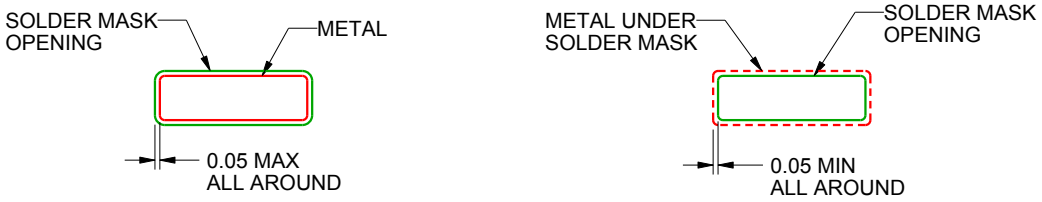


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

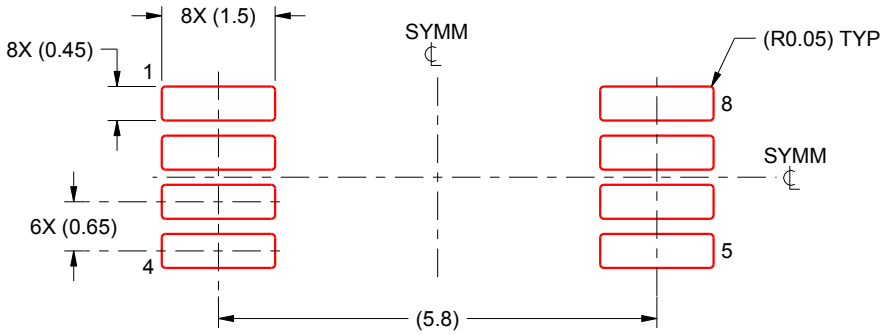


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

LP 3 TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE

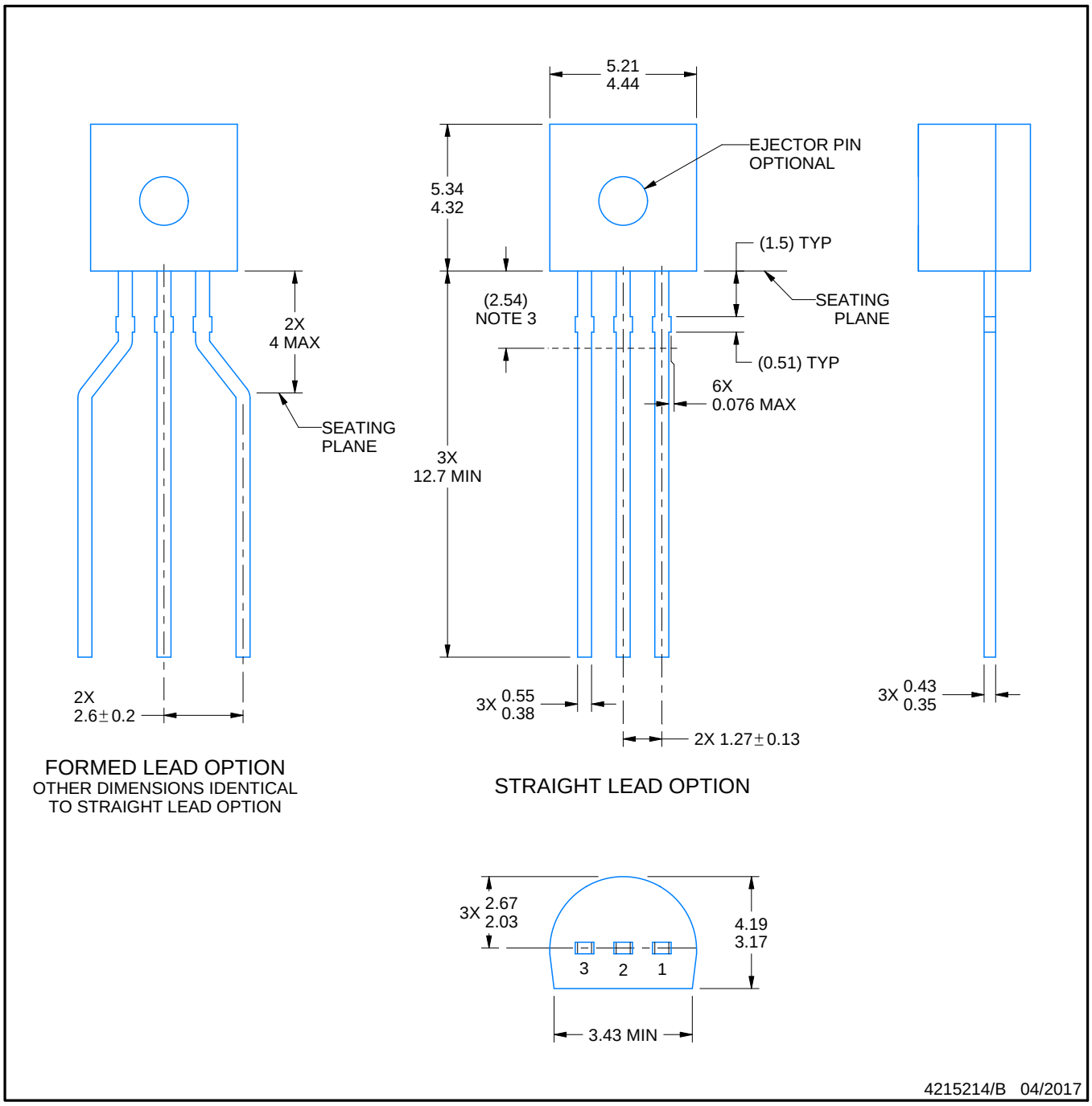
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

LP0003A

PACKAGE OUTLINE

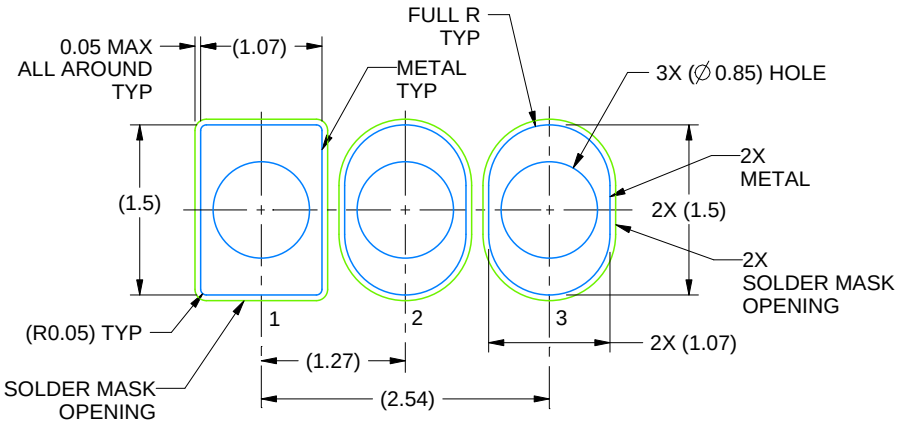
TO-92 - 5.34 mm max height

TO-92

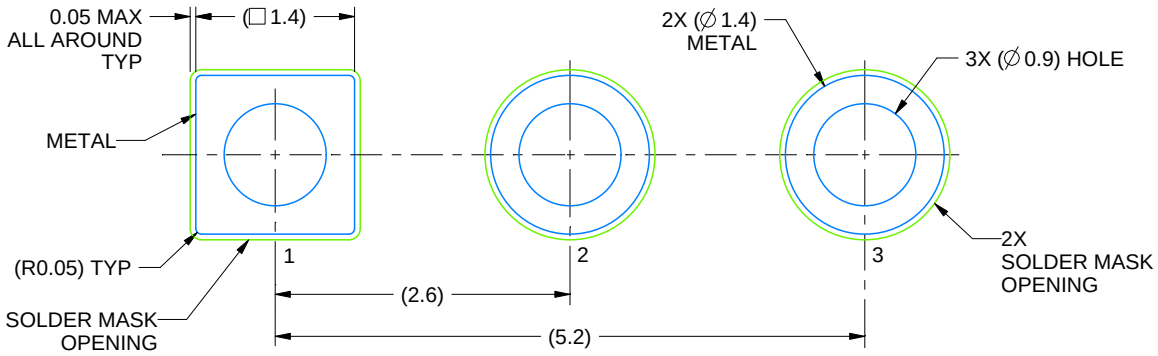


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



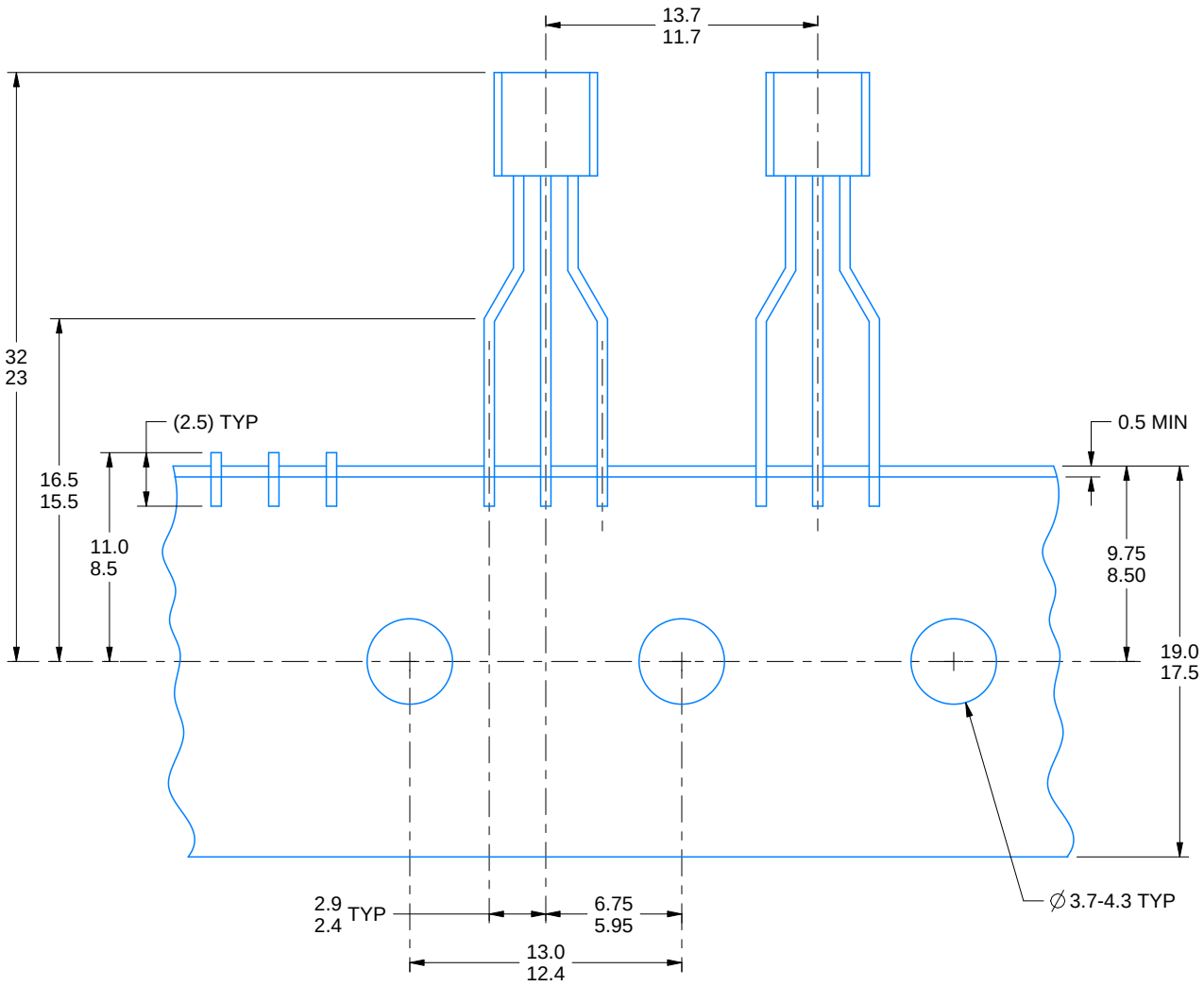
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

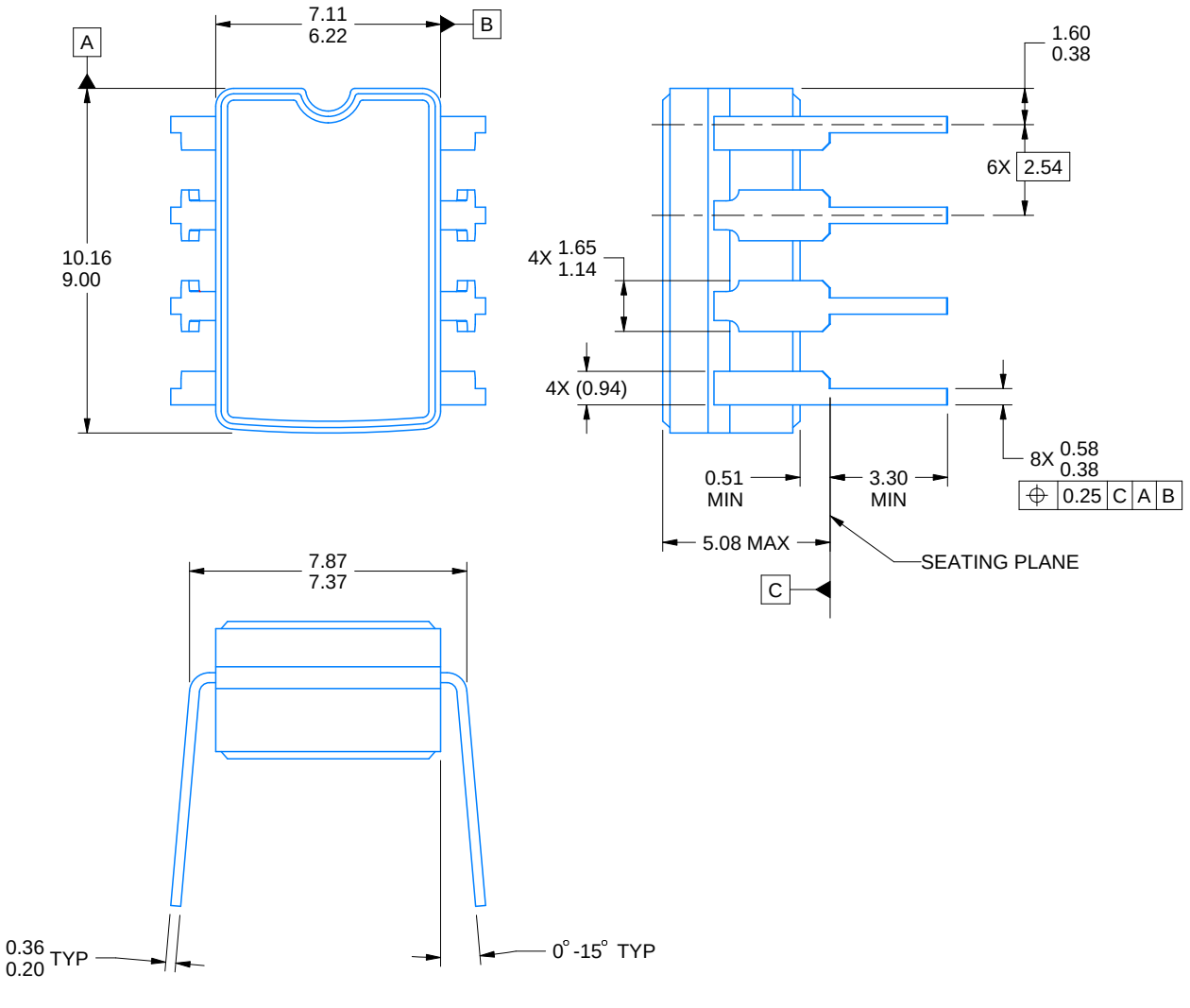
4215214/B 04/2017

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

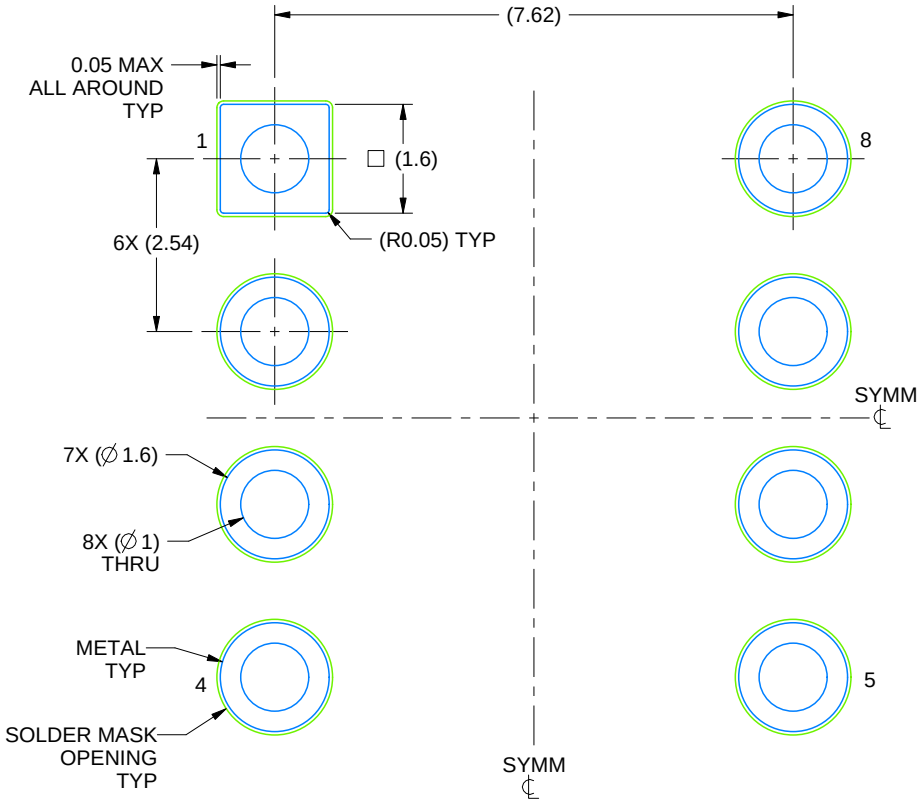
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

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