TLV183x and TLV184x Family of 40V, High-Speed Comparators

1 Features

- Wide supply range: 2.7V to 40V
- 65ns propagation delay
- Low supply current: 75µA per channel
- Rail-to-rail inputs
- Low input offset voltage: 500µV
- Power-on-reset (POR) provides a known startup condition
- Push-pull output option (TLV183x)
- Open-drain output option (TLV184x)
- Split supply option (TLV187x)
- Temperature range: -40°C to +125°C

2 Applications

- Motor drives
- Appliances
- Grid infrastructure
- Factory automation and control
- Traction inverter

3 Description

The TLV183x and TLV184x are high-speed comparators with operating voltages up to 40V. The comparators offer rail-to-rail inputs with push-pull and open-drain output options. These features coupled with 65ns propagation delay make this family well-suited for high speed current sensing and voltage protection applications.

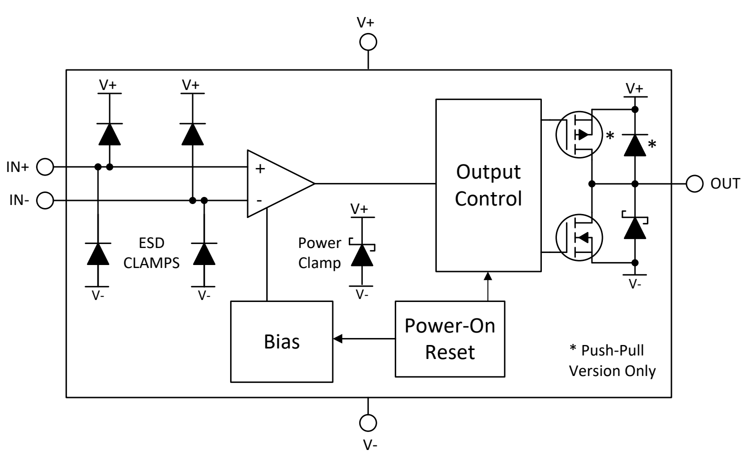
All devices include a Power-On Reset (POR) feature that makes sure the output is in a known state until the minimum supply voltage has been reached. Once this voltage has been reached, the output responds to the inputs, thus preventing false outputs during system power-up and power-down.

The TLV183x comparators have a push-pull output stage, which are designed for applications where symmetry between rising and falling output responses is desired. The TLV184x comparators have an open-drain output stage, making them appropriate for level transition.

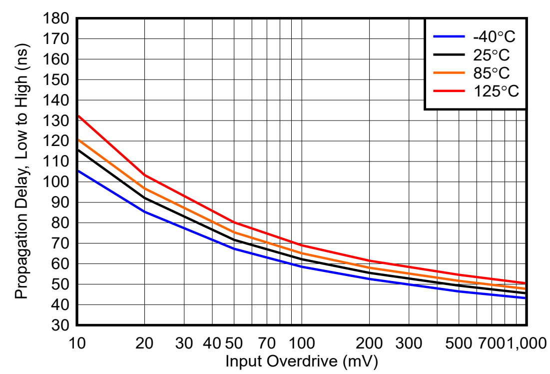
Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
TLV1831, TLV1841	SC-70 (5)	2.00mm × 2.00mm
	SOT-23 (5)	2.90mm × 1.60mm
TLV1832, TLV1842	VSSOP (8)	3.00mm × 3.00mm
	TSSOP (8)	3.00mm × 4.40mm
	WSON (8) (Preview)	2.00mm × 2.00mm
TLV1834, TLV1844	SOT-23 (14) (Preview)	4.20mm × 2.00mm
	WQFN (16) (Preview)	3.00mm × 3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram

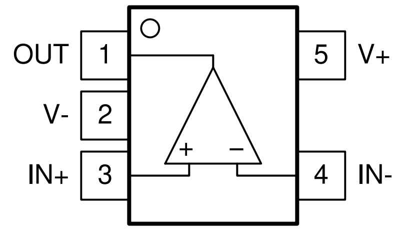


Propagation Delay, (Low to High) vs. Input Overdrive, 12V

Table of Contents

4 Pin Configuration and Functions

Pin Configuration: TLV1831 and TLV1841

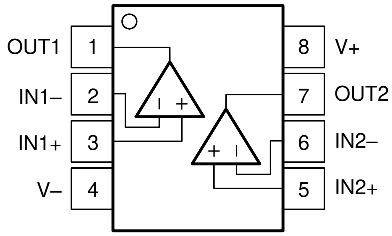


DBV, DCK Packages
SOT-23-5, SC-70-5
Top View
(Standard "north west" pinout)

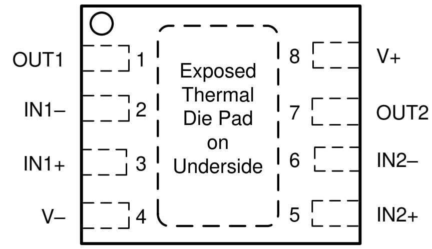
Table 4-1. Pin Functions: TLV1831 and TLV1841

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Output
V-	2	-	Negative supply voltage
IN+	3	I	Non-inverting (+) input
IN-	4	I	Inverting (-) input
V+	5	-	Positive supply voltage

Pin Configurations: TLV1832 and TLV1842



DGK, PW Packages
8-Pin VSSOP, TSSOP
Top View



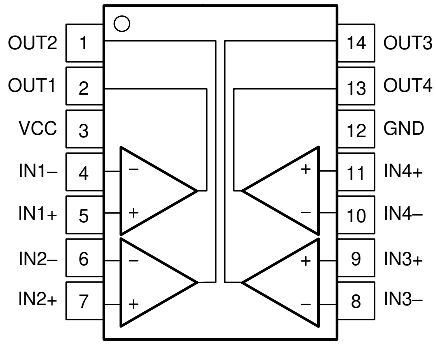
NOTE: Connect exposed thermal pad directly to V- pin.

DSG Package
8-Pad WSON With Exposed Thermal Pad,
Top View

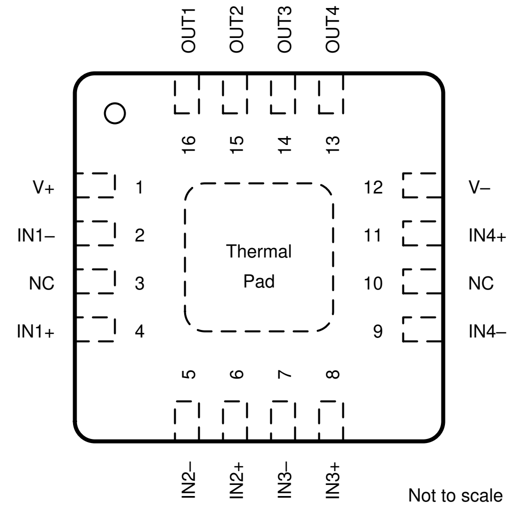
Table 4-2. Pin Functions: TLV1832 and TLV1842

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	O	Output pin of the comparator 1
IN1–	2	I	Inverting input pin of comparator 1
IN1+	3	I	Noninverting input pin of comparator 1
V-	4	—	Negative supply voltage
IN2+	5	I	Noninverting input pin of comparator 2
IN2–	6	I	Inverting input pin of comparator 2
OUT2	7	O	Output pin of the comparator 2
V+	8	—	Positive supply voltage

Pin Configuration and Functions: TLV1834 and TLV1844



DYY Package
14-Pin SOT-23
Top View



NOTE: Connect exposed thermal pad directly to V- pin.

RTE Package,
16-Pad WQFN With Exposed Thermal Pad
Top View

Table 4-3. Pin Functions: TLV1834 and TLV1844

PIN			I/O	DESCRIPTION
NAME	SOT-23	WQFN		
OUT2	1	15	O	Output pin of the comparator 2
OUT1	2	16	O	Output pin of the comparator 1
V+	3	1	-	Positive supply voltage
IN1-	4	2	I	Inverting input pin of the comparator 1
IN1+	5	4	I	Noninverting input pin of the comparator 1
IN2-	6	5	I	Inverting input pin of the comparator 2
IN2+	7	6	I	Noninverting input pin of the comparator 2
IN3-	8	7	I	Inverting input pin of the comparator 3
IN3+	9	8	I	Noninverting input pin of the comparator 3
IN4-	10	9	I	Inverting input pin of the comparator 4
IN4+	11	11	I	Noninverting input pin of the comparator 4
V-	12	12	-	Negative supply voltage
OUT4	13	13	O	Output pin of the comparator 4
OUT3	14	14	O	Output pin of the comparator 3
NC	-	3	-	No internal connection - leave floating or GND
NC	-	10	-	No internal connection - leave floating or GND
Thermal Pad	-	PAD	-	Connect directly to V- pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	–0.3	42	V
Input pins (IN+, IN–) from (V–)[2]	–0.3	(V+) + 0.3	V
Current into input pins (IN+, IN–)	–10	10	mA
Output (OUT) (Open-Drain) from (V–)[3]	–0.3	42	V
Output (OUT) (Push-Pull) from (V–)	–0.3	(V+) + 0.3	V
Output short circuit current[4]	–10	10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings can cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to (V–) and (V+). Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less.
(3) Output (OUT) for open drain can be greater than (V+) and inputs (IN+, IN–) as long as the voltage is within the –0.3V to 42V range
(4) Continuous output short circuits at elevated supply voltages can result in excessive heating and exceeding the maximum allowed junction temperature, leading to eventual device destruction.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC[1]		TLV18x2			UNIT
		PW (TSSOP)	DSG (WSON)	DGK (VSSOP)	
		8 PINS	8 PINS	8 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	157.6	-	-	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	65.7	-	-	°C/W
R_{qJB}	Junction-to-board thermal resistance	96.5	-	-	°C/W
y_{JT}	Junction-to-top characterization parameter	8.1	-	-	°C/W
y_{JB}	Junction-to-board characterization parameter	95.2	-	-	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)		2.7	40	V
Input voltage range from (V–)		–0.2	(V+) + 0.2	V
Output voltage for open drain		–0.2	40	V
Ambient temperature, T_A		–40	125	°C

5.5 Electrical Characteristics

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 12V, V_{CM} = VS/2 at TA = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C	–2.5	±0.3	2.5	mV
		T_A = –40°C to +125°C	–3.0		3.0	mV
dV_{IO}/dT	Input offset voltage drift	T_A = –40°C to +125°C		±1.2		µV/°C
POWER SUPPLY						
I_Q	Quiescent current per comparator, TLV18x1 Only	No Load, Output High T_A = 25°C TLV1831, TLV1841		75	100	µA
		No Load, Output High T_A = –40°C to +125°C TLV1831, TLV1841			105	µA
		No Load, Output Low T_A = 25°C TLV1831, TLV1841		100	135	µA
		No Load, Output Low T_A = –40°C to +125°C TLV1831, TLV1841			140	µA
I_Q	Quiescent current per comparator	No Load, Output High T_A = 25°C		75	95	µA
		No Load, Output High T_A = –40°C to +125°C			100	µA
		No Load, Output Low T_A = 25°C		95	130	µA
		No Load, Output Low T_A = –40°C to +125°C			135	µA
V_{POR}				1.9		V
INPUT BIAS CURRENT						
I_B	Input bias current (1)			500		pA
I_B	Input bias current (1) (2)	T_A = –40°C to +125°C	-5		5	nA
I_{OS}	Input offset current			10		pA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential			5		pF
C_{IC}	Input Capacitance, Common Mode			5		pF
INPUT COMMON MODE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 2.7V to 40V T_A = –40°C to +125°C	(V–) – 0.2		(V+) + 0.2	V
OUTPUT						
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4mA T_A = –40°C to +125°C			400	mV
V_{OH}	Voltage swing from (V+) (for Push-Pull only)	I_{SOURCE} = 4mA T_A = –40°C to +125°C			400	mV
I_{LKG}	Open-drain output leakage current	V_{ID} = +0.1V, V_{PULLUP} = (V+) T_A = –40°C to +125°C		3	70	nA
I_{OL}	Short-circuit current	Sinking T_A = –40°C to +125°C		30		mA
I_{OH}	Short-circuit current	Sourcing T_A = –40°C to +125°C		30		mA

(1) Please see figure for I_{BIAS} vs V_{ID} performance curve
(2) This parameter is verified by design and/or characterization and is not tested in production.

5.6 Switching Characteristics

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 12V, V_{CM} = VS/2, C_L = 15pF at TA = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output						
$T_{PD\text{-}HL}$	Propagation delay time, high-to-low	V_{OD} = 10mV, V_{UD} = 100mV V_{PU} = 5V and R_{PU} = 10k (open-drain output only)		110		ns
$T_{PD\text{-}HL}$	Propagation delay time, high-to-low	V_{OD} = 100mV, V_{UD} = 100mV V_{PU} = 5V and R_{PU} = 10k (open-drain output only)		65		ns
$T_{PD\text{-}LH}$	Propagation delay time, low-to-high, push-pull output	V_{OD} = 10mV, V_{UD} = 100mV		110		ns
$T_{PD\text{-}LH}$	Propagation delay time, low-to-high, push-pull output	V_{OD} = 100mV, V_{UD} = 100mV		65		ns
T_{RISE}	Output Rise Time, 20% to 80%, push-pull output	V_{OD} = 100mV, V_{UD} = 100mV		5		ns
T_{FALL}	Output Fall Time, 80% to 20%	V_{OD} = 100mV, V_{UD} = 100mV		5		ns
F_{TOGGLE}	Toggle Frequency	V_{ID} = 200mV		7.5		MHz
POWER ON TIME						
P_{ON}	Power on-time			80		µs

5.7 Typical Characteristics

At T_A = 25°C, V_S = 12V, V_{CM} = V_S/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV, R_{PU} = 10kΩ, unless otherwise noted.

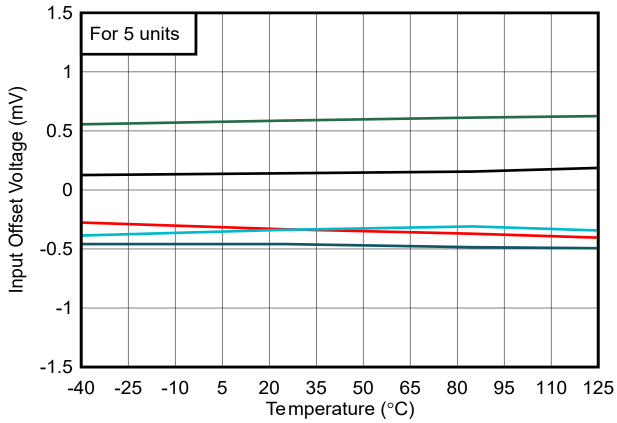


Figure 5-1. Offset vs. Temperature

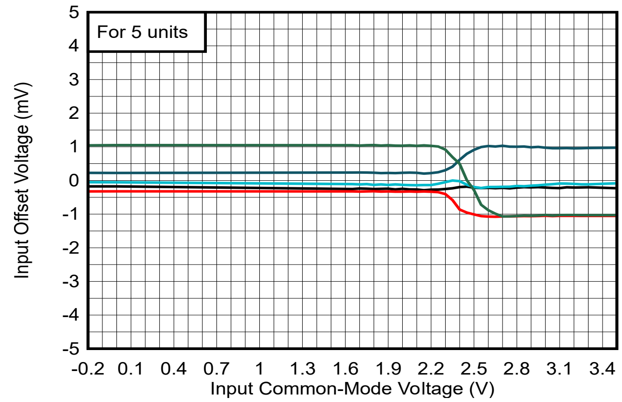


Figure 5-2. Offset vs. Common-Mode, 3.3V

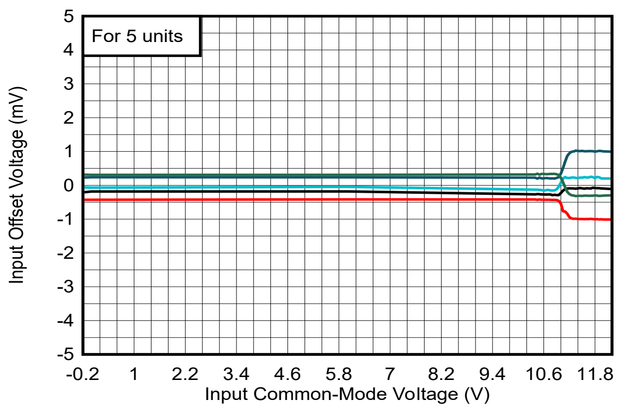


Figure 5-3. Offset Voltage vs. Common-Mode, 12V

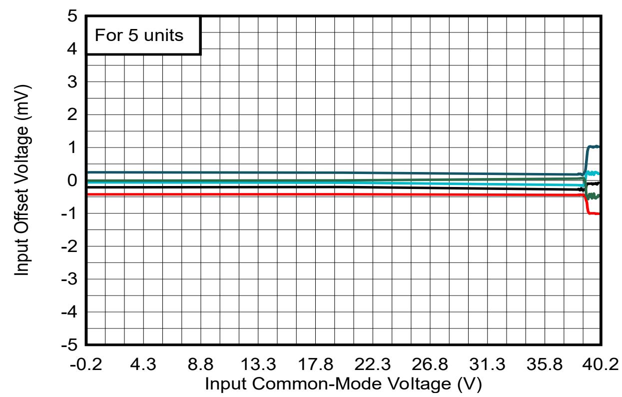


Figure 5-4. Offset Voltage vs. Common-Mode, 40V

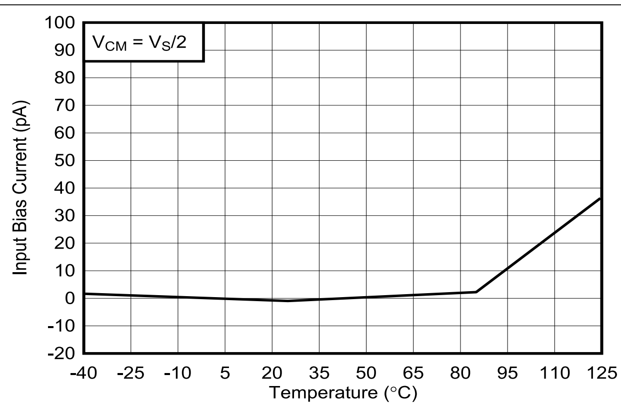


Figure 5-5. Bias Current vs. Temperature, 3.3V

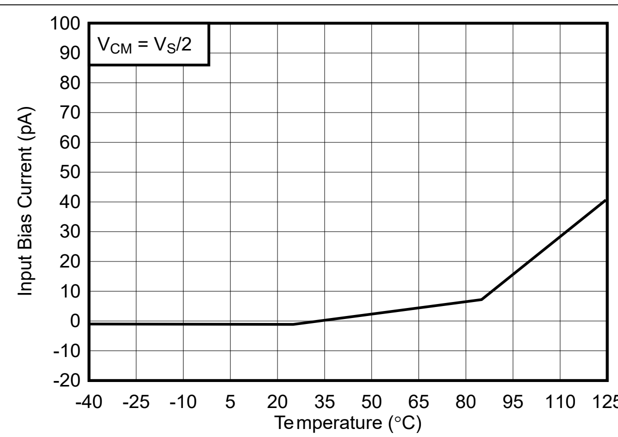


Figure 5-6. Bias Current vs. Temperature, 40V

5.7 Typical Characteristics (continued)

At T_A = 25°C, V_S = 12V, V_{CM} = V_S/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV, R_{PU} = 10kΩ, unless otherwise noted.

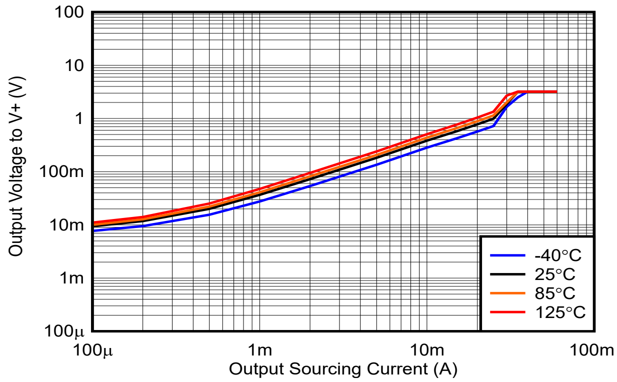


Figure 5-7. Output Voltage vs. Sourcing Current, 3.3V, Push-Pull only

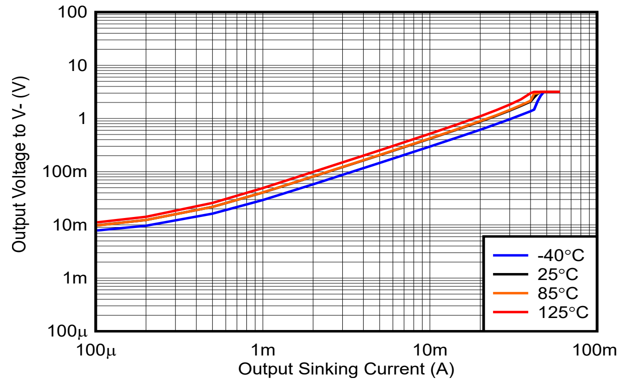


Figure 5-8. Output Voltage vs. Sinking Current, 3.3V

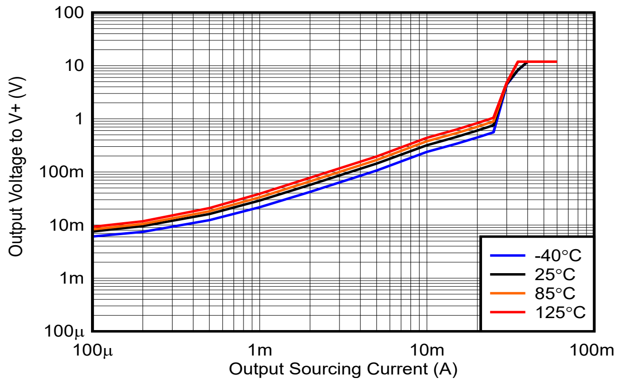


Figure 5-9. Output Voltage vs. Sourcing Current, 12V, Push-Pull only

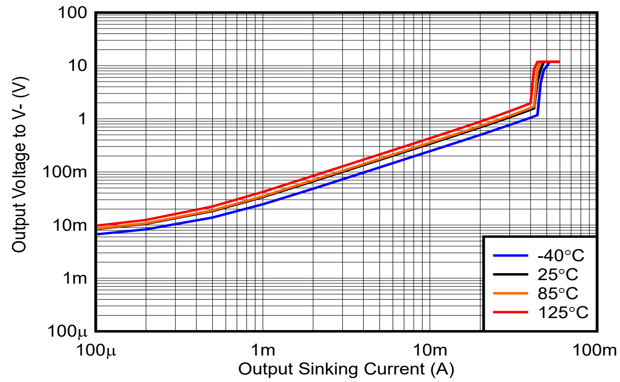


Figure 5-10. Output Voltage vs. Sinking Current, 12V

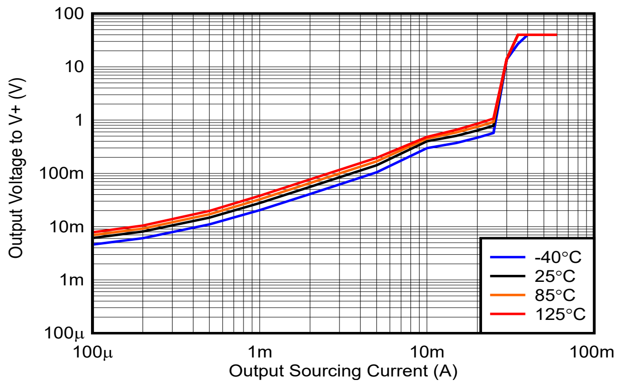


Figure 5-11. Output Voltage vs. Sourcing Current, 40V, Push-Pull only

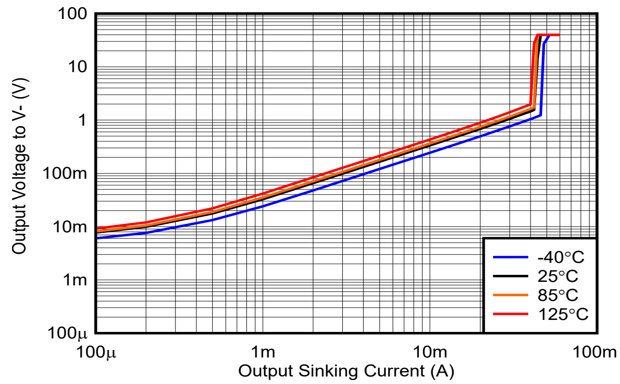


Figure 5-12. Output Voltage vs. Sinking Current, 40V

5.7 Typical Characteristics (continued)

At T_A = 25°C, V_S = 12V, V_{CM} = V_S/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV, R_{PU} = 10kΩ, unless otherwise noted.

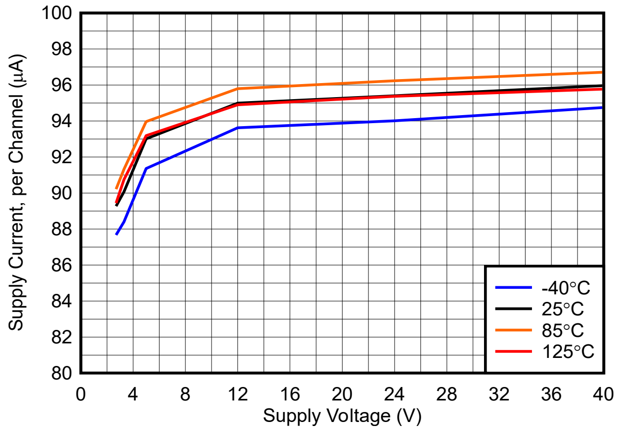


Figure 5-13. Supply Current vs. Supply Voltage, Output Low, No Load

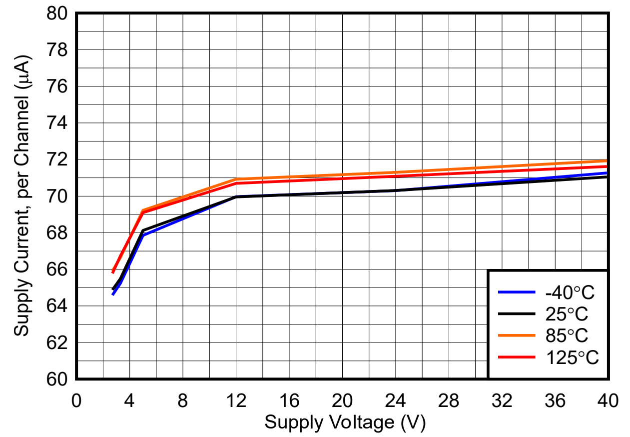


Figure 5-14. Supply Current vs. Supply Voltage, Output High, No Load

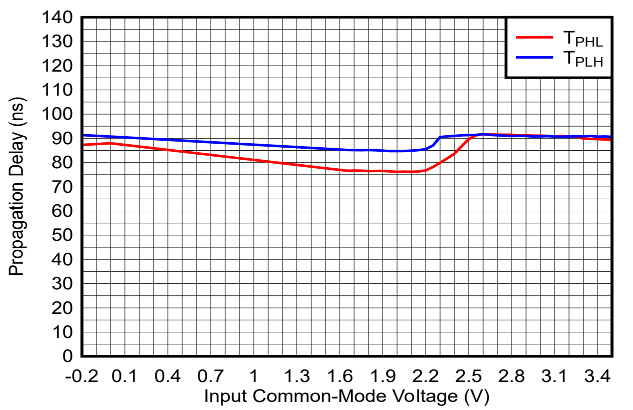


Figure 5-15. Propagation Delay vs. Common-Mode, 3.3V

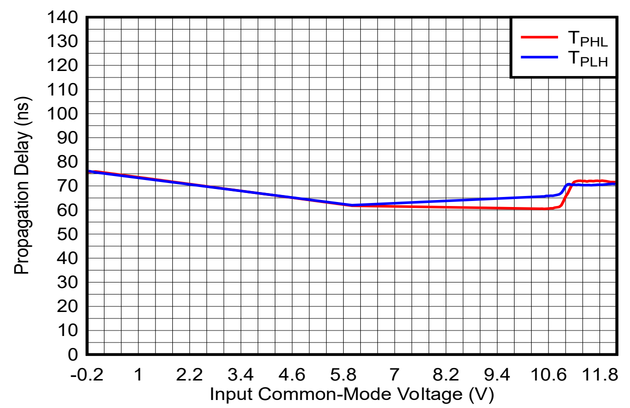


Figure 5-16. Propagation Delay vs. Common-Mode, 12V

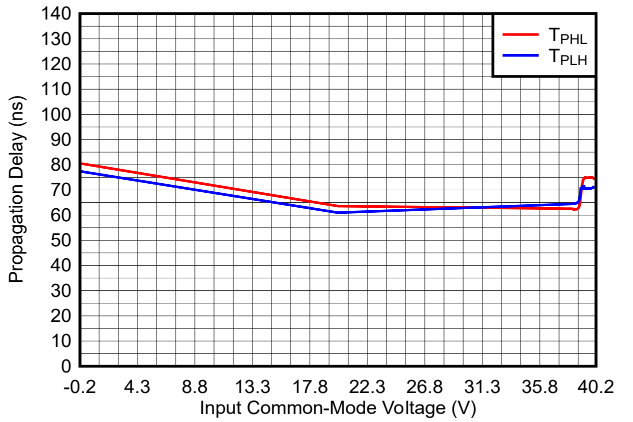


Figure 5-17. Propagation Delay vs. Common-Mode, 40V

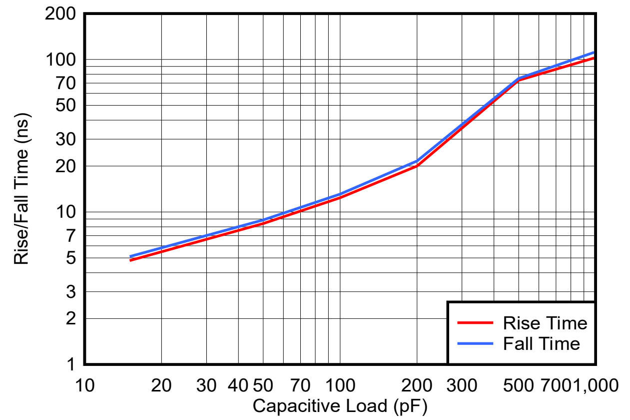


Figure 5-18. Rise/Fall Time vs. Capacitive Load, 12V

5.7 Typical Characteristics (continued)

At T_A = 25°C, V_S = 12V, V_{CM} = V_S/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV, R_{PU} = 10kΩ, unless otherwise noted.

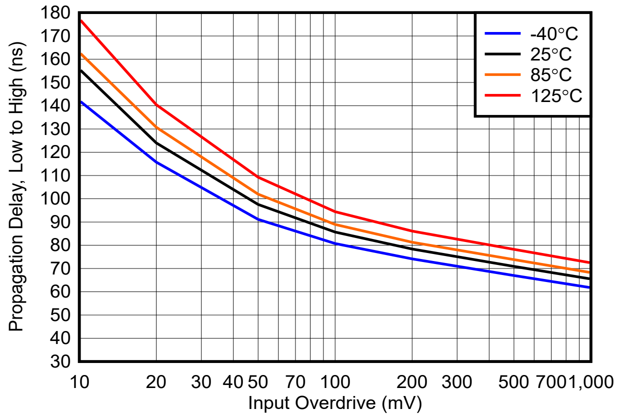


Figure 5-19. Propagation Delay, (Low to High) vs. Input Overdrive, 3.3V

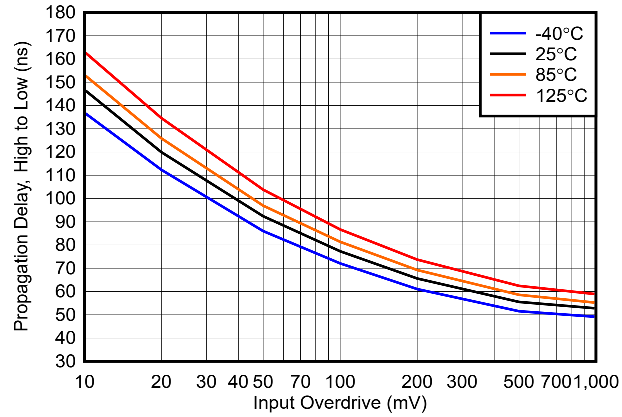


Figure 5-20. Propagation Delay, (High to Low) vs. Input Overdrive, 3.3V

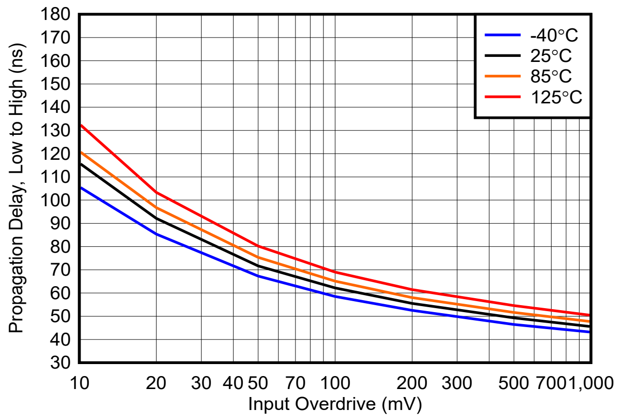


Figure 5-21. Propagation Delay, (Low to High) vs. Input Overdrive, 12V

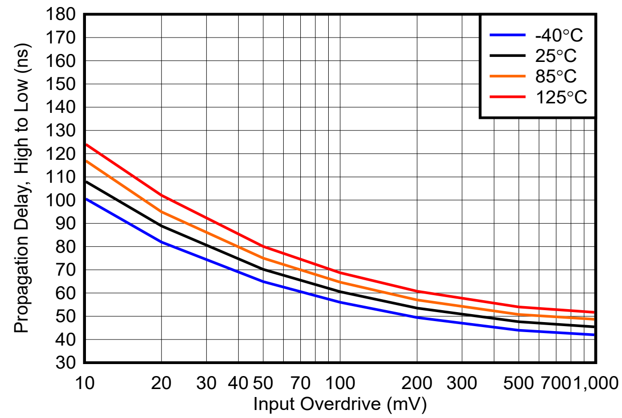


Figure 5-22. Propagation Delay, (High to Low) vs. Input Overdrive, 12V

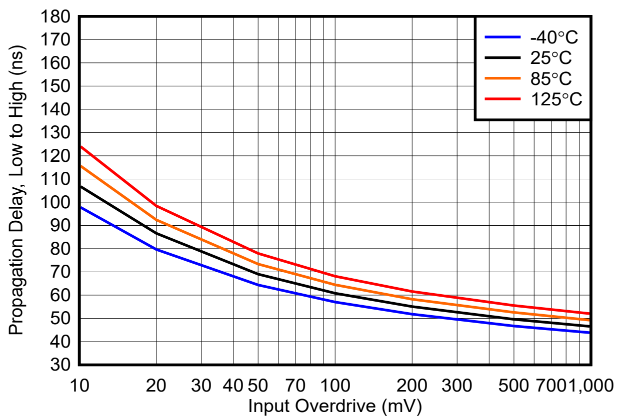


Figure 5-23. Propagation Delay, (Low to High) vs. Input Overdrive, 40V

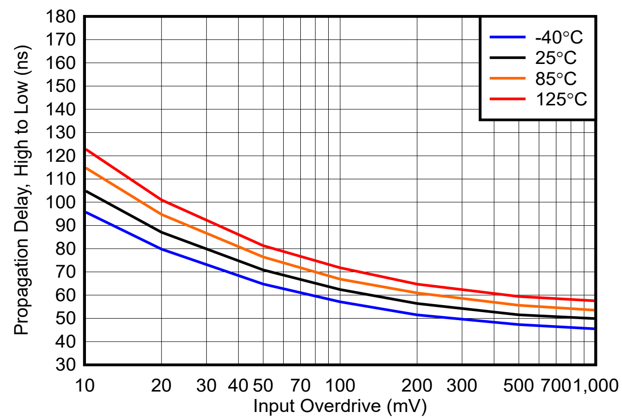


Figure 5-24. Propagation Delay, (High to Low) vs. Input Overdrive, 40V

5.7 Typical Characteristics (continued)

At T_A = 25°C, V_S = 12V, V_{CM} = V_S/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV, R_{PU} = 10kΩ, unless otherwise noted.

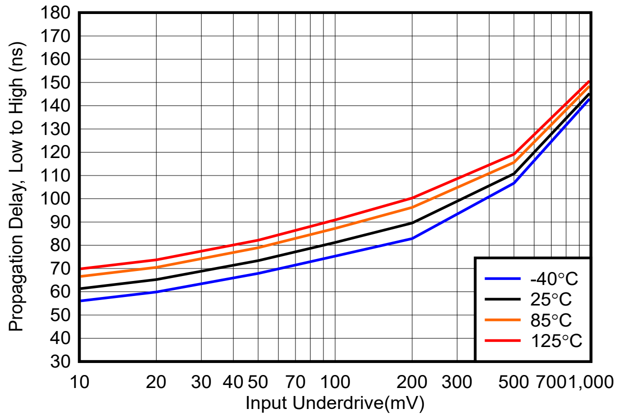


Figure 5-25. Propagation Delay, (Low to High) vs. Input Underdrive, 3.3V

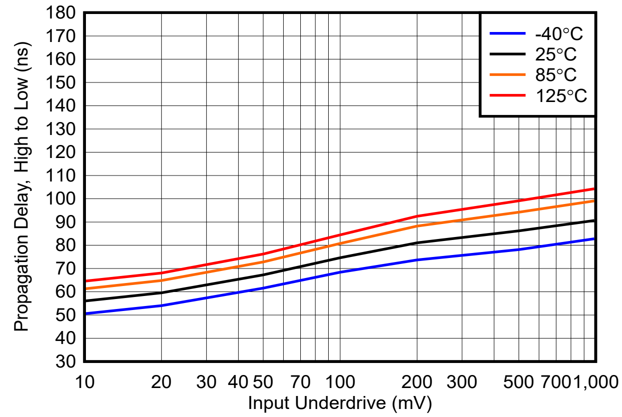


Figure 5-26. Propagation Delay, (High to Low) vs. Input Underdrive, 3.3V

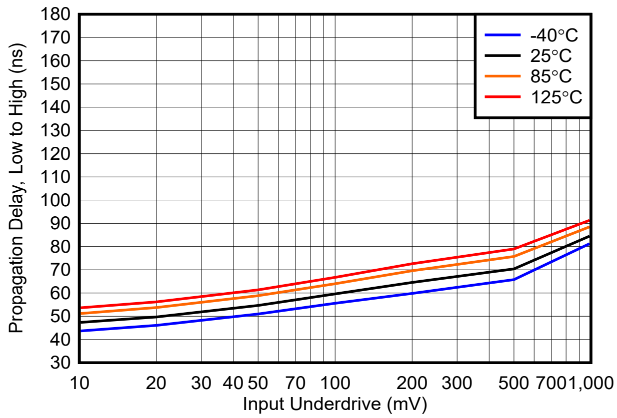


Figure 5-27. Propagation Delay, (Low to High) vs. Input Underdrive, 12V

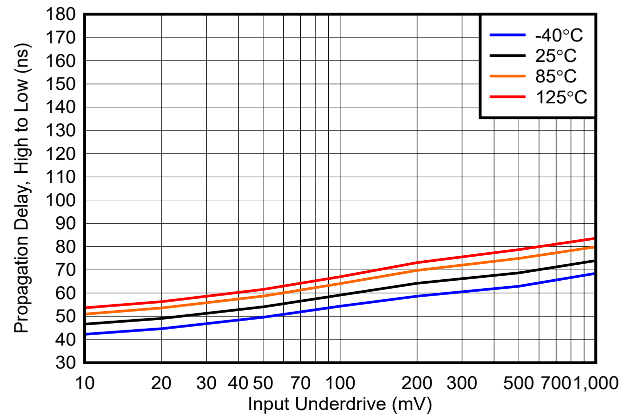


Figure 5-28. Propagation Delay, (High to Low) vs. Input Underdrive, 12V

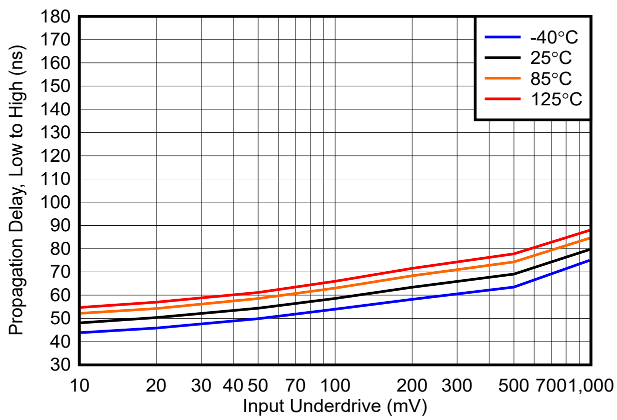


Figure 5-29. Propagation Delay, (Low to High) vs. Input Underdrive, 40V

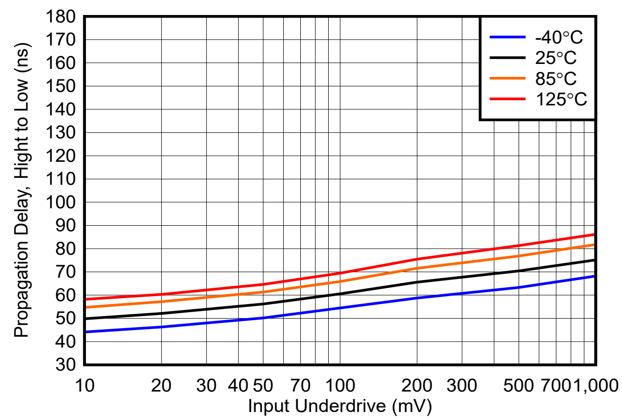


Figure 5-30. Propagation Delay, (High to Low) vs. Input Underdrive, 40V

6 Detailed Description

6.1 Overview

The TLV183x and TLV184x devices are 40V high-speed comparators with push-pull and open-drain output options. Operating down to 2.7V while only consuming only 75µA per channel, the TLV183x and TLV184x are designed for voltage and current sensing applications in high voltage industrial and automotive systems. An internal power-on reset circuit makes sure that the output remains in a known state during power-up and power-down.

6.2 Functional Block Diagrams

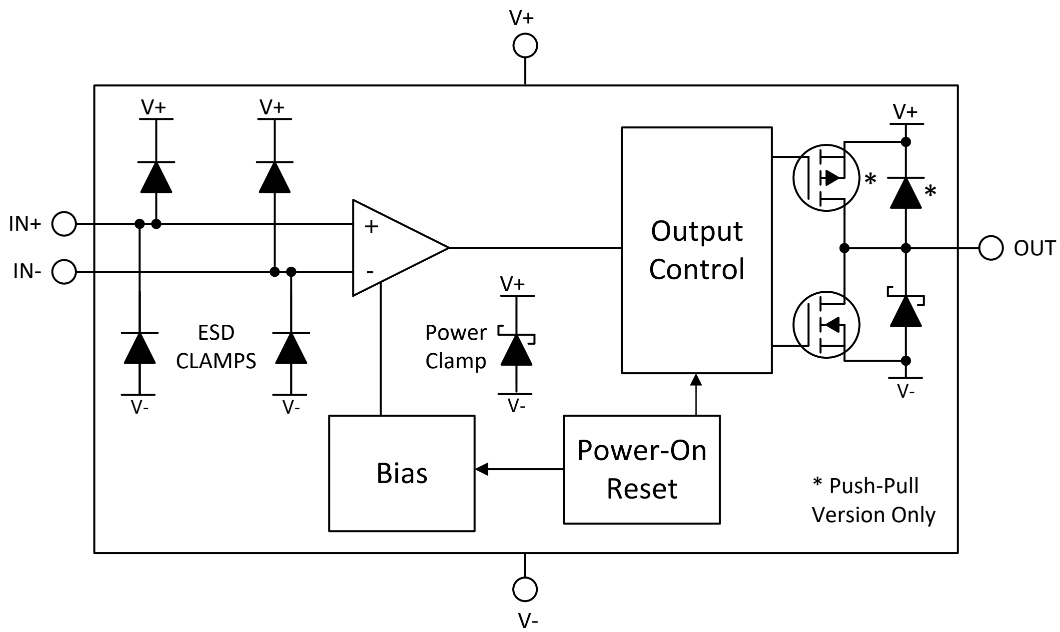


Figure 6-1. Block Diagram

6.3 Feature Description

The TLV183x (push-pull output) and TLV184x (open-drain output) devices are high speed comparators with a typical propagation delay of 65ns and are capable of operating at voltages up to 40V. These comparators are well-suited for high-voltage systems where it is essential to have short-circuit current and over voltage protection for its internal components. These comparators also feature a rail-to-rail input stage capable of operating up to 200mV beyond the power supply rails combined with a maximum 4.5mV input offset and Power-on Reset (POR) for known start-up conditions.

6.4 Device Functional Modes

6.4.1 Inputs

6.4.1.1 Rail-to-Rail Input

The input voltage range extends from 200mV below (V-) to 200mV above (V+), maximizing input dynamic range. The input stage has ESD clamps to the (V+) supply line and therefore the input voltages must not exceed the supply voltages by more than 200mV. Do not apply signals to the rail to rail inputs with no supply voltage. To avoid damaging the inputs when exceeding the recommended input voltage range, an external resistor must be used to limit the current to less than 1mA.

Likewise, unlike high-speed amplifiers, the comparator inputs do not have clamping diodes between them. This allows for applications where the input differential voltage can match the supply voltage (V+). However, when the input differential voltage increases to 2V, bias current increases to the nA range occur. This is a result of internal circuitry intended to minimize propagation delay increases due to large input underdrive amplitudes.

6.4.1.2 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even (V+).

6.4.2 Outputs

6.4.2.1 TLV183x Push-Pull Output

The TLV183x features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for an external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the supply rails ((V+) when output "low" or (V-) when output "High") can result in thermal runaway and eventual device destruction at high (>12V) supply voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output.

6.4.2.2 TLV184x Open-Drain Output

The TLV184x features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage up to 40V, independent of the comparator supply voltage (V+). The open-drain output also allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA to optimize V_{OL} logic levels. Lower pull-up resistor values help increase the rising edge risetime, but at the expense of increasing V_{OL} and higher power dissipation. The risetime is dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1MΩ) create an exponential rising edge due to the output RC time constant and increase the risetime.

Directly shorting the output to (V+) can result in thermal runaway and eventual device destruction at high (>12V) pull-up voltages. If output shorts are possible, a series current limitng resistor is recommended to limit the power dissipation.

Unused open drain outputs must be left floating, or can be tied to the (V-) pin if floating pins are not desired.

6.4.3 ESD Protection

6.4.3.1 Inputs

The rail-to-rail input does have an ESD clamp to (V+) and (V-) and therefore the input voltage must not exceed the supply voltages by more than 200mV. Do not apply signals to the rail to rail inputs with no supply voltage. To avoid damaging the inputs when exceeding the recommended input voltage range, an external resistor must be used to limit the current to less than 1mA.

Similarly, if the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, add a current-limiting resistor in series with the input to limit any transient currents if the clamps conduct. Limit the current to 1mA or less. This series resistance can be part of any resistive input dividers or networks.

6.4.3.2 Outputs

The TLV183x push-pull output ESD protection contains a conventional ESD clamp between the output and (V+), and a ESD clamp between the output and (V-). The output must not exceed the supply rails by more than 200mV.

The TLV184x open-drain output ESD protection consists of an ESD clamping circuit to (V-) only to allow the output to be pulled above (V+) to a maximum of 40V. There is no ESD clamp diode between the output and (V+) on the open-drain output.

6.4.4 Power-On Reset (POR)

The TLV183x and TLV184x devices have an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry is activated for up to 80µs after the V_{POR} of 1.9V is crossed. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

For both TLV183x and TLV184x devices, the POR circuit keeps the output high impedance (Hi-Z) during the POR period (P_{on}).

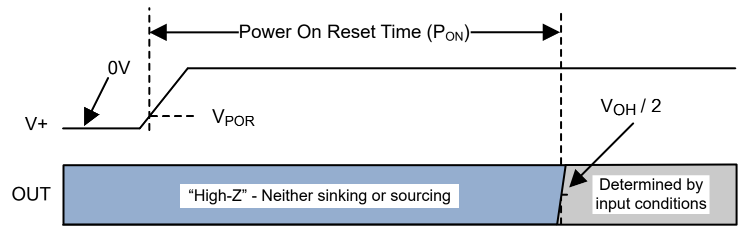


Figure 6-2. Power-On Reset Timing Diagram

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Basic Comparator Definitions

7.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Figure 7-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). Table 7-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

Table 7-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in Figure 7-1 and is measured from the mid-point of the input to the midpoint of the output.

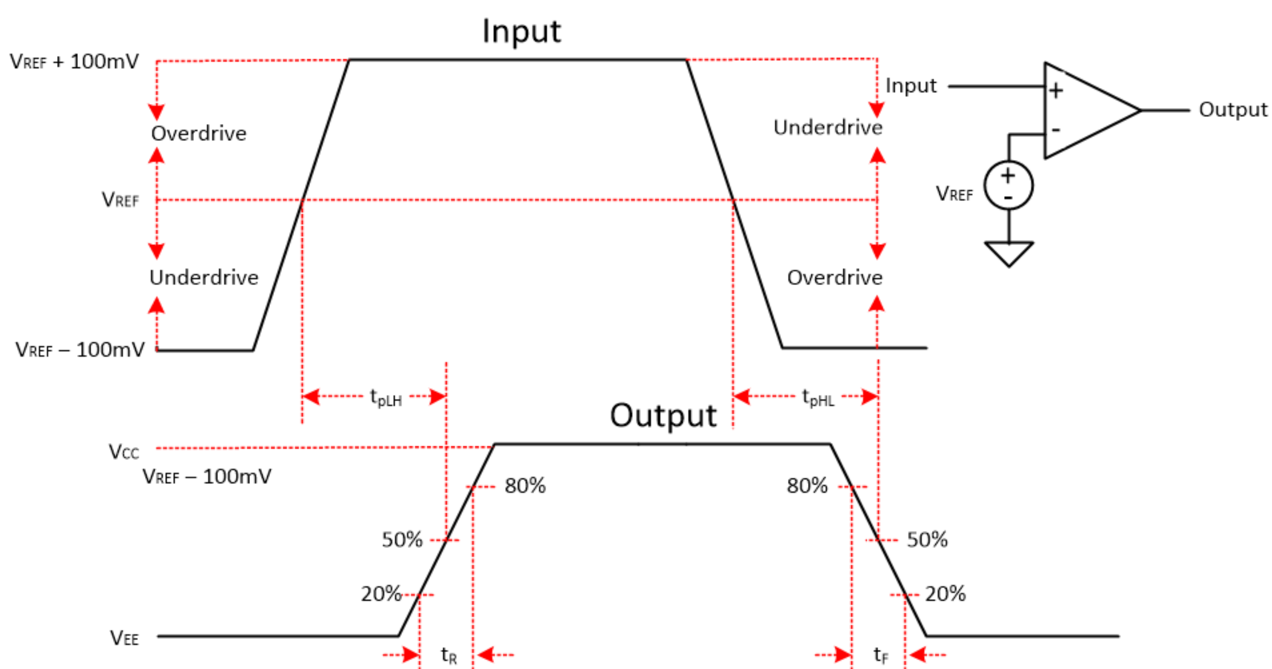


Figure 7-1. Comparator Timing Diagram

7.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the Figure 7-1 example. The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, TI recommends applying the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

7.1.2 Hysteresis

The basic comparator configuration can produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by adding external hysteresis to the comparator.

External hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on the current output state.

The hysteresis transfer curve is shown in Figure 7-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-}. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

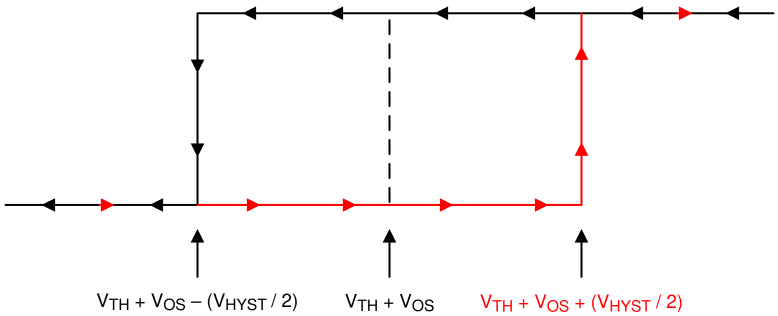


Figure 7-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

7.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 7-3.

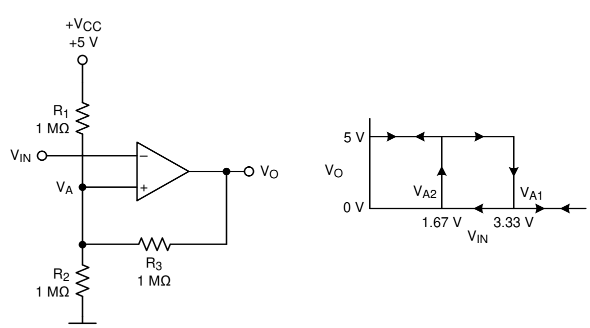


Figure 7-3. TLV183x in an Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 7-3.

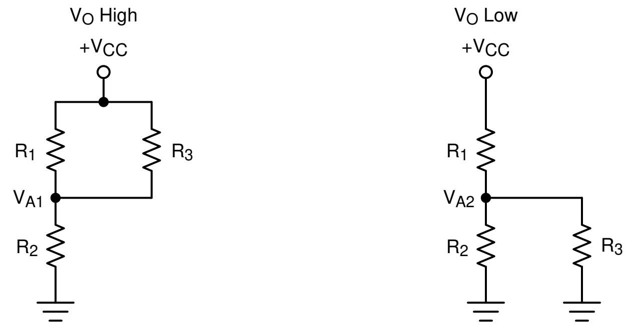


Figure 7-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown in Figure 7-4.

Equation 1 below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown in Equation 2.

Use Equation 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

Equation 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

7.1.2.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in Figure 7-5,

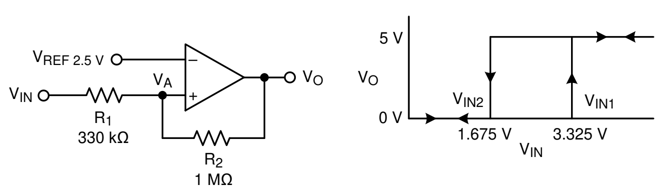


Figure 7-5. TLV183x in a Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 7-6.

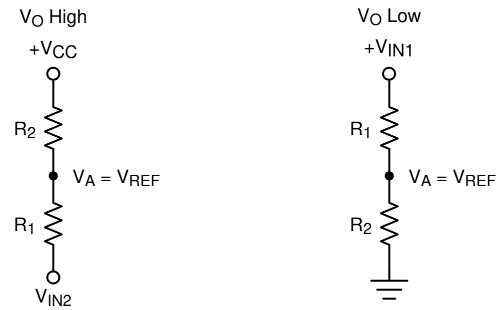


Figure 7-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF},, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use Equation 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use Equation 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

7.1.2.3 Inverting and Non-Inverting Hysteresis using Open-Drain Output

It is also possible to use an open drain output device, such as the TLV184x, but the output pull-up resistor must also be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. Thus, the feedback resistor is actually seen as R2 + R_{PULLUP}. TI recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

7.2 Typical Applications

7.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 7-7 shows a simple window comparator circuit. Window comparators require open drain outputs (TLV184x if the outputs are directly connected together.

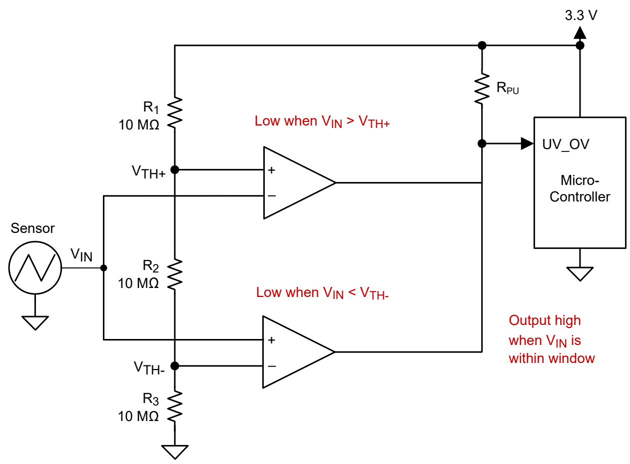


Figure 7-7. Window Comparator

7.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1V
- Alert (logic low output) when an input signal is greater than 2.2V
- Alert signal is active low
- Operate from a 3.3V power supply

7.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 7-7. Connect V+ to a 3.3V power supply and V_{EE} to ground. Make R1, R2 and R3 each 10MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and $V_{TH–}$).

With each resistor being equal, V_{TH+} is 2.2V and V_{TH-} is 1.1V. Large resistor values such as 10MΩ are used to minimize power consumption. The resistor values can be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and noninverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs will be low when the sensor is less than 1.1V or greater than 2.2V. The respective comparator outputs will be high when the sensor is in the range of 1.1V to 2.2V (within the "window"), as shown in Figure 7-8.

7.2.1.3 Application Curve

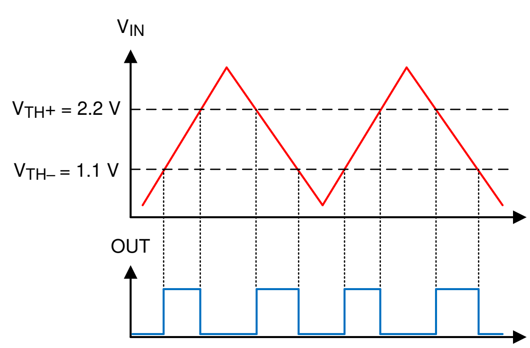


Figure 7-8. Window Comparator Results

For more information, please see Application note SBOA221 "Window comparator circuit".

7.2.2 Square Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source. A push-pull output (TLV183x) is recommended for best symmetry.

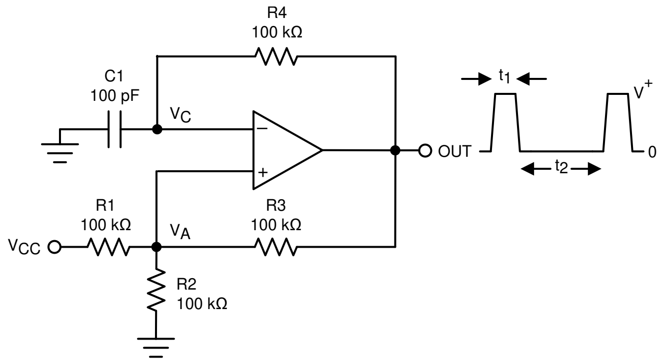


Figure 7-9. Square-Wave Oscillator

7.2.2.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor C_1 and resistor R_4. The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which can help to reduce BOM cost and board space. TI recommends that R4 be over several kilo-ohms to minimize loading of the output.

7.2.2.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

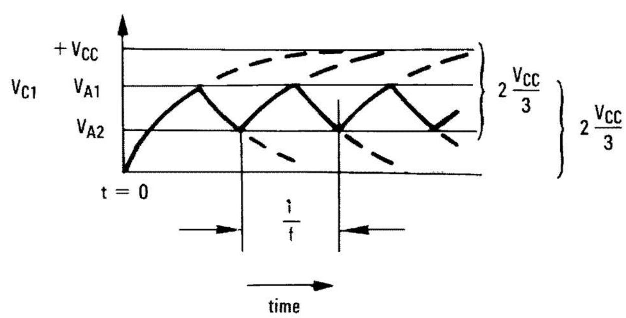


Figure 7-10. Square-Wave Oscillator Timing Thresholds

First consider the output of Figure Square-Wave Oscillator as high, which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at the point is calculated below.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 || R_3} \tag{7}$$

if $R_1 = R_2 = R_3$, then $V_{A1} = 2V_{CC}/3$

At this time the comparator output trips pulling down the output to the negative rail. The value of $V_A$at this point is calculated below.

$$V_{A2} = \frac{V_{CC}(R_2 || R_3)}{R_1 + R_2 || R_3} \tag{8}$$

if $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges though the R_4, and the voltage V_{CC} decreases until it reaches V_{A2}. At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for C_1 from $2V_{CC}/3$ to V_{CC} / 3 then back to $2V_{CC}/3$, which is given by R_4C_1 × ln 2 for each trip. Therefore, the total time duration is calculated as 2 R_4C_1 × ln 2.

The oscillation frequency can be obtained below.

$$f = 1/(2\ R4 \times C1 \times \ln 2) \tag{9}$$

7.2.2.3 Application Performance Plots

The Square-Wave Oscillator Output Waveform shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 10k\Omega$
- C_1 =100pF, C_L = 20pF
- V+ = 5V, V– = GND
- C_{stray} (not shown) from V_A TO GND = 10pF

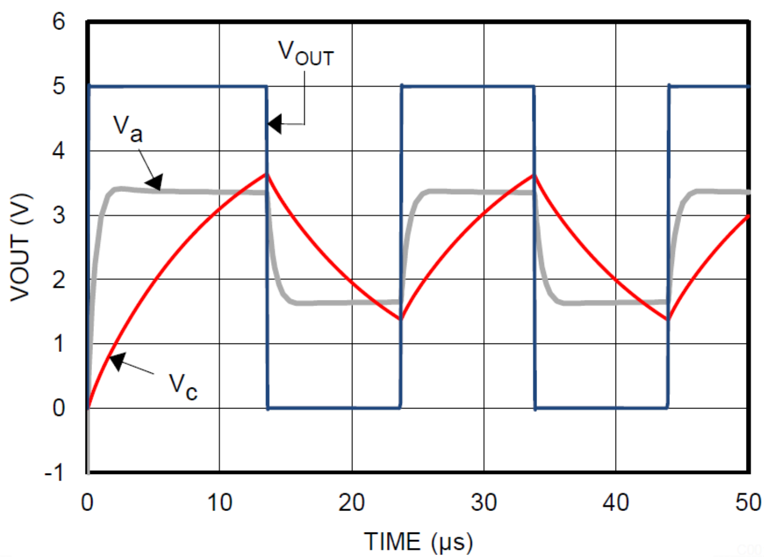


Figure 7-11. Square-Wave Oscillator Output Waveform

7.3 Power Supply Recommendations

Due to fast output edges, bypass capacitors are critical on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic bypass capacitor directly between the (V+) pin and ground pins. Narrow peak currents are drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can impact the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from both "split" supplies ((V+) & (V-)), or "single" supplies ((V+) and GND), with GND applied to the (V-) pin. Input signals must stay within the recommended input range for either type. Note that with a "split" supply the output now swings "low" (V_{OL}) to (V-) potential and not GND.

7.4 Layout

7.4.1 Layout Guidelines

For accurate comparator applications it is important to maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the (V+) and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. As shown in the figure below, it is "OK" to run input and output traces in parallel as long as there is a (V+) or GND trace between output to reduce coupling. A "better" way to reduce coupling is to have the traces ran further away from each other.

When series resistance is added to inputs, place the resistor close to the device. A low value (<100 ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

7.4.2 Layout Example

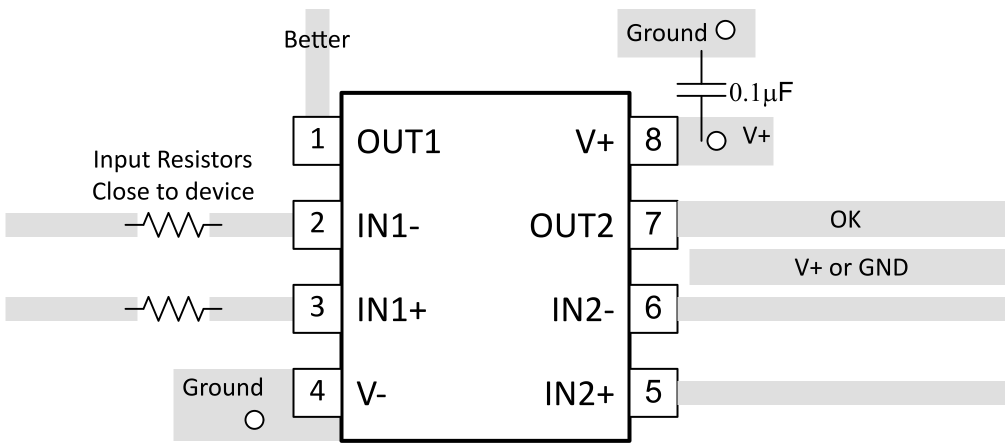


Figure 7-12. Dual Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design— TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design— TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

A Quad of Independently Func Comparators - SNOA654

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2024) to Revision A (November 2024)	Page
• Updated quiescent current and input offset voltage specifications throughout document	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.