

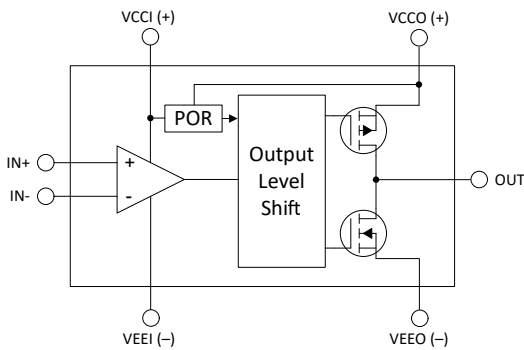
# TLV1871/2 40V High-Speed Comparator with Separate Input and Output Supplies

## 1 Features

- Wide supply range: 2.7V to 40V ( $\pm 1.35V$  to  $\pm 20V$ )
- 65ns propagation delay
- Single or split supplies operation
- "Floating" push-pull output with separate supplies
- Rail-to-rail input
- Power-on-reset (POR)
- Low supply current: 75 $\mu A$  per channel
- Temperature range:  $-40^{\circ}C$  to  $+125^{\circ}C$

## 2 Applications

- [Class D Amplifiers](#)
- [Level Translation](#)
- [Motor Drives](#)
- [Bipolar Zero Cross Detectors](#)



**Simplified Internal Diagram**

## 3 Description

The TLV187x is a 40V high-speed comparator family that offers rail-to-rail inputs and a push-pull output-stage with separate input and output supply pins. These features coupled with 65ns propagation delay make this family well-suited for bipolar zero-cross detection, Class D audio amplifier systems, and other applications where level translation and propagation delay symmetry is needed.

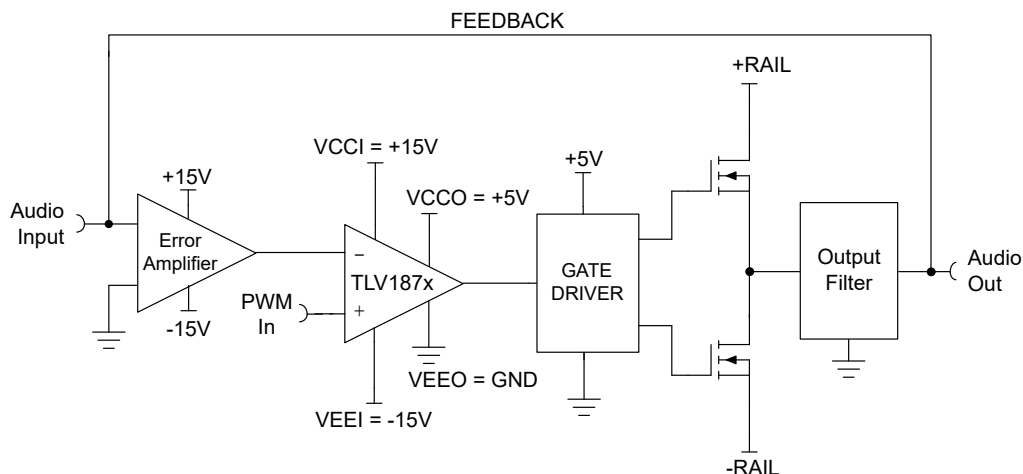
This device includes a Power-On Reset (POR) feature that holds the output in a known state until the minimum supply voltage has been reached before the output responds to the inputs, thus preventing false outputs during system power-up and power-down.

The TLV187x has a push-pull output stage, making them an excellent choice for applications where symmetry between rising and falling output responses is desired. This device offers the ability to level translate for downstream devices at lower voltages due to the separate input and output supplies.

### Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
TLV1871	SOT-23 (8)	1.60mm × 2.90mm
TLV1872	VSSOP (10)	3.00mm × 3.00mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



**Class D Amplifier Example**

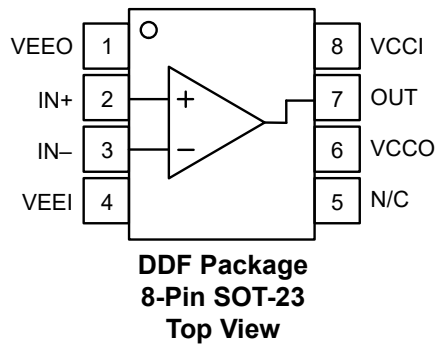


## Table of Contents

<b>1 Features</b> .....	1	6.3 Feature Description.....	15
<b>2 Applications</b> .....	1	6.4 Device Functional Modes.....	16
<b>3 Description</b> .....	1	<b>7 Application and Implementation</b> .....	19
<b>4 Pin Configuration and Functions</b> .....	3	7.1 Application Information.....	19
4.1 Pin Configurations: TLV1871 Single.....	3	7.2 Typical Applications.....	21
Pin Configurations: TLV1872 Dual.....	4	7.3 Power Supply Recommendations.....	22
<b>5 Specifications</b> .....	5	7.4 Layout.....	22
5.1 Absolute Maximum Ratings.....	5	<b>8 Device and Documentation Support</b> .....	23
5.2 ESD Ratings.....	5	8.1 Documentation Support.....	23
5.3 Thermal Information.....	6	8.2 Receiving Notification of Documentation Updates....	23
5.4 Recommended Operating Conditions.....	6	8.3 Support Resources.....	23
5.5 Electrical Characteristics.....	7	8.4 Trademarks.....	23
5.6 Switching Characteristics.....	8	8.5 Electrostatic Discharge Caution.....	23
5.7 Typical Characteristics.....	9	8.6 Glossary.....	23
<b>6 Detailed Description</b> .....	15	<b>9 Revision History</b> .....	24
6.1 Overview.....	15	<b>10 Mechanical, Packaging, and Orderable Information</b> .....	24
6.2 Functional Block Diagram.....	15		

## 4 Pin Configuration and Functions

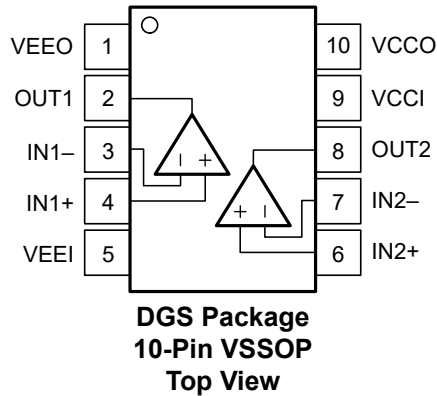
### 4.1 Pin Configurations: TLV1871 Single



**Table 4-1. Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
VEEO	1	—	Output negative supply voltage
IN+	2	I	Non-Inverting input
IN-	3	I	Inverting input
VEEI	4	—	Input negative supply voltage
NC	5	—	No connect
VCCO	6	O	Output positive supply voltage
OUT	7	—	Output
VCCI	8	—	Input positive supply voltage

### Pin Configurations: TLV1872 Dual



**Table 4-2. Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
VEEO	1	—	Output negative supply voltage
OUT1	2	O	Output pin of the comparator 1
IN1-	3	I	Inverting input pin of comparator 1
IN1+	4	I	Non-Inverting input pin of comparator 1
VEEI	5	—	Input negative supply voltage
IN2+	6	I	Non-Inverting input pin of comparator 2
IN2-	7	I	Inverting input pin of comparator 2
OUT2	8	O	Output pin of the comparator 2
VCCI	9	—	Input positive supply voltage
VCCO	10	—	Output positive supply voltage

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Input Supply Voltage: ( $V_{CCI} - V_{EEI}$ )	-0.3	42	V
Output Negative Supply Voltage: $V_{EEO}$	$V_{EEI}$	$V_{EEI} + 20$	V
Output Positive Supply Voltage: $V_{CCO}$	$V_{EEO} - 0.3$	$V_{CCI} + 0.3$	V
Input pins (IN+, IN-) <sup>(2)</sup>	$V_{EEI} - 0.3$	$V_{CCI} + 0.3$	V
Current into input pins (IN+, IN-) <sup>(2)</sup>	-10	10	mA
Output (OUT) from $V_{EEO}$ <sup>(3)</sup>	-0.3	$(V_{CCO}) + 0.3$	V
Output short circuit current <sup>(4) (5)</sup>	-10	10	mA
Junction temperature, $T_J$		150	°C
Storage temperature, $T_{stg}$	-65	150	°C

- Operation outside the Absolute Maximum Ratings can cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- Input terminals are diode-clamped to ( $V_{EEI}$ ) and ( $V_{CCI}$ ). Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less.
- Output (OUT) is diode-clamped to ( $V_{EEO}$ ) and ( $V_{CCO}$ ). Please see the *Outputs and ESD Protection* section of the *Application Information* Section for more information.
- Output sinking and sourcing current is internally limited to <35mA when operating within the Absolute Maximum output voltage limits. The Absolute Maximum Output Current limit specified here is the maximum current through the clamp structure when exceeding the supply voltage below ( $V_{EEO}$ ) or above ( $V_{CCO}$ ).
- Continuous output short circuits at elevated supply voltages can result in excessive heating and exceeding the maximum allowed junction temperature, leading to eventual device destruction.

### 5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TLV1871	TLV1872	UNIT
		DDF (SOT-23)	DGS (WSON)	
		8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165.8	151.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.0	55.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.5	84.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	6.6	3.2	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	83.2	83.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) report.

### 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input Supply Voltage: $V_{CCI} - V_{EEI}$	2.7	40	V
Output Negative Supply Voltage: $V_{EEO}$	$V_{EEI}$	$V_{EEI} + 18$	V
Output Positive Supply Voltage: $V_{CCO}$	$V_{EEO} + 2.7$	$V_{CCI}$	V
Input voltage range from $V_{EEI}$	–0.2	$V_{CCI} + 0.2$	V
Ambient temperature, $T_A$	–40	125	°C

## 5.5 Electrical Characteristics

For  $V_{CCI} = 12V$ ,  $V_{EE1} = 0V$ ,  $V_{CCO} = 3.3V$ ,  $V_{EE0} = 0V$ ,  $V_{CM} = 0V$  at  $T_A = 25^\circ C$  (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage	$T_A = 25^\circ C$	-2.5	$\pm 0.3$	2.5	mV
$V_{OS}$	Input offset voltage	$T_A = -40^\circ C$ to $+125^\circ C$	-3.0		3.0	mV
$dV_{IO}/dT$	Input offset voltage drift	$T_A = -40^\circ C$ to $+125^\circ C$		$\pm 1.2$		$\mu V/^\circ C$
<b>POWER SUPPLY</b>						
$I_Q$	Quiescent current per comparator <sup>(2)</sup>	No Load, Output High $T_A = 25^\circ C$		75	100	$\mu A$
		No Load, Output High $T_A = -40^\circ C$ to $+125^\circ C$			105	$\mu A$
		No Load, Output Low $T_A = 25^\circ C$		100	135	$\mu A$
		No Load, Output Low $T_A = -40^\circ C$ to $+125^\circ C$			140	$\mu A$
$V_{POR}$			1.9		V	
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current <sup>(1)</sup>			500		pA
$I_B$	Input bias current <sup>(1) (3)</sup>	$T_A = -40^\circ C$ to $+125^\circ C$	-5		5	nA
$I_{OS}$	Input offset current			10		pA
<b>INPUT CAPACITANCE</b>						
$C_{ID}$	Input Capacitance, Differential			5		pF
$C_{IC}$	Input Capacitance, Common Mode			5		pF
<b>INPUT COMMON MODE RANGE</b>						
$V_{CM-Range}$	Common-mode voltage range	$V_{CCI} - V_{EE1} = 2.7V$ to $36V$ $T_A = -40^\circ C$ to $+125^\circ C$	$V_{EE1} - 0.2$		$V_{CCI} + 0.2$	V
<b>OUTPUT</b>						
$V_{OL}$	Voltage swing from ( $V_{EE0}$ )	$I_{SINK} = 4mA$ $T_A = -40^\circ C$ to $+125^\circ C$			300	mV
$V_{OH}$	Voltage swing from ( $V_{CCO}$ )	$I_{SOURCE} = 4mA$ $T_A = -40^\circ C$ to $+125^\circ C$			300	mV
$I_{OL}$	Short-circuit current	Sinking $T_A = -40^\circ C$ to $+125^\circ C$		30		mA
$I_{OH}$	Short-circuit current	Sourcing $T_A = -40^\circ C$ to $+125^\circ C$		30		mA

(1) Please see figure for  $I_{BIAS}$  vs  $V_{ID}$  performance curve

(2) Current shown is the sum of the current through  $V_{CCI}$  and  $V_{CCO}$ . Please see Supply Current graphs in Typical Characteristics section.

(3) This parameter is assured by design and/or characterization and is not tested in production.

## 5.6 Switching Characteristics

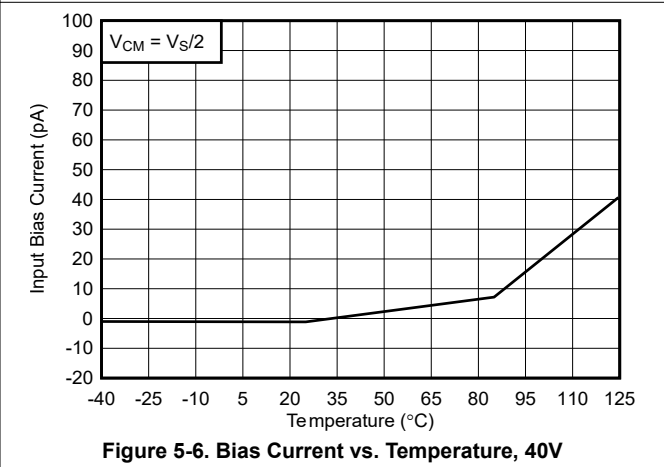
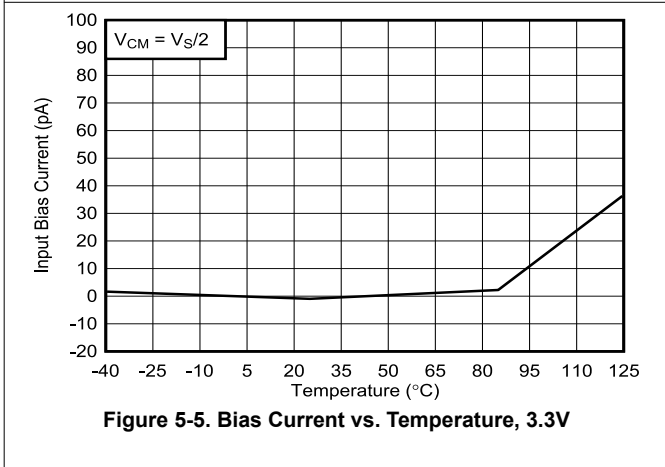
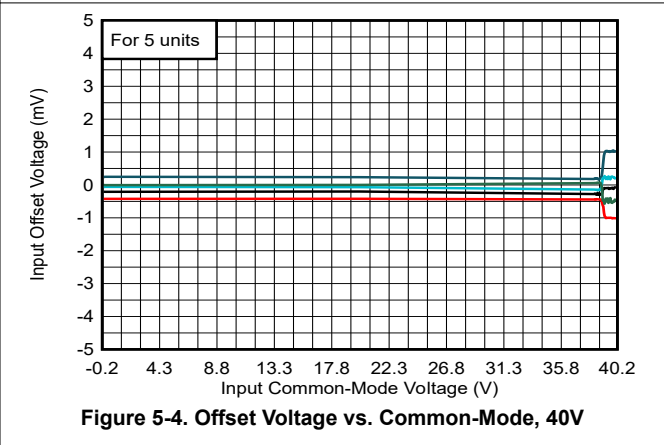
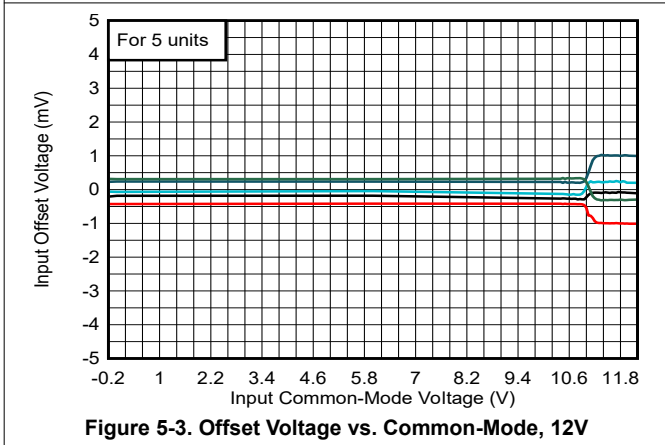
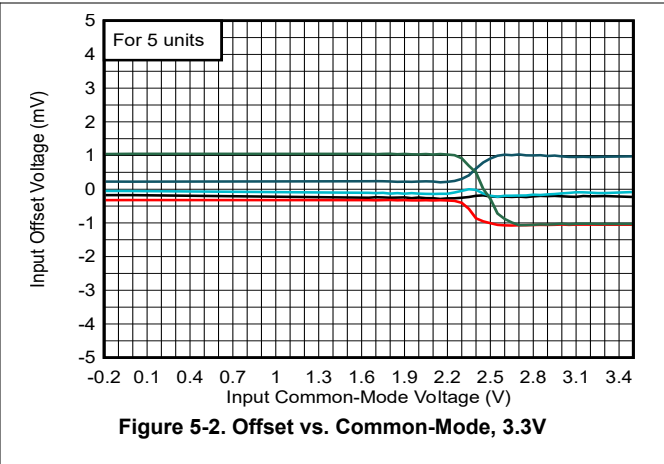
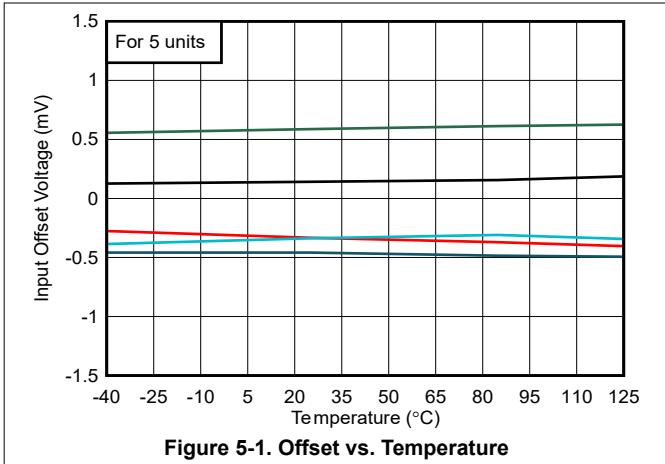
For  $V_{CCI} = 12V$ ,  $V_{EE1} = 0V$ ,  $V_{CCO} = 3.3V$ ,  $V_{EEO} = 0V$ ,  $V_{CM} = VS/2$ ,  $C_L = 15pF$  at  $T_A = 25^\circ C$  (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Output</b>						
$T_{PD-HL}$	Propagation delay time, high-to-low	$V_{OD} = 10mV$ , $V_{UD} = 100mV$		110		ns
$T_{PD-HL}$	Propagation delay time, high-to-low,	$V_{OD} = 100mV$ , $V_{UD} = 100mV$		65		ns
$T_{PD-LH}$	Propagation delay time, low-to-high	$V_{OD} = 10mV$ , $V_{UD} = 100mV$		110		ns
$T_{PD-LH}$	Propagation delay time, low-to-high	$V_{OD} = 100mV$ , $V_{UD} = 100mV$		65		ns
$T_{RISE}$	Output Rise Time, 20% to 80%	$V_{OD} = 100mV$ , $V_{UD} = 100mV$		5		ns
$T_{FALL}$	Output Fall Time, 80% to 20%	$V_{OD} = 100mV$ , $V_{UD} = 100mV$		5		ns
$F_{TOGGLE}$	Toggle Frequency	$V_{ID} = 200mV$		7.5		MHz
<b>POWER ON TIME</b>						
$P_{ON}$	Power on-time			80		$\mu s$



### 5.7 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_{CCI} - V_{EEI} = 12\text{V}$ ,  $V_{CCO} - V_{EEO} = 3.3\text{V}$ ,  $V_{CM} = V_S/2\text{V}$ ,  $C_L = 15\text{pF}$ , Input Overdrive = Input Underdrive = 100mV unless otherwise noted.



### 5.7 Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{CC1} - V_{EE1} = 12\text{V}$ ,  $V_{CCO} - V_{EEO} = 3.3\text{V}$ ,  $V_{CM} = VS/2\text{V}$ ,  $C_L = 15\text{pF}$ , Input Overdrive = Input Underdrive =  $100\text{mV}$  unless otherwise noted.

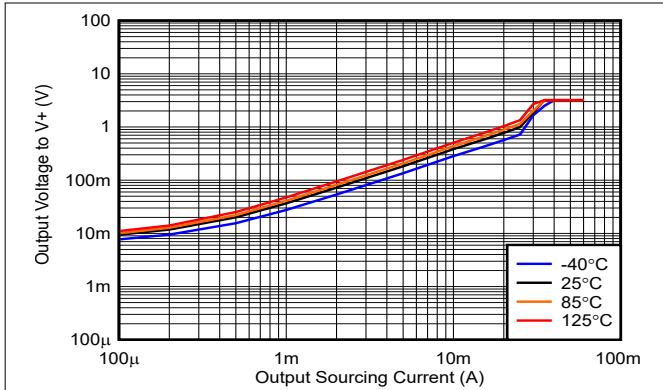


Figure 5-7. Output Voltage vs. Sourcing Current, 3.3V

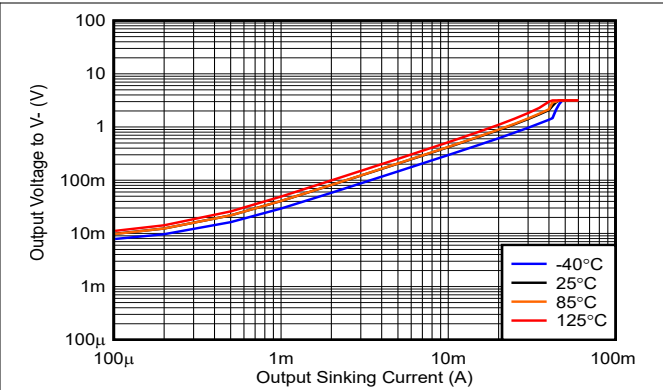


Figure 5-8. Output Voltage vs. Sinking Current, 3.3V

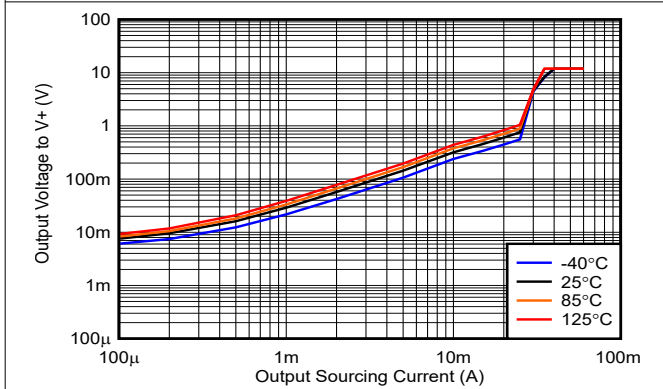


Figure 5-9. Output Voltage vs. Sourcing Current, 12V

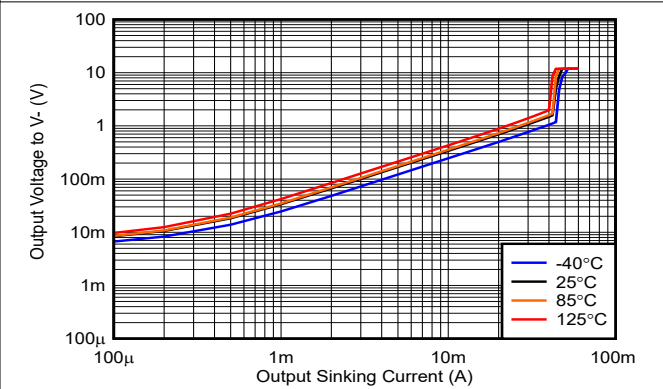


Figure 5-10. Output Voltage vs. Sinking Current, 12V

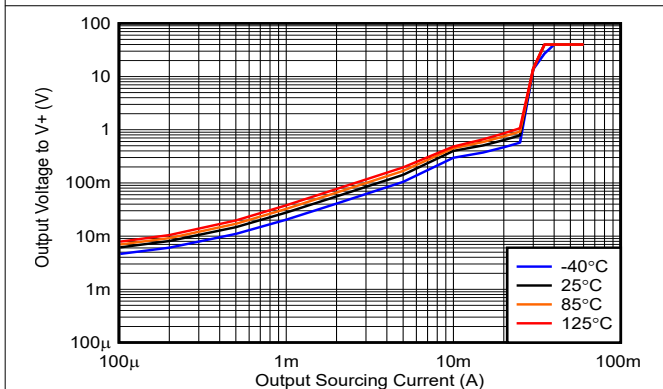


Figure 5-11. Output Voltage vs. Sourcing Current, 40V

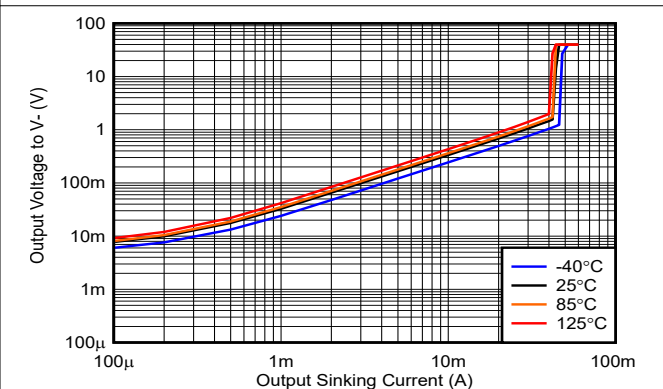


Figure 5-12. Output Voltage vs. Sinking Current, 40V

### 5.7 Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{CCI} - V_{EEI} = 12\text{V}$ ,  $V_{CCO} - V_{EEO} = 3.3\text{V}$ ,  $V_{CM} = VS/2\text{V}$ ,  $C_L = 15\text{pF}$ , Input Overdrive = Input Underdrive = 100mV unless otherwise noted.

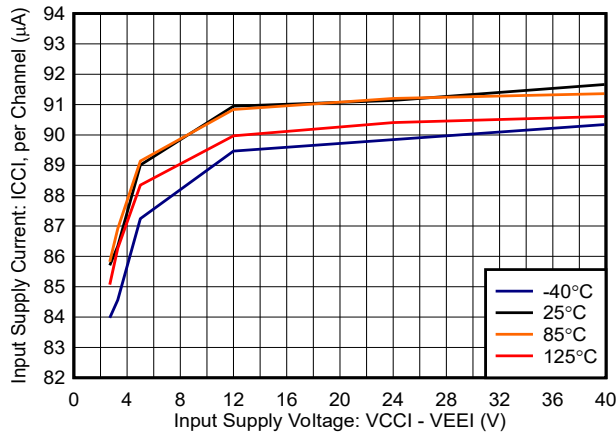


Figure 5-13. Input Supply Current vs. Input Supply Voltage, Output Low, No Load

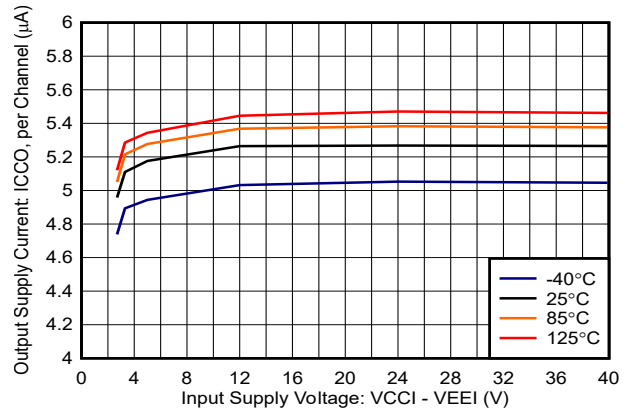


Figure 5-14. Output Supply Current vs. Input Supply Voltage, Output Low, No Load

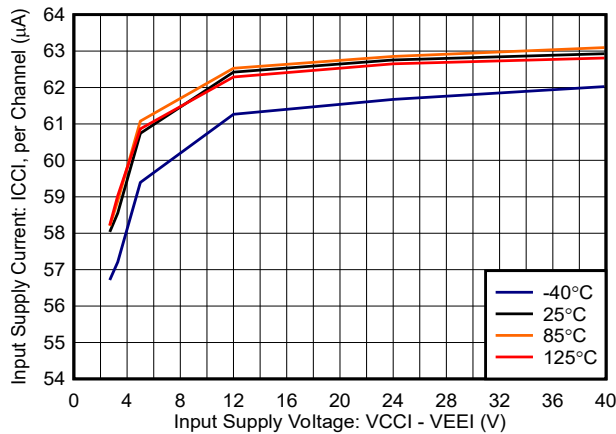


Figure 5-15. Input Supply Current vs. Input Supply Voltage, Output High, No Load

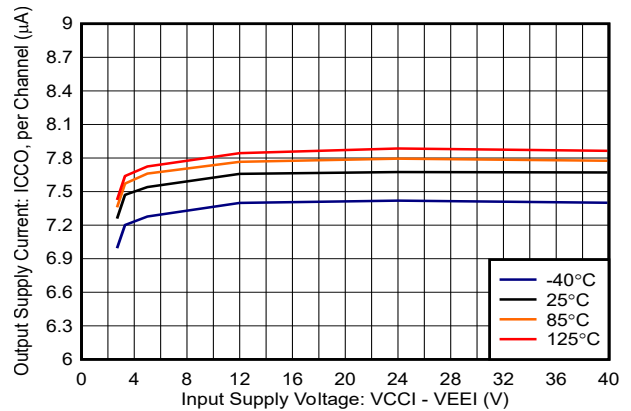


Figure 5-16. Output Supply Current vs. Input Supply Voltage, Output High, No Load

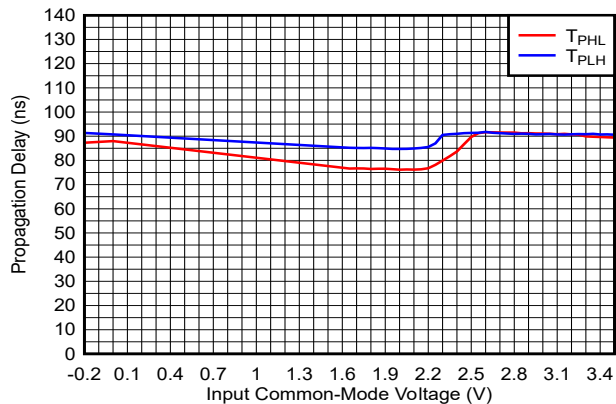


Figure 5-17. Propagation Delay vs. Common-Mode, 3.3V

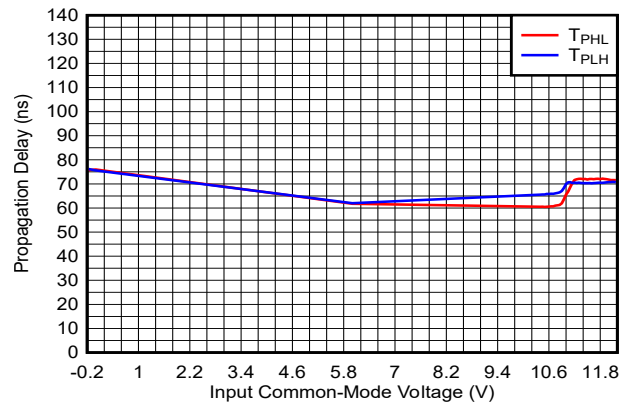


Figure 5-18. Propagation Delay vs. Common-Mode, 12V

### 5.7 Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{CCI} - V_{EEI} = 12\text{V}$ ,  $V_{CCO} - V_{EEO} = 3.3\text{V}$ ,  $V_{CM} = VS/2\text{V}$ ,  $C_L = 15\text{pF}$ , Input Overdrive = Input Underdrive = 100mV unless otherwise noted.

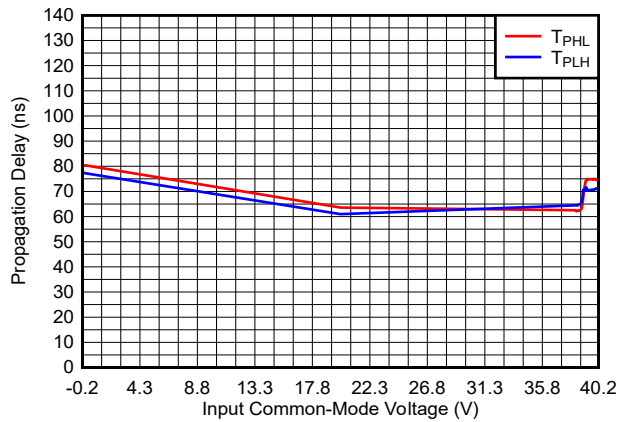


Figure 5-19. Propagation Delay vs. Common-Mode, 40V

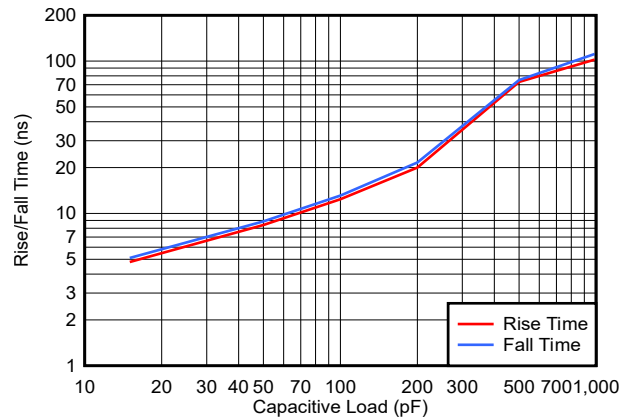


Figure 5-20. Rise/Fall Time vs. Capacitive Load, 12V

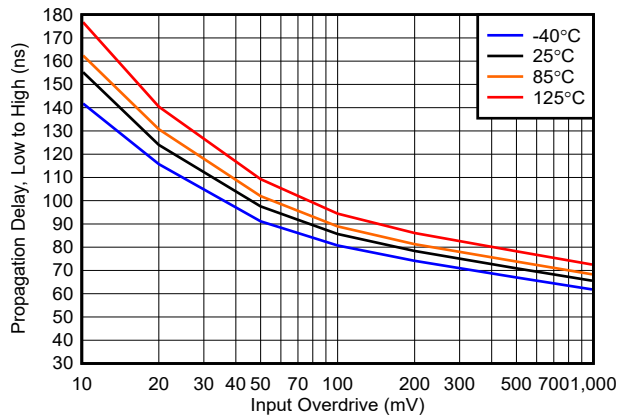


Figure 5-21. Propagation Delay, (Low to High) vs. Input Overdrive, 3.3V

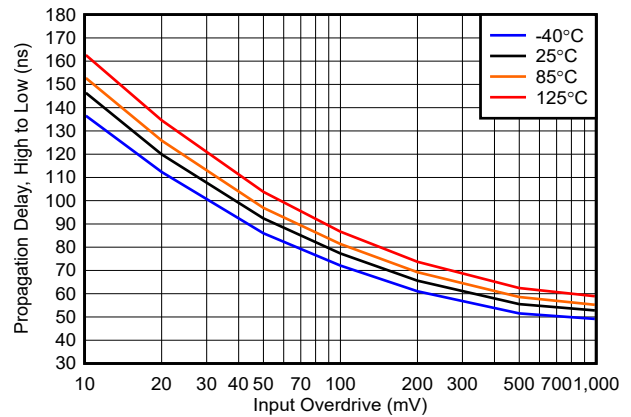


Figure 5-22. Propagation Delay, (High to Low) vs. Input Overdrive, 3.3V

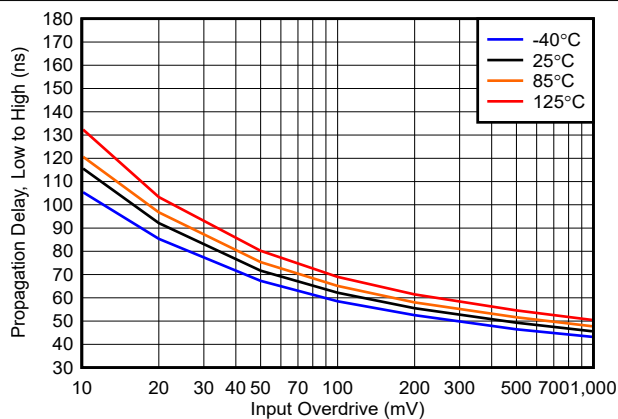


Figure 5-23. Propagation Delay, (Low to High) vs. Input Overdrive, 12V

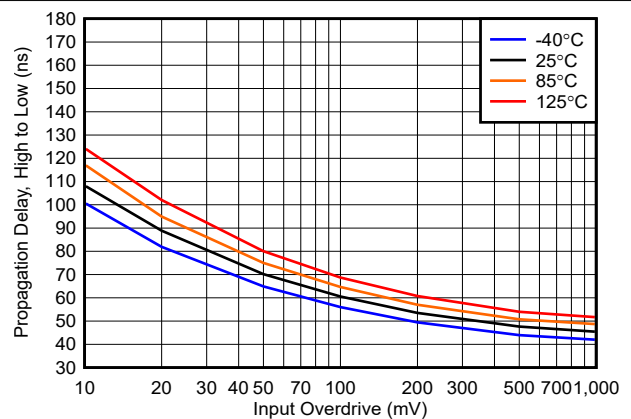
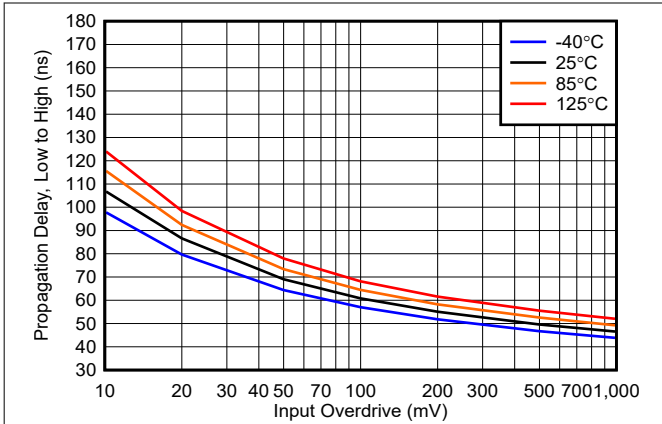


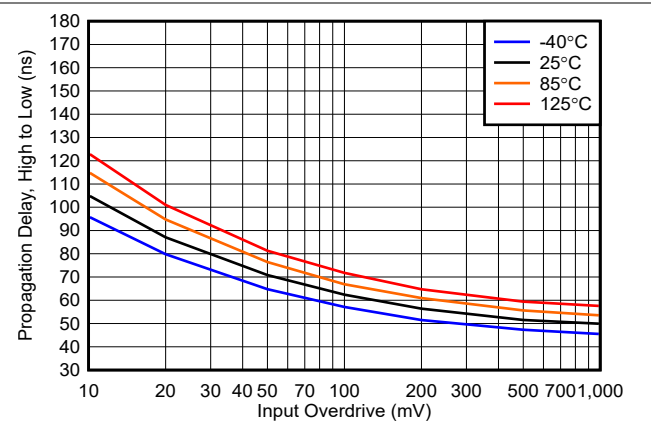
Figure 5-24. Propagation Delay, (High to Low) vs. Input Overdrive, 12V

### 5.7 Typical Characteristics (continued)

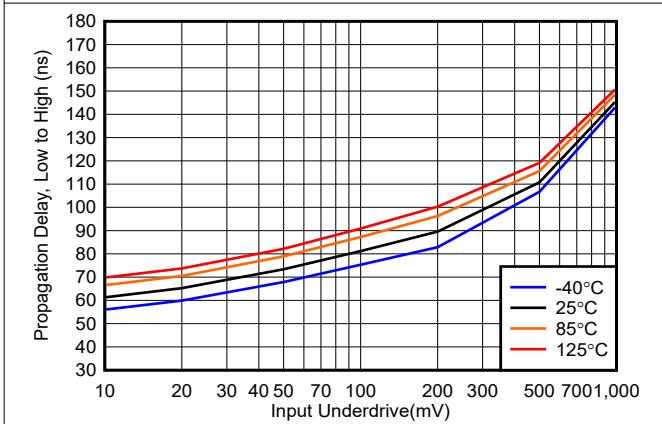
At  $T_A = 25^\circ\text{C}$ ,  $V_{CC1} - V_{EE1} = 12\text{V}$ ,  $V_{CC0} - V_{EE0} = 3.3\text{V}$ ,  $V_{CM} = VS/2\text{V}$ ,  $C_L = 15\text{pF}$ , Input Overdrive = Input Underdrive = 100mV unless otherwise noted.



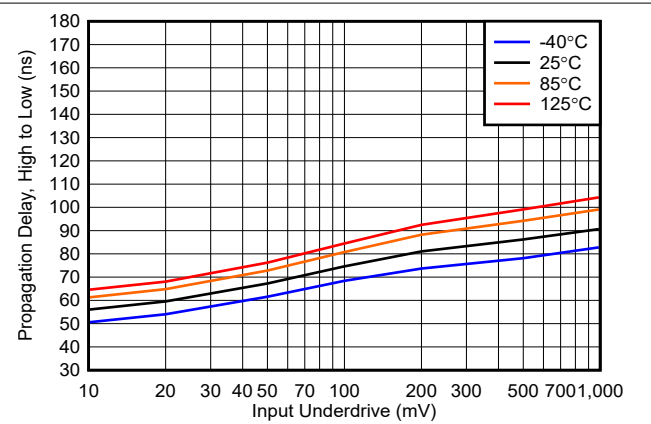
**Figure 5-25. Propagation Delay, (Low to High) vs. Input Overdrive, 40V**



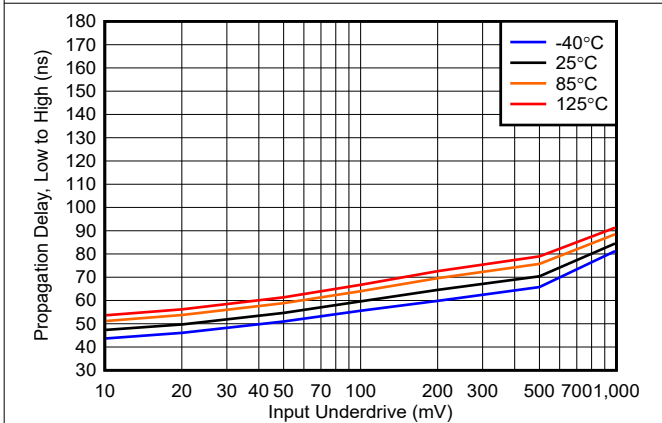
**Figure 5-26. Propagation Delay, (High to Low) vs. Input Overdrive, 40V**



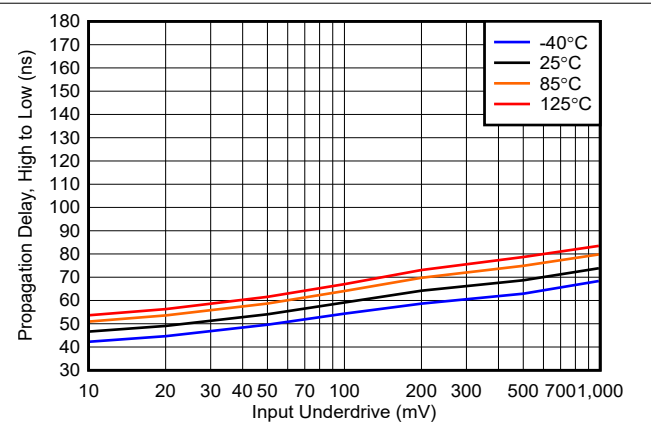
**Figure 5-27. Propagation Delay, (Low to High) vs. Input Underdrive, 3.3V**



**Figure 5-28. Propagation Delay, (High to Low) vs. Input Underdrive, 3.3V**



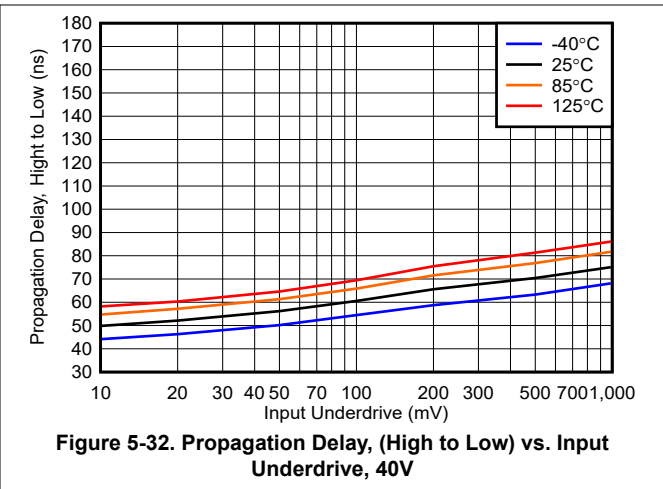
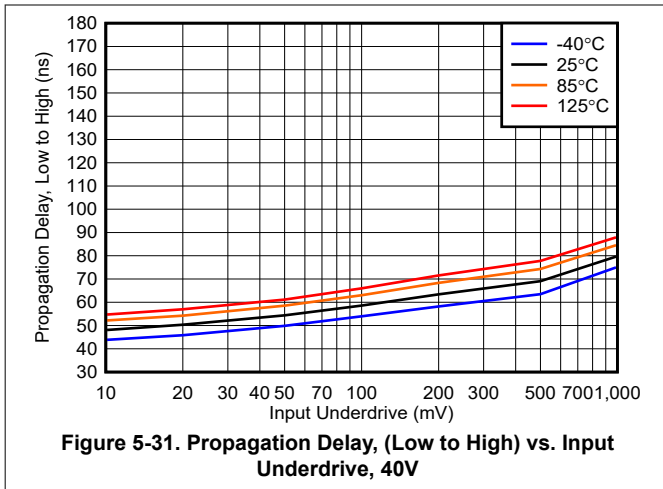
**Figure 5-29. Propagation Delay, (Low to High) vs. Input Underdrive, 12V**



**Figure 5-30. Propagation Delay, (High to Low) vs. Input Underdrive, 12V**

### 5.7 Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{CC1} - V_{EE1} = 12\text{V}$ ,  $V_{CC0} - V_{EE0} = 3.3\text{V}$ ,  $V_{CM} = VS/2\text{V}$ ,  $C_L = 15\text{pF}$ , Input Overdrive = Input Underdrive = 100mV unless otherwise noted.

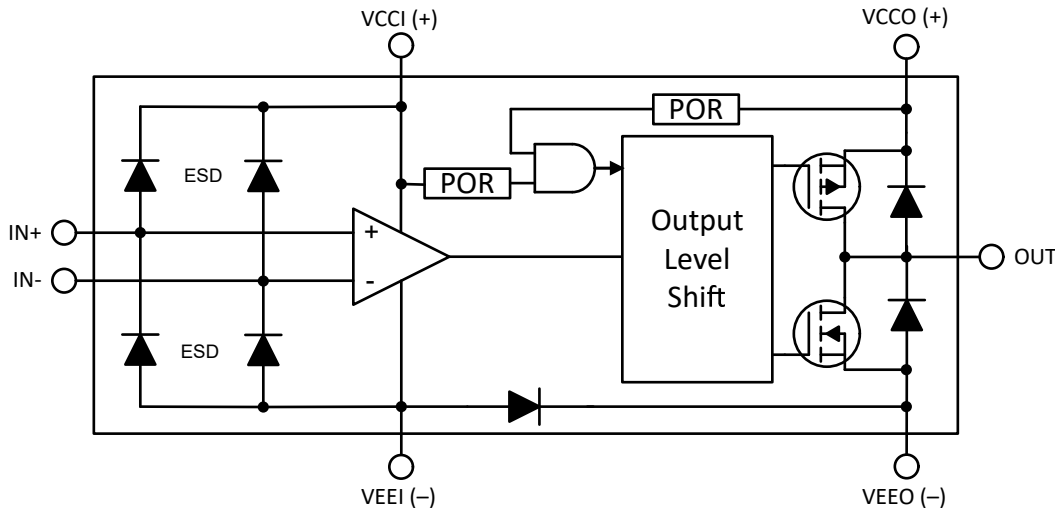


## 6 Detailed Description

### 6.1 Overview

The TLV187x family are 40V high-speed comparators with push-pull output with separate input and output supplies allow for split supply capability on the inputs and level shifted outputs for downstream 5V or 3.3V logic devices. This makes the TLV187x well suited for bipolar zero-cross detection applications or Class-D audio amplifier systems. An internal power-on reset circuit makes sure that the output remains in a known state during power-up and power-down.

### 6.2 Functional Block Diagram



**Figure 6-1. Block Diagram**

### 6.3 Feature Description

The TLV187x (push-pull output) devices are high speed comparators with a typical propagation delay of 65ns and are capable of operating at voltages up to 40V. The separate input and output supplies make these comparators well-suited for applications that need bipolar signals to be level shifted to low voltage logic devices. This also eliminates the need for a pull-up resistor and offers propagation delay and edge-rate symmetry. These comparators also feature a rail-to-rail input stage capable of operating up to 200mV beyond the power supply rails combined with a maximum 2.5mV input offset and Power-On Reset (POR) for known start-up conditions.

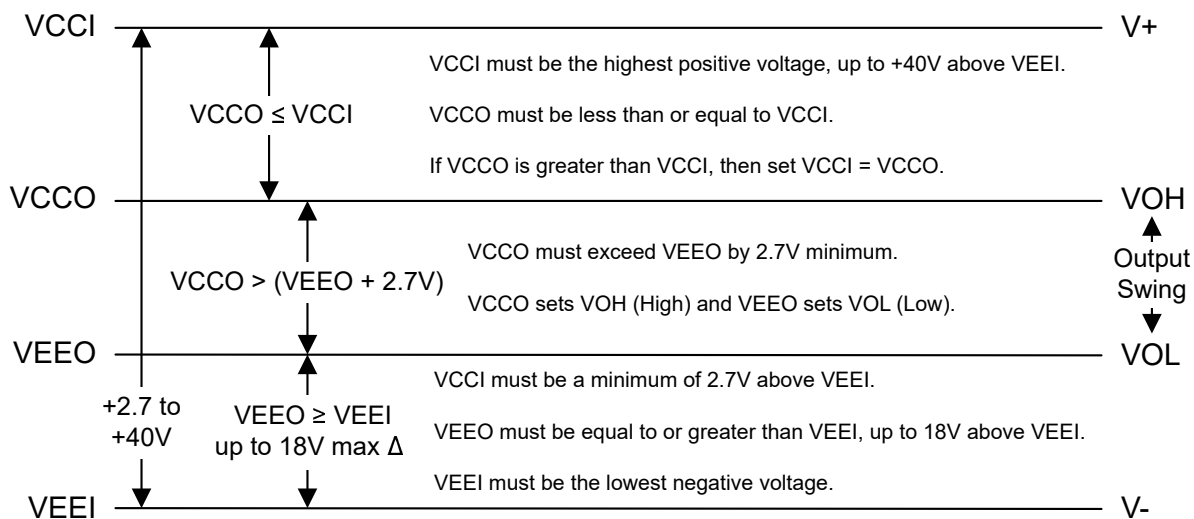
## 6.4 Device Functional Modes

### 6.4.1 Separate Power Supplies

The TLV187x has a unique "floating" output stage where the input and output have separate power supplies to allow defining the output levels without external level shifting. This allows directly sensing bipolar input signals using a split supply, and ground-referenced, low-voltage logic output designed for directly driving processors, ASICs or gate drivers.

The VCCI and VEEL pins supply the power to the input stage and comparator core. The VCCO and VEEO pins provide the power for the output stage and set the output swing.

The VCCO and VEEO pins are bounded by the VEEL and VCCI pins. Please see the [Absolute Maximum Ratings](#) and [Recommended Operating Conditions](#) tables for the specifications. Below is a summary of the limits.



**Figure 6-2. Graphical View of Supply Limits**

VCCI is the positive supply for the input stage and sets the positive input voltage range (Positive VCM). VCCI must be a minimum of 2.7V and up to a maximum of 40V above VEEL to establish the total operating voltage ( $V_s$ ).

VCCO is the positive supply for the output stage, and sets the output high voltage level (VOH). VCCO must be at least 2.7V above VEEO and up to a maximum of VCCI.

VEEO is the negative supply for the output stage, and sets the output low voltage level (VOL). The VEEO pin must be equal to, or greater than the VEEL pin with up to a maximum +18V difference between the VEEL and VEEO pins.

VEEL is the negative supply for the input stage, and sets the negative input voltage range (negative VCM). The VEEL pin is the most negative "substrate" supply of the device. **Therefore the VEEL pin must be at the most negative circuit potential.** There must never be any more than 40V across the entire device with any combination of supply pins.

For example, an application where the input stage is VCCI = +15V, VEEL = -15V, and the output stage is using a single supply with VCCO = +3.3V and VEEO = GND is acceptable.

However, an application where VCCI = +5V, VEEL = GND, and the output stage using a split supply with VCCO = +12V and VEEO = -12V is **NOT** possible as that violates VEEO  $\geq$  VEEL (VEEL is not the lowest negative potential) and VCCI  $<$  VCCO. If VCCI is instead connected to the +12V supply, and the VEEL is connected to the -12V supply, that is acceptable.

Conversely, a negative input voltage application where VCCI = GND, VEEL = -12V, and the output stage using a single supply with VCCO = +3V and VEEO = GND is **NOT** possible as that violates VCCO  $\geq$  VCCI (VEEO



is greater than  $V_{CCI}$ ). In this case, instead tie  $V_{CCI}$  to the +3V output supply and that is acceptable ( $V_{CCI} = V_{CCO}$ ).

Single supply applications are also possible, with both  $V_{EEO}$  and  $V_{EEI}$  at GND, as long as  $V_{CCO}$  is less than or equal to  $V_{CCI}$  ( $V_{CCO} \leq V_{CCI}$ ). So  $V_{CCO} = +3V$  and  $V_{CCI} = +12V$  is acceptable, but  $V_{CCO} = +12V$  and  $V_{CCI} = +3V$  is **NOT** possible (instead, tie  $V_{CCI}$  to the +12V to make acceptable).

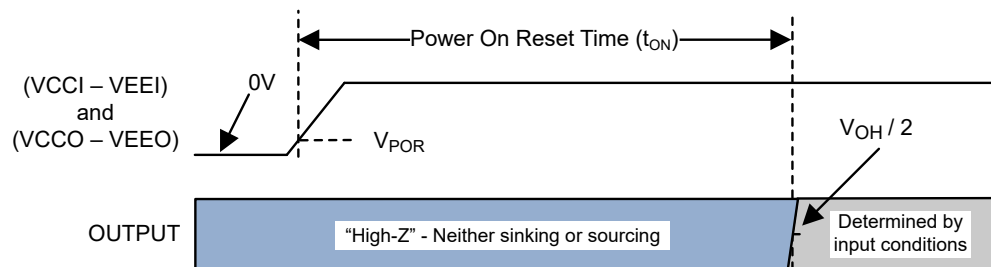
Also possible is to have the output swing between two positive voltage values, such as +2V and +5V, (i.e.,  $V_{EEO} = +2V$ ,  $V_{CCO} = +5V$ ) as long as the above conditions are followed ( $V_{CCI} \geq +5V$  and  $V_{EEO} > V_{EEI}$ ) and there is a minimum of +2.7V between  $V_{EEO}$  and  $V_{CCO}$ .

### 6.4.2 Power-On Reset (POR)

The TLV187x devices have an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supplies are ramping up, the POR circuitry is activated for up to 80 $\mu$ s after the  $V_{POR}$  threshold of 1.7V is crossed.

#### The TLV187x Output is High Impedance ("Hi-Z") During the POR Period ( $t_{ON}$ ).

The input and output POR thresholds are "AND'ed" together. When *BOTH* the input supply ( $V_{CCI}$ - $V_{EEI}$ ) *AND* the output supply ( $V_{CCO}$  -  $V_{EEO}$ ) are greater than the  $V_{POR}$  voltage, then after a delay period ( $t_{ON}$ ), the comparator output reflects the state of the differential input ( $V_{ID}$ ).



**Figure 6-3. Power-On Reset Timing Diagram**

There is no delay on power down. The output enters the POR state immediately when both the supplies fall below  $V_{POR}$ .

### 6.4.3 Inputs

#### 6.4.3.1 Rail-to-Rail Inputs

The input voltage range extends from 200mV below  $V_{EEI}$  to 200mV above  $V_{CCI}$ , maximizing input dynamic range. The input stage has ESD clamps to the  $V_{CCI}$  supply line and therefore the input voltages must not exceed the supply voltages by more than 200mV. Do not apply signals to the rail to rail inputs with no supply voltage. To avoid damaging the inputs when exceeding the recommended input voltage range, an external resistor must be used to limit the current to less than 1mA. Likewise, unlike high-speed amplifiers, the comparator inputs do not have clamping diodes between them. This allows for applications where the input differential voltage can match the supply voltage ( $V_{+}$ ). However, when the input differential voltage increases to 2V, bias current increases to the nA range occur. This is a result of internal circuitry intended to minimize propagation delay increases due to large input underdrive amplitudes.

#### 6.4.3.2 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs can be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even  $V_{CCI}$ .

#### 6.4.4 Push-Pull Output

The TLV187x features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the supply rails can result in thermal runaway and eventual device destruction. If output shorts are possible, a series current limiting resistor in series with the output is recommended to limit the power dissipation.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output.

#### 6.4.5 ESD Protection

The rail-to-rail input has ESD clamps to both VCCI and VEEI, as shown in the [Functional Block Diagram](#), and therefore the input voltage must not exceed the VCCI and VEE0 supply voltages by more than 200mV. Do not apply signals directly to the inputs with no supply voltage without series input current limiting.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, or a signal that can be present while the power is off, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents in case the clamps conduct. The current must be limited to 10mA or less. This series resistance can be part of any resistive input dividers or networks.

The TLV187x push-pull output has ESD clamps to both VCCO and VEE0, as shown in the [Functional Block Diagram](#). The output must not exceed the output supply rails by more than 200mV. Output excursions can be caused by output trace ringing, inductive load kick-back, or externally induced transients.

Due to the high (<10ns) output edge rates, unless matched impedance traces are used, a small series resistor (33 to 100Ω) can be added in series with the output trace to dampen unmatched trace reflections. See the [Layout Example](#) in the [Layout Guidelines](#) section.

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for customer purposes. Customers should validate and test their design implementation to confirm system functionality.

### 7.1 Application Information

#### 7.1.1 Basic Comparator Definitions

##### 7.1.1.1 Operation

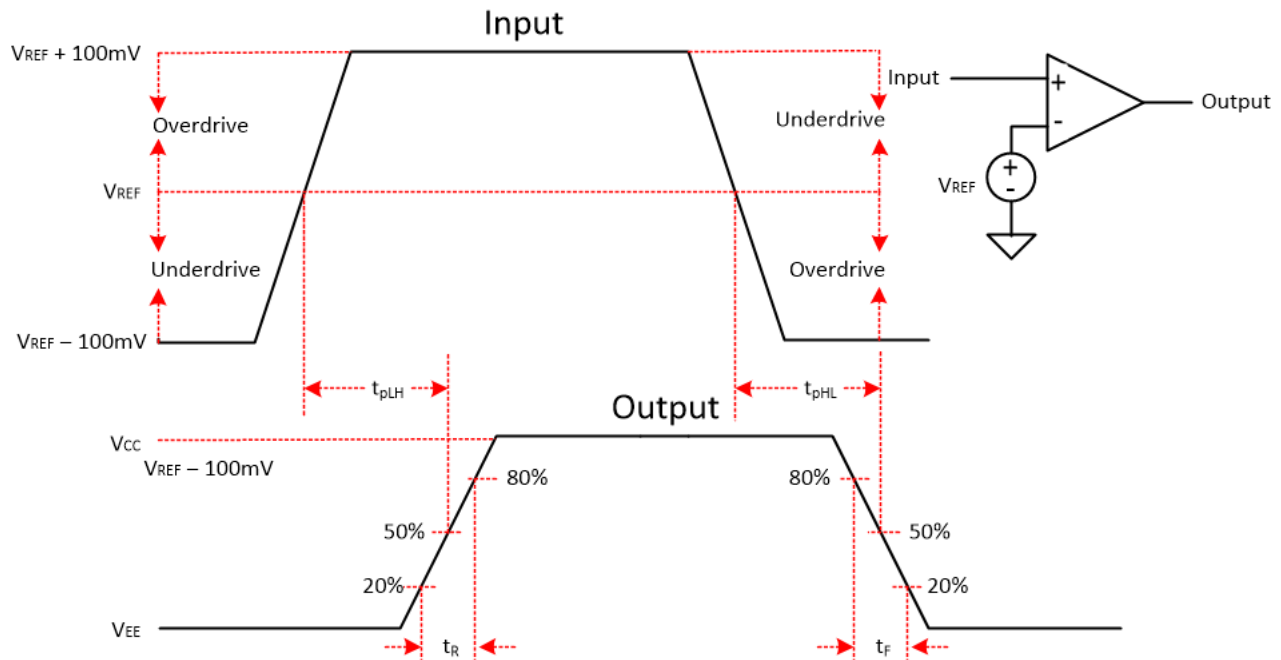
The basic comparator compares the input voltage ( $V_{IN}$ ) on one input to a reference voltage ( $V_{REF}$ ) on the other input. In the [Figure 7-1](#) example below, if  $V_{IN}$  is less than  $V_{REF}$ , the output voltage ( $V_O$ ) is logic low ( $V_{OL}$ ). If  $V_{IN}$  is greater than  $V_{REF}$ , the output voltage ( $V_O$ ) is at logic high ( $V_{OH}$ ). [Table 7-1](#) summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

**Table 7-1. Output Conditions**

Inputs Condition	Output
$IN+ > IN-$	HIGH ( $V_{OH}$ )
$IN+ = IN-$	Indeterminate (chatters - see <a href="#">Hysteresis</a> )
$IN+ < IN-$	LOW ( $V_{OL}$ )

##### 7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as  $t_{pLH}$  and  $t_{pHL}$  in [Figure 7-1](#) and is measured from the mid-point of the input to the midpoint of the output.



**Figure 7-1. Comparator Timing Diagram**

### 7.1.1.3 Overdrive Voltage

The overdrive voltage,  $V_{OD}$ , is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the [Figure 7-1](#) example. The overdrive voltage can influence the propagation delay ( $t_p$ ). The smaller the overdrive voltage, the longer the propagation delay, particularly when  $<100\text{mV}$ . If the fastest speeds are desired, TI recommends applying the highest amount of overdrive possible.

The risetime ( $t_r$ ) and falltime ( $t_f$ ) is the time from the 20% and 80% points of the output waveform.

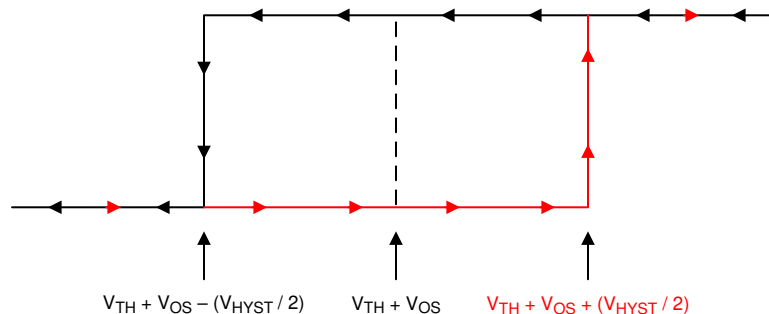
### 7.1.2 Hysteresis

The basic comparator configuration can produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by adding external hysteresis to the comparator.

Since the TLV187x has a minimal amount of internal hysteresis of 2.7mV, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on the current output state.

The hysteresis transfer curve is shown in [Figure 7-2](#). This curve is a function of three components:  $V_{TH}$ ,  $V_{OS}$ , and  $V_{HYST}$ :

- $V_{TH}$  is the actual set voltage or threshold trip voltage.
- $V_{OS}$  is the internal offset voltage between  $V_{IN+}$  and  $V_{IN-}$ . This voltage is added to  $V_{TH}$  to form the actual trip point at which the comparator must respond to change output states.
- $V_{HYST}$  is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.



**Figure 7-2. Hysteresis Transfer Curve**

For more information, please see Application Note SBOA219 "[Comparator with and without hysteresis circuit](#)".

## 7.2 Typical Applications

### 7.2.1 Accurate Bipolar Zero-Cross Detector

Figure 7-3 below shows a bipolar input zero cross detector circuit. The signal source is the secondary of a current or voltage transformer which outputs a bipolar ( $\pm 100$  mVp to  $\pm 12$  Vp) AC signal that swings around 0V (GND). Since the input voltages are not AC coupled, level shifted or further attenuated, DC accurate millivolt zero cross accuracy is possible (even with distorted waveforms). This is due to the direct DC coupled input allowing below-ground bipolar detection range afforded by the split  $\pm 12$ V supplies and rail-to-rail input of the TLV187x. DC coupling also avoids phase shifts caused by AC coupling and non-linearities caused by diode clamping. As the output does not require any further level-shifting or attenuation, the best possible output edge is available for the processor.

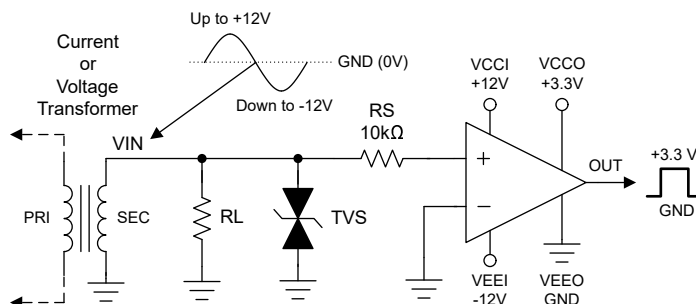


Figure 7-3. Bipolar Zero Cross Circuit using TLV187x

#### 7.2.1.1 Design Requirements

Table 7-2. Design Parameters

PARAMETER	VALUE
Supply Voltage	+3.3V, +12V and -12V
Input Voltage Range	Bipolar $\pm 100$ mVp to $\pm 12$ Vp
Threshold Level	0V (or GND)
Frequency Range	50 - 1000Hz
Logic Output Voltage	0 to 3.3V

#### 7.2.1.2 Detailed Design Procedure

Table 7-2 shows the requirements for the design. The input voltage is bipolar, ranging from  $\pm 100$ mV to  $\pm 12$ V, so split supplies on the comparator input are required.

RL is the required load resistance for the current or voltage transformer. The actual value is recommended by the transformer manufacturer.

RS limits the current into the ESD clamps when the comparator supplies are off and the AC signal can still be present from the transformer. All currents must be limited to 10mA or less (the less the better).

The TVS provides input protection against large transients that can pass through the transformer.

To accommodate the bipolar input range, the input supplies are set to VCCI = +12V, and VEEI = -12V. This allows for a full -12V to +12V input range.

The output supply is set to VCCO = +3.3V, and VEEO = GND for a 0 to 3.3V compatible logic output designed for direct input to a processor.

### 7.2.1.3 Application Performance Plots

Figure 7-4 shows the resulting output of the circuit. The output is high when the AC waveform is above ground, and low when the waveform is below ground.

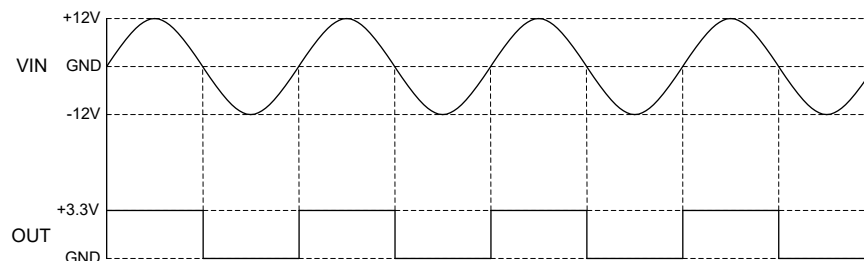


Figure 7-4. Typical Performance Plot for Zero-Cross Circuit

## 7.3 Power Supply Recommendations

Due to the fast output edges, proper bypass capacitors on the supply pin are critical to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic SMT bypass capacitor as directly as possible between the supply pins and ground. Narrow peak currents are drawn during the output transition time due to the push-pull output device. These narrow pulses can cause poorly bypassed supply lines and poor grounds to ring, possibly causing common mode variations that can disturb the input voltage range and create an inaccurate comparison or even oscillations or false-triggers

For more information, please see the [Separate Power Supplies](#) section for more information.

## 7.4 Layout

### 7.4.1 Layout Guidelines

Accurate comparator applications must maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices.

The bypass capacitors must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the VCCx or VEEx and GND pins. Pads need have two or more vias to minimize inductance to the power plane. Shared ground islands need multiple vias to the main ground plane.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a GND trace between output to reduce coupling. When series resistance is added to inputs (RIN), place resistor close to the device.

A low value (<100 ohms) resistor (ROUT) can be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

### 7.4.2 Layout Example

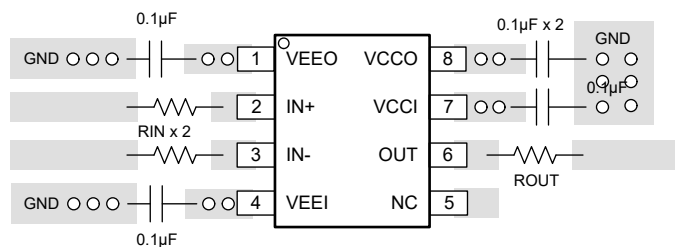


Figure 7-5. Layout Example

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

[TLV1872 Evaluation Module](https://www.ti.com/tool/TLV1872EVM) - <https://www.ti.com/tool/TLV1872EVM>

[Analog Engineers Circuit Cookbook: Amplifiers \(See Comparators section\)](#) - SLYY137

[Precision Design, Comparator with Hysteresis Reference Design](#)— TIDU020

[Window comparator circuit](#) - SBOA221

[Reference Design, Window Comparator Reference Design](#)— TIPD178

[Comparator with and without hysteresis circuit](#) - SBOA219

[Inverting comparator with hysteresis circuit](#) - SNOA997

[Non-Inverting Comparator With Hysteresis Circuit](#) - SBOA313

[A Quad of Independently Func Comparators](#) - SNOA654

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (March 2024) to Revision A (December 2024)</b>	<b>Page</b>
• Remove preview tag and add thermal data for single.....	<a href="#">1</a>

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1871DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3LDH	<a href="#">Samples</a>
TLV1872DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	TL72	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1871DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1872DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1871DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV1872DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0

# DGS0010A



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DDF0008A



# PACKAGE OUTLINE

## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

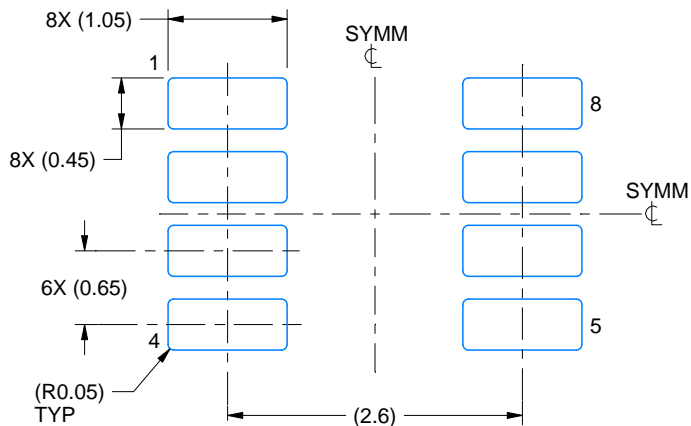


# EXAMPLE BOARD LAYOUT

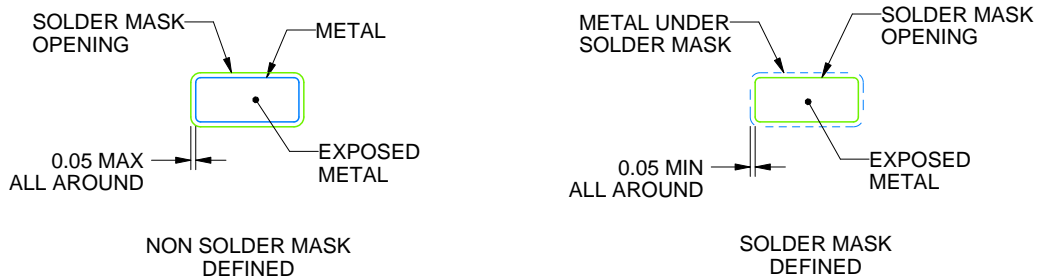
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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