SPRSP45C – MARCH 2020 – REVISED APRIL 2024

TMS320F28002x Real-Time Microcontrollers

1 Features

- TMS320C28x 32-bit DSP core at 100MHz
  - IEEE 754 Floating-Point Unit (FPU)
    - Support for Fast Integer Division (FINTDIV)
  - Trigonometric Math Unit (TMU)
    - Support for Nonlinear Proportional Integral Derivative (NLPID) control
  - CRC Engine and Instructions (VCRC)
  - Ten hardware breakpoints (with ERAD)
- On-chip memory
  - 128KB (64KW) of flash (ECC-protected)
  - 24KB (12KW) of RAM (ECC or parity-protected)
  - Dual-zone security
- Clock and system control
  - Two internal zero-pin 10MHz oscillators
  - Crystal oscillator or external clock input
  - Windowed watchdog timer module
  - Missing clock detection circuitry
  - Dual-clock Comparator (DCC)
- Single 3.3V supply
  - Internal VREG generation
  - Brownout reset (BOR) circuit
- System peripherals
  - 6-channel Direct Memory Access (DMA) controller
  - 43 individually programmable multiplexed General-Purpose Input/Output (GPIO) pins
  - 16 digital inputs on analog pins
  - Enhanced Peripheral Interrupt Expansion (ePIE)
  - Multiple low-power mode (LPM) support
  - Embedded Real-time Analysis and Diagnostic (ERAD)
  - Unique Identification (UID) number
- Communications peripherals
  - One Power-Management Bus (PMBus) interface
  - Two Inter-integrated Circuit (I2C) interfaces
  - One Controller Area Network (CAN) bus port
  - Two Serial Peripheral Interface (SPI) ports
  - One UART-compatible Serial Communication Interface (SCI)
  - Two UART-compatible Local Interconnect Network (LIN) interfaces
  - Fast Serial Interface (FSI) with one transmitter and one receiver (up to 200Mbps)
- Analog system
  - Two 3.45MSPS, 12-bit Analog-to-Digital Converters (ADCs)
    - Up to 16 external channels
    - Four integrated Post-Processing Blocks (PPB) per ADC
  - Four windowed comparators (CMPSS) with 12-bit reference Digital-to-Analog Converters (DACs)
    - Digital glitch filters
- Enhanced control peripherals
  - 14 ePWM channels with eight channels that have high-resolution capability (150ps resolution)
    - Integrated dead-band support
    - Integrated hardware trip zones (TZs)
  - Three Enhanced Capture (eCAP) modules
    - High-resolution Capture (HRCAP) available on one of the three eCAP modules
  - Two Enhanced Quadrature Encoder Pulse (eQEP) modules with support for CW/CCW operation modes
- Configurable Logic Block (CLB)
  - Augments existing peripheral capability
  - Supports position manager solutions
- Host Interface Controller (HIC)
  - Access to internal memory from an external host
- Background CRC (BGCRC)
  - One cycle CRC computation on 32 bits of data
- Diagnostic features
  - Memory Power On Self Test (MPOST)
  - Hardware Built-in Self Test (HWBIST)
- Package options:
  - 80-pin Low-profile Quad Flatpack (LQFP) [PN suffix]
  - 64-pin LQFP [PM suffix]
  - 48-pin LQFP [PT suffix]
- Temperature options:
  - S: –40°C to 125°C junction
  - Q: –40°C to 125°C free-air
    (AEC Q100 qualification for automotive applications)
- Functional Safety Quality-Managed
  - Documentation available to aid ISO 26262, IEC 61508, and IEC 60730 system design

2 Applications

- Appliances
  - Air conditioner outdoor unit
- Building automation
  - Door operator drive control
- Industrial machine & machine tools
  - Automated sorting equipment
  - Textile machine
- EV charging infrastructure
  - AC charging (pile) station
  - DC charging (pile) station
  - EV charging station power module
  - Wireless EV charging station
- Renewable energy storage
  - Energy storage power conversion system (PCS)
- Solar energy
  - Central inverter
  - Micro inverter
  - Solar power optimizer
  - Solar arc protection
  - Rapid shutdown
  - Electricity meter
  - String inverter
- Hybrids, electric & powertrain systems
  - DC/DC converter
  - Inverter & motor control
  - On-board (OBC) & wireless charger
  - Automotive pump
  - Electric power steering (EPS)
- Body electronics & lighting
  - Automotive HVAC compressor module
  - DC/AC inverter
  - Headlight
- AC inverter & VF drives
  - AC drive control module
  - AC drive position feedback
  - AC drive power stage module
- Linear motor transport systems
  - Linear motor power stage
- Single & multi axis servo drives
  - Servo drive position feedback
  - Servo drive power stage module
- Speed controlled BLDC drives
  - AC-input BLDC motor drive
  - DC-input BLDC motor drive
- Industrial power
  - Industrial AC-DC
- UPS
  - Three phase UPS
  - Single phase online UPS
- Telecom & server power
  - Merchant DC/DC
  - Merchant network & server PSU
  - Merchant telecom rectifiers

3 Description

The TMS320F28002x (F28002x) is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to: high power density, high switching frequencies, and supporting the use of GaN and SiC technologies.

These include such applications as:

- Industrial motor drives
- Motor control
- Solar inverters
- Digital power
- Electrical vehicles and transportation
- Sensing and signal processing

The real-time control subsystem is based on TI's 32-bit C28x DSP core, which provides 100MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the Trigonometric Math Unit (TMU) and VCRC (Cyclical Redundancy Check) extended instruction sets, speeding up common algorithms key to real-time control systems.

High-performance analog blocks are integrated on the F28002x real-time microcontroller (MCU) and are closely coupled with the processing and PWM units to provide optimal real-time signal chain performance. Fourteen PWM channels, all supporting frequency-independent resolution modes, enable control of various power stages from a 3-phase inverter to advanced multilevel power topologies.

The inclusion of the Configurable Logic Block (CLB) allows the user to add custom logic and potentially integrate FPGA-like functions into the C2000 real-time MCU.

Interfacing is supported through various industry-standard communication ports (such as SPI, SCI, I2C, PMBus, LIN, and CAN) and offers multiple pin-muxing options for optimal signal placement. The Fast Serial Interface (FSI) enables up to 200Mbps of robust communications across an isolation boundary.

New to the C2000 platform is the Host Interface Controller (HIC), a high-throughput interface that allows an external host to access the resources of the TMS320F28002x directly.

Want to learn more about features that make C2000 MCUs the right choice for your real-time control system? Check out *The Essential Guide for Developing With C2000™ Real-Time Microcontrollers* and visit the C2000™ real-time control MCUs page.

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

Ready to get started? Check out the TMDSCNCD280025C evaluation board and download C2000Ware.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]	BODY SIZE
TMS320F280025	PN (LQFP, 80)	14mm × 14mm	12mm × 12mm
	PM (LQFP, 64)	12mm × 12mm	10mm × 10mm
	PT (LQFP, 48)	9mm × 9mm	7mm × 7mm
TMS320F280025-Q1	PN (LQFP, 80)	14mm × 14mm	12mm × 12mm
	PM (LQFP, 64)	12mm × 12mm	10mm × 10mm
	PT (LQFP, 48)	9mm × 9mm	7mm × 7mm
TMS320F280025C	PN (LQFP, 80)	14mm × 14mm	12mm × 12mm
	PM (LQFP, 64)	12mm × 12mm	10mm × 10mm
	PT (LQFP, 48)	9mm × 9mm	7mm × 7mm
TMS320F280025C-Q1	PN (LQFP, 80)	14mm × 14mm	12mm × 12mm
	PM (LQFP, 64)	12mm × 12mm	10mm × 10mm
	PT (LQFP, 48)	9mm × 9mm	7mm × 7mm
TMS320F280023	PN (LQFP, 80)	14mm × 14mm	12mm × 12mm
	PM (LQFP, 64)	12mm × 12mm	10mm × 10mm
	PT (LQFP, 48)	9mm × 9mm	7mm × 7mm
TMS320F280023-Q1	PN (LQFP, 80)	14mm × 14mm	12mm × 12mm
	PM (LQFP, 64)	12mm × 12mm	10mm × 10mm
	PT (LQFP, 48)	9mm × 9mm	7mm × 7mm
TMS320F280023C	PN (LQFP, 80)	14mm × 14mm	12mm × 12mm
	PM (LQFP, 64)	12mm × 12mm	10mm × 10mm
	PT (LQFP, 48)	9mm × 9mm	7mm × 7mm
TMS320F280021	PT (LQFP, 48)	9mm × 9mm	7mm × 7mm
TMS320F280021-Q1	PT (LQFP, 48)	9mm × 9mm	7mm × 7mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER(1)	CONFIGURABLE LOGIC BLOCK (CLB)	FLASH SIZE
TMS320F280025C	2 Tiles	128KB
TMS320F280025	–	
TMS320F280023C	2 Tiles	64KB
TMS320F280023	–	
TMS320F280021	–	32KB

(1) For more information on these devices, see the Device Comparison table.

3.1 Functional Block Diagram

The Functional Block Diagram shows the CPU system and associated peripherals.

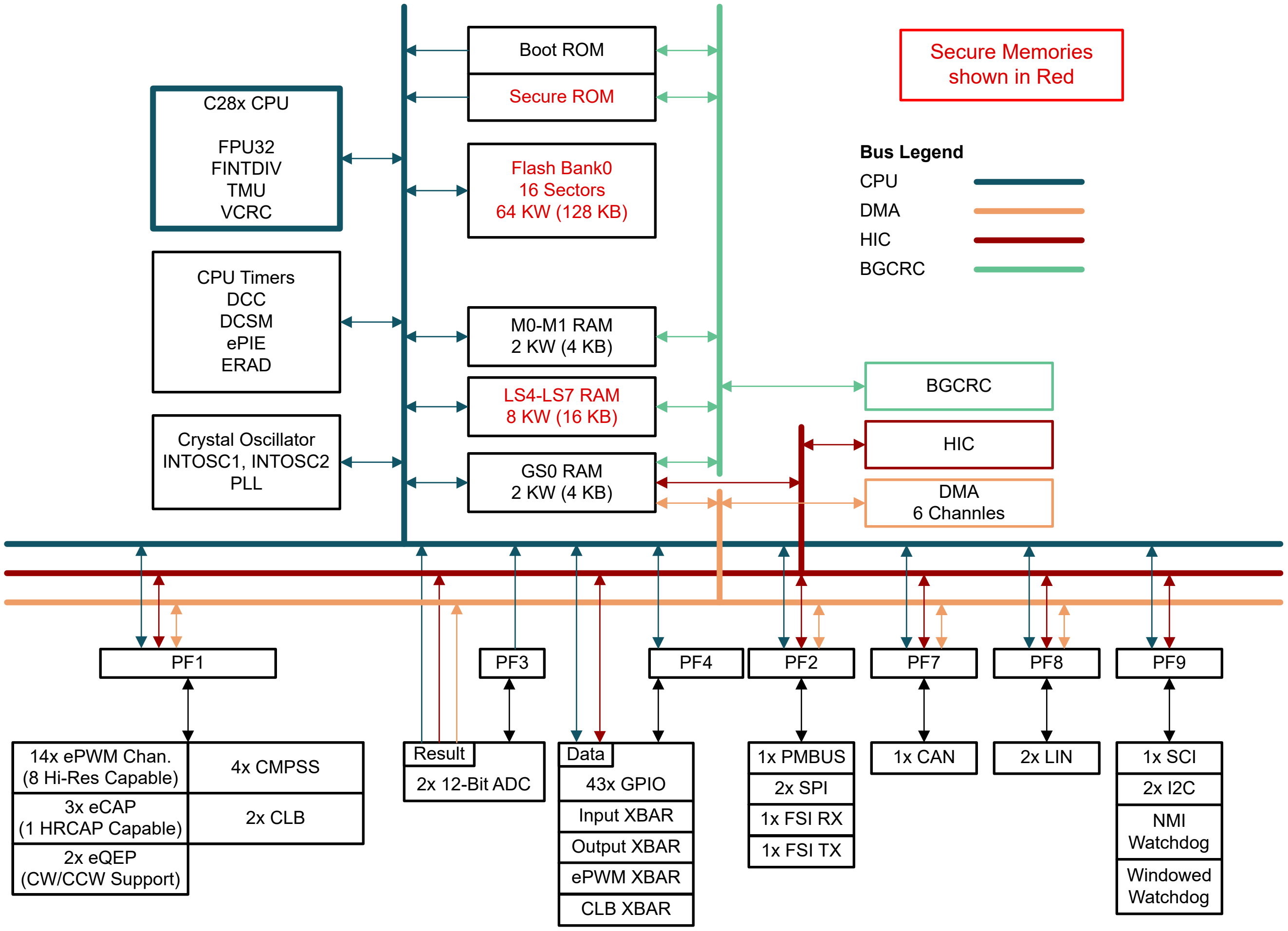


Figure 3-1. Functional Block Diagram

Table of Contents

4 Device Comparison

Table 4-1. Device Comparison

FEATURE [1]		F280025 F280025-Q1 F280025C F280025C-Q1	F280023 F280023-Q1 F280023C	F280021 F280021-Q1
PROCESSOR AND ACCELERATORS				
C28x	Frequency (MHz)	100		
	FPU32	Yes (with new instructions for Fast Integer Division)		
	VCRC	Yes		
	TMU – Type 1	Yes (with new instructions supporting NLPID)		
	Fast Integer Division	Yes		
DMA – Type 0		Yes		
MEMORY				
Flash		128KB (64KW)	64KB (32KW)	32KB (16KW)
RAM	Dedicated and Local Shared RAM	20KB (10KW)		
	Global Shared RAM	4KB (2KW)		
	TOTAL RAM	24KB (12KW)		
Code security for on-chip flash and RAM		Yes		
SYSTEM				
Configurable Logic Block (CLB) [2]		(F280025C-2 tiles)	(F280023C-2 tiles)	-
32-bit CPU timers		3		
Watchdog timer		1		
Nonmaskable Interrupt Watchdog (NMIWD) timers		1		
Crystal oscillator/External clock input		1		
0-pin Internal oscillator		2		
GPIO pins	80-pin PN	43		
	64-pin PM	30		
	48-pin PT	20		
	Additional GPIO	4 (When cJTAG is used, TDI and TDO can be GPIO. When INTOSC is used as clock source, X1 and X2 can be GPIO.) **Note:** These 4 GPIOs are included in the counts above.		
AIO inputs	80-pin PN	16		
	64-pin PM	16		
	48-pin PT	14		
External interrupts		5		
ANALOG PERIPHERALS				
ADC 12-bit	Number of ADCs	2		
	MSPS	3.45		
	Conversion Time (ns) [3]	290		
ADC channels (single-ended)	80-pin PN	16		
	64-pin PM	16		
	48-pin PT	14		
Temperature sensor		1		
CMPSS (each has two comparators and two internal DACs)		4		

Table 4-1. Device Comparison (continued)

FEATURE [1]		F280025 F280025-Q1 F280025C F280025C-Q1	F280023 F280023-Q1 F280023C	F280021 F280021-Q1
CONTROL PERIPHERALS [4]				
eCAP/HRCAP modules – Type 1		3 (1 with HRCAP capability on eCAP3)		
ePWM/HRPWM channels – Type 4		14 (8 with HRPWM capability on ePWM1– PWM4)		
eQEP modules – Type 2		2		
COMMUNICATION PERIPHERALS [4]				
CAN – Type 0		1		
I2C – Type 1		2		
SCI – Type 0 (UART-Compatible)		1		
SPI – Type 2		2		
LIN – Type 1 (UART-Compatible)		2		
PMBus – Type 0		1		
FSI – Type 1		1 (1 RX and 1 TX)		
PACKAGE, TEMPERATURE, AND QUALIFICATION OPTIONS				
S: –40°C to 125°C (T_J)	80-pin PN	F280025 F280025C	F280023 F280023C	–
	64-pin PM			–
	48-pin PT			F280021
Q: –40°C to 125°C (T_A) [5]	80-pin PN	F280025-Q1 F280025C-Q1	F280023-Q1	–
	64-pin PM			–
	48-pin PT			F280021-Q1

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module.
(2) C devices include additional Motor Control libraries in ROM. Contact TI for more information.
(3) Time between start of sample-and-hold window to start of sample-and-hold window of the next conversion.
(4) For devices that are available in more than one package, the peripheral count listed in the smaller package is reduced because the smaller package has less device pins available. The number of peripherals internally present on the device is not reduced co
(5) The letter Q refers to AEC Q100 qualification for automotive applications.

4.1 Related Products

TMS320F2803x Real-Time Microcontrollers
The F2803x series increases the pin-count and memory size options. The F2803x series also introduces the parallel control law accelerator (CLA) option.

TMS320F2807x Real-Time Microcontrollers
The F2807x series offers the most performance, largest pin counts, flash memory sizes, and peripheral options. The F2807x series includes the latest generation of accelerators, ePWM peripherals, and analog technology.

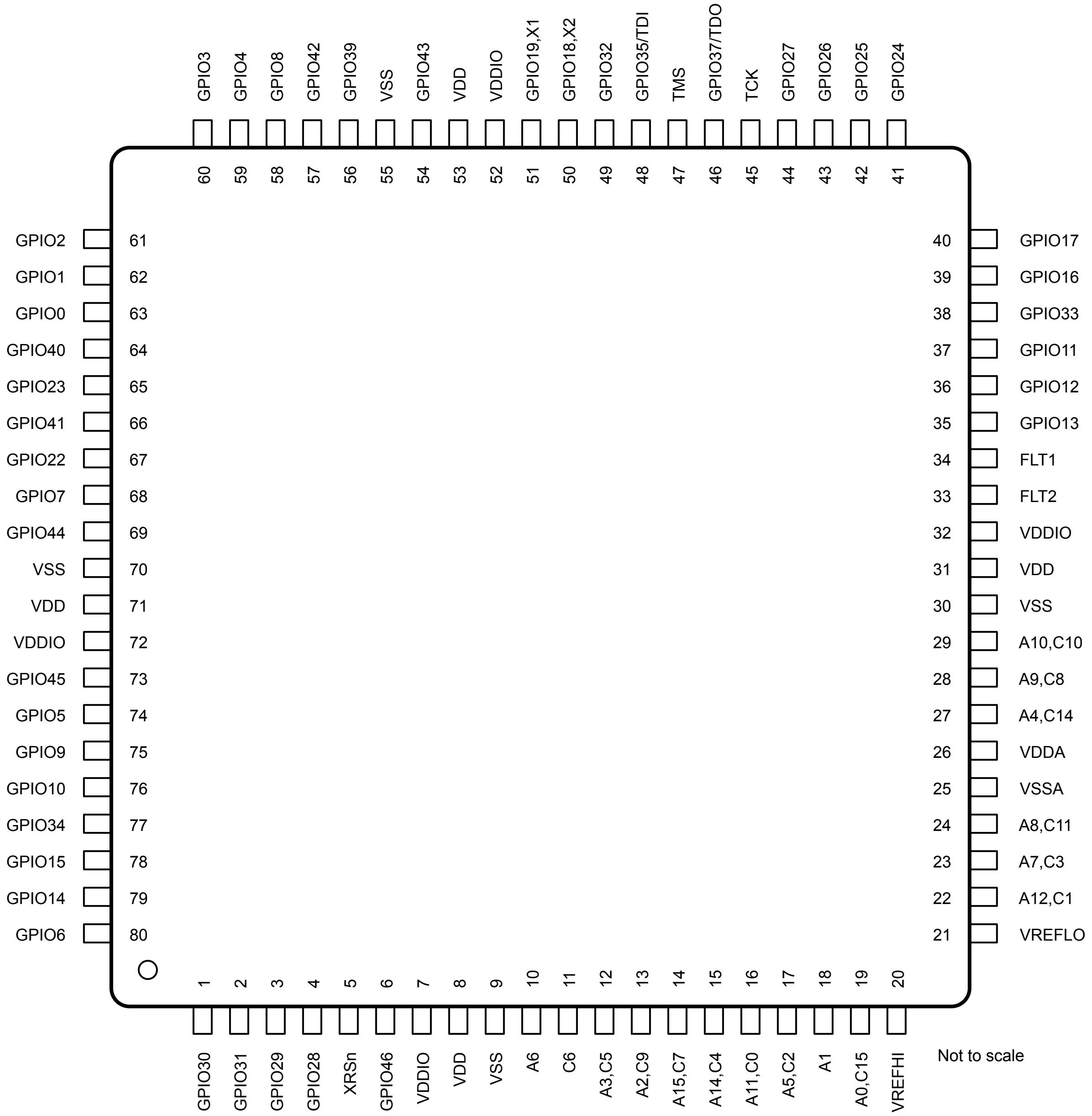
TMS320F28004x Real-Time Microcontrollers
The F28004x series is a reduced version of the F2807x series with the latest generational enhancements.

TMS320F2838x Real-Time Microcontrollers
The F2838x series offers more performance, larger pin counts, flash memory sizes, peripheral and wide variety of connectivity options. The F2838x series includes the latest generation of accelerators, ePWM peripherals, and analog technology. Configurable logic block (CLB) versions are available.

5 Terminal Configuration and Functions

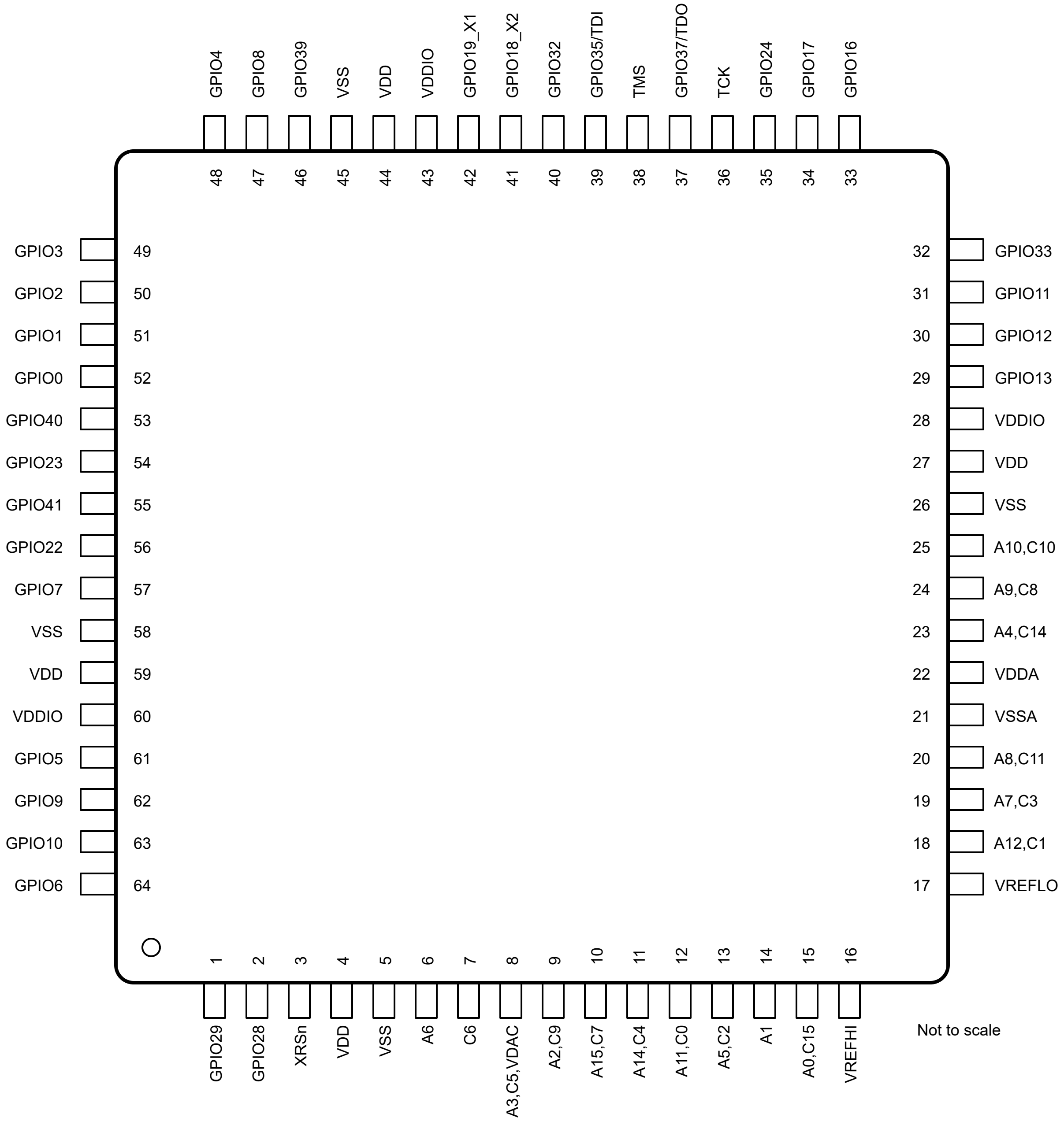
5.1 Pin Diagrams

Figure 5-1 shows the pin assignments on the 80-pin PN low-profile quad flatpack (Q temperature). Figure 5-2 shows the pin assignments on the 64-pin PM low-profile quad flatpack. Figure 5-3 shows the pin assignments on the 48-Pin PT low-profile quad flatpack.



A. Only the GPIO function is shown on GPIO terminals. See Table 5-1 for the complete, muxed signal name.

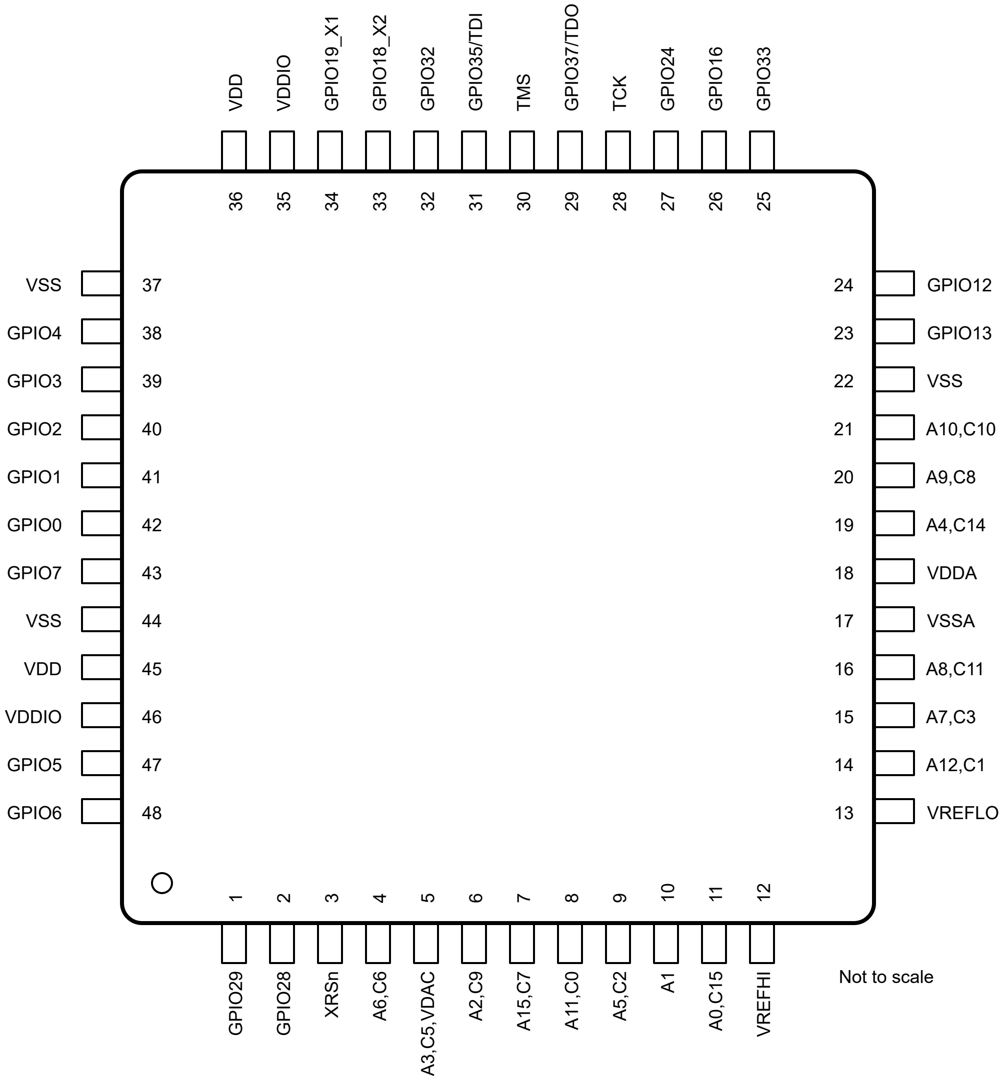
Figure 5-1. 80-Pin PN Low-Profile Quad Flatpack (Top View)



Not to scale

A. Only the GPIO function is shown on GPIO terminals. See Table 5-1 for the complete, muxed signal name.

Figure 5-2. 64-Pin PM Low-Profile Quad Flatpack (Top View)



A. Only the GPIO function is shown on GPIO terminals. See Table 5-1 for the complete, muxed signal name.

Figure 5-3. 48-Pin PT Low-Profile Quad Flatpack (Top View)

5.2 Pin Attributes

Table 5-1. Pin Attributes

SIGNAL NAME	MUX POSITION	80 QFP	64 QFP	48 QFP	PIN TYPE	DESCRIPTION
ANALOG						
A0		19	15	11	I	ADC-A Input 0
C15					I	ADC-C Input 15
CMP3_HP2					I	CMPSS-3 High Comparator Positive Input 2
CMP3_LP2					I	CMPSS-3 Low Comparator Positive Input 2
AIO231	0, 4, 8, 12				I	Analog Pin Used For Digital Input 231
HIC_BASESEL1	15				I	HIC Base Address Range Select 1
A1		18	14	10	I	Analog Input
CMP1_HP4					I	CMPSS-1 High Comparator Positive Input 4
CMP1_LP4					I	CMPSS-1 Low Comparator Positive Input 4
AIO232	0, 4, 8, 12				I	Analog Pin Used For Digital Input 232
HIC_BASESEL0	15				I	HIC Base Address Range Select 0
A10		29	25	21	I	ADC-A Input 10
C10					I	ADC-C Input 10
CMP2_HP3					I	CMPSS-2 High Comparator Positive Input 3
CMP2_HN0					I	CMPSS-2 High Comparator Negative Input 0
CMP2_LP3					I	CMPSS-2 Low Comparator Positive Input 3
CMP2_LN0					I	CMPSS-2 Low Comparator Negative Input 0
AIO230	0, 4, 8, 12				I	Analog Pin Used For Digital Input 230
HIC_BASESEL2	15				I	HIC Base Address Range Select 2
A11		16	12	8	I	ADC-A Input 11
C0					I	ADC-C Input 0
CMP1_HP1					I	CMPSS-1 High Comparator Positive Input 1
CMP1_HN1					I	CMPSS-1 High Comparator Negative Input 1
CMP1_LP1					I	CMPSS-1 Low Comparator Positive Input 1
CMP1_LN1					I	CMPSS-1 Low Comparator Negative Input 1
AIO237	0, 4, 8, 12				I	Analog Pin Used For Digital Input 237
HIC_A6	15				I	HIC Address 6
A12		22	18	14	I	ADC-A Input 12
C1					I	ADC-C Input 1
CMP2_HP1					I	CMPSS-2 High Comparator Positive Input 1
CMP4_HP2					I	CMPSS-4 High Comparator Positive Input 2
CMP2_HN1					I	CMPSS-2 High Comparator Negative Input 1
CMP2_LP1					I	CMPSS-2 Low Comparator Positive Input 1
CMP4_LP2					I	CMPSS-4 Low Comparator Positive Input 2
CMP2_LN1					I	CMPSS-2 Low Comparator Negative Input 1
AIO238	0, 4, 8, 12				I	Analog Pin Used For Digital Input 238
HIC_NCS	15				I	HIC Chip Select
A14		15	11		I	ADC-A Input 14
C4					I	ADC-C Input 4
CMP3_HP4					I	CMPSS-3 High Comparator Positive Input 4
CMP3_LP4					I	CMPSS-3 Low Comparator Positive Input 4
AIO239	0, 4, 8, 12				I	Analog Pin Used For Digital Input 239
HIC_A5	15				I	HIC Address 5

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	80 QFP	64 QFP	48 QFP	PIN TYPE	DESCRIPTION
A15		14	10	7	I	ADC-A Input 15
C7					I	ADC-C Input 7
CMP1_HP3					I	CMPSS-1 High Comparator Positive Input 3
CMP1_HN0					I	CMPSS-1 High Comparator Negative Input 0
CMP1_LP3					I	CMPSS-1 Low Comparator Positive Input 3
CMP1_LN0					I	CMPSS-1 Low Comparator Negative Input 0
AIO233	0, 4, 8, 12				I	Analog Pin Used For Digital Input 233
HIC_A4	15				I	HIC Address 4
A2		13	9	6	I	ADC-A Input 2
C9					I	ADC-C Input 9
CMP1_HP0					I	CMPSS-1 High Comparator Positive Input 0
CMP1_LP0					I	CMPSS-1 Low Comparator Positive Input 0
AIO224	0, 4, 8, 12				I	Analog Pin Used For Digital Input 224
HIC_A3	15				I	HIC Address 3
A3		12	8	5	I	ADC-A Input 3
C5					I	ADC-C Input 5
VDAC					I	Optional external reference voltage for on-chip CMPSS DACs. There is an internal capacitor to VSSA on this pin whether used for ADC input or CMPSS DAC reference which cannot be disabled. If this pin is being used as a reference for the CMPSS DACs, place at least a 1-μF capacitor on this pin.
CMP3_HP3					I	CMPSS-3 High Comparator Positive Input 3
CMP3_HN0					I	CMPSS-3 High Comparator Negative Input 0
CMP3_LP3					I	CMPSS-3 Low Comparator Positive Input 3
CMP3_LN0					I	CMPSS-3 Low Comparator Negative Input 0
AIO242	0, 4, 8, 12				I	Analog Pin Used For Digital Input 242
HIC_A2	15				I	HIC Address 2
A4		27	23	19	I	ADC-A Input 4
C14					I	ADC-C Input 14
CMP2_HP0					I	CMPSS-2 High Comparator Positive Input 0
CMP4_HP3					I	CMPSS-4 High Comparator Positive Input 3
CMP4_HN0					I	CMPSS-4 High Comparator Negative Input 0
CMP2_LP0					I	CMPSS-2 Low Comparator Positive Input 0
CMP4_LP3					I	CMPSS-4 Low Comparator Positive Input 3
CMP4_LN0					I	CMPSS-4 Low Comparator Negative Input 0
AIO225	0, 4, 8, 12				I	Analog Pin Used For Digital Input 225
HIC_NWE	15				I	HIC Data Write Enable
A5		17	13	9	I	ADC-A Input 5
C2					I	ADC-C Input 2
CMP3_HP1					I	CMPSS-3 High Comparator Positive Input 1
CMP3_HN1					I	CMPSS-3 High Comparator Negative Input 1
CMP3_LP1					I	CMPSS-3 Low Comparator Positive Input 1
CMP3_LN1					I	CMPSS-3 Low Comparator Negative Input 1
AIO244	0, 4, 8, 12				I	Analog Pin Used For Digital Input 244
HIC_A7	15				I	HIC Address 7

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	80 QFP	64 QFP	48 QFP	PIN TYPE	DESCRIPTION
A6		10	6	4	I	Analog Input
CMP1_HP2					I	CMPSS-1 High Comparator Positive Input 2
CMP1_LP2					I	CMPSS-1 Low Comparator Positive Input 2
AIO228	0, 4, 8, 12				I	Analog Pin Used For Digital Input 228
HIC_A0	15				I	HIC Address 0
A7		23	19	15	I	ADC-A Input 7
C3					I	ADC-C Input 3
CMP4_HP1					I	CMPSS-4 High Comparator Positive Input 1
CMP4_HN1					I	CMPSS-4 High Comparator Negative Input 1
CMP4_LP1					I	CMPSS-4 Low Comparator Positive Input 1
CMP4_LN1					I	CMPSS-4 Low Comparator Negative Input 1
AIO245	0, 4, 8, 12				I	Analog Pin Used For Digital Input 245
HIC_NOE	15				O	HIC Output Enable
A8		24	20	16	I	ADC-A Input 8
C11					I	ADC-C Input 11
CMP2_HP4					I	CMPSS-2 High Comparator Positive Input 4
CMP4_HP4					I	CMPSS-4 High Comparator Positive Input 4
CMP2_LP4					I	CMPSS-2 Low Comparator Positive Input 4
CMP4_LP4					I	CMPSS-4 Low Comparator Positive Input 4
AIO241	0, 4, 8, 12				I	Analog Pin Used For Digital Input 241
HIC_NBE1	15				I	HIC Byte Enable 1
A9		28	24	20	I	ADC-A Input 9
C8					I	ADC-C Input 8
CMP2_HP2					I	CMPSS-2 High Comparator Positive Input 2
CMP4_HP0					I	CMPSS-4 High Comparator Positive Input 0
CMP2_LP2					I	CMPSS-2 Low Comparator Positive Input 2
CMP4_LP0					I	CMPSS-4 Low Comparator Positive Input 0
AIO227	0, 4, 8, 12				I	Analog Pin Used For Digital Input 227
HIC_NBE0	15				I	HIC Byte Enable 0
C6		11	7	4	I	Analog Input
CMP3_HP0					I	CMPSS-3 High Comparator Positive Input 0
CMP3_LP0					I	CMPSS-3 Low Comparator Positive Input 0
AIO226	0, 4, 8, 12				I	Analog Pin Used For Digital Input 226
HIC_A1	15				I	HIC Address 1
VREFHI		20	16	12	I	ADC- High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2-μF capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHI and VREFLO pins.
VREFLO		21	17	13	I	ADC- Low Reference

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	80 QFP	64 QFP	48 QFP	PIN TYPE	DESCRIPTION
GPIO						
GPIO0	0, 4, 8, 12	63	52	42	I/O	General-Purpose Input Output 0
EPWM1_A	1				O	ePWM-1 Output A
I2CA_SDA	6				I/OD	I2C-A Open-Drain Bidirectional Data
SPIA_STE	7				I/O	SPI-A Slave Transmit Enable (STE)
FSIRXA_CLK	9				I	FSIRX-A Input Clock
CLB_OUTPUTXBAR8	11				O	CLB Output X-BAR Output 8
HIC_BASESEL1	15				I	HIC Base Address Range Select 1
GPIO1	0, 4, 8, 12	62	51	41	I/O	General-Purpose Input Output 1
EPWM1_B	1				O	ePWM-1 Output B
I2CA_SCL	6				I/OD	I2C-A Open-Drain Bidirectional Clock
SPIA_SOMI	7				I/O	SPI-A Slave Out, Master In (SOMI)
CLB_OUTPUTXBAR7	11				O	CLB Output X-BAR Output 7
HIC_A2	13				I	HIC Address 2
FSITXA_TDM_D1	14				I	FSITX-A Time Division Multiplexed Additional Data Input
HIC_D10	15				I/O	HIC Data 10
GPIO2	0, 4, 8, 12	61	50	40	I/O	General-Purpose Input Output 2
EPWM2_A	1				O	ePWM-2 Output A
OUTPUTXBAR1	5				O	Output X-BAR Output 1
PMBUSA_SDA	6				I/OD	PMBus-A Open-Drain Bidirectional Data
SPIA_SIMO	7				I/O	SPI-A Slave In, Master Out (SIMO)
SCIA_TX	9				O	SCI-A Transmit Data
FSIRXA_D1	10				I	FSIRX-A Data Input 1
I2CB_SDA	11				I/OD	I2C-B Open-Drain Bidirectional Data
HIC_A1	13				I	HIC Address 1
CANA_TX	14				O	CAN-A Transmit
HIC_D9	15				I/O	HIC Data 9
GPIO3	0, 4, 8, 12	60	49	39	I/O	General-Purpose Input Output 3
EPWM2_B	1				O	ePWM-2 Output B
OUTPUTXBAR2	2, 5				O	Output X-BAR Output 2
PMBUSA_SCL	6				I/OD	PMBus-A Open-Drain Bidirectional Clock
SPIA_CLK	7				I/O	SPI-A Clock
SCIA_RX	9				I	SCI-A Receive Data
FSIRXA_D0	10				I	FSIRX-A Data Input 0
I2CB_SCL	11				I/OD	I2C-B Open-Drain Bidirectional Clock
HIC_NOE	13				O	HIC Output Enable
CANA_RX	14				I	CAN-A Receive
HIC_D4	15				I/O	HIC Data 4

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	80 QFP	64 QFP	48 QFP	PIN TYPE	DESCRIPTION
GPIO4	0, 4, 8, 12	59	48	38	I/O	General-Purpose Input Output 4
EPWM3_A	1				O	ePWM-3 Output A
OUTPUTXBAR3	5				O	Output X-BAR Output 3
CANA_TX	6				O	CAN-A Transmit
SPIB_CLK	7				I/O	SPI-B Clock
EQEP2_STROBE	9				I/O	eQEP-2 Strobe
FSIRXA_CLK	10				I	FSIRX-A Input Clock
CLB_OUTPUTXBAR6	11				O	CLB Output X-BAR Output 6
HIC_BASESEL2	13				I	HIC Base Address Range Select 2
HIC_NWE	15				I	HIC Data Write Enable
GPIO5	0, 4, 8, 12	74	61	47	I/O	General-Purpose Input Output 5
EPWM3_B	1				O	ePWM-3 Output B
OUTPUTXBAR3	3				O	Output X-BAR Output 3
CANA_RX	6				I	CAN-A Receive
SPIA_STE	7				I/O	SPI-A Slave Transmit Enable (STE)
FSITXA_D1	9				O	FSITX-A Data Output 1
CLB_OUTPUTXBAR5	10				O	CLB Output X-BAR Output 5
HIC_A7	13				I	HIC Address 7
HIC_D4	14				I/O	HIC Data 4
HIC_D15	15				I/O	HIC Data 15
GPIO6	0, 4, 8, 12	80	64	48	I/O	General-Purpose Input Output 6
EPWM4_A	1				O	ePWM-4 Output A
OUTPUTXBAR4	2				O	Output X-BAR Output 4
SYNCOUT	3				O	External ePWM Synchronization Pulse
EQEP1_A	5				I	eQEP-1 Input A
SPIB_SOMI	7				I/O	SPI-B Slave Out, Master In (SOMI)
FSITXA_D0	9				O	FSITX-A Data Output 0
FSITXA_D1	11				O	FSITX-A Data Output 1
HIC_NBE1	13				I	HIC Byte Enable 1
CLB_OUTPUTXBAR8	14				O	CLB Output X-BAR Output 8
HIC_D14	15				I/O	HIC Data 14
GPIO7	0, 4, 8, 12	68	57	43	I/O	General-Purpose Input Output 7
EPWM4_B	1				O	ePWM-4 Output B
OUTPUTXBAR5	3				O	Output X-BAR Output 5
EQEP1_B	5				I	eQEP-1 Input B
SPIB_SIMO	7				I/O	SPI-B Slave In, Master Out (SIMO)
FSITXA_CLK	9				O	FSITX-A Output Clock
CLB_OUTPUTXBAR2	10				O	CLB Output X-BAR Output 2
HIC_A6	13				I	HIC Address 6
HIC_D14	15				I/O	HIC Data 14

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	80 QFP	64 QFP	48 QFP	PIN TYPE	DESCRIPTION
GPIO8	0, 4, 8, 12	58	47		I/O	General-Purpose Input Output 8
EPWM5_A	1				O	ePWM-5 Output A
ADCSOCAO	3				O	ADC Start of Conversion A for External ADC
EQEP1_STROBE	5				I/O	eQEP-1 Strobe
SCIA_TX	6				O	SCI-A Transmit Data
SPIA_SIMO	7				I/O	SPI-A Slave In, Master Out (SIMO)
I2CA_SCL	9				I/OD	I2C-A Open-Drain Bidirectional Clock
FSITXA_D1	10				O	FSITX-A Data Output 1
CLB_OUTPUTXBAR5	11				O	CLB Output X-BAR Output 5
HIC_A0	13				I	HIC Address 0
FSITXA_TDM_CLK	14				I	FSITX-A Time Division Multiplexed Clock Input
HIC_D8	15				I/O	HIC Data 8
GPIO9	0, 4, 8, 12	75	62		I/O	General-Purpose Input Output 9
EPWM5_B	1				O	ePWM-5 Output B
OUTPUTXBAR6	3				O	Output X-BAR Output 6
EQEP1_INDEX	5				I/O	eQEP-1 Index
SCIA_RX	6				I	SCI-A Receive Data
SPIA_CLK	7				I/O	SPI-A Clock
FSITXA_D0	10				O	FSITX-A Data Output 0
LINB_RX	11				I	LIN-B Receive
HIC_BASESEL0	13				I	HIC Base Address Range Select 0
I2CB_SCL	14				I/OD	I2C-B Open-Drain Bidirectional Clock
HIC_NRDY	15				O	HIC Ready
GPIO10	0, 4, 8, 12	76	63		I/O	General-Purpose Input Output 10
EPWM6_A	1				O	ePWM-6 Output A
ADCSOCBO	3				O	ADC Start of Conversion B for External ADC
EQEP1_A	5				I	eQEP-1 Input A
SPIA_SOMI	7				I/O	SPI-A Slave Out, Master In (SOMI)
I2CA_SDA	9				I/OD	I2C-A Open-Drain Bidirectional Data
FSITXA_CLK	10				O	FSITX-A Output Clock
LINB_TX	11				O	LIN-B Transmit
HIC_NWE	13				I	HIC Data Write Enable
FSITXA_TDM_D0	14				I	FSITX-A Time Division Multiplexed Data Input
GPIO11	0, 4, 8, 12	37	31		I/O	General-Purpose Input Output 11
EPWM6_B	1				O	ePWM-6 Output B
OUTPUTXBAR7	3				O	Output X-BAR Output 7
EQEP1_B	5				I	eQEP-1 Input B
SPIA_STE	7				I/O	SPI-A Slave Transmit Enable (STE)
FSIRXA_D1	9				I	FSIRX-A Data Input 1
LINB_RX	10				I	LIN-B Receive
EQEP2_A	11				I	eQEP-2 Input A
SPIA_SIMO	13				I/O	SPI-A Slave In, Master Out (SIMO)
HIC_D6	14				I/O	HIC Data 6
HIC_NBE0	15				I	HIC Byte Enable 0

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	80 QFP	64 QFP	48 QFP	PIN TYPE	DESCRIPTION
GPIO12	0, 4, 8, 12	36	30	24	I/O	General-Purpose Input Output 12
EPWM7_A	1				O	ePWM-7 Output A
EQEP1_STROBE	5				I/O	eQEP-1 Strobe
PMBUSA_CTL	7				I/O	PMBus-A Control Signal - Slave Input/Master Output
FSIRXA_D0	9				I	FSIRX-A Data Input 0
LINB_TX	10				O	LIN-B Transmit
SPIA_CLK	11				I/O	SPI-A Clock
CANA_RX	13				I	CAN-A Receive
HIC_D13	14				I/O	HIC Data 13
HIC_INT	15				O	HIC Device Interrupt
GPIO13	0, 4, 8, 12	35	29	23	I/O	General-Purpose Input Output 13
EPWM7_B	1				O	ePWM-7 Output B
EQEP1_INDEX	5				I/O	eQEP-1 Index
PMBUSA_ALERT	7				I/OD	PMBus-A Open-Drain Bidirectional Alert
FSIRXA_CLK	9				I	FSIRX-A Input Clock
LINB_RX	10				I	LIN-B Receive
SPIA_SOMI	11				I/O	SPI-A Slave Out, Master In (SOMI)
CANA_TX	13				O	CAN-A Transmit
HIC_D11	14				I/O	HIC Data 11
HIC_D5	15				I/O	HIC Data 5
GPIO14	0, 4, 8, 12	79			I/O	General-Purpose Input Output 14
I2CB_SDA	5				I/OD	I2C-B Open-Drain Bidirectional Data
OUTPUTXBAR3	6				O	Output X-BAR Output 3
PMBUSA_SDA	7				I/OD	PMBus-A Open-Drain Bidirectional Data
SPIB_CLK	9				I/O	SPI-B Clock
EQEP2_A	10				I	eQEP-2 Input A
LINB_TX	11				O	LIN-B Transmit
EPWM3_A	13				O	ePWM-3 Output A
CLB_OUTPUTXBAR7	14				O	CLB Output X-BAR Output 7
HIC_D15	15				I/O	HIC Data 15
GPIO15	0, 4, 8, 12	78			I/O	General-Purpose Input Output 15
I2CB_SCL	5				I/OD	I2C-B Open-Drain Bidirectional Clock
OUTPUTXBAR4	6				O	Output X-BAR Output 4
PMBUSA_SCL	7				I/OD	PMBus-A Open-Drain Bidirectional Clock
SPIB_STE	9				I/O	SPI-B Slave Transmit Enable (STE)
EQEP2_B	10				I	eQEP-2 Input B
LINB_RX	11				I	LIN-B Receive
EPWM3_B	13				O	ePWM-3 Output B
CLB_OUTPUTXBAR6	14				O	CLB Output X-BAR Output 6
HIC_D12	15				I/O	HIC Data 12

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	80 QFP	64 QFP	48 QFP	PIN TYPE	DESCRIPTION
GPIO16	0, 4, 8, 12	39	33	26	I/O	General-Purpose Input Output 16
SPIA_SIMO	1				I/O	SPI-A Slave In, Master Out (SIMO)
OUTPUTXBAR7	3				O	Output X-BAR Output 7
EPWM5_A	5				O	ePWM-5 Output A
SCIA_TX	6				O	SCI-A Transmit Data
EQEP1_STROBE	9				I/O	eQEP-1 Strobe
PMBUSA_SCL	10				I/OD	PMBus-A Open-Drain Bidirectional Clock
XCLKOUT	11				O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.
EQEP2_B	13				I	eQEP-2 Input B
SPIB_SOMI	14				I/O	SPI-B Slave Out, Master In (SOMI)
HIC_D1	15				I/O	HIC Data 1
GPIO17	0, 4, 8, 12	40	34		I/O	General-Purpose Input Output 17
SPIA_SOMI	1				I/O	SPI-A Slave Out, Master In (SOMI)
OUTPUTXBAR8	3				O	Output X-BAR Output 8
EPWM5_B	5				O	ePWM-5 Output B
SCIA_RX	6				I	SCI-A Receive Data
EQEP1_INDEX	9				I/O	eQEP-1 Index
PMBUSA_SDA	10				I/OD	PMBus-A Open-Drain Bidirectional Data
CANA_TX	11				O	CAN-A Transmit
HIC_D2	15				I/O	HIC Data 2
GPIO18_X2	0, 4, 8, 12	50	41	33	I/O	General-Purpose Input Output 18_X2
SPIA_CLK	1				I/O	SPI-A Clock
CANA_RX	3				I	CAN-A Receive
EPWM6_A	5				O	ePWM-6 Output A
I2CA_SCL	6				I/OD	I2C-A Open-Drain Bidirectional Clock
EQEP2_A	9				I	eQEP-2 Input A
PMBUSA_CTL	10				I/O	PMBus-A Control Signal - Slave Input/Master Output
XCLKOUT	11				O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.
LINB_TX	13				O	LIN-B Transmit
FSITXA_TDM_CLK	14				I	FSITX-A Time Division Multiplexed Clock Input
HIC_INT	15				O	HIC Device Interrupt
X2	ALT				O	Crystal oscillator output. For more information about the ALT functionality, see the table that is in the External Oscillator (XTAL) section of the System Control chapter in the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	80 QFP	64 QFP	48 QFP	PIN TYPE	DESCRIPTION
GPIO19_X1	0, 4, 8, 12	51	42	34	I/O	General-Purpose Input Output 19_X1
SPIA_STE	1				I/O	SPI-A Slave Transmit Enable (STE)
CANA_TX	3				O	CAN-A Transmit
EPWM6_B	5				O	ePWM-6 Output B
I2CA_SDA	6				I/OD	I2C-A Open-Drain Bidirectional Data
EQEP2_B	9				I	eQEP-2 Input B
PMBUSA_ALERT	10				I/OD	PMBus-A Open-Drain Bidirectional Alert
CLB_OUTPUTXBAR1	11				O	CLB Output X-BAR Output 1
LINB_RX	13				I	LIN-B Receive
FSITXA_TDM_D0	14				I	FSITX-A Time Division Multiplexed Data Input
HIC_NBE0	15				I	HIC Byte Enable 0
X1	ALT				I	Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock. For more information about the ALT functionality, see the table that is in the External Oscillator (XTAL) section of the System Control chapter in the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.
GPIO22	0, 4, 8, 12	67	56		I/O	General-Purpose Input Output 22
EQEP1_STROBE	1				I/O	eQEP-1 Strobe
SPIB_CLK	6				I/O	SPI-B Clock
LINA_TX	9				O	LIN-A Transmit
CLB_OUTPUTXBAR1	10				O	CLB Output X-BAR Output 1
LINB_TX	11				O	LIN-B Transmit
HIC_A5	13				I	HIC Address 5
EPWM4_A	14				O	ePWM-4 Output A
HIC_D13	15				I/O	HIC Data 13
GPIO23	0, 4, 8, 12	65	54		I/O	General-Purpose Input Output 23
EQEP1_INDEX	1				I/O	eQEP-1 Index
SPIB_STE	6				I/O	SPI-B Slave Transmit Enable (STE)
LINA_RX	9				I	LIN-A Receive
LINB_RX	11				I	LIN-B Receive
HIC_A3	13				I	HIC Address 3
EPWM4_B	14				O	ePWM-4 Output B
HIC_D11	15				I/O	HIC Data 11
GPIO24	0, 4, 8, 12	41	35	27	I/O	General-Purpose Input Output 24
OUTPUTXBAR1	1				O	Output X-BAR Output 1
EQEP2_A	2				I	eQEP-2 Input A
SPIB_SIMO	6				I/O	SPI-B Slave In, Master Out (SIMO)
LINB_TX	9				O	LIN-B Transmit
PMBUSA_SCL	10				I/OD	PMBus-A Open-Drain Bidirectional Clock
SCIA_TX	11				O	SCI-A Transmit Data
ERRORSTS	13				O	Error Status Output. When used, this signal requires an external pulldown.
HIC_D3	15				I/O	HIC Data 3

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	80 QFP	64 QFP	48 QFP	PIN TYPE	DESCRIPTION
GPIO25	0, 4, 8, 12	42			I/O	General-Purpose Input Output 25
OUTPUTXBAR2	1				O	Output X-BAR Output 2
EQEP2_B	2				I	eQEP-2 Input B
EQEP1_A	5				I	eQEP-1 Input A
SPIB_SOMI	6				I/O	SPI-B Slave Out, Master In (SOMI)
FSITXA_D1	9				O	FSITX-A Data Output 1
PMBUSA_SDA	10				I/OD	PMBus-A Open-Drain Bidirectional Data
SCIA_RX	11				I	SCI-A Receive Data
HIC_BASESEL0	14				I	HIC Base Address Range Select 0
GPIO26	0, 4, 8, 12	43			I/O	General-Purpose Input Output 26
OUTPUTXBAR3	1, 5				O	Output X-BAR Output 3
EQEP2_INDEX	2				I/O	eQEP-2 Index
SPIB_CLK	6				I/O	SPI-B Clock
FSITXA_D0	9				O	FSITX-A Data Output 0
PMBUSA_CTL	10				I/O	PMBus-A Control Signal - Slave Input/Master Output
I2CA_SDA	11				I/OD	I2C-A Open-Drain Bidirectional Data
HIC_D0	14				I/O	HIC Data 0
HIC_A1	15				I	HIC Address 1
GPIO27	0, 4, 8, 12	44			I/O	General-Purpose Input Output 27
OUTPUTXBAR4	1, 5				O	Output X-BAR Output 4
EQEP2_STROBE	2				I/O	eQEP-2 Strobe
SPIB_STE	6				I/O	SPI-B Slave Transmit Enable (STE)
FSITXA_CLK	9				O	FSITX-A Output Clock
PMBUSA_ALERT	10				I/OD	PMBus-A Open-Drain Bidirectional Alert
I2CA_SCL	11				I/OD	I2C-A Open-Drain Bidirectional Clock
HIC_D1	14				I/O	HIC Data 1
HIC_A4	15				I	HIC Address 4
GPIO28	0, 4, 8, 12	4	2	2	I/O	General-Purpose Input Output 28
SCIA_RX	1				I	SCI-A Receive Data
EPWM7_A	3				O	ePWM-7 Output A
OUTPUTXBAR5	5				O	Output X-BAR Output 5
EQEP1_A	6				I	eQEP-1 Input A
EQEP2_STROBE	9				I/O	eQEP-2 Strobe
LINA_TX	10				O	LIN-A Transmit
SPIB_CLK	11				I/O	SPI-B Clock
ERRORSTS	13				O	Error Status Output. When used, this signal requires an external pulldown.
I2CB_SDA	14				I/OD	I2C-B Open-Drain Bidirectional Data
HIC_NOE	15				O	HIC Output Enable

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	80 QFP	64 QFP	48 QFP	PIN TYPE	DESCRIPTION
GPIO29	0, 4, 8, 12	3	1	1	I/O	General-Purpose Input Output 29
SCIA_TX	1				O	SCI-A Transmit Data
EPWM7_B	3				O	ePWM-7 Output B
OUTPUTXBAR6	5				O	Output X-BAR Output 6
EQEP1_B	6				I	eQEP-1 Input B
EQEP2_INDEX	9				I/O	eQEP-2 Index
LINA_RX	10				I	LIN-A Receive
SPIB_STE	11				I/O	SPI-B Slave Transmit Enable (STE)
ERRORSTS	13				O	Error Status Output. When used, this signal requires an external pulldown.
I2CB_SCL	14				I/OD	I2C-B Open-Drain Bidirectional Clock
HIC_NCS	15				I	HIC Chip Select
GPIO30	0, 4, 8, 12	1			I/O	General-Purpose Input Output 30
CANA_RX	1				I	CAN-A Receive
SPIB_SIMO	3				I/O	SPI-B Slave In, Master Out (SIMO)
OUTPUTXBAR7	5				O	Output X-BAR Output 7
EQEP1_STROBE	6				I/O	eQEP-1 Strobe
FSIRXA_CLK	9				I	FSIRX-A Input Clock
EPWM1_A	11				O	ePWM-1 Output A
HIC_D8	14				I/O	HIC Data 8
GPIO31	0, 4, 8, 12	2			I/O	General-Purpose Input Output 31
CANA_TX	1				O	CAN-A Transmit
SPIB_SOMI	3				I/O	SPI-B Slave Out, Master In (SOMI)
OUTPUTXBAR8	5				O	Output X-BAR Output 8
EQEP1_INDEX	6				I/O	eQEP-1 Index
FSIRXA_D1	9				I	FSIRX-A Data Input 1
EPWM1_B	11				O	ePWM-1 Output B
HIC_D10	14				I/O	HIC Data 10
GPIO32	0, 4, 8, 12	49	40	32	I/O	General-Purpose Input Output 32
I2CA_SDA	1				I/OD	I2C-A Open-Drain Bidirectional Data
SPIB_CLK	3				I/O	SPI-B Clock
LINA_TX	6				O	LIN-A Transmit
FSIRXA_D0	9				I	FSIRX-A Data Input 0
CANA_TX	10				O	CAN-A Transmit
ADCSOCBO	13				O	ADC Start of Conversion B for External ADC
HIC_INT	15				O	HIC Device Interrupt
GPIO33	0, 4, 8, 12	38	32	25	I/O	General-Purpose Input Output 33
I2CA_SCL	1				I/OD	I2C-A Open-Drain Bidirectional Clock
SPIB_STE	3				I/O	SPI-B Slave Transmit Enable (STE)
OUTPUTXBAR4	5				O	Output X-BAR Output 4
LINA_RX	6				I	LIN-A Receive
FSIRXA_CLK	9				I	FSIRX-A Input Clock
CANA_RX	10				I	CAN-A Receive
EQEP2_B	11				I	eQEP-2 Input B
ADCSOCAO	13				O	ADC Start of Conversion A for External ADC
HIC_D0	15				I/O	HIC Data 0

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	80 QFP	64 QFP	48 QFP	PIN TYPE	DESCRIPTION
GPIO34	0, 4, 8, 12	77			I/O	General-Purpose Input Output 34
OUTPUTXBAR1	1				O	Output X-BAR Output 1
PMBUSA_SDA	6				I/OD	PMBus-A Open-Drain Bidirectional Data
HIC_NBE1	13				I	HIC Byte Enable 1
I2CB_SDA	14				I/OD	I2C-B Open-Drain Bidirectional Data
HIC_D9	15				I/O	HIC Data 9
GPIO35	0, 4, 8, 12	48	39	31	I/O	General-Purpose Input Output 35
SCIA_RX	1				I	SCI-A Receive Data
I2CA_SDA	3				I/OD	I2C-A Open-Drain Bidirectional Data
CANA_RX	5				I	CAN-A Receive
PMBUSA_SCL	6				I/OD	PMBus-A Open-Drain Bidirectional Clock
LINA_RX	7				I	LIN-A Receive
EQEP1_A	9				I	eQEP-1 Input A
PMBUSA_CTL	10				I/O	PMBus-A Control Signal - Slave Input/Master Output
HIC_NWE	14				I	HIC Data Write Enable
TDI	15				I	JTAG Test Data Input (TDI) - TDI is the default mux selection for the pin. The internal pullup is disabled by default. The internal pullup should be enabled or an external pullup added on the board if this pin is used as JTAG TDI to avoid a floating input.
GPIO37	0, 4, 8, 12	46	37	29	I/O	General-Purpose Input Output 37
OUTPUTXBAR2	1				O	Output X-BAR Output 2
I2CA_SCL	3				I/OD	I2C-A Open-Drain Bidirectional Clock
SCIA_TX	5				O	SCI-A Transmit Data
CANA_TX	6				O	CAN-A Transmit
LINA_TX	7				O	LIN-A Transmit
EQEP1_B	9				I	eQEP-1 Input B
PMBUSA_ALERT	10				I/OD	PMBus-A Open-Drain Bidirectional Alert
HIC_NRDY	14				O	HIC Ready
TDO	15				O	JTAG Test Data Output (TDO) - TDO is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating; the internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input.
GPIO39	0, 4, 8, 12	56	46		I/O	General-Purpose Input Output 39
FSIRXA_CLK	7				I	FSIRX-A Input Clock
EQEP2_INDEX	9				I/O	eQEP-2 Index
CLB_OUTPUTXBAR2	11				O	CLB Output X-BAR Output 2
SYNCOUT	13				O	External ePWM Synchronization Pulse
EQEP1_INDEX	14				I/O	eQEP-1 Index
HIC_D7	15				I/O	HIC Data 7

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	80 QFP	64 QFP	48 QFP	PIN TYPE	DESCRIPTION
GPIO40	0, 4, 8, 12	64	53		I/O	General-Purpose Input Output 40
SPIB_SIMO	1				I/O	SPI-B Slave In, Master Out (SIMO)
EPWM2_B	5				O	ePWM-2 Output B
PMBUSA_SDA	6				I/OD	PMBus-A Open-Drain Bidirectional Data
FSIRXA_D0	7				I	FSIRX-A Data Input 0
EQEP1_A	10				I	eQEP-1 Input A
LINB_TX	11				O	LIN-B Transmit
HIC_NBE1	14				I	HIC Byte Enable 1
HIC_D5	15				I/O	HIC Data 5
GPIO41	0, 4, 8, 12	66	55		I/O	General-Purpose Input Output 41
EPWM2_A	5				O	ePWM-2 Output A
PMBUSA_SCL	6				I/OD	PMBus-A Open-Drain Bidirectional Clock
FSIRXA_D1	7				I	FSIRX-A Data Input 1
EQEP1_B	10				I	eQEP-1 Input B
LINB_RX	11				I	LIN-B Receive
HIC_A4	13				I	HIC Address 4
SPIB_SOMI	14				I/O	SPI-B Slave Out, Master In (SOMI)
HIC_D12	15				I/O	HIC Data 12
GPIO42	0, 4, 8, 12	57			I/O	General-Purpose Input Output 42
LINA_RX	2				I	LIN-A Receive
OUTPUTXBAR5	3				O	Output X-BAR Output 5
PMBUSA_CTL	5				I/O	PMBus-A Control Signal - Slave Input/Master Output
I2CA_SDA	6				I/OD	I2C-A Open-Drain Bidirectional Data
EQEP1_STROBE	10				I/O	eQEP-1 Strobe
CLB_OUTPUTXBAR3	11				O	CLB Output X-BAR Output 3
HIC_D2	14				I/O	HIC Data 2
HIC_A6	15				I	HIC Address 6
GPIO43	0, 4, 8, 12	54			I/O	General-Purpose Input Output 43
OUTPUTXBAR6	3				O	Output X-BAR Output 6
PMBUSA_ALERT	5				I/OD	PMBus-A Open-Drain Bidirectional Alert
I2CA_SCL	6				I/OD	I2C-A Open-Drain Bidirectional Clock
EQEP1_INDEX	10				I/O	eQEP-1 Index
CLB_OUTPUTXBAR4	11				O	CLB Output X-BAR Output 4
HIC_D3	14				I/O	HIC Data 3
HIC_A7	15				I	HIC Address 7
GPIO44	0, 4, 8, 12	69			I/O	General-Purpose Input Output 44
OUTPUTXBAR7	3				O	Output X-BAR Output 7
EQEP1_A	5				I	eQEP-1 Input A
FSITXA_CLK	7				O	FSITX-A Output Clock
CLB_OUTPUTXBAR3	10				O	CLB Output X-BAR Output 3
HIC_D7	13				I/O	HIC Data 7
HIC_D5	15				I/O	HIC Data 5

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	80 QFP	64 QFP	48 QFP	PIN TYPE	DESCRIPTION
GPIO45	0, 4, 8, 12	73			I/O	General-Purpose Input Output 45
OUTPUTXBAR8	3				O	Output X-BAR Output 8
FSITXA_D0	7				O	FSITX-A Data Output 0
CLB_OUTPUTXBAR4	10				O	CLB Output X-BAR Output 4
HIC_D6	15				I/O	HIC Data 6
GPIO46	0, 4, 8, 12	6			I/O	General-Purpose Input Output 46
LINA_TX	3				O	LIN-A Transmit
FSITXA_D1	7				O	FSITX-A Data Output 1
HIC_NWE	15				I	HIC Data Write Enable
GPIO61	0, 4, 8, 12				I/O	General-Purpose Input Output 61
GPIO62	0, 4, 8, 12				I/O	General-Purpose Input Output 62
GPIO63	0, 4, 8, 12				I/O	General-Purpose Input Output 63
TEST, JTAG, AND RESET						
FLT1		34			I/O	Flash test pin 1. Reserved for TI. Must be left unconnected.
FLT2		33			I/O	Flash test pin 2. Reserved for TI. Must be left unconnected.
TCK		45	36	28	I	JTAG test clock with internal pullup.
TMS		47	38	30	I/O	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation.
XRSn		5	3	3	I/OD	Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device.

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	80 QFP	64 QFP	48 QFP	PIN TYPE	DESCRIPTION
POWER AND GROUND						
VDD		8, 31, 53, 71	4, 27, 44, 59	36, 45		1.2-V Digital Logic Power Pins. See the *Power Management Module (PMM)* section for usage details.
VDDA		26	22	18		3.3-V Analog Power Pins. Place a minimum 2.2-µF decoupling capacitor on each pin. See the *Power Management Module (PMM)* section for usage details.
VDDIO		7, 32, 52, 72	28, 43, 60	35, 46		3.3-V Digital I/O Power Pins. See the *Power Management Module (PMM)* section for usage details.
VSS		9, 30, 55, 70	5, 26, 45, 58	22, 37, 44		Digital Ground
VSSA		25	21	17		Analog Ground

5.3 Signal Descriptions

5.3.1 Analog Signals

Table 5-2. Analog Signals

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	80 QFP	64 QFP	48 QFP
A0	I	ADC-A Input 0		19	15	11
A1	I	Analog Input		18	14	10
A2	I	ADC-A Input 2		13	9	6
A3	I	ADC-A Input 3		12	8	5
A4	I	ADC-A Input 4		27	23	19
A5	I	ADC-A Input 5		17	13	9
A6	I	Analog Input		10	6	4
A7	I	ADC-A Input 7		23	19	15
A8	I	ADC-A Input 8		24	20	16
A9	I	ADC-A Input 9		28	24	20
A10	I	ADC-A Input 10		29	25	21
A11	I	ADC-A Input 11		16	12	8
A12	I	ADC-A Input 12		22	18	14
A14	I	ADC-A Input 14		15	11	
A15	I	ADC-A Input 15		14	10	7
AIO224	I	Analog Pin Used For Digital Input 224		13	9	6
AIO225	I	Analog Pin Used For Digital Input 225		27	23	19
AIO226	I	Analog Pin Used For Digital Input 226		11	7	4
AIO227	I	Analog Pin Used For Digital Input 227		28	24	20
AIO228	I	Analog Pin Used For Digital Input 228		10	6	4
AIO230	I	Analog Pin Used For Digital Input 230		29	25	21
AIO231	I	Analog Pin Used For Digital Input 231		19	15	11
AIO232	I	Analog Pin Used For Digital Input 232		18	14	10
AIO233	I	Analog Pin Used For Digital Input 233		14	10	7
AIO237	I	Analog Pin Used For Digital Input 237		16	12	8
AIO238	I	Analog Pin Used For Digital Input 238		22	18	14
AIO239	I	Analog Pin Used For Digital Input 239		15	11	
AIO241	I	Analog Pin Used For Digital Input 241		24	20	16
AIO242	I	Analog Pin Used For Digital Input 242		12	8	5
AIO244	I	Analog Pin Used For Digital Input 244		17	13	9
AIO245	I	Analog Pin Used For Digital Input 245		23	19	15
C0	I	ADC-C Input 0		16	12	8
C1	I	ADC-C Input 1		22	18	14
C2	I	ADC-C Input 2		17	13	9
C3	I	ADC-C Input 3		23	19	15

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	80 QFP	64 QFP	48 QFP
C4	I	ADC-C Input 4		15	11	
C5	I	ADC-C Input 5		12	8	5
C6	I	Analog Input		11	7	4
C7	I	ADC-C Input 7		14	10	7
C8	I	ADC-C Input 8		28	24	20
C9	I	ADC-C Input 9		13	9	6
C10	I	ADC-C Input 10		29	25	21
C11	I	ADC-C Input 11		24	20	16
C14	I	ADC-C Input 14		27	23	19
C15	I	ADC-C Input 15		19	15	11
CMP1_HN0	I	CMPSS-1 High Comparator Negative Input 0		14	10	7
CMP1_HN1	I	CMPSS-1 High Comparator Negative Input 1		16	12	8
CMP1_HP0	I	CMPSS-1 High Comparator Positive Input 0		13	9	6
CMP1_HP1	I	CMPSS-1 High Comparator Positive Input 1		16	12	8
CMP1_HP2	I	CMPSS-1 High Comparator Positive Input 2		10	6	4
CMP1_HP3	I	CMPSS-1 High Comparator Positive Input 3		14	10	7
CMP1_HP4	I	CMPSS-1 High Comparator Positive Input 4		18	14	10
CMP1_LN0	I	CMPSS-1 Low Comparator Negative Input 0		14	10	7
CMP1_LN1	I	CMPSS-1 Low Comparator Negative Input 1		16	12	8
CMP1_LP0	I	CMPSS-1 Low Comparator Positive Input 0		13	9	6
CMP1_LP1	I	CMPSS-1 Low Comparator Positive Input 1		16	12	8
CMP1_LP2	I	CMPSS-1 Low Comparator Positive Input 2		10	6	4
CMP1_LP3	I	CMPSS-1 Low Comparator Positive Input 3		14	10	7
CMP1_LP4	I	CMPSS-1 Low Comparator Positive Input 4		18	14	10
CMP2_HN0	I	CMPSS-2 High Comparator Negative Input 0		29	25	21
CMP2_HN1	I	CMPSS-2 High Comparator Negative Input 1		22	18	14

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	80 QFP	64 QFP	48 QFP
CMP2_HP0	I	CMPSS-2 High Comparator Positive Input 0		27	23	19
CMP2_HP1	I	CMPSS-2 High Comparator Positive Input 1		22	18	14
CMP2_HP2	I	CMPSS-2 High Comparator Positive Input 2		28	24	20
CMP2_HP3	I	CMPSS-2 High Comparator Positive Input 3		29	25	21
CMP2_HP4	I	CMPSS-2 High Comparator Positive Input 4		24	20	16
CMP2_LN0	I	CMPSS-2 Low Comparator Negative Input 0		29	25	21
CMP2_LN1	I	CMPSS-2 Low Comparator Negative Input 1		22	18	14
CMP2_LP0	I	CMPSS-2 Low Comparator Positive Input 0		27	23	19
CMP2_LP1	I	CMPSS-2 Low Comparator Positive Input 1		22	18	14
CMP2_LP2	I	CMPSS-2 Low Comparator Positive Input 2		28	24	20
CMP2_LP3	I	CMPSS-2 Low Comparator Positive Input 3		29	25	21
CMP2_LP4	I	CMPSS-2 Low Comparator Positive Input 4		24	20	16
CMP3_HN0	I	CMPSS-3 High Comparator Negative Input 0		12	8	5
CMP3_HN1	I	CMPSS-3 High Comparator Negative Input 1		17	13	9
CMP3_HP0	I	CMPSS-3 High Comparator Positive Input 0		11	7	4
CMP3_HP1	I	CMPSS-3 High Comparator Positive Input 1		17	13	9
CMP3_HP2	I	CMPSS-3 High Comparator Positive Input 2		19	15	11
CMP3_HP3	I	CMPSS-3 High Comparator Positive Input 3		12	8	5
CMP3_HP4	I	CMPSS-3 High Comparator Positive Input 4		15	11	
CMP3_LN0	I	CMPSS-3 Low Comparator Negative Input 0		12	8	5
CMP3_LN1	I	CMPSS-3 Low Comparator Negative Input 1		17	13	9

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	80 QFP	64 QFP	48 QFP
CMP3_LP0	I	CMPSS-3 Low Comparator Positive Input 0		11	7	4
CMP3_LP1	I	CMPSS-3 Low Comparator Positive Input 1		17	13	9
CMP3_LP2	I	CMPSS-3 Low Comparator Positive Input 2		19	15	11
CMP3_LP3	I	CMPSS-3 Low Comparator Positive Input 3		12	8	5
CMP3_LP4	I	CMPSS-3 Low Comparator Positive Input 4		15	11	
CMP4_HN0	I	CMPSS-4 High Comparator Negative Input 0		27	23	19
CMP4_HN1	I	CMPSS-4 High Comparator Negative Input 1		23	19	15
CMP4_HP0	I	CMPSS-4 High Comparator Positive Input 0		28	24	20
CMP4_HP1	I	CMPSS-4 High Comparator Positive Input 1		23	19	15
CMP4_HP2	I	CMPSS-4 High Comparator Positive Input 2		22	18	14
CMP4_HP3	I	CMPSS-4 High Comparator Positive Input 3		27	23	19
CMP4_HP4	I	CMPSS-4 High Comparator Positive Input 4		24	20	16
CMP4_LN0	I	CMPSS-4 Low Comparator Negative Input 0		27	23	19
CMP4_LN1	I	CMPSS-4 Low Comparator Negative Input 1		23	19	15
CMP4_LP0	I	CMPSS-4 Low Comparator Positive Input 0		28	24	20
CMP4_LP1	I	CMPSS-4 Low Comparator Positive Input 1		23	19	15
CMP4_LP2	I	CMPSS-4 Low Comparator Positive Input 2		22	18	14
CMP4_LP3	I	CMPSS-4 Low Comparator Positive Input 3		27	23	19
CMP4_LP4	I	CMPSS-4 Low Comparator Positive Input 4		24	20	16
HIC_A0	I	HIC Address 0		10	6	4
HIC_A1	I	HIC Address 1		11	7	4
HIC_A2	I	HIC Address 2		12	8	5
HIC_A3	I	HIC Address 3		13	9	6
HIC_A4	I	HIC Address 4		14	10	7

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	80 QFP	64 QFP	48 QFP
HIC_A5	I	HIC Address 5		15	11	
HIC_A6	I	HIC Address 6		16	12	8
HIC_A7	I	HIC Address 7		17	13	9
HIC_BASESEL0	I	HIC Base Address Range Select 0		18	14	10
HIC_BASESEL1	I	HIC Base Address Range Select 1		19	15	11
HIC_BASESEL2	I	HIC Base Address Range Select 2		29	25	21
HIC_NBE0	I	HIC Byte Enable 0		28	24	20
HIC_NBE1	I	HIC Byte Enable 1		24	20	16
HIC_NCS	I	HIC Chip Select		22	18	14
HIC_NOE	O	HIC Output Enable		23	19	15
HIC_NWE	I	HIC Data Write Enable		27	23	19
VDAC	I	Optional external reference voltage for on-chip CMPSS DACs. There is an internal capacitor to VSSA on this pin whether used for ADC input or CMPSS DAC reference which cannot be disabled. If this pin is being used as a reference for the CMPSS DACs, place at least a 1-µF capacitor on this pin.		12	8	5
VREFHI	I	ADC- High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2-µF capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHI and VREFLO pins.		20	16	12
VREFLO	I	ADC- Low Reference		21	17	13

5.3.2 Digital Signals

Table 5-3. Digital Signals

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	80 QFP	64 QFP	48 QFP
ADCSOCAO	O	ADC Start of Conversion A for External ADC	33, 8	38, 58	32, 47	25
ADCSOCBO	O	ADC Start of Conversion B for External ADC	10, 32	49, 76	40, 63	32
CANA_RX	I	CAN-A Receive	12, 18, 3, 30, 33, 35, 5	1, 36, 38, 48, 50, 60, 74	30, 32, 39, 41, 49, 61	24, 25, 31, 33, 39, 47
CANA_TX	O	CAN-A Transmit	13, 17, 19, 2, 31, 32, 37, 4	2, 35, 40, 46, 49, 51, 59, 61	29, 34, 37, 40, 42, 48, 50	23, 29, 32, 34, 38, 40

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	80 QFP	64 QFP	48 QFP
CLB_OUTPUTXBAR1	O	CLB Output X-BAR Output 1	19, 22	51, 67	42, 56	34
CLB_OUTPUTXBAR2	O	CLB Output X-BAR Output 2	39, 7	56, 68	46, 57	43
CLB_OUTPUTXBAR3	O	CLB Output X-BAR Output 3	42, 44	57, 69		
CLB_OUTPUTXBAR4	O	CLB Output X-BAR Output 4	43, 45	54, 73		
CLB_OUTPUTXBAR5	O	CLB Output X-BAR Output 5	5, 8	58, 74	47, 61	47
CLB_OUTPUTXBAR6	O	CLB Output X-BAR Output 6	15, 4	59, 78	48	38
CLB_OUTPUTXBAR7	O	CLB Output X-BAR Output 7	1, 14	62, 79	51	41
CLB_OUTPUTXBAR8	O	CLB Output X-BAR Output 8	6	63, 80	52, 64	42, 48
EPWM1_A	O	ePWM-1 Output A	30	1, 63	52	42
EPWM1_B	O	ePWM-1 Output B	1, 31	2, 62	51	41
EPWM2_A	O	ePWM-2 Output A	2, 41	61, 66	50, 55	40
EPWM2_B	O	ePWM-2 Output B	3, 40	60, 64	49, 53	39
EPWM3_A	O	ePWM-3 Output A	14, 4	59, 79	48	38
EPWM3_B	O	ePWM-3 Output B	15, 5	74, 78	61	47
EPWM4_A	O	ePWM-4 Output A	22, 6	67, 80	56, 64	48
EPWM4_B	O	ePWM-4 Output B	23, 7	65, 68	54, 57	43
EPWM5_A	O	ePWM-5 Output A	16, 8	39, 58	33, 47	26
EPWM5_B	O	ePWM-5 Output B	17, 9	40, 75	34, 62	
EPWM6_A	O	ePWM-6 Output A	10, 18	50, 76	41, 63	33
EPWM6_B	O	ePWM-6 Output B	11, 19	37, 51	31, 42	34
EPWM7_A	O	ePWM-7 Output A	12, 28	36, 4	2, 30	2, 24
EPWM7_B	O	ePWM-7 Output B	13, 29	3, 35	1, 29	1, 23
EQEP1_A	I	eQEP-1 Input A	10, 25, 28, 35, 40, 44, 6	4, 42, 48, 64, 69, 76, 80	2, 39, 53, 63, 64	2, 31, 48
EQEP1_B	I	eQEP-1 Input B	11, 29, 37, 41, 7	3, 37, 46, 66, 68	1, 31, 37, 55, 57	1, 29, 43
EQEP1_INDEX	I/O	eQEP-1 Index	13, 17, 23, 31, 39, 43, 9	2, 35, 40, 54, 56, 65, 75	29, 34, 46, 54, 62	23
EQEP1_STROBE	I/O	eQEP-1 Strobe	12, 16, 22, 30, 42, 8	1, 36, 39, 57, 58, 67	30, 33, 47, 56	24, 26
EQEP2_A	I	eQEP-2 Input A	11, 14, 18, 24	37, 41, 50, 79	31, 35, 41	27, 33
EQEP2_B	I	eQEP-2 Input B	15, 16, 19, 25, 33	38, 39, 42, 51, 78	32, 33, 42	25, 26, 34
EQEP2_INDEX	I/O	eQEP-2 Index	26, 29, 39	3, 43, 56	1, 46	1
EQEP2_STROBE	I/O	eQEP-2 Strobe	27, 28, 4	4, 44, 59	2, 48	2, 38
ERRORSTS	O	Error Status Output. When used, this signal requires an external pulldown.	24, 28, 29	3, 4, 41	1, 2, 35	1, 2, 27
FSIRXA_CLK	I	FSIRX-A Input Clock	13, 30, 33, 39, 4	1, 35, 38, 56, 59, 63	29, 32, 46, 48, 52	23, 25, 38, 42

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	80 QFP	64 QFP	48 QFP
FSIRXA_D0	I	FSIRX-A Data Input 0	12, 3, 32, 40	36, 49, 60, 64	30, 40, 49, 53	24, 32, 39
FSIRXA_D1	I	FSIRX-A Data Input 1	11, 2, 31, 41	2, 37, 61, 66	31, 50, 55	40
FSITXA_CLK	O	FSITX-A Output Clock	10, 27, 44, 7	44, 68, 69, 76	57, 63	43
FSITXA_D0	O	FSITX-A Data Output 0	26, 45, 6, 9	43, 73, 75, 80	62, 64	48
FSITXA_D1	O	FSITX-A Data Output 1	25, 46, 5, 6, 8	42, 58, 6, 74, 80	47, 61, 64	47, 48
FSITXA_TDM_CLK	I	FSITX-A Time Division Multiplexed Clock Input	18, 8	50, 58	41, 47	33
FSITXA_TDM_D0	I	FSITX-A Time Division Multiplexed Data Input	10, 19	51, 76	42, 63	34
FSITXA_TDM_D1	I	FSITX-A Time Division Multiplexed Additional Data Input	1	62	51	41
GPIO0	I/O	General-Purpose Input Output 0		63	52	42
GPIO1	I/O	General-Purpose Input Output 1	1	62	51	41
GPIO2	I/O	General-Purpose Input Output 2	2	61	50	40
GPIO3	I/O	General-Purpose Input Output 3	3	60	49	39
GPIO4	I/O	General-Purpose Input Output 4	4	59	48	38
GPIO5	I/O	General-Purpose Input Output 5	5	74	61	47
GPIO6	I/O	General-Purpose Input Output 6	6	80	64	48
GPIO7	I/O	General-Purpose Input Output 7	7	68	57	43
GPIO8	I/O	General-Purpose Input Output 8	8	58	47	
GPIO9	I/O	General-Purpose Input Output 9	9	75	62	
GPIO10	I/O	General-Purpose Input Output 10	10	76	63	
GPIO11	I/O	General-Purpose Input Output 11	11	37	31	
GPIO12	I/O	General-Purpose Input Output 12	12	36	30	24
GPIO13	I/O	General-Purpose Input Output 13	13	35	29	23
GPIO14	I/O	General-Purpose Input Output 14	14	79		
GPIO15	I/O	General-Purpose Input Output 15	15	78		
GPIO16	I/O	General-Purpose Input Output 16	16	39	33	26
GPIO17	I/O	General-Purpose Input Output 17	17	40	34	
GPIO18_X2	I/O	General-Purpose Input Output 18_X2	18	50	41	33
GPIO19_X1	I/O	General-Purpose Input Output 19_X1	19	51	42	34
GPIO22	I/O	General-Purpose Input Output 22	22	67	56	
GPIO23	I/O	General-Purpose Input Output 23	23	65	54	
GPIO24	I/O	General-Purpose Input Output 24	24	41	35	27
GPIO25	I/O	General-Purpose Input Output 25	25	42		
GPIO26	I/O	General-Purpose Input Output 26	26	43		
GPIO27	I/O	General-Purpose Input Output 27	27	44		
GPIO28	I/O	General-Purpose Input Output 28	28	4	2	2

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	80 QFP	64 QFP	48 QFP
GPIO29	I/O	General-Purpose Input Output 29	29	3	1	1
GPIO30	I/O	General-Purpose Input Output 30	30	1		
GPIO31	I/O	General-Purpose Input Output 31	31	2		
GPIO32	I/O	General-Purpose Input Output 32	32	49	40	32
GPIO33	I/O	General-Purpose Input Output 33	33	38	32	25
GPIO34	I/O	General-Purpose Input Output 34	34	77		
GPIO35	I/O	General-Purpose Input Output 35	35	48	39	31
GPIO37	I/O	General-Purpose Input Output 37	37	46	37	29
GPIO39	I/O	General-Purpose Input Output 39	39	56	46	
GPIO40	I/O	General-Purpose Input Output 40	40	64	53	
GPIO41	I/O	General-Purpose Input Output 41	41	66	55	
GPIO42	I/O	General-Purpose Input Output 42	42	57		
GPIO43	I/O	General-Purpose Input Output 43	43	54		
GPIO44	I/O	General-Purpose Input Output 44	44	69		
GPIO45	I/O	General-Purpose Input Output 45	45	73		
GPIO46	I/O	General-Purpose Input Output 46	46	6		
GPIO61	I/O	General-Purpose Input Output 61	61			
GPIO62	I/O	General-Purpose Input Output 62	62			
GPIO63	I/O	General-Purpose Input Output 63	63			
HIC_A0	I	HIC Address 0	8	58	47	
HIC_A1	I	HIC Address 1	2, 26	43, 61	50	40
HIC_A2	I	HIC Address 2	1	62	51	41
HIC_A3	I	HIC Address 3	23	65	54	
HIC_A4	I	HIC Address 4	27, 41	44, 66	55	
HIC_A5	I	HIC Address 5	22	67	56	
HIC_A6	I	HIC Address 6	42, 7	57, 68	57	43
HIC_A7	I	HIC Address 7	43, 5	54, 74	61	47
HIC_BASESEL0	I	HIC Base Address Range Select 0	25, 9	42, 75	62	
HIC_BASESEL1	I	HIC Base Address Range Select 1		63	52	42
HIC_BASESEL2	I	HIC Base Address Range Select 2	4	59	48	38
HIC_D0	I/O	HIC Data 0	26, 33	38, 43	32	25
HIC_D1	I/O	HIC Data 1	16, 27	39, 44	33	26
HIC_D2	I/O	HIC Data 2	17, 42	40, 57	34	
HIC_D3	I/O	HIC Data 3	24, 43	41, 54	35	27
HIC_D4	I/O	HIC Data 4	3, 5	60, 74	49, 61	39, 47
HIC_D5	I/O	HIC Data 5	13, 40, 44	35, 64, 69	29, 53	23
HIC_D6	I/O	HIC Data 6	11, 45	37, 73	31	
HIC_D7	I/O	HIC Data 7	39, 44	56, 69	46	

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	80 QFP	64 QFP	48 QFP
HIC_D8	I/O	HIC Data 8	30, 8	1, 58	47	
HIC_D9	I/O	HIC Data 9	2, 34	61, 77	50	40
HIC_D10	I/O	HIC Data 10	1, 31	2, 62	51	41
HIC_D11	I/O	HIC Data 11	13, 23	35, 65	29, 54	23
HIC_D12	I/O	HIC Data 12	15, 41	66, 78	55	
HIC_D13	I/O	HIC Data 13	12, 22	36, 67	30, 56	24
HIC_D14	I/O	HIC Data 14	6, 7	68, 80	57, 64	43, 48
HIC_D15	I/O	HIC Data 15	14, 5	74, 79	61	47
HIC_INT	O	HIC Device Interrupt	12, 18, 32	36, 49, 50	30, 40, 41	24, 32, 33
HIC_NBE0	I	HIC Byte Enable 0	11, 19	37, 51	31, 42	34
HIC_NBE1	I	HIC Byte Enable 1	34, 40, 6	64, 77, 80	53, 64	48
HIC_NCS	I	HIC Chip Select	29	3	1	1
HIC_NOE	O	HIC Output Enable	28, 3	4, 60	2, 49	2, 39
HIC_NRDY	O	HIC Ready	37, 9	46, 75	37, 62	29
HIC_NWE	I	HIC Data Write Enable	10, 35, 4, 46	48, 59, 6, 76	39, 48, 63	31, 38
I2CA_SCL	I/OD	I2C-A Open-Drain Bidirectional Clock	1, 18, 27, 33, 37, 43, 8	38, 44, 46, 50, 54, 58, 62	32, 37, 41, 47, 51	25, 29, 33, 41
I2CA_SDA	I/OD	I2C-A Open-Drain Bidirectional Data	10, 19, 26, 32, 35, 42	43, 48, 49, 51, 57, 63, 76	39, 40, 42, 52, 63	31, 32, 34, 42
I2CB_SCL	I/OD	I2C-B Open-Drain Bidirectional Clock	15, 29, 3, 9	3, 60, 75, 78	1, 49, 62	1, 39
I2CB_SDA	I/OD	I2C-B Open-Drain Bidirectional Data	14, 2, 28, 34	4, 61, 77, 79	2, 50	2, 40
LINA_RX	I	LIN-A Receive	23, 29, 33, 35, 42	3, 38, 48, 57, 65	1, 32, 39, 54	1, 25, 31
LINA_TX	O	LIN-A Transmit	22, 28, 32, 37, 46	4, 46, 49, 6, 67	2, 37, 40, 56	2, 29, 32
LINB_RX	I	LIN-B Receive	11, 13, 15, 19, 23, 41, 9	35, 37, 51, 65, 66, 75, 78	29, 31, 42, 54, 55, 62	23, 34
LINB_TX	O	LIN-B Transmit	10, 12, 14, 18, 22, 24, 40	36, 41, 50, 64, 67, 76, 79	30, 35, 41, 53, 56, 63	24, 27, 33
OUTPUTXBAR1	O	Output X-BAR Output 1	2, 24, 34	41, 61, 77	35, 50	27, 40
OUTPUTXBAR2	O	Output X-BAR Output 2	25, 3, 37	42, 46, 60	37, 49	29, 39
OUTPUTXBAR3	O	Output X-BAR Output 3	14, 26, 4, 5	43, 59, 74, 79	48, 61	38, 47
OUTPUTXBAR4	O	Output X-BAR Output 4	15, 27, 33, 6	38, 44, 78, 80	32, 64	25, 48
OUTPUTXBAR5	O	Output X-BAR Output 5	28, 42, 7	4, 57, 68	2, 57	2, 43
OUTPUTXBAR6	O	Output X-BAR Output 6	29, 43, 9	3, 54, 75	1, 62	1
OUTPUTXBAR7	O	Output X-BAR Output 7	11, 16, 30, 44	1, 37, 39, 69	31, 33	26
OUTPUTXBAR8	O	Output X-BAR Output 8	17, 31, 45	2, 40, 73	34	
PMBUSA_ALERT	I/OD	PMBus-A Open-Drain Bidirectional Alert	13, 19, 27, 37, 43	35, 44, 46, 51, 54	29, 37, 42	23, 29, 34

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	80 QFP	64 QFP	48 QFP
PMBUSA_CTL	I/O	PMBus-A Control Signal - Slave Input/Master Output	12, 18, 26, 35, 42	36, 43, 48, 50, 57	30, 39, 41	24, 31, 33
PMBUSA_SCL	I/OD	PMBus-A Open-Drain Bidirectional Clock	15, 16, 24, 3, 35, 41	39, 41, 48, 60, 66, 78	33, 35, 39, 49, 55	26, 27, 31, 39
PMBUSA_SDA	I/OD	PMBus-A Open-Drain Bidirectional Data	14, 17, 2, 25, 34, 40	40, 42, 61, 64, 77, 79	34, 50, 53	40
SCIA_RX	I	SCI-A Receive Data	17, 25, 28, 3, 35, 9	4, 40, 42, 48, 60, 75	2, 34, 39, 49, 62	2, 31, 39
SCIA_TX	O	SCI-A Transmit Data	16, 2, 24, 29, 37, 8	3, 39, 41, 46, 58, 61	1, 33, 35, 37, 47, 50	1, 26, 27, 29, 40
SPIA_CLK	I/O	SPI-A Clock	12, 18, 3, 9	36, 50, 60, 75	30, 41, 49, 62	24, 33, 39
SPIA_SIMO	I/O	SPI-A Slave In, Master Out (SIMO)	11, 16, 2, 8	37, 39, 58, 61	31, 33, 47, 50	26, 40
SPIA_SOMI	I/O	SPI-A Slave Out, Master In (SOMI)	1, 10, 13, 17	35, 40, 62, 76	29, 34, 51, 63	23, 41
SPIA_STE	I/O	SPI-A Slave Transmit Enable (STE)	11, 19, 5	37, 51, 63, 74	31, 42, 52, 61	34, 42, 47
SPIB_CLK	I/O	SPI-B Clock	14, 22, 26, 28, 32, 4	4, 43, 49, 59, 67, 79	2, 40, 48, 56	2, 32, 38
SPIB_SIMO	I/O	SPI-B Slave In, Master Out (SIMO)	24, 30, 40, 7	1, 41, 64, 68	35, 53, 57	27, 43
SPIB_SOMI	I/O	SPI-B Slave Out, Master In (SOMI)	16, 25, 31, 41, 6	2, 39, 42, 66, 80	33, 55, 64	26, 48
SPIB_STE	I/O	SPI-B Slave Transmit Enable (STE)	15, 23, 27, 29, 33	3, 38, 44, 65, 78	1, 32, 54	1, 25
SYNCOUT	O	External ePWM Synchronization Pulse	39, 6	56, 80	46, 64	48
TDI	I	JTAG Test Data Input (TDI) - TDI is the default mux selection for the pin. The internal pullup is disabled by default. The internal pullup should be enabled or an external pullup added on the board if this pin is used as JTAG TDI to avoid a floating input.	35	48	39	31
TDO	O	JTAG Test Data Output (TDO) - TDO is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating; the internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input.	37	46	37	29

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	80 QFP	64 QFP	48 QFP
X1	I	Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock. For more information about the ALT functionality, see the table that is in the External Oscillator (XTAL) section of the System Control chapter in the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.	19	51	42	34
X2	O	Crystal oscillator output. For more information about the ALT functionality, see the table that is in the External Oscillator (XTAL) section of the System Control chapter in the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.	18	50	41	33
XCLKOUT	O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.	16, 18	39, 50	33, 41	26, 33

5.3.3 Power and Ground

Table 5-4. Power and Ground

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	80 QFP	64 QFP	48 QFP
VDD		1.2-V Digital Logic Power Pins. See the Power Management Module (PMM) section for usage details.		31, 53, 71, 8	27, 4, 44, 59	36, 45
VDDA		3.3-V Analog Power Pins. Place a minimum 2.2-µF decoupling capacitor on each pin. See the Power Management Module (PMM) section for usage details.		26	22	18
VDDIO		3.3-V Digital I/O Power Pins. See the Power Management Module (PMM) section for usage details.		32, 52, 7, 72	28, 43, 60	35, 46
VSS		Digital Ground		30, 55, 70, 9	26, 45, 5, 58	22, 37, 44
VSSA		Analog Ground		25	21	17

5.3.4 Test, JTAG, and Reset

Table 5-5. Test, JTAG, and Reset

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	80 QFP	64 QFP	48 QFP
FLT1	I/O	Flash test pin 1. Reserved for TI. Must be left unconnected.		34		
FLT2	I/O	Flash test pin 2. Reserved for TI. Must be left unconnected.		33		
TCK	I	JTAG test clock with internal pullup.		45	36	28
TMS	I/O	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation.		47	38	30
XRSn	I/OD	Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device.		5	3	3

5.4 Pin Multiplexing

5.4.1 GPIO Muxed Pins

Table 5-6 lists the GPIO muxed pins. The default mode for each GPIO pin is the GPIO function, except GPIO35 and GPIO37, which default to TDI and TDO, respectively. Secondary functions can be selected by setting both the GPyGMUXn.GPIOz and GPyMUXn.GPIOz register bits. The GPyGMUXn register should be configured before the GPyMUXn to avoid transient pulses on GPIOs from alternate mux selections. Columns that are not shown and blank cells are reserved GPIO Mux settings. GPIO ALT functions cannot be configured with the GPyMUXn and GPyGMUXn registers. These are special functions that need to be configured from the module.

Note

GPIO20, GPIO21, GPIO36 and GPIO38 do not exist on this device. GPIO61 to GPIO63 exist but are not pinned out on any packages. Boot ROM enables pullups on GPIO61 to GPIO63. For more details, see Section 5.5.

5.4.1.1 GPIO Muxed Pins Table

Table 5-6. GPIO Muxed Pins

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO0	EPWM1_A				I2CA_SDA	SPIA_STE	FSIRXA_CLK		CLB_OUTPUTXBAR8			HIC_BASESEL1	
GPIO1	EPWM1_B				I2CA_SCL	SPIA_SOMI			CLB_OUTPUTXBAR7	HIC_A2	FSITXA_TDM_D1	HIC_D10	
GPIO2	EPWM2_A			OUTPUTXBAR1	PMBUSA_SDA	SPIA_SIMO	SCIA_TX	FSIRXA_D1	I2CB_SDA	HIC_A1	CANA_TX	HIC_D9	
GPIO3	EPWM2_B	OUTPUTXBAR2		OUTPUTXBAR2	PMBUSA_SCL	SPIA_CLK	SCIA_RX	FSIRXA_D0	I2CB_SCL	HIC_NOE	CANA_RX	HIC_D4	
GPIO4	EPWM3_A			OUTPUTXBAR3	CANA_TX	SPIB_CLK	EQEP2_STROBE	FSIRXA_CLK	CLB_OUTPUTXBAR6	HIC_BASESEL2		HIC_NWE	
GPIO5	EPWM3_B		OUTPUTXBAR3		CANA_RX	SPIA_STE	FSITXA_D1	CLB_OUTPUTXBAR5		HIC_A7	HIC_D4	HIC_D15	
GPIO6	EPWM4_A	OUTPUTXBAR4	SYNCOUT	EQEP1_A		SPIB_SOMI	FSITXA_D0		FSITXA_D1	HIC_NBE1	CLB_OUTPUTXBAR8	HIC_D14	
GPIO7	EPWM4_B		OUTPUTXBAR5	EQEP1_B		SPIB_SIMO	FSITXA_CLK	CLB_OUTPUTXBAR2		HIC_A6		HIC_D14	
GPIO8	EPWM5_A		ADCSOCAO	EQEP1_STROBE	SCIA_TX	SPIA_SIMO	I2CA_SCL	FSITXA_D1	CLB_OUTPUTXBAR5	HIC_A0	FSITXA_TDM_CLK	HIC_D8	
GPIO9	EPWM5_B		OUTPUTXBAR6	EQEP1_INDEX	SCIA_RX	SPIA_CLK		FSITXA_D0	LINB_RX	HIC_BASESEL0	I2CB_SCL	HIC_NRDY	
GPIO10	EPWM6_A		ADCSOCBO	EQEP1_A		SPIA_SOMI	I2CA_SDA	FSITXA_CLK	LINB_TX	HIC_NWE	FSITXA_TDM_D0		
GPIO11	EPWM6_B		OUTPUTXBAR7	EQEP1_B		SPIA_STE	FSIRXA_D1	LINB_RX	EQEP2_A	SPIA_SIMO	HIC_D6	HIC_NBE0	
GPIO12	EPWM7_A			EQEP1_STROBE		PMBUSA_CTL	FSIRXA_D0	LINB_TX	SPIA_CLK	CANA_RX	HIC_D13	HIC_INT	
GPIO13	EPWM7_B			EQEP1_INDEX		PMBUSA_ALERT	FSIRXA_CLK	LINB_RX	SPIA_SOMI	CANA_TX	HIC_D11	HIC_D5	
GPIO14				I2CB_SDA	OUTPUTXBAR3	PMBUSA_SDA	SPIB_CLK	EQEP2_A	LINB_TX	EPWM3_A	CLB_OUTPUTXBAR7	HIC_D15	
GPIO15				I2CB_SCL	OUTPUTXBAR4	PMBUSA_SCL	SPIB_STE	EQEP2_B	LINB_RX	EPWM3_B	CLB_OUTPUTXBAR6	HIC_D12	
GPIO16	SPIA_SIMO		OUTPUTXBAR7	EPWM5_A	SCIA_TX		EQEP1_STROBE	PMBUSA_SCL	XCLKOUT	EQEP2_B	SPIB_SOMI	HIC_D1	
GPIO17	SPIA_SOMI		OUTPUTXBAR8	EPWM5_B	SCIA_RX		EQEP1_INDEX	PMBUSA_SDA	CANA_TX			HIC_D2	
GPIO18_X2	SPIA_CLK		CANA_RX	EPWM6_A	I2CA_SCL		EQEP2_A	PMBUSA_CTL	XCLKOUT	LINB_TX	FSITXA_TDM_CLK	HIC_INT	X2
GPIO19_X1	SPIA_STE		CANA_TX	EPWM6_B	I2CA_SDA		EQEP2_B	PMBUSA_ALERT	CLB_OUTPUTXBAR1	LINB_RX	FSITXA_TDM_D0	HIC_NBE0	X1
GPIO22	EQEP1_STROBE				SPIB_CLK		LINA_TX	CLB_OUTPUTXBAR1	LINB_TX	HIC_A5	EPWM4_A	HIC_D13	
GPIO23	EQEP1_INDEX				SPIB_STE		LINA_RX		LINB_RX	HIC_A3	EPWM4_B	HIC_D11	
GPIO24	OUTPUTXBAR1	EQEP2_A			SPIB_SIMO		LINB_TX	PMBUSA_SCL	SCIA_TX	ERRORSTS		HIC_D3	
GPIO25	OUTPUTXBAR2	EQEP2_B		EQEP1_A	SPIB_SOMI		FSITXA_D1	PMBUSA_SDA	SCIA_RX		HIC_BASESEL0		
GPIO26	OUTPUTXBAR3	EQEP2_INDEX		OUTPUTXBAR3	SPIB_CLK		FSITXA_D0	PMBUSA_CTL	I2CA_SDA		HIC_D0	HIC_A1	
GPIO27	OUTPUTXBAR4	EQEP2_STROBE		OUTPUTXBAR4	SPIB_STE		FSITXA_CLK	PMBUSA_ALERT	I2CA_SCL		HIC_D1	HIC_A4	

Table 5-6. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO28	SCIA_RX		EPWM7_A	OUTPUTXBAR5	EQEP1_A		EQEP2_STROBE	LINA_TX	SPIB_CLK	ERRORSTS	I2CB_SDA	HIC_NOE	
GPIO29	SCIA_TX		EPWM7_B	OUTPUTXBAR6	EQEP1_B		EQEP2_INDEX	LINA_RX	SPIB_STE	ERRORSTS	I2CB_SCL	HIC_NCS	
GPIO30	CANA_RX		SPIB_SIMO	OUTPUTXBAR7	EQEP1_STROBE		FSIRXA_CLK		EPWM1_A		HIC_D8		
GPIO31	CANA_TX		SPIB_SOMI	OUTPUTXBAR8	EQEP1_INDEX		FSIRXA_D1		EPWM1_B		HIC_D10		
GPIO32	I2CA_SDA		SPIB_CLK		LINA_TX		FSIRXA_D0	CANA_TX		ADCSOCBO		HIC_INT	
GPIO33	I2CA_SCL		SPIB_STE	OUTPUTXBAR4	LINA_RX		FSIRXA_CLK	CANA_RX	EQEP2_B	ADCSOCAO		HIC_D0	
GPIO34	OUTPUTXBAR1				PMBUSA_SDA					HIC_NBE1	I2CB_SDA	HIC_D9	
GPIO35	SCIA_RX		I2CA_SDA	CANA_RX	PMBUSA_SCL	LINA_RX	EQEP1_A	PMBUSA_CTL			HIC_NWE	TDI	
GPIO37	OUTPUTXBAR2		I2CA_SCL	SCIA_TX	CANA_TX	LINA_TX	EQEP1_B	PMBUSA_ALERT			HIC_NRDY	TDO	
GPIO39						FSIRXA_CLK	EQEP2_INDEX		CLB_OUTPUTXBAR2	SYNCOUT	EQEP1_INDEX	HIC_D7	
GPIO40	SPIB_SIMO			EPWM2_B	PMBUSA_SDA	FSIRXA_D0		EQEP1_A	LINB_TX		HIC_NBE1	HIC_D5	
GPIO41				EPWM2_A	PMBUSA_SCL	FSIRXA_D1		EQEP1_B	LINB_RX	HIC_A4	SPIB_SOMI	HIC_D12	
GPIO42		LINA_RX	OUTPUTXBAR5	PMBUSA_CTL	I2CA_SDA			EQEP1_STROBE	CLB_OUTPUTXBAR3		HIC_D2	HIC_A6	
GPIO43			OUTPUTXBAR6	PMBUSA_ALERT	I2CA_SCL			EQEP1_INDEX	CLB_OUTPUTXBAR4		HIC_D3	HIC_A7	
GPIO44			OUTPUTXBAR7	EQEP1_A		FSITXA_CLK		CLB_OUTPUTXBAR3		HIC_D7		HIC_D5	
GPIO45			OUTPUTXBAR8			FSITXA_D0		CLB_OUTPUTXBAR4				HIC_D6	
GPIO46			LINA_TX			FSITXA_D1						HIC_NWE	
GPIO61													
GPIO62													
GPIO63													
AIO224												HIC_A3	
AIO225												HIC_NWE	
AIO226												HIC_A1	
AIO227												HIC_NBE0	
AIO228												HIC_A0	
AIO230												HIC_BASESEL2	
AIO231												HIC_BASESEL1	
AIO232												HIC_BASESEL0	
AIO233												HIC_A4	
AIO237												HIC_A6	
AIO238												HIC_NCS	
AIO239												HIC_A5	
AIO241												HIC_NBE1	
AIO242												HIC_A2	

Table 5-6. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
AIO244												HIC_A7	
AIO245												HIC_NOE	

Note

The analog pins that contain AIOs are in analog mode by default. AIO mode is enabled by configuring the AMSEL option of GPIOH for the analog pin. In addition, if using the HIC mux options on the AIO pins, an external pullup is required.

5.4.2 Digital Inputs on ADC Pins (AIOs)

GPIOs on port H (GPIO224–GPIO245) are multiplexed with analog pins. These are also referred to as AIOs. These pins can only function in input mode. By default, these pins will function as analog pins and the GPIOs are in a high-Z state. The GPHAMSEL register is used to configure these pins for digital or analog operation.

Note

If digital signals with sharp edges (high dv/dt) are connected to the AIOs, cross-talk can occur with adjacent analog signals. The user should therefore limit the edge rate of signals connected to AIOs if adjacent channels are being used for analog functions.

5.4.3 GPIO Input X-BAR

The Input X-BAR is used to route signals from a GPIO to many different IP blocks such as the ADCs, eCAPs, ePWMs, and external interrupts (see Figure 5-4). Table 5-7 lists the input X-BAR destinations. For details on configuring the Input X-BAR, see the Crossbar (X-BAR) chapter of the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.

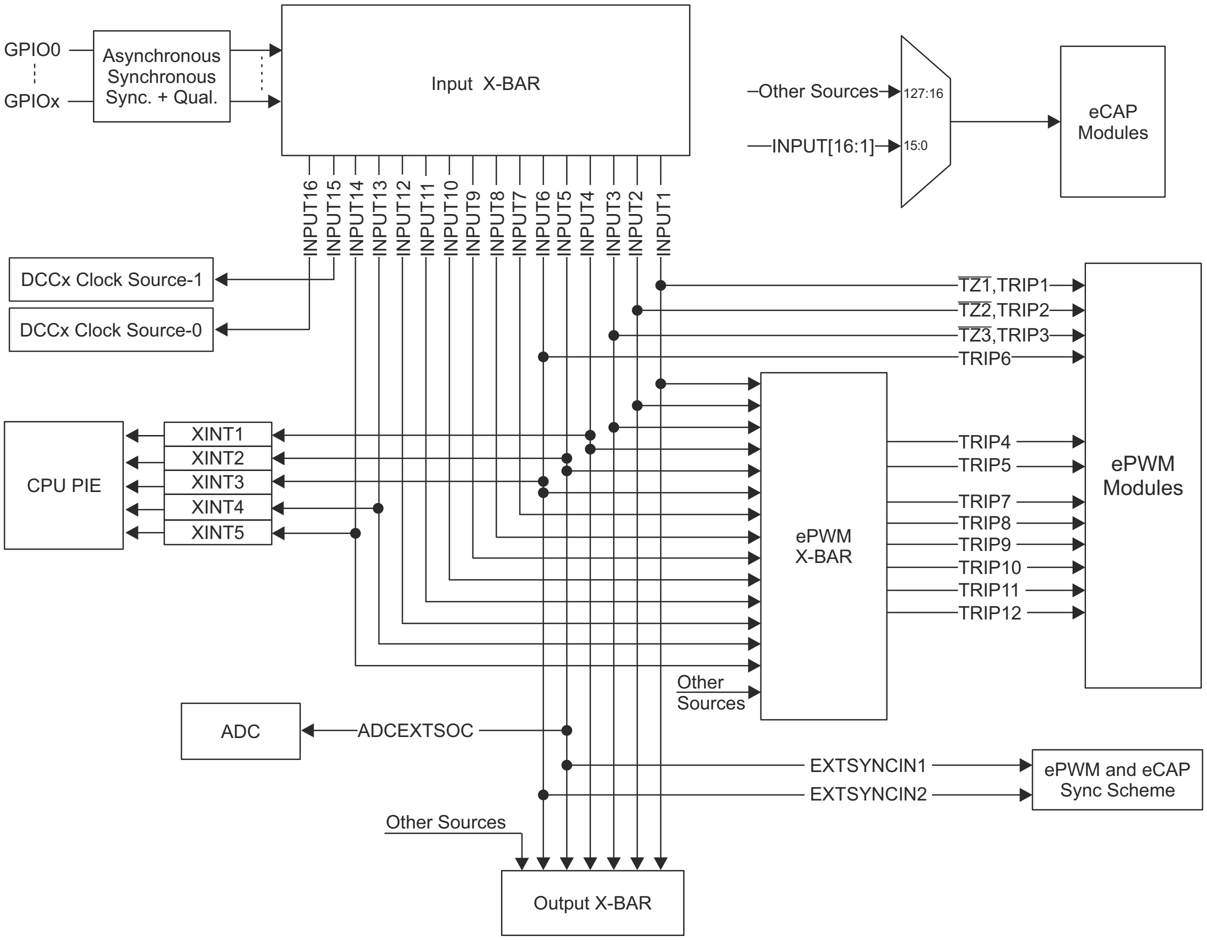


Figure 5-4. Input X-BAR

Table 5-7. Input X-BAR Destinations

INPUT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECAP / HRCAP	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
EPWM X-BAR	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes		
CLB X-BAR	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes		
OUTPUT X-BAR	Yes	Yes	Yes	Yes	Yes	Yes										
CPU XINT				XINT1	XINT2	XINT3							XINT4	XINT5		
EPWM TRIP	TZ1, TRIP1	TZ2, TRIP2	TZ3, TRIP3			TRIP6										
ADC START OF CONVERSION					ADCEXTSOC											
EPWM / ECAP SYNC					EXTSYNCIN1	EXTSYNCIN2										
DCCx															CLK1	CLK0

5.4.4 GPIO Output X-BAR, CLB X-BAR, CLB Output X-BAR, and ePWM X-BAR

The Output X-BAR has eight outputs that can be selected on the GPIO mux as OUTPUTXBARx. The CLB X-BAR has eight outputs that are connected to the CLB global mux as AUXSIGx. The CLB Output X-BAR has eight outputs that can be selected on the GPIO mux as CLB_OUTPUTXBARx. The ePWM X-BAR has eight outputs that are connected to the TRIPx inputs of the ePWM. The sources for the Output X-BAR, CLB X-BAR, CLB Output X-BAR, and ePWM X-BAR are shown in Figure 5-5. For details on the Output X-BAR, CLB X-BAR, CLB Output X-BAR, and ePWM X-BAR, see the Crossbar (X-BAR) chapter of the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.

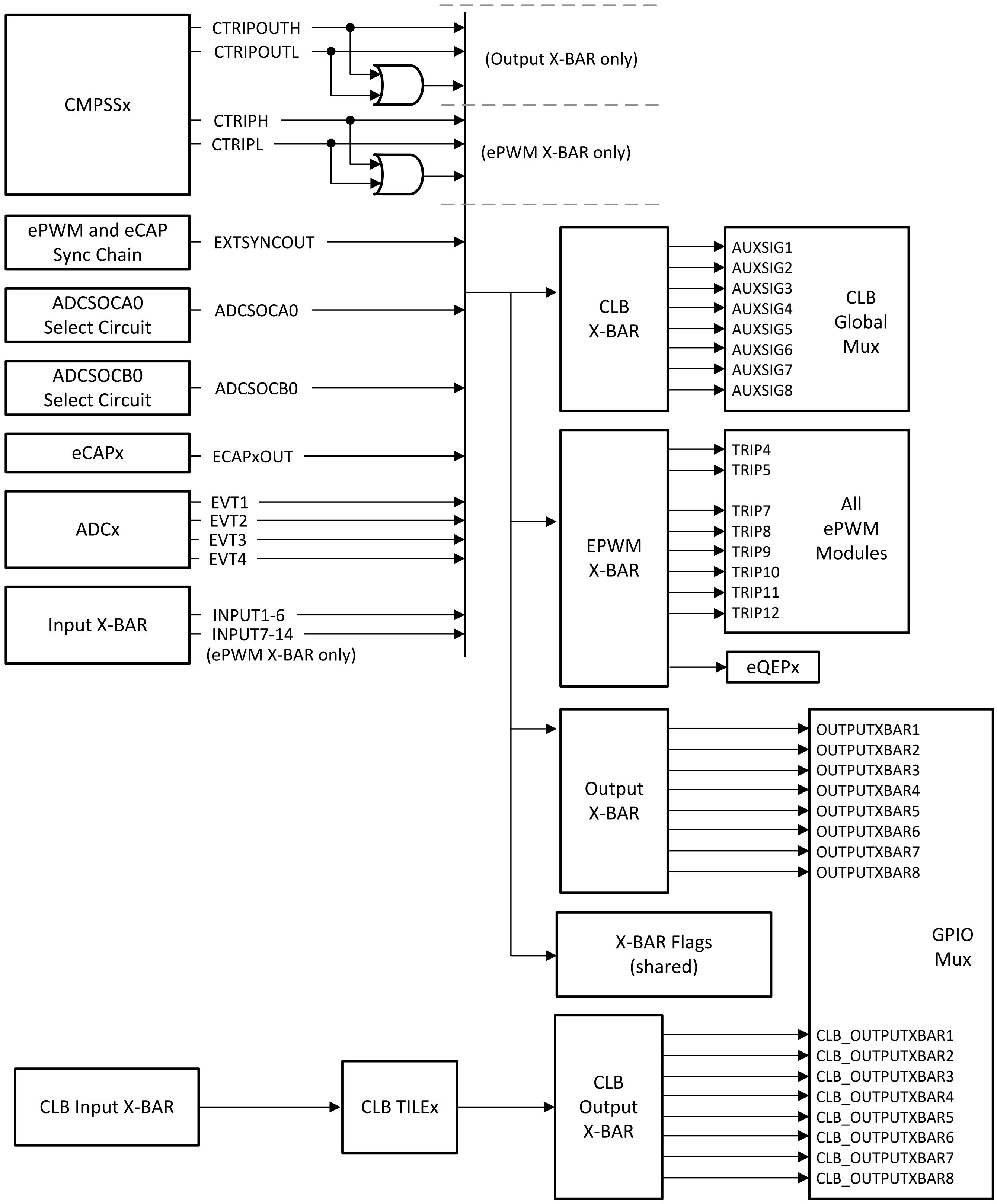


Figure 5-5. Output X-BAR, CLB X-BAR, CLB Output X-BAR, and ePWM X-BAR Sources

5.5 Pins With Internal Pullup and Pulldown

Some pins on the device have internal pullups or pulldowns. Table 5-8 lists the pull direction and when it is active. The pullups on GPIO pins are disabled by default and can be enabled through software. To avoid any floating unbonded inputs, the Boot ROM will enable internal pullups on GPIO pins that are not bonded out in a particular package. Other pins noted in Table 5-8 with pullups and pulldowns are always on and cannot be disabled.

Table 5-8. Pins With Internal Pullup and Pulldown

PIN	RESET (XRSn = 0)	DEVICE BOOT	APPLICATION
GPIOx	Pullup disabled	Pullup disabled(1)	Application defined
GPIO35/TDI	Pullup disabled		Application defined
GPIO37/TDO	Pullup disabled		Application defined
TCK	Pullup active		
TMS	Pullup active		
XRSn	Pullup active		
Other pins (including AIOs)	No pullup or pulldown present		

(1) Pins not bonded out in a given package will have the internal pullups enabled by the Boot ROM.

5.6 Connections for Unused Pins

For applications that do not need to use all functions of the device, Table 5-9 lists acceptable conditioning for any unused pins. When multiple options are listed in Table 5-9, any option is acceptable. Pins not listed in Table 5-9 must be connected according to Section 5.

Table 5-9. Connections for Unused Pins

SIGNAL NAME	ACCEPTABLE PRACTICE
ANALOG	
VREFHI	Tie to VDDA (applies only if ADC is not used in the application)
VREFLO	Tie to VSSA
Analog input pins	• No Connect • Tie to VSSA • Tie to VSSA through resistor
DIGITAL	
FLT1 (Flash Test pin 1)	• No Connect • Tie to VSS through 4.7-kΩ or larger resistor
FLT2 (Flash Test pin 2)	• No Connect • Tie to VSS through 4.7-kΩ or larger resistor
GPIOx	• No connection (input mode with internal pullup enabled) • No connection (output mode with internal pullup disabled) • Pullup or pulldown resistor (any value resistor, input mode, and with internal pullup disabled)
GPIO35/TDI	When TDI mux option is selected (default), the GPIO is in Input mode. • Internal pullup enabled • External pullup resistor
GPIO37/TDO	When TDO mux option is selected (default), the GPIO is in Output mode only during JTAG activity; otherwise, it is in a tri-state condition. The pin must be biased to avoid extra current on the input buffer. • Internal pullup enabled • External pullup resistor
TCK	• No Connect • Pullup resistor
TMS	Pullup resistor
GPIO19/X1	Turn XTAL off and: • Input mode with internal pullup enabled • Input mode with external pullup or pulldown resistor • Output mode with internal pullup disabled
GPIO18/X2	Turn XTAL off and: • Input mode with internal pullup enabled • Input mode with external pullup or pulldown resistor • Output mode with internal pullup disabled
POWER AND GROUND	
VDD	All VDD pins must be connected per Section 5.3. Pins should not be used to bias any external circuits.
VDDA	If a dedicated analog supply is not used, tie to VDDIO.
VDDIO	All VDDIO pins must be connected per Section 5.3.
VSS	All VSS pins must be connected to board ground.
VSSA	If an analog ground is not used, tie to VSS.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage	VDDIO with respect to VSS	–0.3	4.6	V
	VDDA with respect to VSSA	–0.3	4.6	
Input voltage(6)	V_{IN} (3.3 V)	–0.3	4.6	V
Output voltage	V_O	–0.3	4.6	V
Input clamp current – per pin(4) (5)	I_{IK} - V_{IN} < VSS/VSSA - V_{IN} > VDDIO/VDDA	–20	20	mA
Input clamp current – total for all inputs(5)	$I_{IKTOTAL}$ - V_{IN} < VSS/VSSA - V_{IN} > VDDIO/VDDA	–20	20	mA
Output current	Digital output (per pin), I_{OUT}	–20	20	mA
Free-Air temperature	T_A	–40	125	°C
Operating junction temperature	T_J	–40	150	°C
Storage temperature(3)	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device beyond the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *Semiconductor and IC Package Thermal Metrics Application Report*.
(4) Continuous clamp current per pin is ±2 mA.
(5) Applying a V_{IN} greater than VDDIO/VDDA or less than VSS/VSSA will turn on the ESD current clamping diode causing additional current flow to the respective supply rail. If this occurs, the current must be kept within the MIN/MAX listed to prevent permanent damage to the device.
(6) Input clamp current must also be observed.

6.2 ESD Ratings – Commercial

				VALUE	UNIT
F280025, F280025C, F280023, F280023C in 80-pin PN package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 80-pin PN: 1, 20, 21, 40, 41, 60, 61, 80	±750	
F280025, F280025C, F280023, F280023C in 64-pin PM package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 64-pin PM: 1, 16, 17, 32, 33, 48, 49, 64	±750	
F280025, F280025C, F280023, F280023C, F280021 in 48-pin PT package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 48-pin PT: 1, 12, 13, 24, 25, 36, 37, 48	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings – Automotive

				VALUE	UNIT
F280025-Q1, F280025C-Q1, F280023-Q1 in 80-pin PN package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 80-pin PN: 1, 20, 21, 40, 41, 60, 61, 80	±750	
F280025-Q1, F280025C-Q1, F280023-Q1 in 64-pin PM package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 64-pin PM: 1, 16, 17, 32, 33, 48, 49, 64	±750	
F280025-Q1, F280025C-Q1, F280023-Q1, F280021-Q1 in 48-pin PT package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 48-pin PT: 1, 12, 13, 24, 25, 36, 37, 48	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, VDDIO and VDDA	Internal BOR enabled[3]	$V_{BOR\text{-}VDDIO}$(MAX) + $V_{BOR\text{-}GB}$ [2]	3.3	3.63	V
	Internal BOR disabled	2.8	3.3	3.63	
Device ground, VSS			0		V
Analog ground, VSSA			0		V
SR_{SUPPLY}	Supply ramp rate of VDDIO, VDDA with respect to VSS.[4]				
V_{IN} [6]	Digital input voltage	VSS – 0.3		VDDIO + 0.3	V
	Analog input voltage	VSSA – 0.3		VDDA + 0.3	V
$V_{BOR\text{-}GB}$	VDDIO BOR guard band[5]		0.1		V
Junction temperature, T_J [1]		–40		145	°C
Free-Air temperature, T_A		–40		125	°C

(1) Operation above T_J = 105°C for extended duration will reduce the lifetime of the device. See *Calculating Useful Lifetimes of Embedded Processors* for more information.
(2) The VDDIO BOR voltage ($V_{BOR\text{-}VDDIO}$[MAX]) in Electrical Characteristics table determines the lower voltage bound for device operation. TI recommends that system designers budget an additional guard band ($V_{BOR\text{-}GB}$) as shown in Supply Voltages figure.
(3) Internal BOR is enabled by default.
(4) See the *Power Management Module Operating Conditions* table.
(5) TI recommends $V_{BOR\text{-}GB}$ to avoid BOR resets due to normal supply noise or load-transient events on the 3.3-V VDDIO system regulator. Good system regulator design and decoupling capacitance (following the system regulator specifications) are important to prevent activation of the BOR during normal device operation. The value of $V_{BOR\text{-}GB}$ is a system-level design consideration; the voltage listed here is typical for many applications.
(6) Applying a V_{IN} greater than VDDIO/VDDA or less than VSS/VSSA will turn on the ESD current clamping diode causing additional current flow to the respective supply rail. VDDIO/VDDA voltage will internally rise and could impact other electrical characteristics.

Supply Voltages

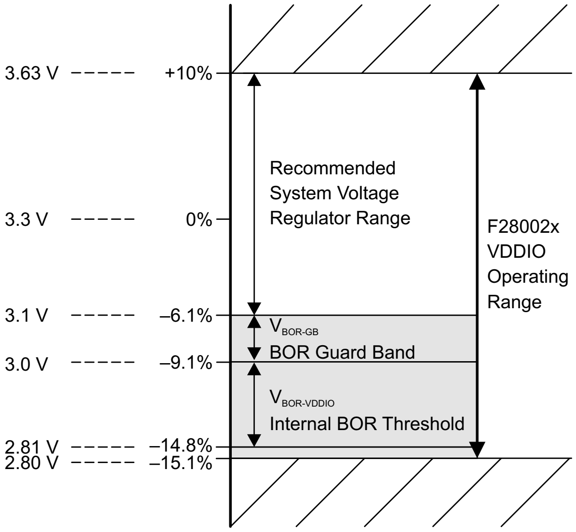


Figure 6-1. Supply Voltages

6.5 Power Consumption Summary

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations. Section 6.5.1 lists the system current consumption values.

6.5.1 System Current Consumption

over operating free-air temperature range (unless otherwise noted).
TYP : V_{nom}, 30°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING MODE						
I_{DDIO}	VDDIO current consumption during operational usage	This is an estimation of current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency.		35	72	mA
I_{DDA}	VDDA current consumption during operational usage			3	5	mA
IDLE MODE						
I_{DDIO}	VDDIO current consumption while device is in Idle mode	- CPU is in IDLE mode - Flash is powered down - XCLKOUT is turned off - Pull up is enabled for IO pins		16	33	mA
I_{DDA}	VDDA current consumption while device is in Idle mode			0.01	0.1	mA
STANDBY MODE						
I_{DDIO}	VDDIO current consumption while device is in Standby mode	- CPU is in STANDBY mode - Flash is powered down - XCLKOUT is turned off - Pull up is enabled for IO pins		8	22	mA
I_{DDA}	VDDA current consumption while device is in Standby mode			0.01	0.1	mA
HALT MODE						
I_{DDIO}	VDDIO current consumption while device is in Halt mode	- CPU is in HALT mode - Flash is powered down - XCLKOUT is turned off - Pull up is enabled for IO pins		1	16	mA
I_{DDA}	VDDA current consumption while device is in Halt mode			0.01	0.1	mA
FLASH ERASE/PROGRAM						
I_{DDIO}	VDDIO current consumption during Erase/Program cycle(1)	- CPU is running from RAM. - SYSCLK at 100 MHz. - I/Os are inputs with pullups enabled. - Peripheral clocks are turned off.		72	106	mA
I_{DDA}	VDDA current consumption during Erase/Program cycle			0.1	2.5	mA
RESET MODE						
I_{DDIO}	VDDIO current consumption while reset is active(2)			8.6		mA
I_{DDA}	VDDA current consumption while reset is active(2)			0.1		mA

(1) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.
(2) This is the current consumption while reset is active, that is, XRSn is low.

6.5.2 Operating Mode Test Description

Section 6.5.1 and Section 6.5.4.1 list the current consumption values for the operational mode of the device. The operational mode provides an estimation of what an application might encounter. The test condition for these measurements has the following properties:

- Code is executing from RAM.
- FLASH is read and kept in active state.
- No external components are driven by I/O pins.
- All peripherals have clocks enabled.
- All CPUs are actively executing code.
- All analog peripherals are powered up. ADCs and DACs are periodically converting.

6.5.3 Current Consumption Graphs

Figure 6-2, Figure 6-3, Figure 6-4, Figure 6-5, and Figure 6-6 show a typical representation of the relationship between frequency, temperature, core supply, and current consumption on the device. Actual results will vary based on the system implementation and conditions.

Figure 6-3 shows the typical operating current profile across temperature and core supply voltage. Figure 6-4 shows the typical idle current profile across temperature and core supply voltage. Figure 6-5 shows the typical standby current profile across temperature and core supply voltage. Figure 6-6 shows the typical halt current profile across temperature and core supply voltage.

Note

Data for Figure 6-2 was collected at 30°C.

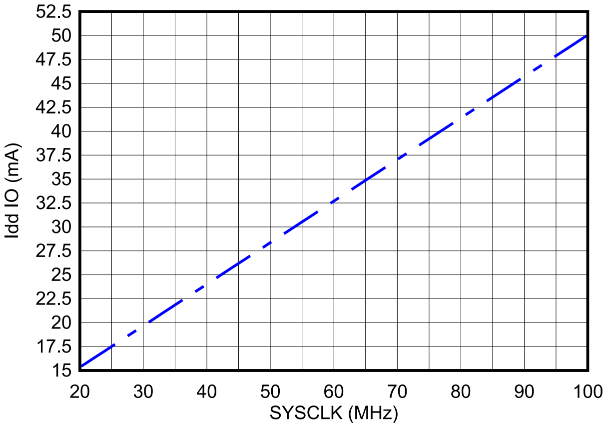


Figure 6-2. Operating Current Versus Frequency

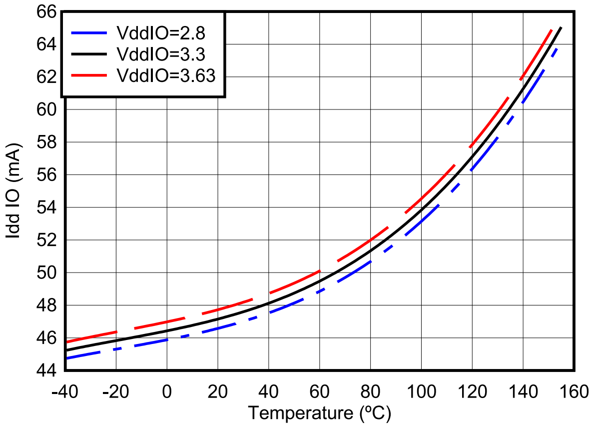


Figure 6-3. Operating Current Versus Temperature

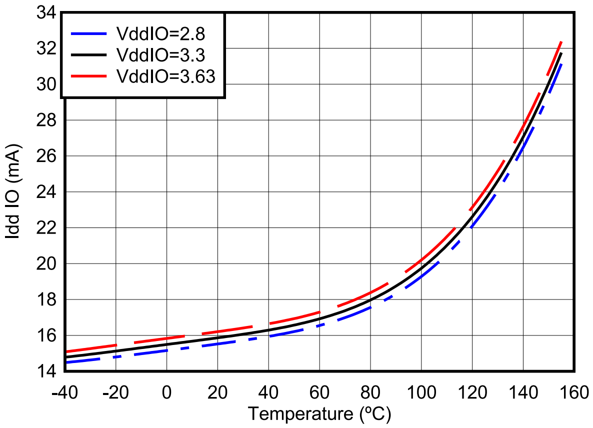


Figure 6-4. Current Versus Temperature – IDLE Mode

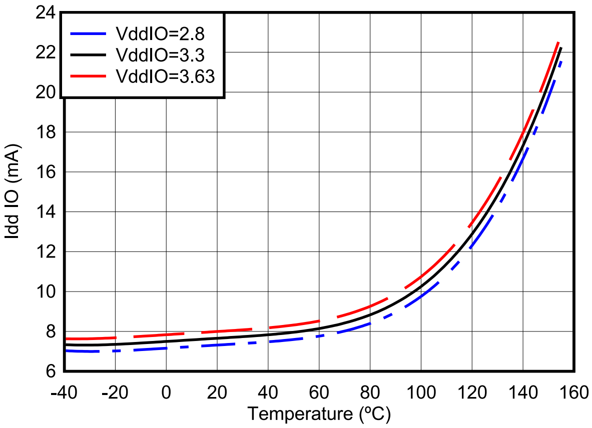


Figure 6-5. Current Versus Temperature – STANDBY Mode

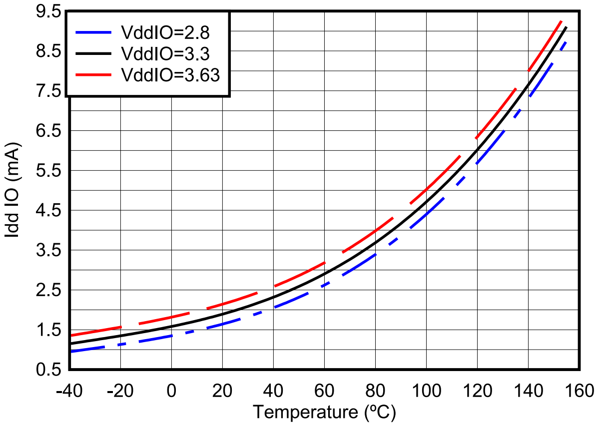


Figure 6-6. Current Versus Temperature – HALT Mode

6.5.4 Reducing Current Consumption

The F28002x devices provide some methods to reduce the device current consumption:

- One of the two low-power modes—IDLE or STANDBY—could be entered during idle periods in the application.
- The flash module may be powered down if the code is run from RAM.
- Disable the pullups on pins that assume an output function.
- Each peripheral has an individual clock-enable bit (PCLKCRx). Reduced current consumption may be achieved by turning off the clock to any peripheral that is not used in a given application. Section 6.5.4.1 lists the typical current reduction that may be achieved by disabling the clocks using the PCLKCRx register.
- To realize the lowest VDDA current consumption in an LPM, see the Analog-to-Digital Converter (ADC) chapter of the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual* to ensure each module is powered down as well.

6.5.4.1 Typical Current Reduction per Disabled Peripheral

PERIPHERAL	I_{DDIO} CURRENT REDUCTION (mA)
ADC(1)	0.67
BGCRC	0.26
CAN	1.18
CLB	1.18
CMPSS(1)	0.34
CPU TIMER	0.02
CPUCRC	0.01
DCC	0.18
DMA	0.56
eCAP1 and eCAP2	0.22
eCAP3(2)	0.28
ePWM	0.78
eQEP	0.11
FSI	0.74
HIC	0.21
HRPWM	0.87
I2C	0.24
LIN	0.32
PBIST	0.19
PMBUS	0.26
SCI	0.16
SPI	0.08

(1) This current represents the current drawn by the digital portion of the each module.
(2) eCAP3 can also be configured as HRCAP.

6.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital and Analog IO							
V_{OH}	High-level output voltage		$I_{OH} = I_{OH}$ MIN	VDDIO * 0.8			V
			I_{OH} = –100 μA	VDDIO – 0.2			
V_{OL}	Low-level output voltage		$I_{OL} = I_{OL}$ MAX			0.4	V
			I_{OL} = 100 μA			0.2	
I_{OH}	High-level output source current for all output pins			–4			mA
I_{OL}	Low-level output sink current for all output pins					4	mA
R_{OH}	High-level output impedance for all output pins			45	65	100	Ω
R_{OL}	Low-level output impedance for all output pins			45	60	90	Ω
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
$V_{HYSTERESIS}$	Input hysteresis			125			mV
$I_{PULLDOWN}$	Input current	Pins with pulldown	VDDIO = 3.3 V V_{IN} = VDDIO		120		μA
I_{PULLUP}	Input current	Digital inputs with pullup enabled[1]	VDDIO = 3.3 V V_{IN} = 0 V		160		μA
I_{LEAK}	Pin leakage	Digital inputs	Pullups and outputs disabled 0 V ≤ V_{IN} ≤ VDDIO			0.1	μA
		Analog pins (except ADCINA3/VDAC)	Analog drivers disabled 0 V ≤ V_{IN} ≤ VDDA			0.1	
		ADCINA3/VDAC			2	11	
C_I	Input capacitance	Digital inputs			2		pF
		Analog pins[2]					
VREG and BOR							
$V_{POR-VDDIO}$	VDDIO power on reset voltage	VDDIO power on reset voltage			2.3		V
$V_{BOR-VDDIO}$	VDDIO brown out reset voltage[3]			2.81		3.0	V
V_{VREG}	Internal voltage regulator output			1.14	1.2	1.32	V

(1) See Pins With Internal Pullup and Pulldown table for a list of pins with a pullup or pulldown.
(2) The analog pins are specified separately; see Per-Channel Parasitic Capacitance table.
(3) See the Supply Voltages figure in the Recommended Operating Conditions section.

6.7 Thermal Resistance Characteristics for PN Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	14.2	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	21.9	N/A
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	49.9	0
		38.3	150
		36.7	250
		34.4	500
Psi_{JT}	Junction-to-package top	0.8	0
		1.18	150
		1.34	250
		1.62	500
Psi_{JB}	Junction-to-board	21.6	0
		20.7	150
		20.5	250
		20.1	500

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

6.8 Thermal Resistance Characteristics for PM Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	12.4	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	25.6	N/A
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	51.8	0
$R\Theta_{JMA}$	Junction-to-moving air thermal resistance	42.2	150
		39.4	250
		36.5	500
Psi_{JT}	Junction-to-package top	0.5	0
		0.9	150
		1.1	250
		1.4	500
Psi_{JB}	Junction-to-board	25.1	0
		23.8	150
		23.4	250
		22.7	500

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

6.9 Thermal Resistance Characteristics for PT Package

		°C/W[1]	AIR FLOW (lfm)[2]
$R\Theta_{JC}$	Junction-to-case thermal resistance	13.6	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	30.6	N/A
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	64	0
		50.4	150
		48.2	250
		45	500
Psi_{JT}	Junction-to-package top	0.56	0
		0.94	150
		1.1	250
		1.38	500
Psi_{JB}	Junction-to-board	30.1	0
		28.7	150
		28.4	250
		28	500

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

6.10 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T_A) varies with the end application and product design. The critical factor that affects reliability and functionality is T_J, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T_J within the specified limits. T_{case} should be measured to estimate the operating junction temperature T_J. T_{case} is normally measured at the center of the package top-side surface. The thermal application report *Semiconductor and IC Package Thermal Metrics* helps to understand the thermal metrics and definitions.

6.11 System

6.11.1 Power Management Module (PMM)

6.11.1.1 Introduction

The Power Management Module (PMM) handles all the power management functions required for device operation.

6.11.1.2 Overview

The block diagram of the PMM is shown in Figure 6-7. As can be seen, the PMM comprises of various subcomponents, which are described in the subsequent sections.

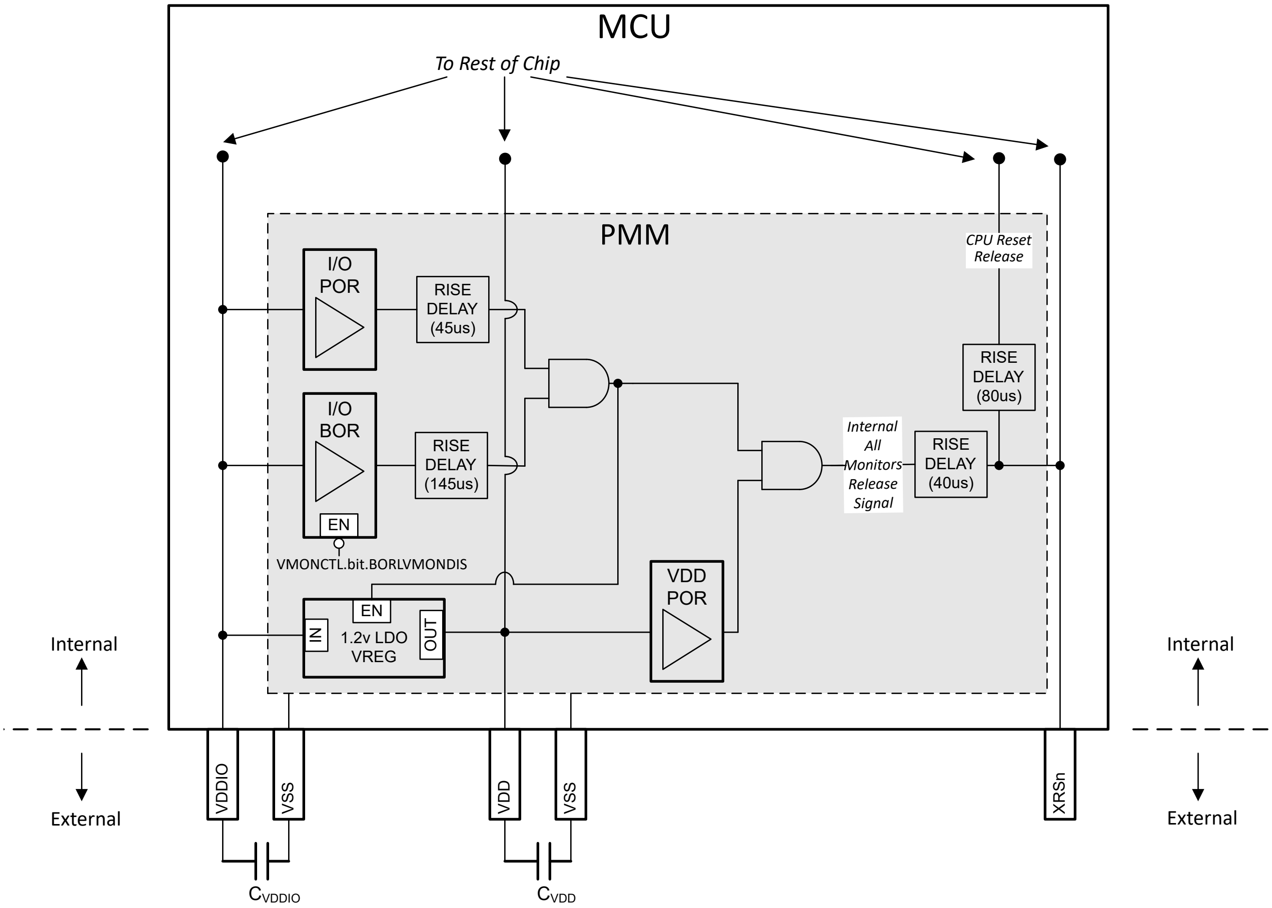


Figure 6-7. PMM Block Diagram

6.11.1.2.1 Power Rail Monitors

The PMM has voltage monitors on the supply rails that release the XRSn signal high once the voltages cross the set threshold during power up. They also function to trip the XRSn signal low if any of the voltages drop below the programmed levels. The various voltage monitors are described in subsequent sections.

Note

Not all the voltage monitors are supported for device operation in an application after boot up. In the case where a voltage monitor is not supported, an external supervisor is recommended if the device needs supply voltage monitoring while the application is running.

The three voltage monitors (I/O POR, I/O BOR, VDD POR) all have to release their respective outputs before the device begins operation (that is, XRSn goes high). However, if any of the voltage monitors trips, XRSn is driven low. The I/Os are held in high impedance when any of the voltage monitors trip.

6.11.1.2.1.1 I/O POR (Power-On Reset) Monitor

The I/O POR monitor supervises the VDDIO rail. During power up, this is the first monitor to release (that is, first to untrip) on VDDIO.

6.11.1.2.1.2 I/O BOR (Brown-Out Reset) Monitor

The I/O BOR monitor also supervises the VDDIO rail. During power up, this is the second monitor to release (that is, second to untrip) on VDDIO. This monitor has a tighter tolerance compared to the I/O POR.

Any drop in voltage below the recommended operating voltages will trip the I/O BOR and reset the device but this can be disabled by setting VMONCTL.bit.BORLVMONDIS to 1. The I/O BOR can only be disabled after the device has fully booted up. If the I/O BOR is disabled, the I/O POR will reset the device for voltage drops.

Note

The level at which the I/O POR trips is well below the minimum recommended voltage for VDDIO, and therefore should not be used for device supervision.

Figure 6-8 shows the operating region of the I/O BOR.

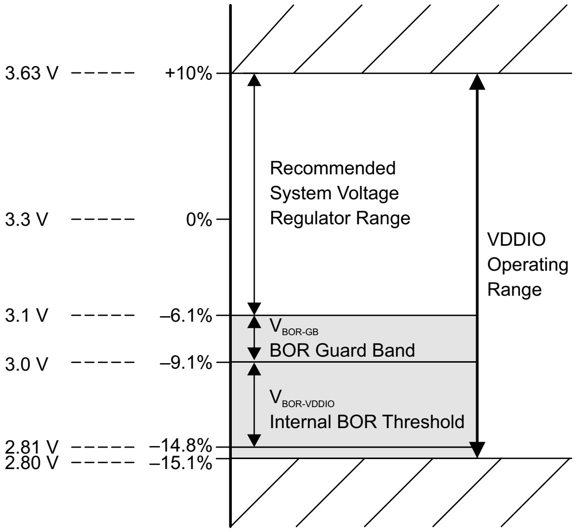


Figure 6-8. I/O BOR Operating Region

6.11.1.2.1.3 VDD POR (Power-On Reset) Monitor

The VDD POR monitor supervises the VDD rail. During power up, this monitor releases (that is, untrips) once the voltage crosses the programmed trip level on VDD.

Note

VDD POR is programmed at a level below the minimum recommended voltage for VDD, and therefore it should not be relied upon for VDD supervision if that is required in the application.

6.11.1.2.2 External Supervisor Usage

VDDIO Monitoring: The I/O BOR is supported for application use, so an external supervisor is not required to monitor the I/O rail.

VDD Monitoring:

- VDD supplied from the internal VREG: The VDD supply is derived from the VDDIO supply. The VREG is designed in such a way that a valid VDDIO supply(monitored by the IO BOR) implies a valid VDD supply.

Note

The use of an external supervisor with the internal VREG is not supported.

6.11.1.2.3 Delay Blocks

The delay blocks in the path of the voltage monitors work together to delay the release time between the voltage monitors and XRSn. This is to ensure that the voltages are stable when XRSn releases. The delay blocks are only active during power up (that is, when VDDIO and VDD are ramping up).

The delay blocks contribute to the minimum slew rates specified in Power Management Module Electrical Data and Timing for the power rails.

Note

The delay numbers specified in the block diagram are typical numbers.

6.11.1.2.4 Internal 1.2-V LDO Voltage Regulator (VREG)

The internal VREG is supplied by the VDDIO rail and can generate the 1.2 V required to power the VDD pins. Although the internal VREG eliminates the need to use an external supply for VDD, decoupling capacitors are still required on the VDD pins for VREG stability and transients. See the *VDD Decoupling* section for details.

6.11.1.3 External Components

6.11.1.3.1 Decoupling Capacitors

VDDIO and VDD require decoupling capacitors for correct operation. The requirements are outlined in subsequent sections.

6.11.1.3.1.1 VDDIO Decoupling

Place a minimum amount of decoupling capacitance on VDDIO. See the C_{VDDIO} parameter in Power Management Module Electrical Data and Timing. The actual amount of decoupling capacitance to use is a requirement of the power supply driving VDDIO. Either of the configurations outlined below is acceptable:

- **Configuration 1:** Place a decoupling capacitor on each VDDIO pin per the C_{VDDIO} parameter.
- **Configuration 2:** Install a single decoupling capacitor that is the equivalent of C_{VDDIO} * VDDIO pins.

Note

Having the decoupling capacitor or capacitors close to the device pins is critical.

6.11.1.3.1.2 VDD Decoupling

Place a minimum amount of decoupling capacitance on VDD. See the C_{VDD} TOTAL parameter in Power Management Module Electrical Data and Timing.

Either of the configurations outlined below is acceptable:

- **Configuration 1:** Divide C_{VDD} TOTAL equally across the VDD pins. In this configuration, the VDD pins may be separated at the PCB level.
- **Configuration 2:** Install a single decoupling capacitor with value of C_{VDD} TOTAL. In this configuration, all VDD pins must be connected to each other on the PCB.

Note

Having the decoupling capacitor or capacitors close to the device pins is critical.

6.11.1.4 Power Sequencing

6.11.1.4.1 Supply Pins Ganging

Connecting all 3.3-V rails together and supplying from a single source are strongly recommended. This list includes:

- VDDIO
- VDDA

In addition, connect all power pins to avoid leaving any unconnected.

In internal VREG mode, tying the VDD pins together is optional as long as each VDD pin has a capacitor connected to pin. See the *VDD Decoupling* section for VDD decoupling configurations.

The analog modules on the device have fairly high PSRR; therefore, in most cases, noise on VDDA will have to exceed the recommended operating conditions of the supply rails before the analog modules see performance degradation. Therefore, supplying VDDA separately typically offers minimal benefits. Nevertheless, for the purposes of noise improvement, placing a pi filter between VDDIO and VDDA is acceptable.

Note

All the supply pins per rail are tied together internally. For example, all VDDIO pins are tied together internally, all VDD pins are tied together internally, and so forth.

6.11.1.4.2 Signal Pins Power Sequence

Before powering the device, do not apply voltage larger than 0.3 V above VDDIO or 0.3 V below VSS to any digital pin and 0.3 V above VDDA or 0.3 V below VSSA to any analog pin (including VREFHI). Simply, the signal pins should only be driven after XRSn goes high, provided all the 3.3-V rails are tied together. This sequencing is still required even if VDDIO and VDDA are not tied together.

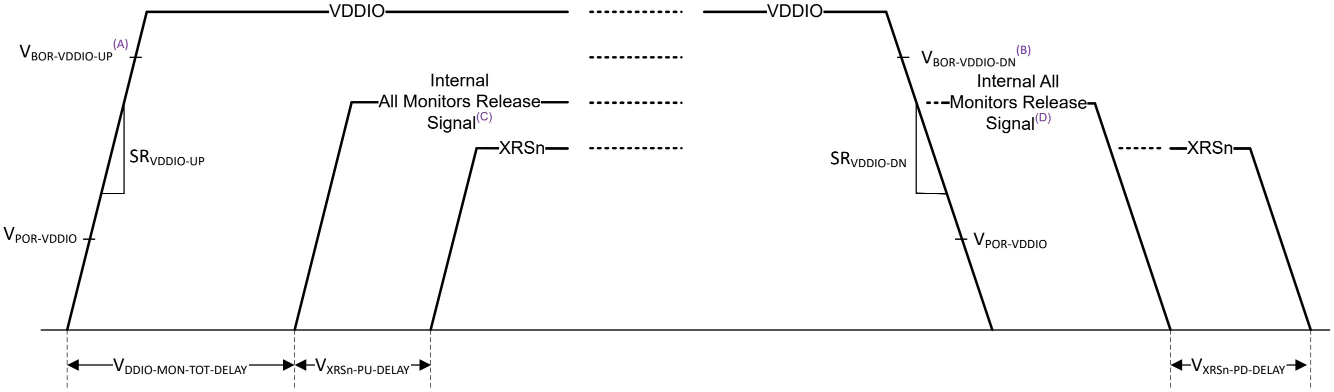
CAUTION

If the above sequence is violated, device malfunction and possibly damage can occur as current will flow through unintended parasitic paths in the device.

6.11.1.4.3 Supply Pins Power Sequence

6.11.1.4.3.1 Internal VREG/VDD Mode Sequence

Figure 6-9 depicts the power sequencing requirements for internal VREG mode. The values for all the parameters indicated can be found in Power Management Module Electrical Data and Timing.



A. This trip point is the trip point before XRSn releases. See the *Power Management Module Characteristics* table.
B. This trip point is the trip point after XRSn releases. See the *Power Management Module Characteristics* table.
C. During power up, the All Monitors Release Signal goes high after all POR and BOR monitors are released. See the *PMM Block Diagram*.
D. During power down, the All Monitors Release Signal goes low if any of the POR or BOR monitors are tripped. See the *PMM Block Diagram*.

Figure 6-9. Internal VREG Power Up Sequence

- **For Power Up:**
  1. VDDIO (that is, the 3.3-V rail) should come up with the minimum slew rate specified.
  2. The Internal VREG powers up after the I/O monitors (I/O POR and I/O BOR) are released.
  3. After the times specified by $V_{DDIO-MON-TOT-DELAY}$ and $V_{XRSN-PU-DELAY}$, XRSn will be released and the device starts the boot-up sequence.

     There is an additional delay between XRSn releasing (that is, going high) and the boot-up sequence starting. See Figure 6-7.
  4. The I/O BOR monitor has different release points during power up and power down.
- **For Power Down:**
  1. The only requirement on VDDIO during power down is the slew rate.
  2. The I/O BOR monitor has different release points during power up and power down.
  3. The I/O BOR tripping will cause XRSn to go low after $V_{XRSN-PD-DELAY}$ and also power down the Internal VREG.

Note

The *All Monitors Release Signal* is an internal signal.

Note

If there is an external circuit driving XRSn (for example, a supervisor), the boot-up sequence does not start until the XRSn pin is released by all internal and external sources.

6.11.1.4.3.2 Supply Sequencing Summary and Effects of Violations

The acceptable power-up sequence for the rails is summarized below. "Power up" here means the rail in question has reached the minimum recommended operating voltage.

CAUTION

Non-acceptable sequences leads to reliability concerns and possibly damage.

For simplicity, connecting all 3.3-V rails together and following the descriptions in Supply Pins Power Sequence is recommended.

Table 6-1. Internal VREG Sequence Summary

CASE	RAILS POWER-UP ORDER		ACCEPTABLE
	VDDIO	VDDA	
A	1	2	Yes
B	2	1	-
C	1	1	Yes

Note

The analog modules on the device should only be powered after VDDA has reached the minimum recommended operating voltage.

6.11.1.4.3.3 Supply Slew Rate

VDDIO has a minimum slew rate requirement. If the minimum slew rate is not met, XRSn might toggle a few times until VDDIO crosses the I/O BOR region.

Note

The toggling on XRSn has no adverse effect on the device as boot only starts once XRSn is steadily high. However if XRSn from the device is used to gate the reset signal of other ICs, then the slew rate requirement should be met to prevent this toggling.

6.11.1.5 Power Management Module Electrical Data and Timing

6.11.1.5.1 Power Management Module Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VREG}	Internal Voltage Regulator Output		1.14	1.2	1.32	V
$V_{VREG\text{-}PU}$	Internal Voltage Regulator Power Up Time				350	µs
$V_{VREG\text{-}INRUSH}$ (5)	Internal Voltage Regulator Inrush Current			650		mA
$V_{POR\text{-}VDDIO}$	VDDIO Power on Reset Voltage	Before and After XRSn Release		2.3		V
$V_{BOR\text{-}VDDIO\text{-}UP}$ (1)	VDDIO Brown Out Reset Voltage on Ramp Up	Before XRSn Release		2.7		V
$V_{BOR\text{-}VDDIO\text{-}DN}$ (1)	VDDIO Brown Out Reset Voltage on Ramp Down	After XRSn Release	2.81		3.0	V
$V_{XRSn\text{-}PU\text{-}DELAY}$ (2)	XRSn Release Delay after Supplies are Ramped Up During Power Up	This is the final delay		40		µs
$V_{XRSn\text{-}PD\text{-}DELAY}$ (3)	XRSn Trip Delay after Supplies are Ramped Down During Power Down			2		µs
$V_{DDIO\text{-}MON\text{-}TOT\text{-}DELAY}$	Total Delays in Path of VDDIO Monitors (POR, BOR)			145		µs
$V_{XRSn\text{-}MON\text{-}RELEASE\text{-}DELAY}$	XRSn Release Delay after a VDDIO BOR	Supplies Within Operating Range		140		µs
	XRSn Release Delay after a VDDIO POR Event			185		µs

(1) See the *Supply Voltages* figure.
(2) Supplies are considered fully ramped up after they cross the minimum recommended operating conditions for the respective rail. All POR and BOR monitors need to be released before this delay takes effect. RC network delay will add to this.
(3) On power down, any of the POR or BOR monitors that trips will immediately trip XRSn. This delay is the time between any of the POR, BOR monitors tripping and XRSn going low. It is variable and depends on the ramp down rate of the supply. RC network delay will add to this.
(4) This is the transient current drawn on the VDDIO rail when the internal VREG turns on. Due to this, there might be some voltage drops on the VDDIO rail when the VREG turns on which could cause the VREG to ramp up in steps. There is no detriment to the device from this but the effect can be reduced if desired by using sufficient decoupling capacitors on VDDIO or picking an LDO/DC-DC that can supply this transient current.

6.11.1.5.2 Power Management Module Operating Conditions

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General						
C_{VDDIO} [1] [2]	VDDIO Capacitance Per Pin[6]		0.1			µF
C_{VDDA} [1] [2]	VDDA Capacitance Per Pin[6]		2.2			µF
$SR_{VDDIO-UP}$ [3]	Supply Ramp Up Rate of 3.3V Rail (VDDIO)		8		100	mV/µs
$SR_{VDDIO-DN}$ [3]	Supply Ramp Down Rate of 3.3V Rail (VDDIO)		20		100	mV/µs
$V_{BOR-VDDIO-GB}$ [5]	VDDIO Brown Out Reset Voltage Guardband			0.1		V
Internal VREG						
C_{VDD} TOTAL[4]	Total Nominal VDD Capacitance[6]		10		22	µF

(1) The exact value of the decoupling capacitance depends on the system voltage regulation solution that is supplying these pins.
(2) It is recommended to tie the 3.3V rails (VDDIO, VDDA) together and supply them from a single source.
(3) See the *Supply Slew Rate* section. Supply ramp rate faster than the maximum can trigger the on-chip ESD protection.
(4) See the *Power Management Module (PMM)* section on possible configurations for the total decoupling capacitance.
(5) TI recommends $V_{BOR-VDDIO-GB}$ to avoid BOR-VDDIO resets due to normal supply noise or load-transient events on the 3.3-V VDDIO system regulator. Good system regulator design and decoupling capacitance (following the system regulator specifications) are important to prevent activation of the BOR-VDDIO during normal device operation. The value of $V_{BOR-VDDIO-GB}$ is a system-level design consideration; the voltage listed here is typical for many applications.
(6) Max capacitor tolerance should be 20%.

6.11.2 Reset Timing

XRSn is the device reset pin. It functions as an input and open-drain output. The device has a built-in power-on reset (POR). During power up, the POR circuit drives the XRSn pin low. A watchdog or NMI watchdog reset will also drive the pin low. An external open-drain circuit may drive the pin to assert a device reset.

A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between XRSn and VDDIO. A capacitor should be placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Figure 6-10 shows the recommended reset circuit.

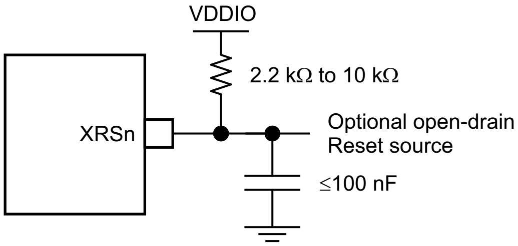


Figure 6-10. Reset Circuit

6.11.2.1 Reset Sources

Table 6-2 summarizes the various reset signals and their effect on the device.

Table 6-2. Reset Signals

RESET SOURCE	CPU CORE RESET (C28x, FPU, VCU)	PERIPHERALS RESET	JTAG/ DEBUG LOGIC RESET	I/Os	XRSn OUTPUT
POR	Yes	Yes	Yes	Hi-Z	Yes
XRSn Pin	Yes	Yes	No	Hi-Z	–
WDRS	Yes	Yes	No	Hi-Z	Yes
NMIWDRS	Yes	Yes	No	Hi-Z	Yes
SYSRS (Debugger Reset)	Yes	Yes	No	Hi-Z	No
SCCRESET	Yes	Yes	No	Hi-Z	No

The parameter $t_{h(boot\text{-}mode)}$ must account for a reset initiated from any of these sources.

See the Resets section of the System Control chapter in the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.

CAUTION

Some reset sources are internally driven by the device. Some of these sources will drive XRSn low, use this to disable any other devices driving the boot pins. The SCCRESET and debugger reset sources do not drive XRSn; therefore, the pins used for boot mode should not be actively driven by other devices in the system. The boot configuration has a provision for changing the boot pins in OTP; for more details, see the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.

6.11.2.2 Reset Electrical Data and Timing

Section 6.11.2.2.1 lists the reset (XRSn) timing requirements. Section 6.11.2.2.2 lists the reset (XRSn) switching characteristics. Figure 6-11 shows the power-on reset. Figure 6-12 shows the warm reset.

6.11.2.2.1 Reset (XRSn) Timing Requirements

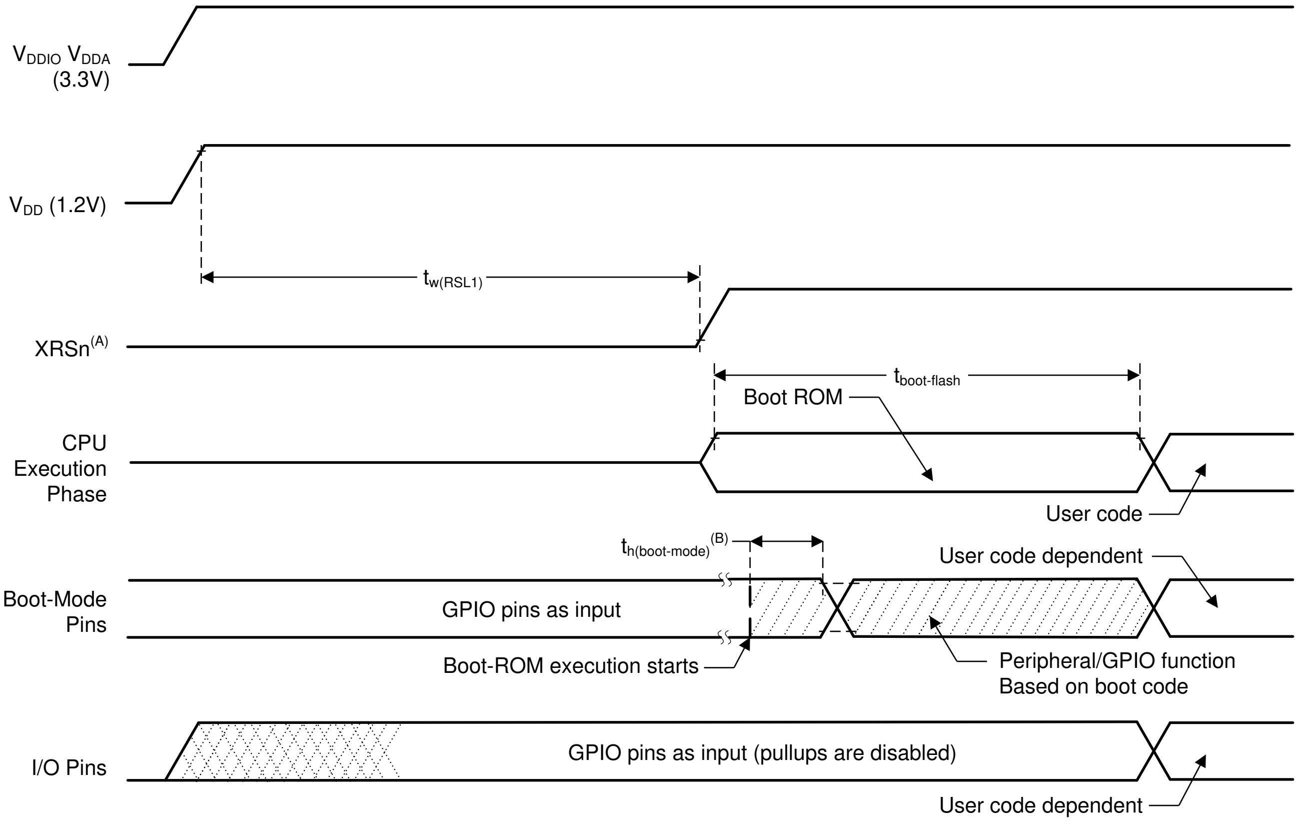
			MIN	MAX	UNIT
$t_{h(boot\text{-}mode)}$	Hold time for boot-mode pins		1.5		ms
$t_{w(RSL2)}$	Pulse duration, XRSn low on warm reset	All cases	3.2		μs
		Low-power modes used in application and SYSCLKDIV > 16	3.2 * (SYSCLKDIV/16)		

6.11.2.2.2 Reset (XRSn) Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, XRSn driven low by device after supplies are stable		100		μs
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog		$512t_{c(OSCCLK)}$		cycles
$t_{boot\text{-}flash}$	Boot-ROM execution time to first instruction fetch in flash			900	μs

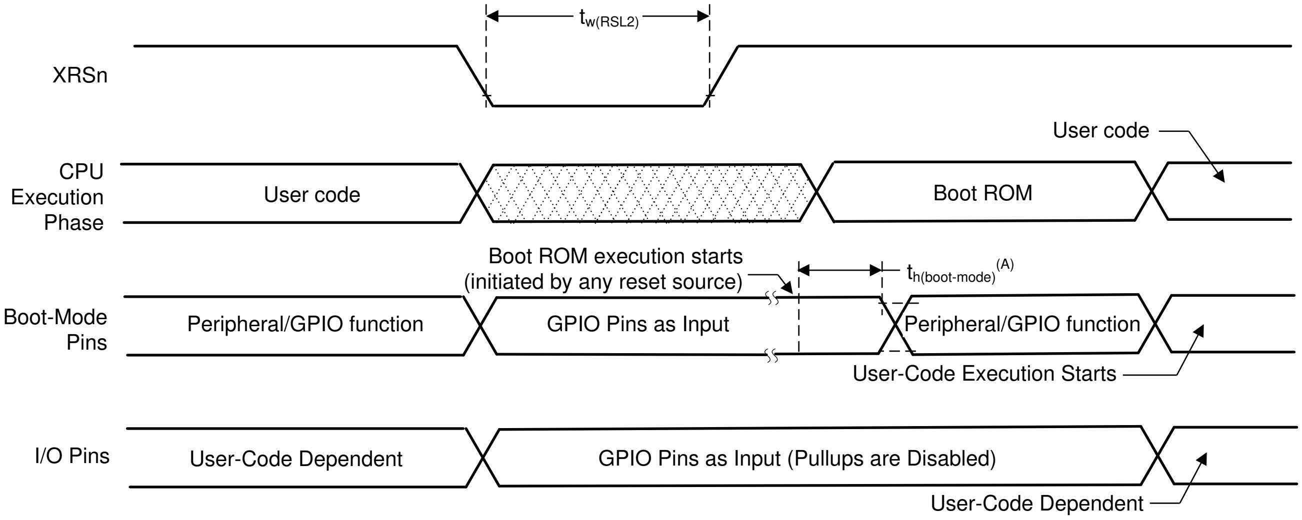
6.11.2.2.3 Reset Timing Diagrams



A. The XRSn pin can be driven externally by a supervisor or an external pullup resistor, see Table 5-1. On-chip POR logic will hold this pin low until the supplies are in a valid range.

B. After reset from any source (see Section 6.11.2.1), the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-11. Power-on Reset



A. After reset from any source (see Section 6.11.2.1), the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-12. Warm Reset

6.11.3 Clock Specifications

6.11.3.1 Clock Sources

Table 6-3 lists clock sources. Figure 6-13 shows the clocking system. Figure 6-14 shows the PLL.

Table 6-3. Possible Reference Clock Sources

CLOCK SOURCE	DESCRIPTION
INTOSC1	Internal oscillator 1. Zero-pin overhead 10-MHz internal oscillator.
INTOSC2(1)	Internal oscillator 2. Zero-pin overhead 10-MHz internal oscillator.
X1 (XTAL)	External crystal or resonator connected between the X1 and X2 pins or single-ended clock connected to the X1 pin.

(1) On reset, internal oscillator 2 (INTOSC2) is the default clock source for the PLL (OSCCLK).

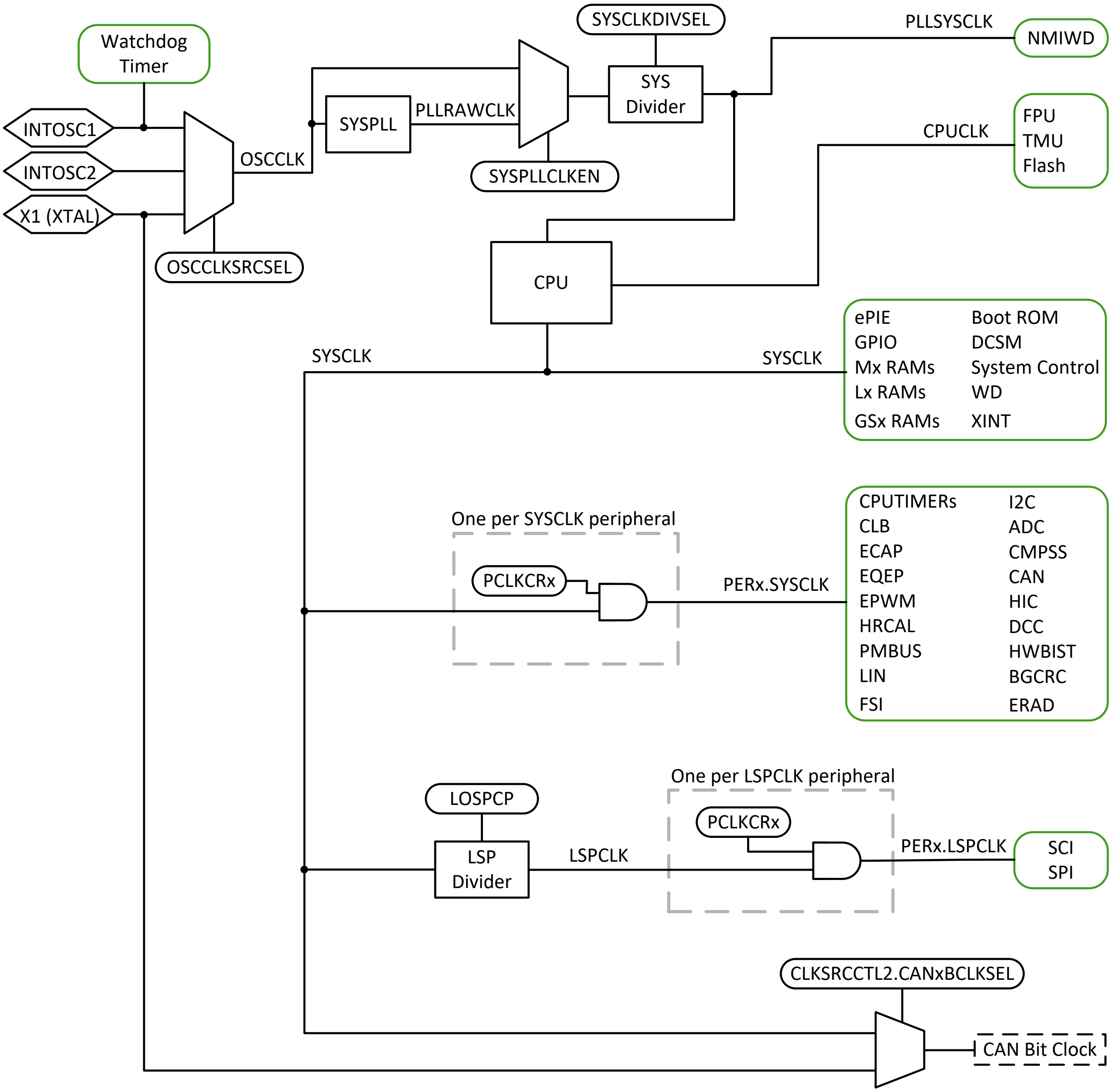


Figure 6-13. Clocking System

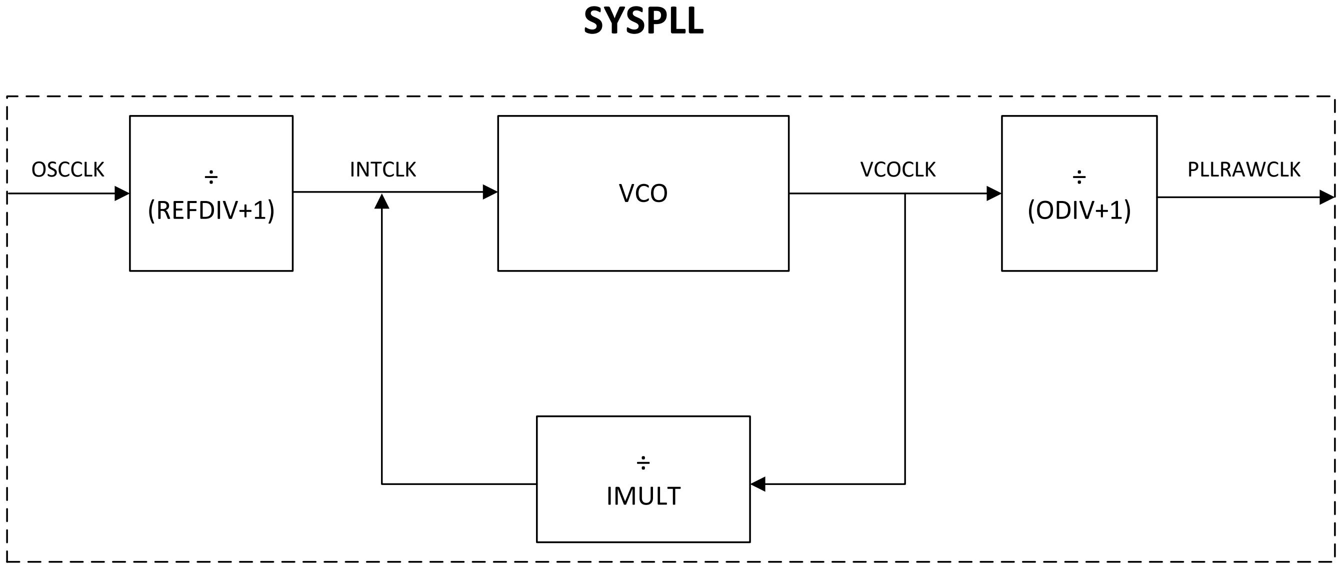


Figure 6-14. System PLL

In Figure 6-14,

$$f_{PLLRAWCLK} = \frac{f_{OSCCLK}}{(REFDIV + 1)} \times \frac{IMULT}{(ODIV + 1)}$$

6.11.3.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks, PLL lock times, frequencies of the internal clocks, and the frequency and switching characteristics of the output clock.

6.11.3.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times

Section 6.11.3.2.1.1 lists the frequency requirements for the input clocks. Section 6.11.3.2.1.2 lists the XTAL oscillator characteristics. Section 6.11.3.2.1.3 lists the X1 timing requirements. Section 6.11.3.2.1.4 lists the APLL characteristics. Section 6.11.3.2.1.5 lists the switching characteristics of the output clock, XCLKOUT. Section 6.11.3.2.1.6 provides the clock frequencies for the internal clocks.

6.11.3.2.1.1 Input Clock Frequency

		MIN	MAX	UNIT
$f_{(XTAL)}$	Frequency, X1/X2, from external crystal or resonator	10	20	MHz
$f_{(X1)}$	Frequency, X1, from external oscillator	10	25	MHz

6.11.3.2.1.2 XTAL Oscillator Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
X1 V_{IL}	Valid low-level input voltage	–0.3		0.3 * VDDIO	V
X1 V_{IH}	Valid high-level input voltage	0.7 * VDDIO		VDDIO + 0.3	V

6.11.3.2.1.3 X1 Timing Requirements

		MIN	MAX	UNIT
$t_{f(X1)}$	Fall time, X1		6	ns
$t_{r(X1)}$	Rise time, X1		6	ns
$t_{w(X1L)}$	Pulse duration, X1 low as a percentage of $t_{c(X1)}$	45%	55%	
$t_{w(X1H)}$	Pulse duration, X1 high as a percentage of $t_{c(X1)}$	45%	55%	

6.11.3.2.1.4 APLL Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
PLL Lock time				
SYS PLL Lock Time(1)			5µs + (1024 * (REFDIV + 1) * $t_{c(OSCCLK)}$)	us

(1) The PLL lock time here defines the typical time that takes for the PLL to lock once PLL is enabled (SYSPLLCTL1[PLLENA]=1). Additional time to verify the PLL clock using Dual Clock Comparator (DCC) is not accounted here. TI recommends using the latest example software from C2000Ware for initializing the PLLs. For the system PLL, see InitSysPll() or SysCtl_setClock().

6.11.3.2.1.5 XCLKOUT Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER(1)		MIN	MAX	UNIT
$t_{f(XCO)}$	Fall time, XCLKOUT		5	ns
$t_{r(XCO)}$	Rise time, XCLKOUT		5	ns
$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2(2)	H + 2(2)	ns
$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2(2)	H + 2(2)	ns
$f_{(XCO)}$	Frequency, XCLKOUT		50	MHz

(1) A load of 40 pF is assumed for these parameters.
(2) $H = 0.5t_{c(XCO)}$

6.11.3.2.1.6 Internal Clock Frequencies

		MIN	NOM	MAX	UNIT
$f_{(SYSCLK)}$	Frequency, device (system) clock	2		100	MHz
$t_{c(SYSCLK)}$	Period, device (system) clock	10		500	ns
$f_{(INTCLK)}$	Frequency, system PLL going into VCO (after REFDIV)	2		20	MHz
$f_{(VCOCLK)}$	Frequency, system PLL VCO (before ODIV)	220		600	MHz
$f_{(PLLRAWCLK)}$	Frequency, system PLL output (before SYSCLK divider)	6		200	MHz
$f_{(PLL)}$	Frequency, PLLSYSCLK	2		100	MHz
$f_{(PLL\_LIMP)}$	Frequency, PLL Limp Frequency (1)		45/(ODIV+1)		MHz
$f_{(LSP)}$	Frequency, LSPCLK	2		100	MHz
$t_{c(LSPCLK)}$	Period, LSPCLK	10		500	ns
$f_{(OSCCLK)}$	Frequency, OSCCLK (INTOSC1 or INTOSC2 or XTAL or X1)		See respective clock		MHz
$f_{(EPWM)}$	Frequency, EPWMCLK			100	MHz
$f_{(HRPWM)}$	Frequency, HRPWMCLK	60		100	MHz

(1) PLL output frequency when OSCCLK is dead (Loss of OSCCLK causes PLL to Limp).

6.11.3.3 Input Clocks and PLLs

In addition to the internal 0-pin oscillators, three types of external clock sources are supported:

- A single-ended 3.3-V external clock. The clock signal should be connected to X1, as shown in Figure 6-15, with the XTALCR.SE bit set to 1.
- An external crystal. The crystal should be connected across X1 and X2 with its load capacitors connected to VSS as shown in Figure 6-16.
- An external resonator. The resonator should be connected across X1 and X2 with its ground connected to VSS as shown in Figure 6-17.

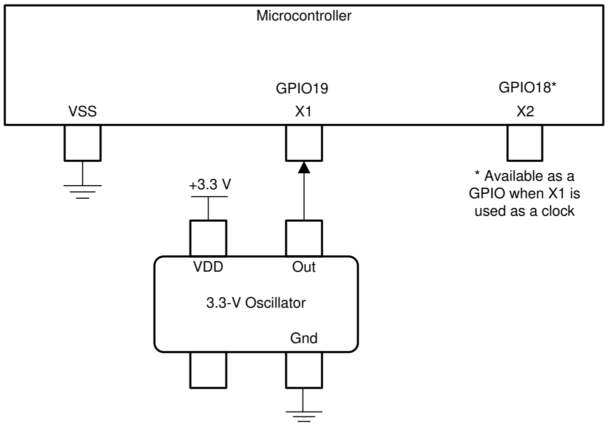


Figure 6-15. Single-ended 3.3-V External Clock

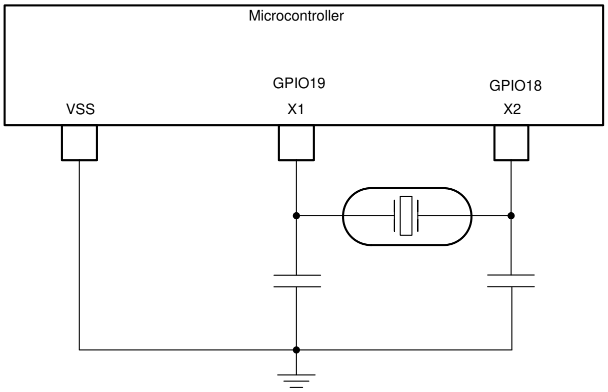


Figure 6-16. External Crystal

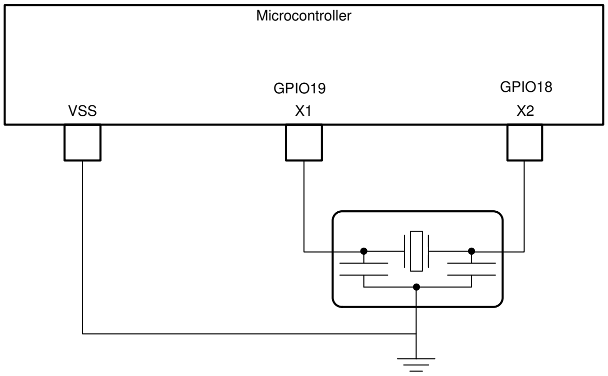


Figure 6-17. External Resonator

6.11.3.4 XTAL Oscillator

6.11.3.4.1 Introduction

The crystal oscillator in this device is an embedded electrical oscillator that, when paired with a compatible quartz crystal (or a ceramic resonator), can generate the system clock required by the device.

6.11.3.4.2 Overview

The following sections describe the components of the electrical oscillator and crystal.

6.11.3.4.2.1 Electrical Oscillator

The electrical oscillator in this device is a Pierce oscillator. It is a positive feedback inverter circuit that requires a tuning circuit in order to oscillate. When this oscillator is paired with a compatible crystal, a tank circuit is formed. This tank circuit oscillates at the fundamental frequency of the crystal. On this device, the oscillator is designed to operate in parallel resonance mode due to the shunt capacitor (C0) and required load capacitors (CL). Figure 6-18 illustrates the components of the electrical oscillator and the tank circuit.

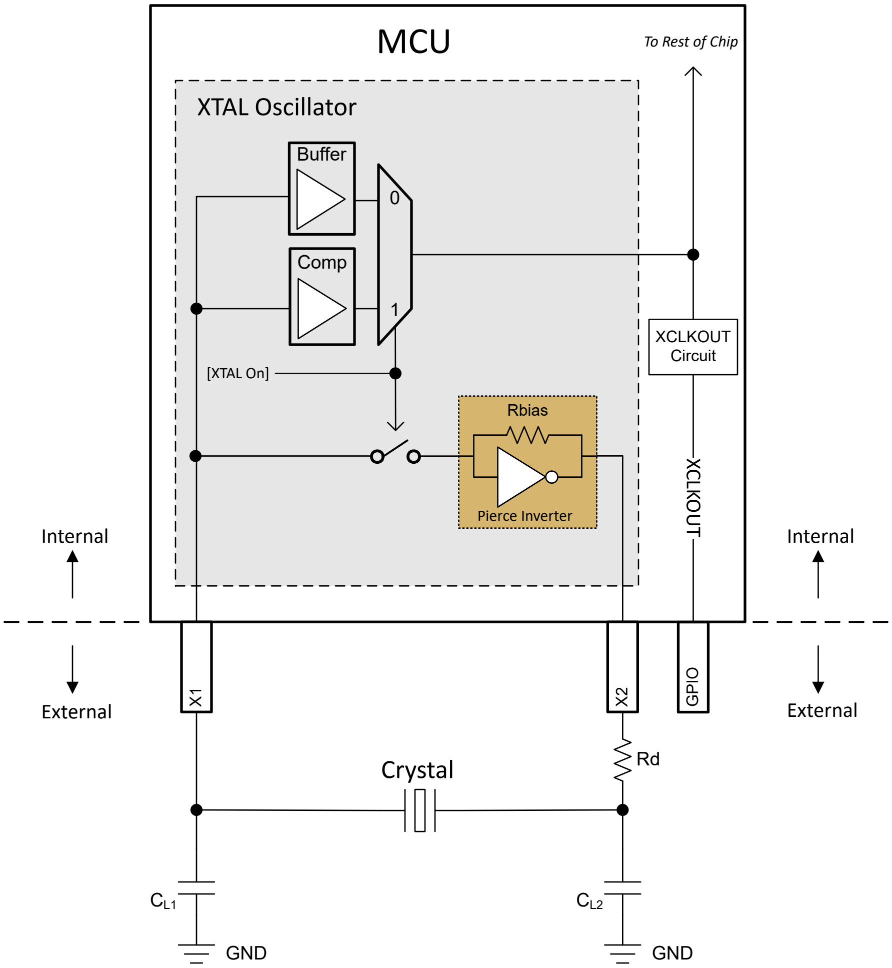


Figure 6-18. Electrical Oscillator Block Diagram

6.11.3.4.2.1.1 Modes of Operation

The electrical oscillator in this device has two modes of operation: crystal mode and single-ended mode.

6.11.3.4.2.1.1.1 Crystal Mode of Operation

In the crystal mode of operation, a quartz crystal with load capacitors has to be connected to X1 and X2.

This mode of operation is engaged when [XTAL On] = 1, which is achieved by setting XTALCR.OSCOFF = 0 and XTALCR.SE = 0. There is an internal bias resistor for the feedback loop so an external one should not be used. Adding an external bias resistor will create a parallel resistance with the internal Rbias, moving the bias point of operation and possibly leading to clipped waveforms, out-of-specification duty cycle, and reduction in the effective negative resistance.

In this mode of operation, the resultant clock on X1 is passed through a comparator (Comp) to the rest of the chip. The clock on X1 needs to meet the VIH and VIL of the comparator. See the *XTAL Oscillator Characteristics* table for the VIH and VIL requirements of the comparator.

6.11.3.4.2.1.1.2 Single-Ended Mode of Operation

In the single-ended mode of operation, a clock signal is connected to X1 with X2 left unconnected. A quartz crystal should not be used in this mode.

This mode is enabled when [XTAL On] = 0, which can be achieved by setting XTALCR.OSCOFF = 1 and XTALCR.SE = 1.

In this mode of operation, the clock on X1 is passed through a buffer (Buffer) to the rest of the chip. See the *X1 Input Level Characteristics When Using an External Clock Source (Not a Crystal)* table for the input requirements of the buffer.

6.11.3.4.2.1.2 XTAL Output on XCLKOUT

The output of the electrical oscillator that is fed to the rest of the chip can be brought out on XCLKOUT for observation by configuring the CLKSRCCTL3.XCLKOUTSEL and XCLKOUTDIVSEL.XCLKOUTDIV registers. See the *GPIO Muxed Pins* table for a list of GPIOs that XCLKOUT comes out on.

6.11.3.4.2.2 Quartz Crystal

Electrically, a quartz crystal can be represented by an LCR (Inductor-Capacitor-Resistor) circuit. However, unlike an LCR circuit, crystals have very high Q due to the low motional resistance and are also very underdamped. Components of the crystal are shown in Figure 6-19 and explained below.

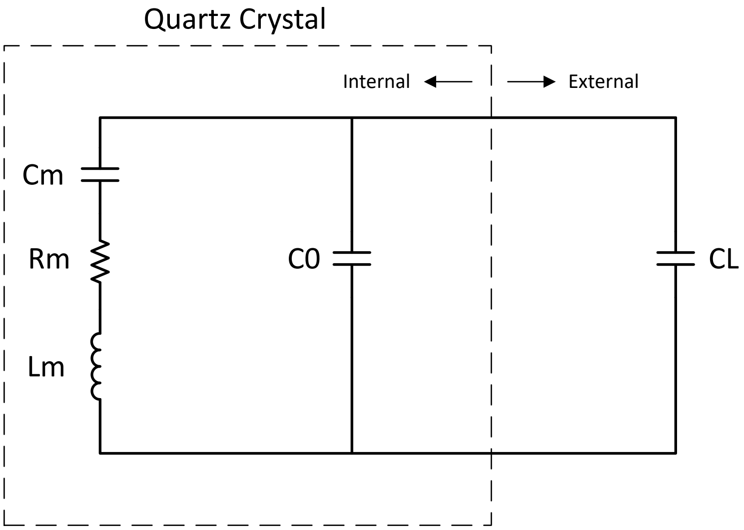


Figure 6-19. Crystal Electrical Representation

Cm (Motional capacitance): Denotes the elasticity of the crystal.

Rm (Motional resistance): Denotes the resistive losses within the crystal. This is not the ESR of the crystal but can be approximated as such depending on the values of the other crystal components.

Lm (Motional inductance): Denotes the vibrating mass of the crystal.

C0 (Shunt capacitance): The capacitance formed from the two crystal electrodes and stray package capacitance.

CL (Load capacitance): This is the effective capacitance seen by the crystal at its electrodes. It is external to the crystal. The frequency ppm specified in the crystal data sheet is usually tied to the CL parameter.

Note that most crystal manufacturers specify CL as the effective capacitance seen at the crystal pins, while some crystal manufacturers specify CL as the capacitance on just one of the crystal pins. Check with the crystal manufacturer for how the CL is specified in order to use the correct values in calculations.

From Figure 6-18, CL1 and CL2 are in series; so, to find the equivalent total capacitance seen by the crystal, the capacitance series formula has to be applied which simply evaluates to [CL1]/2 if CL1 = CL2.

It is recommended that a stray PCB capacitance be added to this value. 3 pF to 5 pF are reasonable estimates, but the actual value will depend on the PCB in question.

Note that the load capacitance is a requirement of both the electrical oscillator and crystal. The value chosen has to satisfy both the electrical oscillator and the crystal.

The effect of CL on the crystal is frequency-pulling. If the effective load capacitance is lower than the target, the crystal frequency will increase and vice versa. However, the effect of frequency-pulling is usually very minimal and typically results in less than 10-ppm variation from the nominal frequency.

6.11.3.4.2.3 GPIO Modes of Operation

Refer to the *External Oscillator (XTAL)* section of the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.

6.11.3.4.3 Functional Operation

6.11.3.4.3.1 ESR – Effective Series Resistance

Effective Series Resistance is the resistive load the crystal presents to the electrical oscillator at resonance. The higher the ESR, the lower the Q, and less likely the crystal will start up or maintain oscillation. The relationship between ESR and the crystal components is indicated below.

$$ESR = Rm * \left(1 + \frac{C0}{CL}\right)^2 \tag{1}$$

Note that ESR is not the same as motional resistance of the crystal, but can be approximated as such if the effective load capacitance is much greater than the shunt capacitance.

6.11.3.4.3.2 Rneg – Negative Resistance

Negative resistance is the impedance presented by the electrical oscillator to the crystal. It is the amount of energy the electrical oscillator must supply to the crystal to overcome the losses incurred during oscillation. Rneg depicts a circuit that provides rather than consume energy and can also be viewed as the overall gain of the circuit.

The generally accepted practice is to have Rneg > 3x ESR to 5x ESR to ensure the crystal starts up under all conditions. Note that it takes slightly more energy to start up the crystal than it does to sustain oscillation; therefore, if it can be ensured that the negative resistance requirement is met at start-up, then oscillation sustenance will not be an issue.

Figure 6-20 and Figure 6-21 show the variation between negative resistance and the crystal components for this device. As can be seen from the graphs, the crystal shunt capacitance (C0) and effective load capacitance (CL) greatly influence the negative resistance of the electrical oscillator. Note that these are typical graphs; so, refer to Table 6-4 for minimum and maximum values for design considerations.

6.11.3.4.3.3 Start-up Time

Start-up time is an important consideration when selecting the components of the crystal circuit. As mentioned in the Rneg – Negative Resistance section, for reliable start-up across all conditions, it is recommended that the Rneg > 3x ESR to 5x ESR of the crystal.

Crystal ESR and the dampening resistor (Rd) greatly affect the start-up time. The higher the two values, the longer the crystal takes to start up. Longer start-up times are usually a sign that the crystal and components are not a correct match.

Refer to Crystal Oscillator Specifications for the typical start-up times. Note that the numbers specified here are typical numbers provided for guidance only. Actual start-up time depends heavily on the crystal in question and the external components.

6.11.3.4.3.4 DL – Drive Level

Drive level refers to how much power is provided by the electrical oscillator and dissipated by the crystal. The maximum drive level specified in the crystal manufacturer’s data sheet is usually the maximum the crystal can dissipate without damage or significant reduction in operating life. On the other hand, the drive level specified by the electrical oscillator is the maximum power it can provide. The actual power provided by the electrical oscillator is not necessarily the maximum power and depends on the crystal and board components.

For cases where the actual drive level from the electrical oscillator exceeds the maximum drive level specification of the crystal, a dampening resistor (Rd) should be installed to limit the current and reduce the power dissipated by the crystal. Note that Rd reduces the circuit gain; and therefore, the actual value to use should be evaluated to make sure all other conditions for start-up and sustained oscillation are met.

6.11.3.4.4 How to Choose a Crystal

Using Crystal Oscillator Specifications as a reference:

1. Pick a crystal frequency (for example, 20 MHz).
2. Check that the ESR of the crystal <=50 Ω per specifications for 20 MHz.
3. Check that the load capacitance requirement of the crystal manufacturer is within 6 pF and 12 pF per specifications for 20 MHz.
    - As mentioned, CL1 and CL2 are in series; so, provided CL1 = CL2, effective load capacitance CL = [CL1]/2.
    - Adding board parasitics to this results in CL = [CL1]/2 + Cstray
4. Check that the maximum drive level of the crystal >= 1 mW. If this requirement is not met, a dampening resistor Rd can be used. Refer to DL – Drive Level on other points to consider when using Rd.

6.11.3.4.5 Testing

It is recommended that the user have the crystal manufacturer completely characterize the crystal with their board to ensure the crystal always starts up and maintains oscillation.

Below is a brief overview of some measurements that can be performed:

Due to how sensitive the crystal circuit is to capacitance, it is recommended that scope probes not be connected to X1 and X2. If scope probes must be used to monitor X1/X2, an active probe with less than 1-pF input capacitance should be used.

Frequency

1. Bring out the XTAL on XCLKOUT.
2. Measure this frequency as the crystal frequency.

Negative Resistance

1. Bring out the XTAL on XCLKOUT.
2. Place a potentiometer in series with the crystal between the load capacitors.
3. Increase the resistance of the potentiometer until the clock on XCLKOUT stops.
4. This resistance plus the crystal’s actual ESR is the negative resistance of the electrical oscillator.

Start-Up Time

1. Turn off the XTAL.
2. Bring out the XTAL on XCLKOUT.
3. Turn on the XTAL and measure how long it takes the clock on XCLKOUT to stay within 45% and 55% duty cycle.

6.11.3.4.6 Common Problems and Debug Tips

Crystal Fails to Start Up

- Go through the How to Choose a Crystal section and make sure there are no violations.

Crystal Takes a Long Time to Start Up

- If a dampening resistor Rd is installed, it is too high.
- If no dampening resistor is installed, either the crystal ESR is too high or the overall circuit gain is too low due to high load capacitance.

6.11.3.4.7 Crystal Oscillator Specifications

6.11.3.4.7.1 Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time(1)	f = 10 MHz	ESR MAX = 110 Ω CL1 = CL2 = 24 pF C0 = 7 pF			4	ms
	f = 20 MHz	ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF			2	ms
Crystal drive level (DL)					1	mW

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

6.11.3.4.7.2 Crystal Equivalent Series Resistance (ESR) Requirements

For the Crystal Equivalent Series Resistance (ESR) Requirements table:

1. Crystal shunt capacitance (C0) should be less than or equal to 7 pF.
2. ESR = Negative Resistance/3

Table 6-4. Crystal Equivalent Series Resistance (ESR) Requirements

CRYSTAL FREQUENCY (MHz)	MAXIMUM ESR (Ω) (CL1 = CL2 = 12 pF)	MAXIMUM ESR (Ω) (CL1 = CL2 = 24 pF)
10	55	110
12	50	95
14	50	90
16	45	75
18	45	65
20	45	50

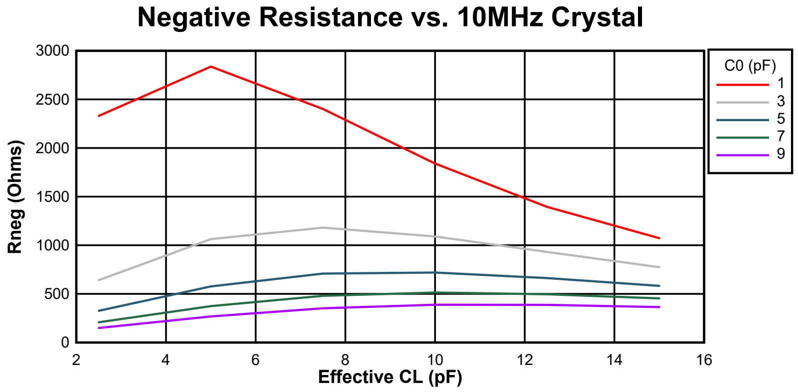


Figure 6-20. Negative Resistance Variation at 10 MHz

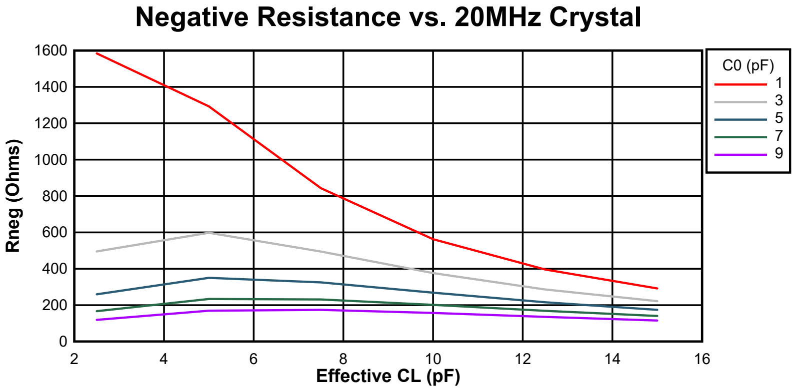


Figure 6-21. Negative Resistance Variation at 20 MHz

6.11.3.5 Internal Oscillators

To reduce production board costs and application development time, all F28002x devices contain two independent internal oscillators, referred to as INTOSC1 and INTOSC2. By default, INTOSC2 is set as the source for the system reference clock (OSCCLK) and INTOSC1 is set as the backup clock source.

Applications requiring tighter clock tolerance can use the SCI baud tuning example available in C2000Ware (C2000Ware_3_03_00_00\driverlib\f28002x\examples\sci\baud_tune_via_uart) to enable baud matching better than 1% accuracy.

Section 6.11.3.5.1 provides the electrical characteristics of the internal oscillators.

6.11.3.5.1 INTOSC Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{INTOSC}	Frequency, INTOSC1 and INTOSC2	-40°C to 125°C	9.84 (–1.6%)	10	10.14 (1.4%)	MHz
		-30°C to 90°C	9.88 (–1.2%)			
		-10°C to 85°C	9.91 (–0.9%)			
		-10°C to 70°C	9.93 (–0.7%)			
$f_{INTOSC-STABILITY}$	Frequency stability	30°C, Nominal VDDIO		±0.1		%
$t_{INT0SC-ST}$	Start-up and settling time				20	µs

6.11.4 Flash Parameters

Table 6-5 lists the minimum required Flash wait states with different clock sources and frequencies. Wait state is the value set in register FRDCNTL[RWAIT].

Table 6-5. Minimum Required Flash Wait States with Different Clock Sources and Frequencies

CPUCLK (MHz)	EXTERNAL OSCILLATOR OR CRYSTAL		INTOSC1 OR INTOSC2	
	NORMAL OPERATION	BANK OR PUMP SLEEP[1]	NORMAL OPERATION	BANK OR PUMP SLEEP[1]
97 < CPUCLK ≤ 100	4		4	5
80 < CPUCLK ≤ 97				4
77 < CPUCLK ≤ 80	3		3	4
60 < CPUCLK ≤ 77				3
58 < CPUCLK ≤ 60	2		2	3
40 < CPUCLK ≤ 58				2
38 < CPUCLK ≤ 40	1		1	2
20 < CPUCLK ≤ 38				1
19 < CPUCLK ≤ 20	0		0	1
CPUCLK ≤ 19				0

(1) Flash SLEEP operations require an extra wait state when using INTOSC as the clock source for the frequency ranges indicated. Any wait state FRDCNTL[RWAIT] change must be made before beginning a SLEEP mode operation. This setting impacts both flash banks.

The F28002x devices have an improved 128-bit prefetch buffer that provides high flash code execution efficiency across wait states. Figure 6-22 and Figure 6-23 illustrate typical efficiency across wait-state settings compared to previous-generation devices with a 64-bit prefetch buffer. Wait-state execution efficiency with a prefetch buffer will depend on how many branches are present in application software. Two examples of linear code and if-then-else code are provided.

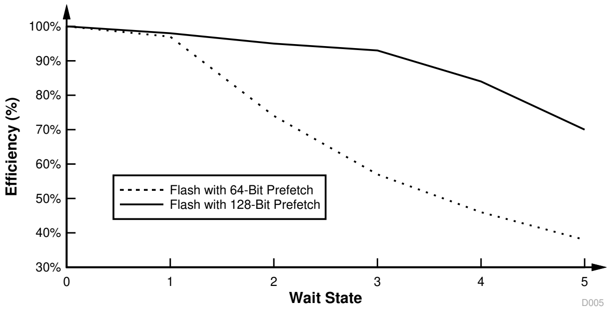


Figure 6-22. Application Code With Heavy 32-Bit Floating-Point Math Instructions

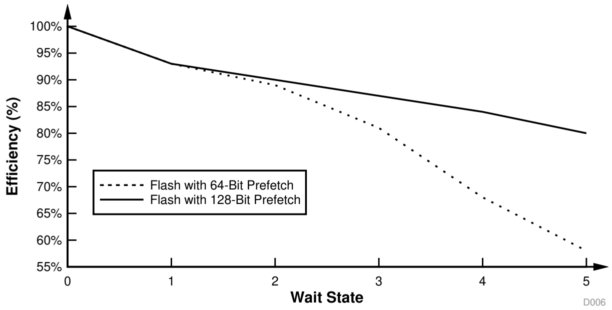


Figure 6-23. Application Code With 16-Bit If-Else Instructions

Table 6-6 lists the Flash parameters.

Table 6-6. Flash Parameters

PARAMETER		MIN	TYP	MAX	UNIT
Program Time(1)	128 data bits + 16 ECC bits		150	300	µs
	8KB sector		50	100	ms
Erase Time(2) (3) at < 25 cycles	8KB sector		15	56	ms
Erase Time(2) (3) at 1000 cycles	8KB sector		25	133	ms
Erase Time(2) (3) at 2000 cycles	8KB sector		30	226	ms
Erase Time(2) (3) at 20K cycles	8KB sector		120	1026	ms
N_{wec} Write/Erase Cycles per sector				20000	cycles
N_{wec} Write/Erase Cycles for entire Flash (combined all sectors)(4)				100000	cycles
$t_{retention}$ Data retention duration at T_J = 85ºC		20			years

(1) Program time is at the maximum device frequency. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:
- Code that uses flash API to program the flash
- Flash API itself
- Flash data to be programmed

In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. The transfer time will significantly vary depending on the speed of the JTAG debug probe used.
Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. The program time does not degrade with write/erase (W/E) cycling, but the erase time does.
Erase time includes Erase verify by the CPU and does not involve any data transfer.

(2) Erase time includes Erase verify by the CPU.

(3) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required prior to programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.

(4) Each sector, by itself, can only be erased/programmed 20,000 times. If you choose to use a sector (or multiple sectors) like an EEPROM, you can erase/program only those sectors (still limited to 20,000 cycles) without erasing/programming the entire Flash memory. Therefore, the total number of W/E cycles from a device perspective can exceed 20,000 cycles. However, even this number should not exceed 100,000 cycles.

Note

The Main Array flash programming must be aligned to 64-bit address boundaries and each 64-bit word may only be programmed once per write/erase cycle.

The DCSM OTP programming must be aligned to 128-bit address boundaries and each 128-bit word may only be programmed once. The exceptions are:

1. The DCSM Zx-LINKPOINTER1 and Zx-LINKPOINTER2 values in the DCSM OTP should be programmed together, and may be programmed 1 bit at a time as required by the DCSM operation.
2. The DCSM Zx-LINKPOINTER3 values in the DCSM OTP may be programmed 1 bit at a time on a 64-bit boundary to separate it from Zx-PSWDLOCK, which must only be programmed once.

6.11.5 RAM Specifications

RAM TYPE	SIZE	FETCH TIME (Cycles)	READ TIME (Cycles)	STORE TIME (Cycles)	BUS WIDTH	NUMBER OF BUSSES AVAILABLE(1)	NUMBER OF WAIT STATES	BURST ACCESS
GS RAM	4KB	2	2	1	16/32 bits	3	0	No
LS RAM	16KB	2	2	1	16/32 bits	1	0	No
M0	2KB	2	2	1	16/32 bits	1	0	No
M1	2KB	2	2	1	16/32 bits	1	0	No

(1) Number of Busses Available means how many masters (DMA, CPU) have access.

6.11.6 ROM Specifications

ROM TYPE	SIZE	FETCH TIME (Cycles)	READ TIME (Cycles)	STORE TIME (Cycles)	BUS WIDTH	NUMBER OF BUSSES AVAILABLE(1)	NUMBER OF WAIT STATES	BURST ACCESS
Boot ROM	128KB	2	2	1	16/32 bits	1	0	No
Secure ROM	64KB	2	2	1	16/32 bits	1	0	No

(1) Number of Busses Available means how many masters (DMA, CPU) have access.

6.11.7 Emulation/JTAG

The JTAG (IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture) port has four dedicated pins: TMS, TDI, TDO, and TCK. The cJTAG (IEEE Standard 1149.7-2009 for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture) port is a compact JTAG interface requiring only two pins (TMS and TCK), which allows other device functionality to be muxed to the traditional GPIO35 (TDI) and GPIO37 (TDO) pins.

Typically, no buffers are needed on the JTAG signals when the distance between the MCU target and the JTAG header is smaller than 6 inches (15.24 cm), and no other devices are present on the JTAG chain. Otherwise, each signal should be buffered. Additionally, for most JTAG debug probe operations at 10 MHz, no series resistors are needed on the JTAG signals. However, if high emulation speeds are expected (35 MHz or so), 22-Ω resistors should be placed in series on each JTAG signal.

The PD (Power Detect) terminal of the JTAG debug probe header should be connected to the board's 3.3-V supply. Header GND terminals should be connected to board ground. TDIS (Cable Disconnect Sense) should also be connected to board ground. The JTAG clock should be looped from the header TCK output terminal back to the RTCK input terminal of the header (to sense clock continuity by the JTAG debug probe). This MCU does not support the EMU0 and EMU1 signals that are present on 14-pin and 20-pin emulation headers. These signals should always be pulled up at the emulation header through a pair of board pullup resistors ranging from 2.2 kΩ to 4.7 kΩ (depending on the drive strength of the debugger ports). Typically, a 2.2-kΩ value is used.

Header terminal $\overline{\text{RESET}}$ is an open-drain output from the JTAG debug probe header that enables board components to be reset through JTAG debug probe commands (available only through the 20-pin header). Figure 6-24 shows how the 14-pin JTAG header connects to the MCU's JTAG port signals. Figure 6-25 shows how to connect to the 20-pin JTAG header. The 20-pin JTAG header terminals EMU2, EMU3, and EMU4 are not used and should be grounded.

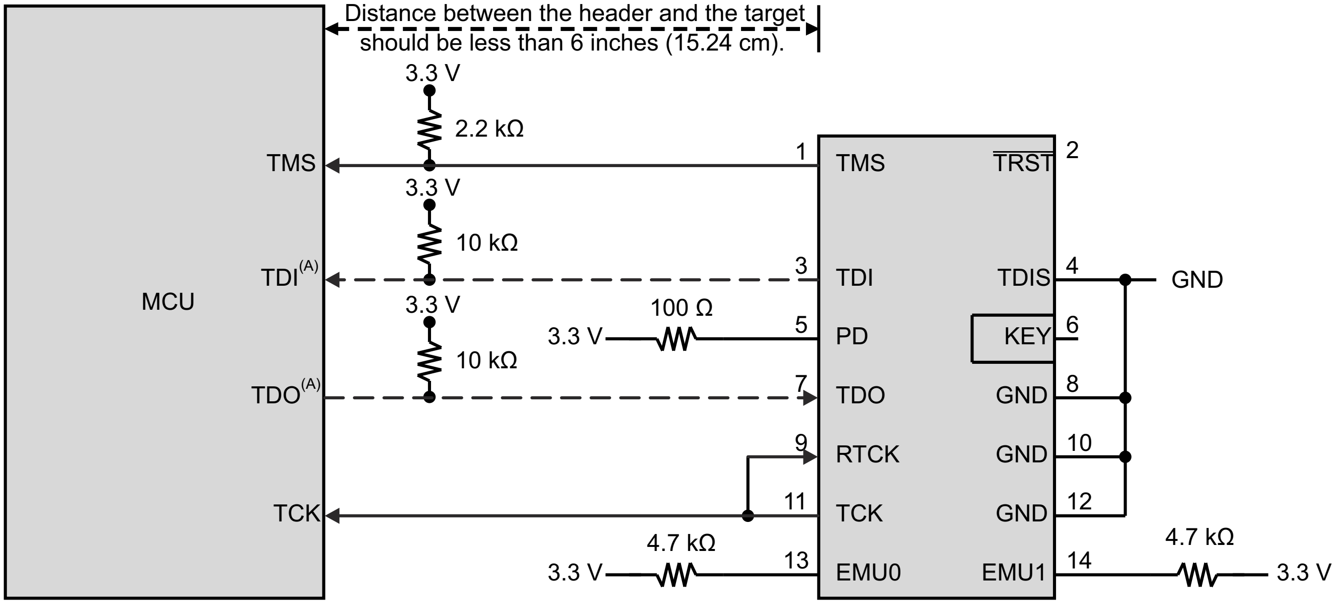
For more information about hardware breakpoints and watchpoints, see Hardware Breakpoints and Watchpoints for C28x in CCS.

For more information about JTAG emulation, see the *XDS Target Connection Guide*.

Note

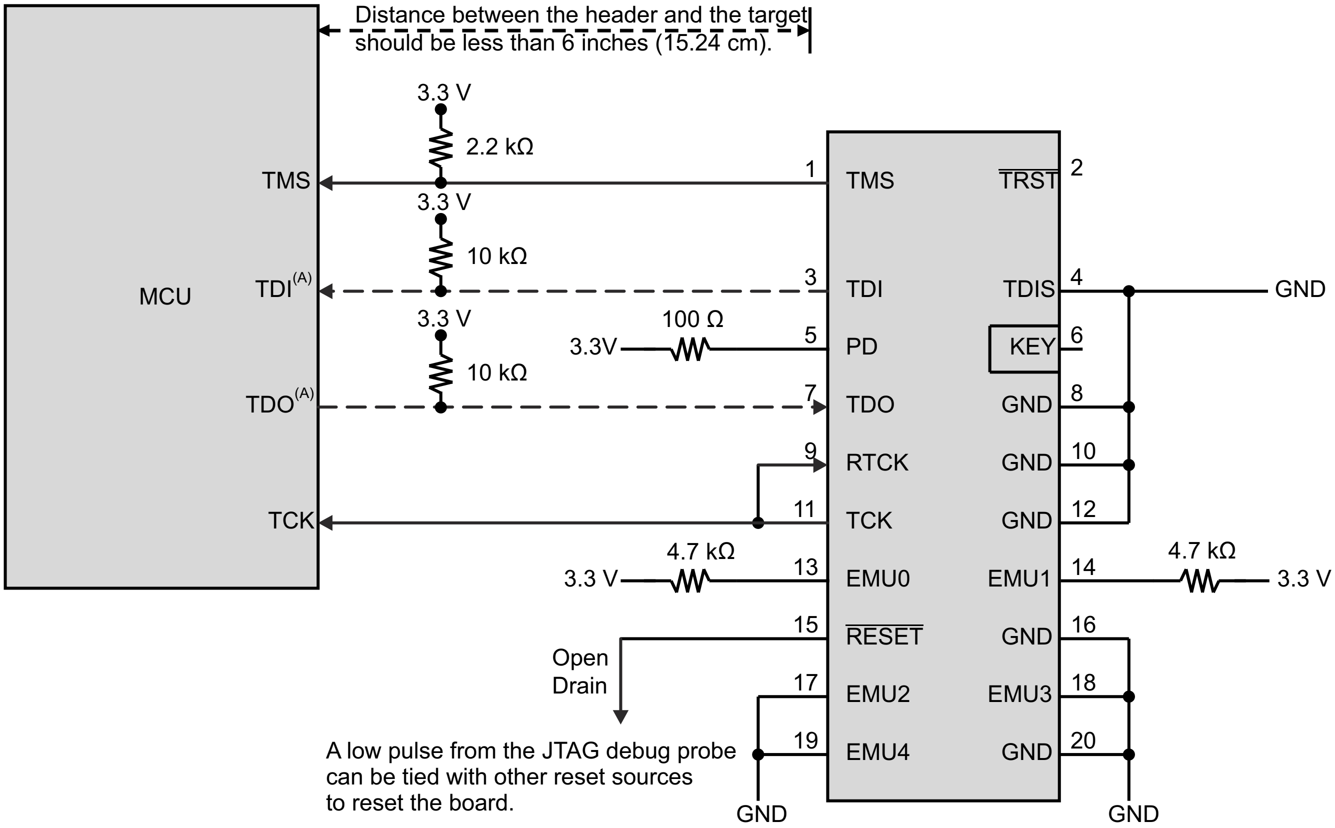
JTAG Test Data Input (TDI) is the default mux selection for the pin. The internal pullup is disabled by default. If this pin is used as JTAG TDI, the internal pullup should be enabled or an external pullup added on the board to avoid a floating input. In the cJTAG option, this pin can be used as GPIO.

JTAG Test Data Output (TDO) is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating. The internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. In the cJTAG option, this pin can be used as GPIO.



A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-24. Connecting to the 14-Pin JTAG Header



A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-25. Connecting to the 20-Pin JTAG Header

6.11.7.1 JTAG Electrical Data and Timing

Section 6.11.7.1.1 lists the JTAG timing requirements. Section 6.11.7.1.2 lists the JTAG switching characteristics. Figure 6-26 shows the JTAG timing.

6.11.7.1.1 JTAG Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time, TCK	66.66		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	26.66		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	26.66		ns
3	$t_{su(TDI-TCKH)}$	Input setup time, TDI valid to TCK high	13		ns
	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	13		
4	$t_{h(TCKH-TDI)}$	Input hold time, TDI valid from TCK high	7		ns
	$t_{h(TCKH-TMS)}$	Input hold time, TMS valid from TCK high	7		

6.11.7.1.2 JTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
2	$t_{d(TCKL-TDO)}$	Delay time, TCK low to TDO valid	6	25	ns

6.11.7.1.3 JTAG Timing Diagram

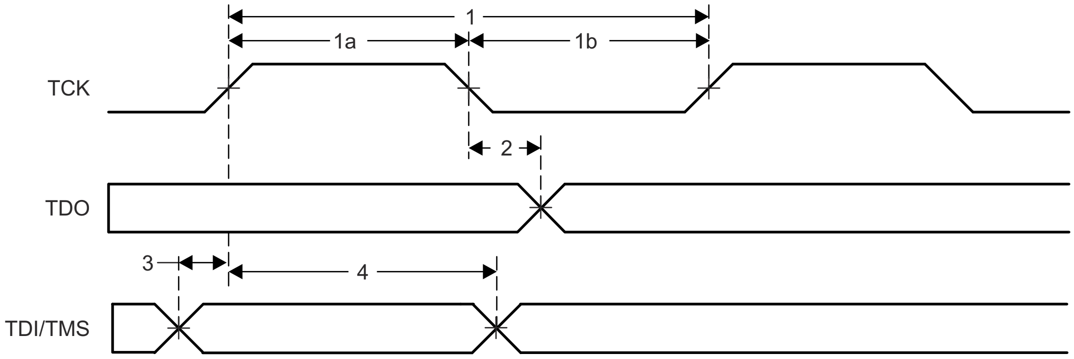


Figure 6-26. JTAG Timing

6.11.7.2 cJTAG Electrical Data and Timing

Section 6.11.7.2.1 lists the cJTAG timing requirements. Section 6.11.7.2.2 lists the cJTAG switching characteristics. Figure 6-27 shows the cJTAG timing.

6.11.7.2.1 cJTAG Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time, TCK	100		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	40		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	40		ns
3	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	15		ns
	$t_{su(TMS-TCKL)}$	Input setup time, TMS valid to TCK low	15		ns
4	$t_{h(TCKH-TMS)}$	Input hold time, TMS valid from TCK high	2		ns
	$t_{h(TCKL-TMS)}$	Input hold time, TMS valid from TCK low	2		ns

6.11.7.2.2 cJTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
2	$t_{d(TCKL-TMS)}$	Delay time, TCK low to TMS valid	6	20	ns
5	$t_{dis(TCKH-TMS)}$	Delay time, TCK high to TMS disable		20	ns

6.11.7.2.3 cJTAG Timing Diagram

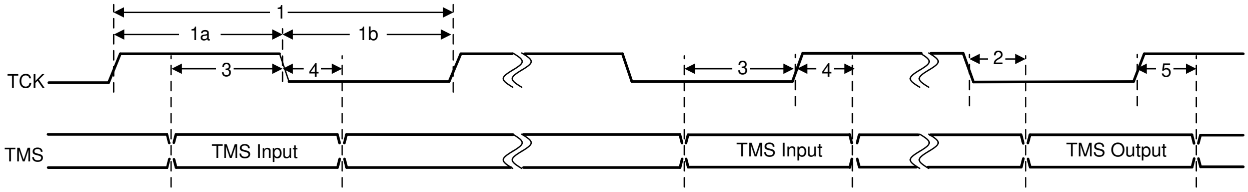


Figure 6-27. cJTAG Timing

6.11.8 GPIO Electrical Data and Timing

The peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. On reset, GPIO pins are configured as inputs. For specific inputs, the user can also select the number of input qualification cycles to filter unwanted noise glitches.

The GPIO module contains an Output X-BAR which allows an assortment of internal signals to be routed to a GPIO in the GPIO mux positions denoted as OUTPUTXBARx. The GPIO module also contains an Input X-BAR which is used to route signals from any GPIO input to different IP blocks such as the ADCs, eCAPs, ePWMs, and external interrupts. For more details, see the X-BAR chapter in the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.

6.11.8.1 GPIO – Output Timing

Section 6.11.8.1.1 lists the general-purpose output switching characteristics. Figure 6-28 shows the general-purpose output timing.

6.11.8.1.1 General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
$t_{r(GPIO)}$	Rise time, GPIO switching low to high	All GPIOs		8[1]	ns
$t_{f(GPIO)}$	Fall time, GPIO switching high to low	All GPIOs		8[1]	ns
f_{GPIO}	Toggling frequency, all GPIOs			25	MHz

[1] Rise time and fall time vary with load. These values assume a 40-pF load.

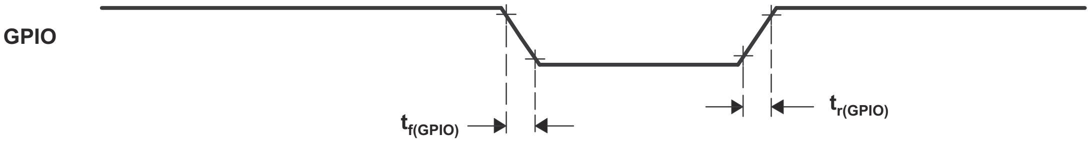


Figure 6-28. General-Purpose Output Timing

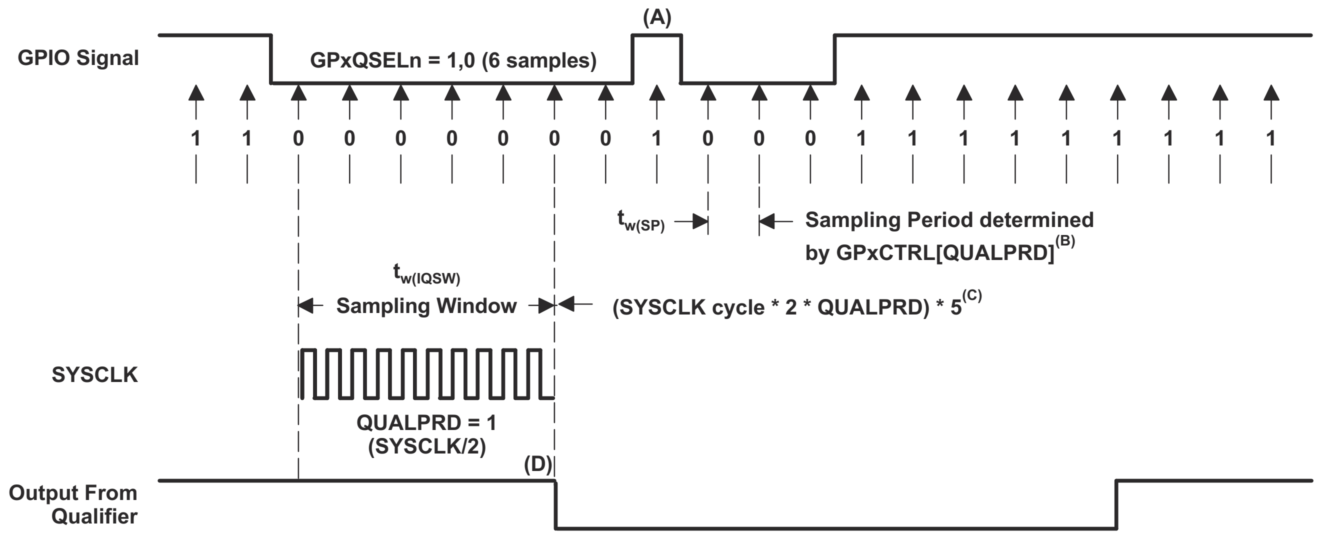
6.11.8.2 GPIO – Input Timing

6.11.8.2.1 General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SYSCLK)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SYSCLK)}$ * QUALPRD		
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * (n[(1)] – 1)		cycles
$t_{w(GPI)}$ [(2)]	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.

6.11.8.2.2 Sampling Mode



A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLK cycle. For any other value "n", the qualification sampling period in 2n SYSCLK cycles (that is, at every 2n SYSCLK cycles, the GPIO pin will be sampled).
B. The qualification period selected through the GPxCTRL register applies to groups of eight GPIO pins.
C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.
D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLK cycles or greater. In other words, the inputs should be stable for (5 × QUALPRD × 2) SYSCLK cycles. This would ensure 5 sampling periods for detection to occur. Because external signals are driven asynchronously, an 13-SYSCLK-wide pulse ensures reliable recognition.

Figure 6-29. Sampling Mode

6.11.8.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLK.

Sampling frequency = SYSCLK/(2 × QUALPRD), if QUALPRD ≠ 0

Sampling frequency = SYSCLK, if QUALPRD = 0

Sampling period = SYSCLK cycle × 2 × QUALPRD, if QUALPRD ≠ 0

In the previous equations, SYSCLK cycle indicates the time period of SYSCLK.

Sampling period = SYSCLK cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 2, if QUALPRD = 0

Case 2:

Qualification using 6 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 5, if QUALPRD = 0

Figure 6-30 shows the general-purpose input timing.

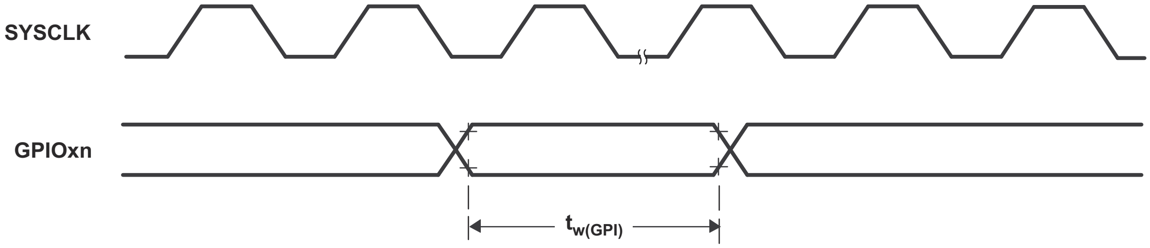


Figure 6-30. General-Purpose Input Timing

6.11.9 Interrupts

The C28x CPU has fourteen peripheral interrupt lines. Two of them (INT13 and INT14) are connected directly to CPU timers 1 and 2, respectively. The remaining twelve are connected to peripheral interrupt signals through the enhanced Peripheral Interrupt Expansion (ePIE) module. The ePIE multiplexes up to sixteen peripheral interrupts into each CPU interrupt line. It also expands the vector table to allow each interrupt to have its own ISR. This allows the CPU to support a large number of peripherals.

An interrupt path is divided into three stages—the peripheral, the ePIE, and the CPU. Each stage has its own enable and flag registers. This system allows the CPU to handle one interrupt while others are pending, implement and prioritize nested interrupts in software, and disable interrupts during certain critical tasks.

Figure 6-31 shows the interrupt architecture for this device.

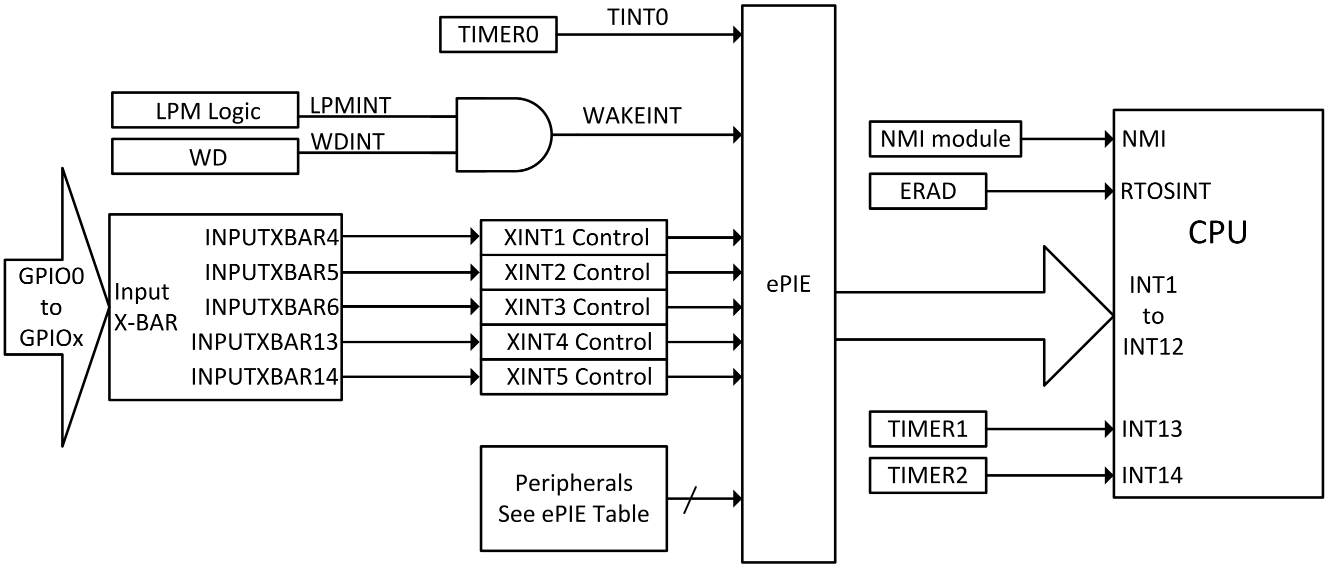


Figure 6-31. Device Interrupt Architecture

6.11.9.1 External Interrupt (XINT) Electrical Data and Timing

Section 6.11.9.1.1 lists the external interrupt timing requirements. Section 6.11.9.1.2 lists the external interrupt switching characteristics. Figure 6-32 shows the external interrupt timing. For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.11.9.1.1 External Interrupt Timing Requirements

			MIN	MAX	UNIT
$t_{w(INT)}$	Pulse duration, INT input low/high	Synchronous	$2t_{c(SYSCLK)}$		cycles
		With qualifier[1]	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		

(1) For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.11.9.1.2 External Interrupt Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER[1]		MIN	MAX	UNIT
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch [2]	$t_{w(IQSW)} + 14t_{c(SYSCLK)}$	$t_{w(IQSW)} + t_{w(SP)} + 14t_{c(SYSCLK)}$	cycles

(1) For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.
(2) This assumes that the ISR is in a single-cycle memory.

6.11.9.1.3 External Interrupt Timing

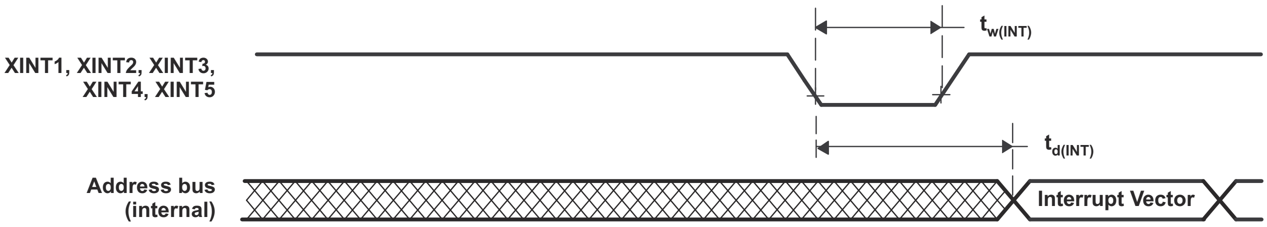


Figure 6-32. External Interrupt Timing

6.11.10 Low-Power Modes

This device has HALT, IDLE and STANDBY as clock-gating low-power modes.

Further details, as well as the entry and exit procedure, for all of the low-power modes can be found in the Low Power Modes section of the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.

6.11.10.1 Clock-Gating Low-Power Modes

IDLE and HALT modes on this device are similar to those on other C28x devices. Table 6-7 describes the effect on the system when any of the clock-gating low-power modes are entered.

Table 6-7. Effect of Clock-Gating Low-Power Modes on the Device

MODULES/ CLOCK DOMAIN	IDLE	STANDBY	HALT
SYSCLK	Active	Gated	Gated
CPUCLK	Gated	Gated	Gated
Clock to modules connected to PERx.SYSCLK	Active	Gated	Gated
WDCLK	Active	Active	Gated if CLKSRCCTL1.WDHALTI = 0
PLL	Powered	Powered	Software must power down PLL before entering HALT.
INTOSC1	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
INTOSC2	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
Flash(1)	Powered	Powered	Powered
XTAL(2)	Powered	Powered	Powered

(1) The Flash module is not powered down by hardware in any LPM. It may be powered down using software if required by the application. For more information, see the Flash and OTP Memory section of the System Control chapter in the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.

(2) The XTAL is not powered down by hardware in any LPM. It may be powered down by software setting the XTALCR.OSCOFF bit to 1. This can be done at any time during the application if the XTAL is not required.

6.11.10.2 Low-Power Mode Wake-up Timing

Section 6.11.10.2.1 lists the IDLE mode timing requirements, Section 6.11.10.2.2 lists the IDLE mode switching characteristics, and Figure 6-33 shows the timing diagram for IDLE mode. For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.11.10.2.1 IDLE Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		

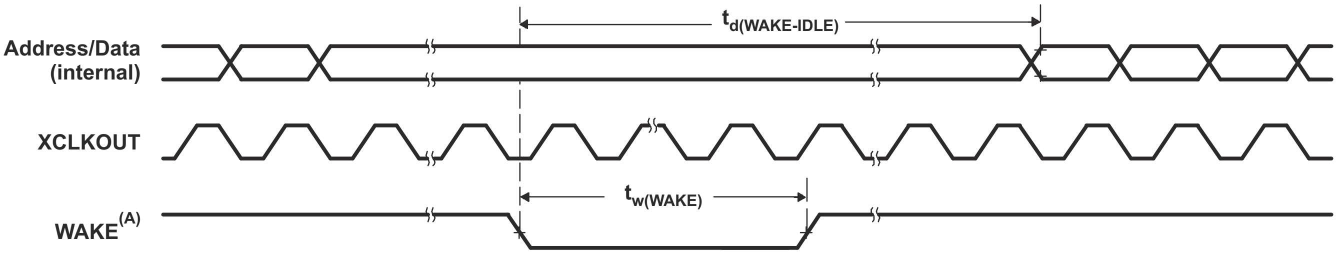
6.11.10.2.2 IDLE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume[1]	From Flash (active state)	Without input qualifier		$40t_{c(SYSCLK)}$	cycles
			With input qualifier		$40t_{c(SYSCLK)} + t_{w(WAKE)}$	cycles
		From Flash (sleep state)	Without input qualifier		$6700t_{c(SYSCLK)}$ [2]	cycles
			With input qualifier		$6700t_{c(SYSCLK)}$ [2] + $t_{w(WAKE)}$	cycles
		From RAM	Without input qualifier		$25t_{c(SYSCLK)}$	cycles
			With input qualifier		$25t_{c(SYSCLK)} + t_{w(WAKE)}$	cycles

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.
(2) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. This value can be realized when SYSCLK is 200 MHz, RWAIT is 3, and FPAC1[PSLEEP] is 0x860.

6.11.10.2.3 IDLE Entry and Exit Timing Diagram



A. WAKE can be any enabled interrupt, $\overline{\text{WDINT}}$ or XRSn. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

Figure 6-33. IDLE Entry and Exit Timing Diagram

Section 6.11.10.2.4 lists the STANDBY mode timing requirements, Section 6.11.10.2.5 lists the STANDBY mode switching characteristics, and Figure 6-34 shows the timing diagram for STANDBY mode.

6.11.10.2.4 STANDBY Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	QUALSTDBY = 0 | $2t_{c(OSCCLK)}$	$3t_{c(OSCCLK)}$		cycles
		QUALSTDBY > 0 | (2 + QUALSTDBY)$t_{c(OSCCLK)}$ (1)	(2 + QUALSTDBY) * $t_{c(OSCCLK)}$		

(1) QUALSTDBY is a 6-bit field in the LPMCR register.

6.11.10.2.5 STANDBY Mode Switching Characteristics

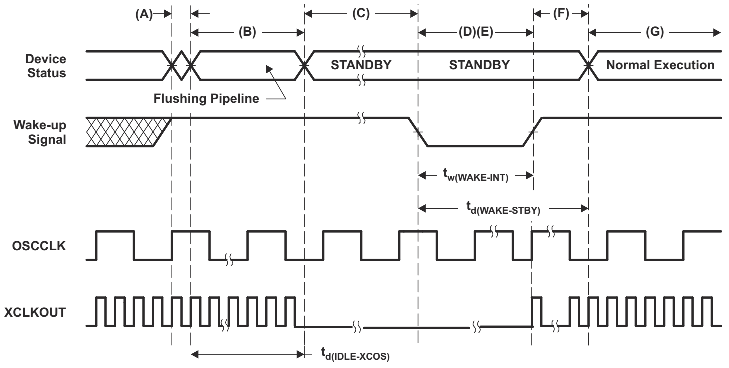
over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop			$16t_{c(INTOSC1)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume[(1)]	Wakeup from flash (Flash module in active state)		$175t_{c(SYSCLK)} + t_{w(WAKE-INT)}$	cycles
$t_{d(WAKE-STBY)}$		Wakeup from flash (Flash module in sleep state)		$6700t_{c(SYSCLK)}$ (2) $+ t_{w(WAKE-INT)}$	cycles
$t_{d(WAKE-STBY)}$		Wakeup from RAM		$3t_{c(OSC)} + 15t_{c(SYSCLK)} + t_{w(WAKE-INT)}$	cycles

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.

(2) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. This value can be realized when SYSCLK is 200 MHz, RWAIT is 3, and FPAC1[PSLEEP] is 0x860.

6.11.10.2.6 STANDBY Entry and Exit Timing Diagram



A. IDLE instruction is executed to put the device into STANDBY mode.
B. The LPM block responds to the STANDBY signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
D. The external wake-up signal is driven active.
E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wakeup behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wakeup pulses.
F. After a latency period, the STANDBY mode is exited.
G. Normal execution resumes. The device will respond to the interrupt (if enabled).

Figure 6-34. STANDBY Entry and Exit Timing Diagram

Section 6.11.10.2.7 lists the HALT mode timing requirements, Section 6.11.10.2.8 lists the HALT mode switching characteristics, and Figure 6-35 shows the timing diagram for HALT mode.

6.11.10.2.7 HALT Mode Timing Requirements

		MIN	MAX	UNIT
$t_{w(WAKE\text{-}GPIO)}$	Pulse duration, GPIO wake-up signal(1)	$t_{oscst} + 2t_{c(OSCCLK)}$		cycles
$t_{w(WAKE\text{-}XRS)}$	Pulse duration, $\overline{XRS}$ wake-up signal(1)	$t_{oscst} + 8t_{c(OSCCLK)}$		cycles

(1) For applications using X1/X2 for OSCCLK, the user must characterize their specific oscillator start-up time as it is dependent on circuit/layout external to the device. See the *Crystal Oscillator Electrical Characteristics* table for more information. For applications using INTOSC1 or INTOSC2 for OSCCLK, see the *Internal Oscillators* section for t_{oscst}. Oscillator start-up time does not apply to applications using a single-ended crystal on the X1 pin, as it is powered externally to the device.

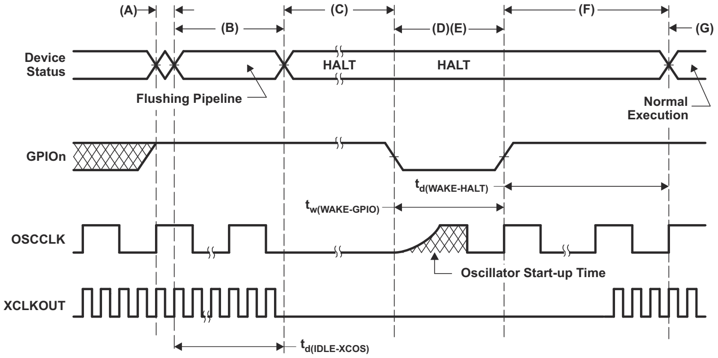
6.11.10.2.8 HALT Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(IDLE\text{-}XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop		$16t_{c(INTOSC1)}$	cycles
$t_{d(WAKE\text{-}HALT)}$	Delay time, external wake signal end to CPU1 program execution resume			cycles
	Wakeup from Flash - Flash module in active state		$75t_{c(OSCCLK)}$	
	Wakeup from Flash - Flash module in sleep state		$17500t_{c(OSCCLK)}$ (1)	
	Wakeup from RAM		$75t_{c(OSCCLK)}$	

(1) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. This value can be realized when SYSCLK is 200 MHz, RWAIT is 3, and FPAC1[PSLEEP] is 0x860.

6.11.10.2.9 HALT Entry and Exit Timing Diagram



A. IDLE instruction is executed to put the device into HALT mode.
B. The LPM block responds to the HALT signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes very little power. It is possible to keep the zero-pin internal oscillators (INTOSC1 and INTOSC2) and the watchdog alive in HALT MODE. This is done by writing 1 to CLKSRCCTL1.WDHALTI. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
D. When the GPIOn pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Because the falling edge of the GPIO pin asynchronously begins the wake-up procedure, care should be taken to maintain a low noise environment before entering and during HALT mode.
E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after some latency. The HALT mode is now exited.
G. Normal operation resumes.
H. The user must relock the PLL upon HALT wakeup to ensure a stable PLL lock.

Figure 6-35. HALT Entry and Exit Timing Diagram

6.12 Analog Peripherals

The analog subsystem module is described in this section.

The analog modules on this device include the ADC, temperature sensor, and CMPSS.

The analog subsystem has the following features:

- Flexible voltage references
  - – The ADCs are referenced to VREFHI and VSSA pins
    - VREFHI pin voltage can be driven in externally or can be generated by an internal bandgap voltage reference
    - The internal voltage reference range can be selected to be 0V to 3.3V or 0V to 2.5V
  - – The comparator DACs are referenced to VDDA and VSSA
    - Alternately, these DACs can be referenced to the VDAC pin and VSSA
- Flexible pin usage
  - – Comparator subsystem inputs and digital inputs are multiplexed with ADC inputs
  - – Internal connection to V_{REFLO} on all ADCs for offset self-calibration

Figure 6-36 shows the Analog Subsystem Block Diagram for the 80-pin PN and 64-pin PM LQFPs.

Figure 6-37 shows the Analog Subsystem Block Diagram for the 48-pin PT LQFP.

Table 6-8 lists the analog pins and internal connections. Table 6-9 lists descriptions of analog signals.Figure 6-38 shows the analog group connections.

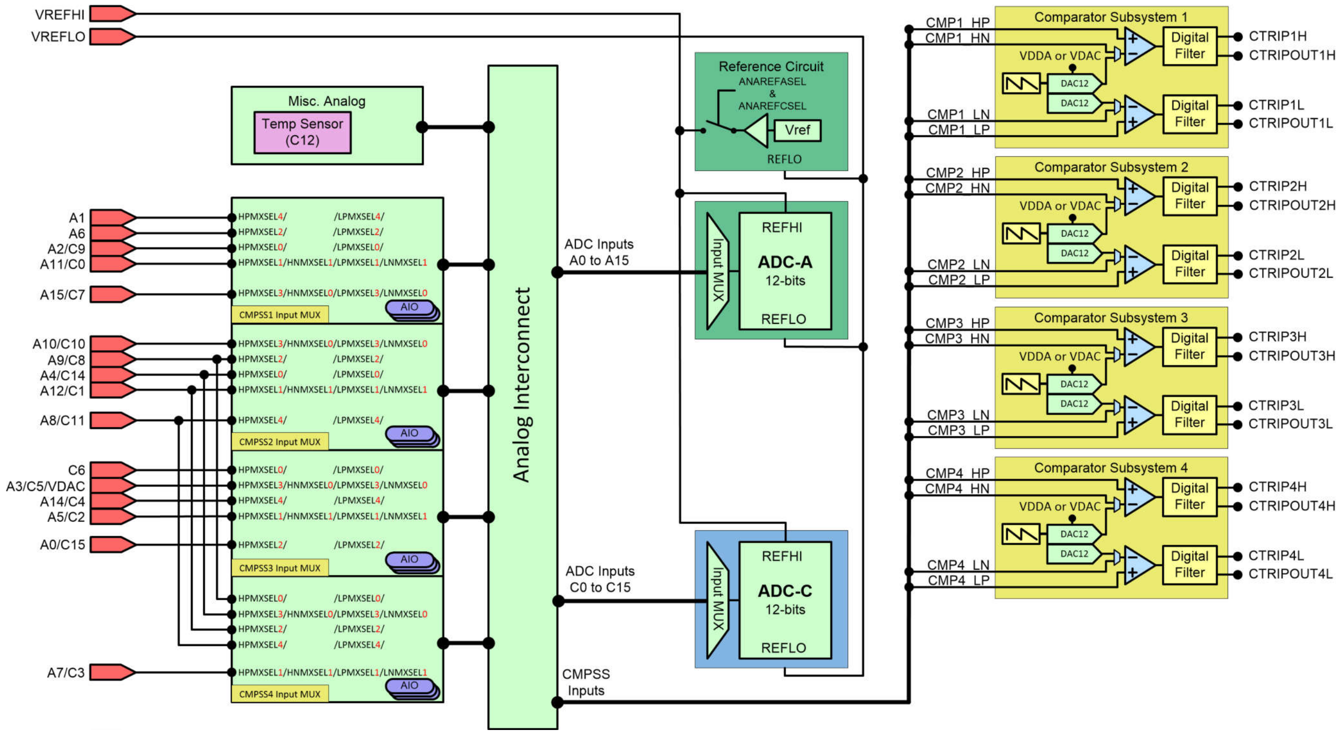


Figure 6-36. Analog Subsystem Block Diagram (80-Pin PN and 64-Pin PM LQFPs)

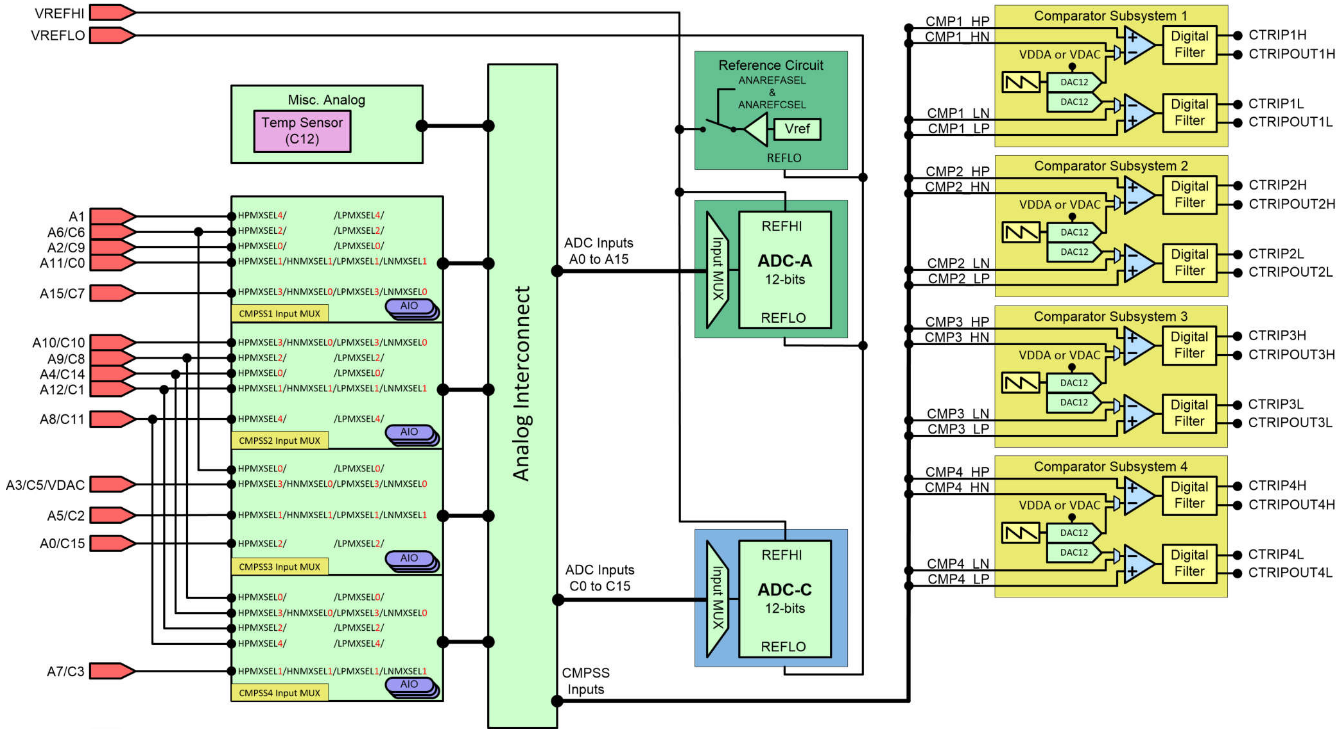


Figure 6-37. Analog Subsystem Block Diagram (48-Pin PT LQFP)

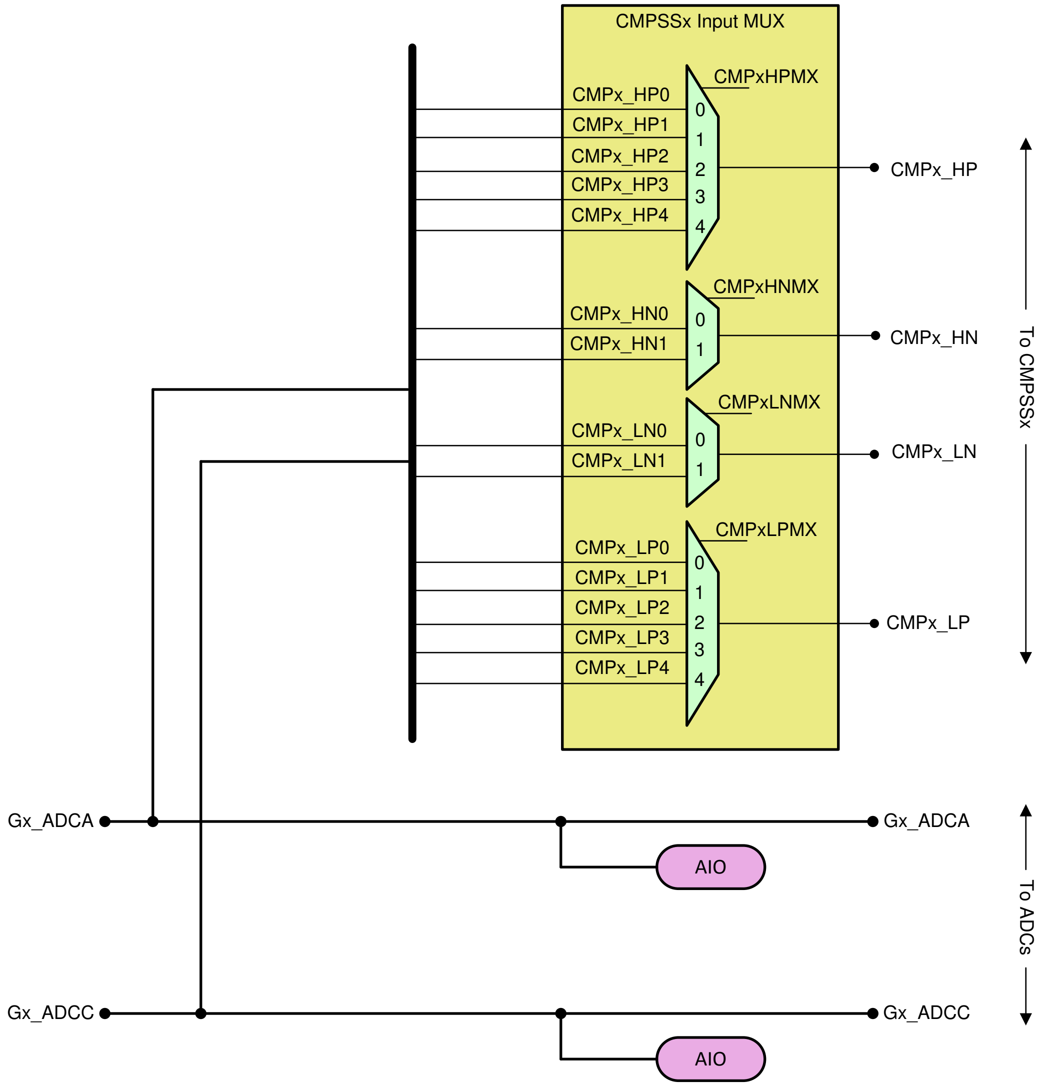


Figure 6-38. Analog Group Connections

6.12.1 Analog Pins and Internal Connections

Table 6-8. Analog Pins and Internal Connections

Pin Name	Package Pin			ADC		Comparator Subsystem (MUX)				AIO Input
	80 QFP	64 QFP	48 QFN	A	C	High Positive	High Negative	Low Positive	Low Negative	
VREFHI	20	16	12							
VREFLO	21	17	13	A13	C13					
Analog Group 1						**CMP1**				
A6	10	6	4(3)	A6	–	CMP1_HP2 (HPMXSEL=2)		CMP1_LP2 (LPMXSEL=2)		AIO228
A2/C9	13	9	6	A2	C9	CMP1_HP0 (HPMXSEL=0)		CMP1_LP0 (LPMXSEL=0)		AIO224
A15/C7	14	10	7	A15	C7	CMP1_HP3 (HPMXSEL=3)	CMP1_HN0 (HNMXSEL=0)	CMP1_LP3 (LPMXSEL=3)	CMP1_LN0 (LNMXSEL=0)	AIO233
A11/C0	16	12	8	A11	C0	CMP1_HP1 (HPMXSEL=1)	CMP1_HN1 (HNMXSEL=1)	CMP1_LP1 (LPMXSEL=1)	CMP1_LN1 (LNMXSEL=1)	AIO237
A1	18	14	10	A1	–	CMP1_HP4 (HPMXSEL=4)		CMP1_LP4 (LPMXSEL=4)		AIO232
Analog Group 2						**CMP2**				
A10/C10	29	25	21	A10	C10	CMP2_HP3 (HPMXSEL=3)	CMP2_HN0 (HNMXSEL=0)	CMP2_LP3 (LPMXSEL=3)	CMP2_LN0 (LNMXSEL=0)	AIO230
Analog Group 3						**CMP3**				
C6	11	7	4(3)	–	C6	CMP3_HP0 (HPMXSEL=0)		CMP3_LP0 (LPMXSEL=0)		AIO226
A3/C5/VDAC(1)	12	8	5	A3	C5	CMP3_HP3 (HPMXSEL=3)	CMP3_HN0 (HNMXSEL=0)	CMP3_LP3 (LPMXSEL=3)	CMP3_LN0 (LNMXSEL=0)	AIO242
A14/C4	15	11	–	A14	C4	CMP3_HP4 (HPMXSEL=4)		CMP3_LP4 (LPMXSEL=4)		AIO239
A5/C2	17	13	9	A5	C2	CMP3_HP1 (HPMXSEL=1)	CMP3_HN1 (HNMXSEL=1)	CMP3_LP1 (LPMXSEL=1)	CMP3_LN1 (LNMXSEL=1)	AIO244
A0/C15	19	15	11	A0	C15	CMP3_HP2 (HPMXSEL=2)		CMP3_LP2 (LPMXSEL=2)		AIO231
Analog Group 4						**CMP4**				
A7/C3	23	19	15	A7	C3	CMP4_HP1 (HPMXSEL=1)	CMP4_HN1 (HNMXSEL=1)	CMP4_LP1 (LPMXSEL=1)	CMP4_LN1 (LNMXSEL=1)	AIO245

Table 6-8. Analog Pins and Internal Connections (continued)

Pin Name	Package Pin			ADC		Comparator Subsystem (MUX)				AIO Input
	80 QFP	64 QFP	48 QFN	A	C	High Positive	High Negative	Low Positive	Low Negative	
Combined Analog Group 2/4						**CMP2/4**				
A12/C1	22	18	14	A12	C1	CMP2_HP1 (HPMXSEL=1) CMP4_HP2 (HPMXSEL=2)	CMP2_HN1 (HNMXSEL=1)	CMP2_LP1 (LPMXSEL=1) CMP4_LP2 (LPMXSEL=2)	CMP2_LN1 (LNMXSEL=1)	AIO238
A8/C11	24	20	16	A8	C11	CMP2_HP4 (HPMXSEL=4) CMP4 _HP4 (HPMXSEL=4)		CMP2_LP4 (LPMXSEL=4) CMP4_LP4 (LPMXSEL=4)		AIO241
A4/C14	27	23	19	A4	C14	CMP2_HP0 (HPMXSEL=0) CMP4_HP3 (HPMXSEL=3)	CMP4_HN0 (HNMXSEL=0)	CMP0_LP0 (LPMXSEL=0) CMP4_LP3 (LPMXSEL=3)	CMP4_LN0 (LNMXSEL=0)	AIO225
A9/C8	28	24	20	A9	C8	CMP2_HP2 (HPMXSEL=2) CMP4_HP0 (HPMXSEL=0)		CMP2_LP2 (LPMXSEL=2) CMP4_LP0 (LPMXSEL=0)		AIO227
Other Analog										
TempSensor(2)	–	–	–	–	C12					

(1) Optional external reference voltage for on-chip COMPDACs. There is an internal capacitance to VSSA on this pin whether used for ADC input or COMPDAC reference. If used as a VDAC reference, place at least a 1-μF capacitor on this pin.
(2) Internal connection only; does not come to a device pin.
(3) A6 and C6 is double bonded as pin # 4.

6.12.2 Analog Signal Descriptions

Table 6-9. Analog Signal Descriptions

SIGNAL NAME	DESCRIPTION
AIOx	Digital input on ADC pin
Ax	ADC A Input
Cx	ADC C Input
CMPx_HNy	Comparator subsystem high comparator negative input
CMPx_HPy	Comparator subsystem high comparator positive input
CMPx_LNy	Comparator subsystem low comparator negative input
CMPx_LPy	Comparator subsystem low comparator positive input
TempSensor	Internal temperature sensor
VDAC	Optional external reference voltage for on-chip COMPDACs. There is an internal capacitance to VSSA on this pin whether used for ADC input or COMPDAC reference which cannot be disabled. If this pin is being used as a reference for the on-chip COMPDACs, place at least a 1-uF capacitor on this pin.

6.12.3 Analog-to-Digital Converter (ADC)

The ADC module described here is a successive approximation (SAR) style ADC with resolution of 12 bits. This section refers to the analog circuits of the converter as the “core,” and includes the channel-select MUX, the sample-and-hold (S/H) circuit, the successive approximation circuits, voltage reference circuits, and other analog support circuits. The digital circuits of the converter are referred to as the “wrapper” and include logic for programmable conversions, result registers, interfaces to analog circuits, interfaces to the peripheral buses, post-processing circuits, and interfaces to other on-chip modules.

Each ADC module consists of a single sample-and-hold (S/H) circuit. The ADC module is designed to be duplicated multiple times on the same chip, allowing simultaneous sampling or independent operation of multiple ADCs. The ADC wrapper is start-of-conversion (SOC)-based (see the SOC Principle of Operation section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*).

Each ADC has the following features:

- Resolution of 12 bits
- Ratiometric external reference set by VREFHI/VREFLO
- Selectable internal reference of 2.5 V or 3.3 V
- Single-ended signaling
- Input multiplexer with up to 16 channels
- 16 configurable SOCs
- 16 individually addressable result registers
- Multiple trigger sources
  - S/W: software immediate start
  - All ePWMs: ADCSOC A or B
  - GPIO XINT2
  - CPU Timers 0/1/2
  - ADCINT1/2
- Four flexible PIE interrupts
- Burst-mode triggering option
- Four post-processing blocks, each with:
  - Saturating offset calibration
  - Error from setpoint calculation
  - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
  - Trigger-to-sample delay capture

Note

Not every channel may be pinned out from all ADCs. See Section 5 to determine which channels are available.

The block diagram for the ADC core and ADC wrapper are shown in Figure 6-39.

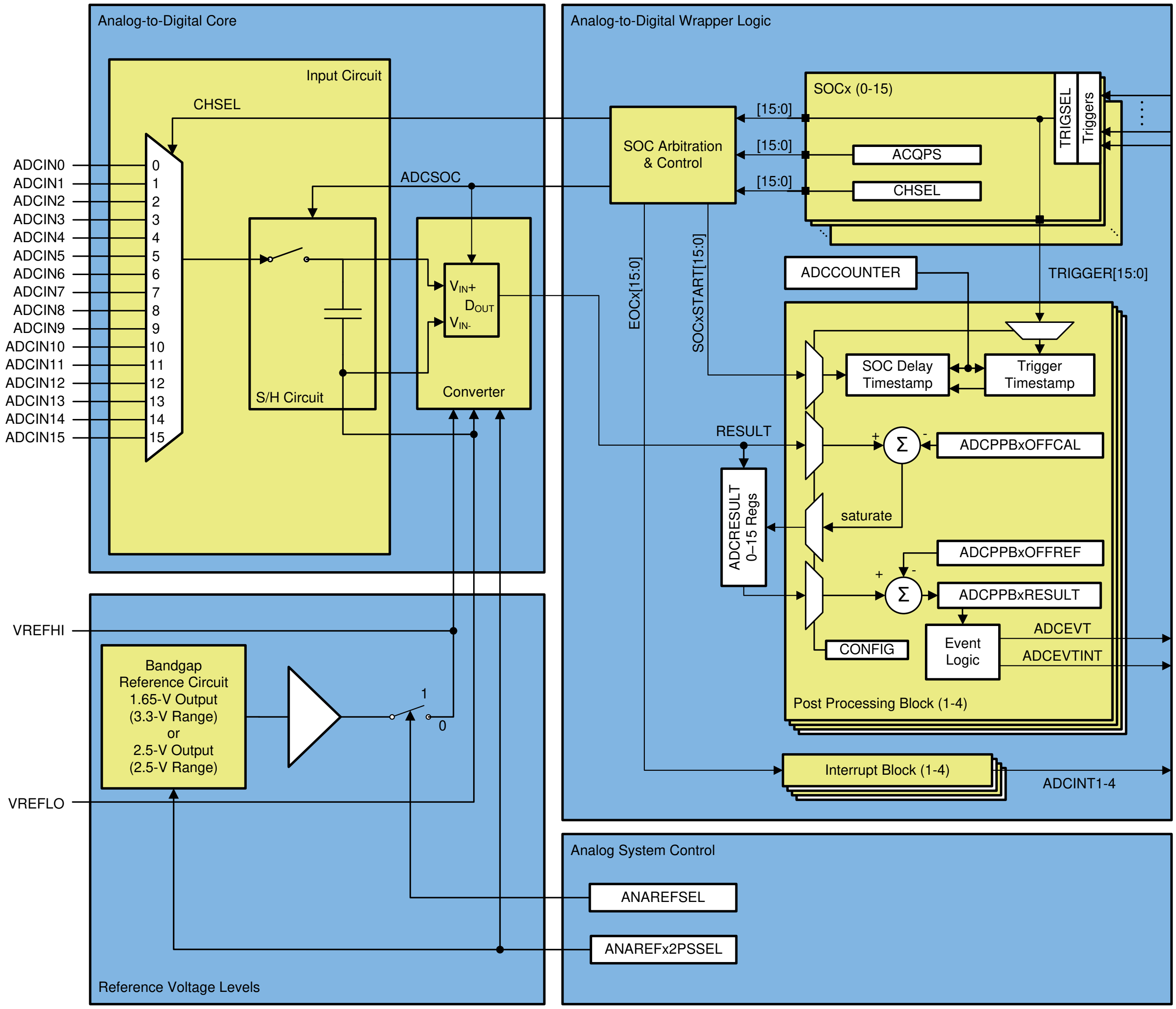


Figure 6-39. ADC Module Block Diagram

6.12.3.1 ADC Configurability

Some ADC configurations are individually controlled by the SOCs, while others are globally controlled per ADC module. Table 6-10 summarizes the basic ADC options and their level of configurability.

Table 6-10. ADC Options and Configuration Levels

OPTIONS	CONFIGURABILITY
Clock	Per module(1)
Resolution	Not configurable (12-bit resolution only)
Signal mode	Not configurable (single-ended signal mode only)
Reference voltage source	Common for both ADC modules
Trigger source	Per SOC(1)
Converted channel	Per SOC
Acquisition window duration	Per SOC(1)
EOC location	Per module
Burst mode	Per module(1)

(1) Writing these values differently to different ADC modules could cause the ADCs to operate asynchronously. For guidance on when the ADCs are operating synchronously or asynchronously, see the Ensuring Synchronous Operation section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.

6.12.3.1.1 Signal Mode

The ADC supports single-ended signaling. The input voltage to the converter is sampled through a single pin (ADCINx), referenced to VREFLO. Figure 6-40 shows the single-ended signaling mode.

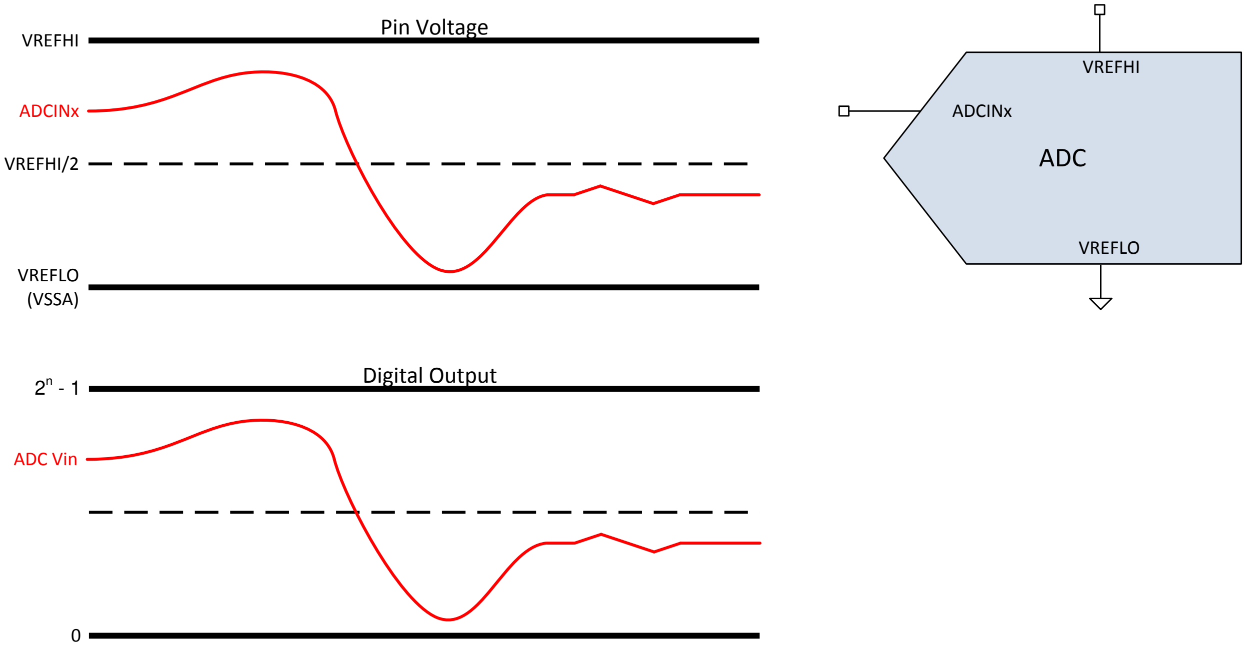


Figure 6-40. Single-ended Signaling Mode

6.12.3.2 ADC Electrical Data and Timing

Section 6.12.3.2.1 lists the ADC operating conditions. Section 6.12.3.2.2 lists the ADC electrical characteristics.

Note

The ADC inputs should be kept below VDDA + 0.3 V. If an ADC input goes above this level, ADC disturbances to other channels may occur by two mechanisms:

- ADC input overvoltage will overdrive the CMPSS mux, disturbing all other channels which share a common CMPSS mux. This disturbance will be continuous regardless of if the overvoltage input is sampled by the ADC
- When the ADC samples the overvoltage ADC input, VREFHI will be pulled up to a higher level. This will disturb subsequent ADC conversions on any channel until the V_{REF} stabilizes

Note

The VREFHI pin must be kept below VDDA + 0.3 V to ensure proper functional operation. If the VREFHI pin exceeds this level, a blocking circuit may activate, and the internal value of VREFHI may float to 0 V internally, giving improper ADC conversion.

6.12.3.2.1 ADC Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)		5		50	MHz
Sample rate	100-MHz SYSCLK			3.45	MSPS
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	With 50 Ω or less R_s	75			ns
VREFHI	External Reference	2.4	2.5 or 3.0	VDDA	V
VREFHI(2)	Internal Reference = 3.3V Range		1.65		V
	Internal Reference = 2.5V Range		2.5		V
VREFLO		VSSA		VSSA	V
VREFHI - VREFLO	External Reference	2.4		VDDA	V
Conversion range	Internal Reference = 3.3 V Range	0		3.3	V
	Internal Reference = 2.5 V Range	0		2.5	V
	External Reference	VREFLO		VREFHI	V

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) In internal reference mode, the reference voltage is driven out of the VREFHI pin by the device. The user should not drive a voltage into the pin in this mode.

6.12.3.2.2 ADC Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles	100-MHz SYSCLK	10.1		11	ADCCLKs
Power Up Time	External Reference mode			500	µs
	Internal Reference mode			5000	µs
	Internal Reference mode, when switching between 2.5-V range and 3.3-V range.			5000	µs
VREFHI input current[(1)]			130		µA
Internal Reference Capacitor Value[(2)]		2.2			µF
External Reference Capacitor Value[(2)]		2.2			µF
DC Characteristics					
Gain Error	Internal reference	–45		45	LSB
	External reference	–5	±3	5	
Offset Error		–5	±2	5	LSB
Channel-to-Channel Gain Error[(4)]			2		LSB
Channel-to-Channel Offset Error[(4)]			2		LSB
ADC-to-ADC Gain Error[(5)]	Identical VREFHI and VREFLO for all ADCs		4		LSB
ADC-to-ADC Offset Error[(5)]	Identical VREFHI and VREFLO for all ADCs		2		LSB
DNL Error		>–1	±0.5	1	LSB
INL Error		–2	±1.0	2	LSB
ADC-to-ADC Isolation	VREFHI = 2.5 V, synchronous ADCs	–1		1	LSBs
AC Characteristics					
SNR[(3)]	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1		68.8		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC		60.1		
THD[(3)]	VREFHI = 2.5 V, fin = 100 kHz		–80.6		dB
SFDR[(3)]	VREFHI = 2.5 V, fin = 100 kHz		79.2		dB
SINAD[(3)]	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1		68.5		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC		60.0		
ENOB[(3)]	VREFHI = int/ext 2.5 V, fin = 100 kHz, SYSCLK from X1, Single ADC		11.0		bits
	VREFHI = int/ext 2.5 V, fin = 100 kHz, SYSCLK from X1, synchronous ADCs		11.0		
	VREFHI = int 3.3 V, fin = 100 kHz, SYSCLK from X1, Single ADC		10.6		
	VREFHI = int 3.3 V, fin = 100 kHz, SYSCLK from X1, synchronous ADCs		10.6		
	asynchronous ADCs		Not Supported		

6.12.3.2.2 ADC Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	VDD = 1.2-V DC + 100mV DC up to Sine at 1 kHz		60		dB
	VDD = 1.2-V DC + 100 mV DC up to Sine at 300 kHz		57		
	VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		60		
	VDDA = 3.3-V DC + 200 mV Sine at 900 kHz		57		

(1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
(3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
(4) Variation across all channels belonging to the same ADC module.
(5) Worst case variation compared to other ADC modules.

6.12.3.2.3 ADC INL and DNL

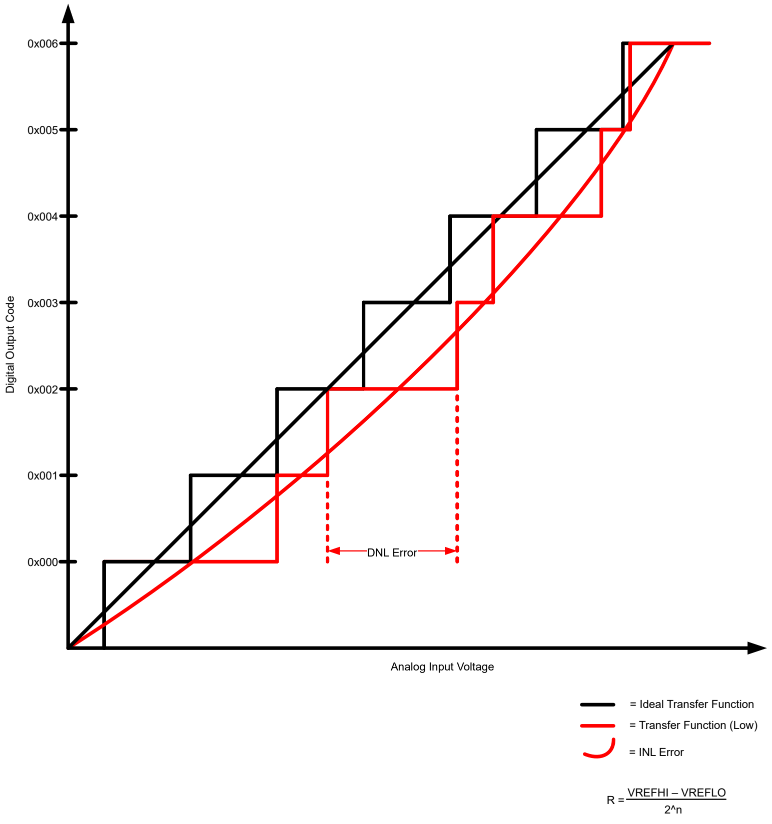


Figure 6-41. ADC INL and DNL

6.12.3.2.4 ADC Input Model

The ADC input characteristics are given by Table 6-11 and Figure 6-42.

Table 6-11. Input Model Parameters

	DESCRIPTION	REFERENCE MODE	VALUE
C_p	Parasitic input capacitance	All	See Table 6-12
R_{on}	Sampling switch resistance	External Reference, 2.5-V Internal Reference	500 Ω
		3.3-V Internal Reference	860 Ω
C_h	Sampling capacitor	External Reference, 2.5-V Internal Reference	12.5 pF
		3.3-V Internal Reference	7.5 pF
R_s	Nominal source impedance	All	50 Ω

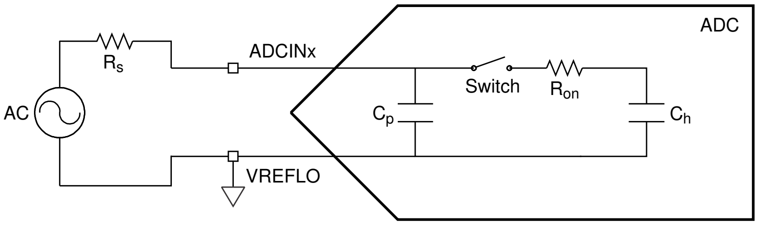


Figure 6-42. Input Model

This input model should be used with actual signal source impedance to determine the acquisition window duration. For more information, see the following:

- Choosing an Acquisition Window Duration section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*
- *Charge-Sharing Driving Circuits for C2000 ADCs Application Report*
- *ADC Input Circuit Evaluation for C2000 MCUs Application Report*

Table 6-12 lists the parasitic capacitance on each channel.

Table 6-12. Per-Channel Parasitic Capacitance

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
ADCINA0/ADCINC15	3.3	15.8
ADCINA1	2.4	4.9
ADCINA2/ADCINC9	2.9	5.4
ADCINA3/ADCINC5(1)	71.4	73.9
ADCINA4/ADCINC14	4.5	7
ADCINA5/ADCINC2	2.7	5.2
ADCINA6	2.6	5.1
ADCINA7/ADCINC3	4.2	6.7
ADCINA8/ADCINC11	4.5	7
ADCINA9/ADCINC8	3.4	5.9
ADCINA10/ADCINC10	2.9	5.4
ADCINA11/ADCINC0	2.9	5.4
ADCINA12/ADCINC1	4.7	7.2
ADCINA14/ADCINC4	2.5	5

Table 6-12. Per-Channel Parasitic Capacitance (continued)

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
ADCINA15/ADCINC7	3.3	5.8
ADCINC6	2.9	5.4

(1) Pin also used to supply reference voltage for COMPDAC and includes an internal decoupling capacitor.

6.12.3.2.5 ADC Timing Diagrams

Figure 6-43 shows the ADC conversion timings for two SOCs given the following assumptions:

- SOC0 and SOC1 are configured to use the same trigger.
- No other SOCs are converting or pending when the trigger occurs.
- The round-robin pointer is in a state that causes SOC0 to convert first.
- ADCINTSEL is configured to set an ADCINT flag upon end of conversion for SOC0 (whether this flag propagates through to the CPU to cause an interrupt is determined by the configurations in the PIE module).

Table 6-13 lists the descriptions of the ADC timing parameters. Table 6-14 lists the ADC timings.

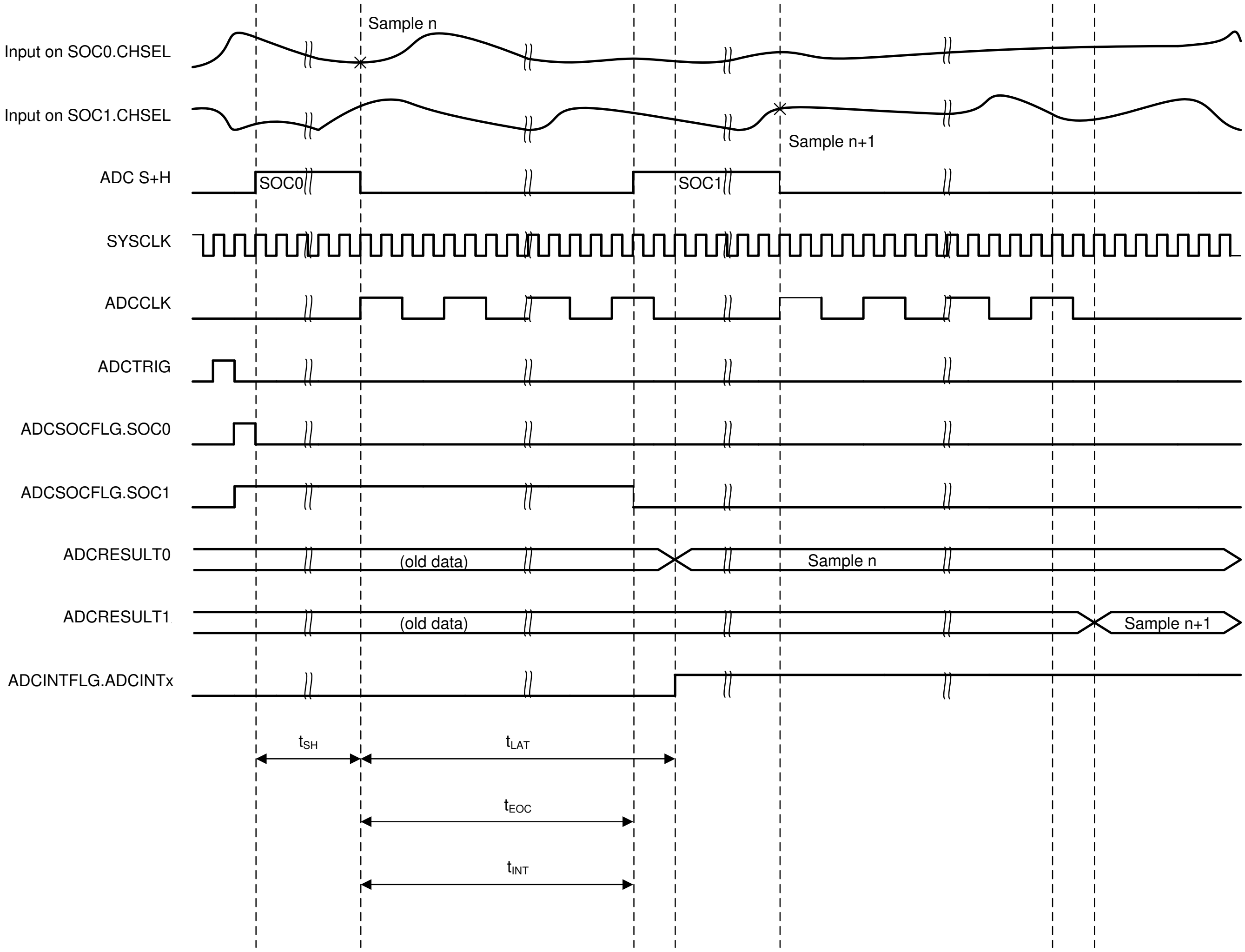


Figure 6-43. ADC Timings

Table 6-13. ADC Timing Parameters

PARAMETER	DESCRIPTION
t_{SH}	The duration of the S+H window. At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is given by (ACQPS + 1) SYSCLK cycles. ACQPS can be configured individually for each SOC, so t_{SH} will not necessarily be the same for different SOCs. **Note:** The value on the S+H capacitor will be captured approximately 5 ns before the end of the S+H window regardless of device clock settings.
t_{LAT}	The time from the end of the S+H window until the ADC results latch in the ADCRESULTx register. If the ADCRESULTx register is read before this time, the previous conversion results will be returned.
t_{EOC}	The time from the end of the S+H window until the S+H window for the next ADC conversion can begin. The subsequent sample can start before the conversion results are latched.
t_{INT}	The time from the end of the S+H window until an ADCINT flag is set (if configured). If the INTPULSEPOS bit in the ADCCTL1 register is set, t_{INT} will coincide with the conversion results being latched into the result register. If the INTPULSEPOS bit is 0, t_{INT} will coincide with the end of the S+H window. If t_{INT} triggers a read of the ADC result register (directly through DMA or indirectly by triggering an ISR that reads the result), care must be taken to ensure the read occurs after the results latch (otherwise, the previous results will be read). If the INTPULSEPOS bit is 0, and the OFFSET field in the ADCINTCYCLE register is not 0, then there will be a delay of OFFSET SYSCLK cycles before the ADCINT flag is set. This delay can be used to enter the ISR or trigger the DMA at exactly the time the sample is ready.

Table 6-14. ADC Timings

ADCCLK PRESCALE		SYSCLK CYCLES				ADCCLK CYCLES
ADCCTL2 [PRESCALE]	RATIO ADCCLK:SYSCLK	t_{EOC}	t_{LAT} (1)	$t_{INT(EARLY)}$ (2)	$t_{INT(LATE)}$	t_{EOC}
0	1	11	13	1	11	11
2	2	21	23	1	21	10.5
4	3	31	34	1	31	10.3
6	4	41	44	1	41	10.3
8	5	51	55	1	51	10.2
10	6	61	65	1	61	10.2
12	7	71	76	1	71	10.1
14	8	81	86	1	81	10.1

(1) Refer to the "ADC: DMA Read of Stale Result" advisory in the *TMS320F28002x Real-Time MCUs Silicon Errata*.
(2) By default, t_{INT} occurs one SYSCLK cycle after the S+H window if INTPULSEPOS is 0. This can be changed by writing to the OFFSET field in the ADCINTCYCLE register.

6.12.4 Temperature Sensor

6.12.4.1 Temperature Sensor Electrical Data and Timing

The temperature sensor can be used to measure the device junction temperature. The temperature sensor is sampled through an internal connection to the ADC and translated into a temperature through TI-provided software. When sampling the temperature sensor, the ADC must meet the acquisition time in Section 6.12.4.1.1.

6.12.4.1.1 Temperature Sensor Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{acc}	Temperature Accuracy	External reference		±15		°C
$t_{startup}$	Start-up time (TSNSCTL[ENABLE] to sampling temperature sensor)			500		µs
t_{acq}	ADC acquisition time		450			ns

6.12.5 Comparator Subsystem (CMPSS)

Each CMPSS contains two comparators, two reference 12-bit DACs, two digital filters, and one ramp generator. Comparators are denoted "H" or "L" within each module, where “H” and “L” represent high and low, respectively. Each comparator generates a digital output that indicates whether the voltage on the positive input is greater than the voltage on the negative input. The positive input of the comparator can be driven from an external pin or by the PGA . The negative input can be driven by an external pin or by the programmable reference 12-bit DAC. Each comparator output passes through a programmable digital filter that can remove spurious trip signals. An unfiltered output is also available if filtering is not required. A ramp generator circuit is optionally available to control the reference 12-bit DAC value for the high comparator in the subsystem. There are two outputs from each CMPSS module. These two outputs pass through the digital filters and crossbar before connecting to the ePWM modules or GPIO pin. Figure 6-44 shows the CMPSS connectivity.

Note

For more information about the muxing of CMPSS pins, see the Analog Pins and Internal Connections table and the Pin Attributes table.

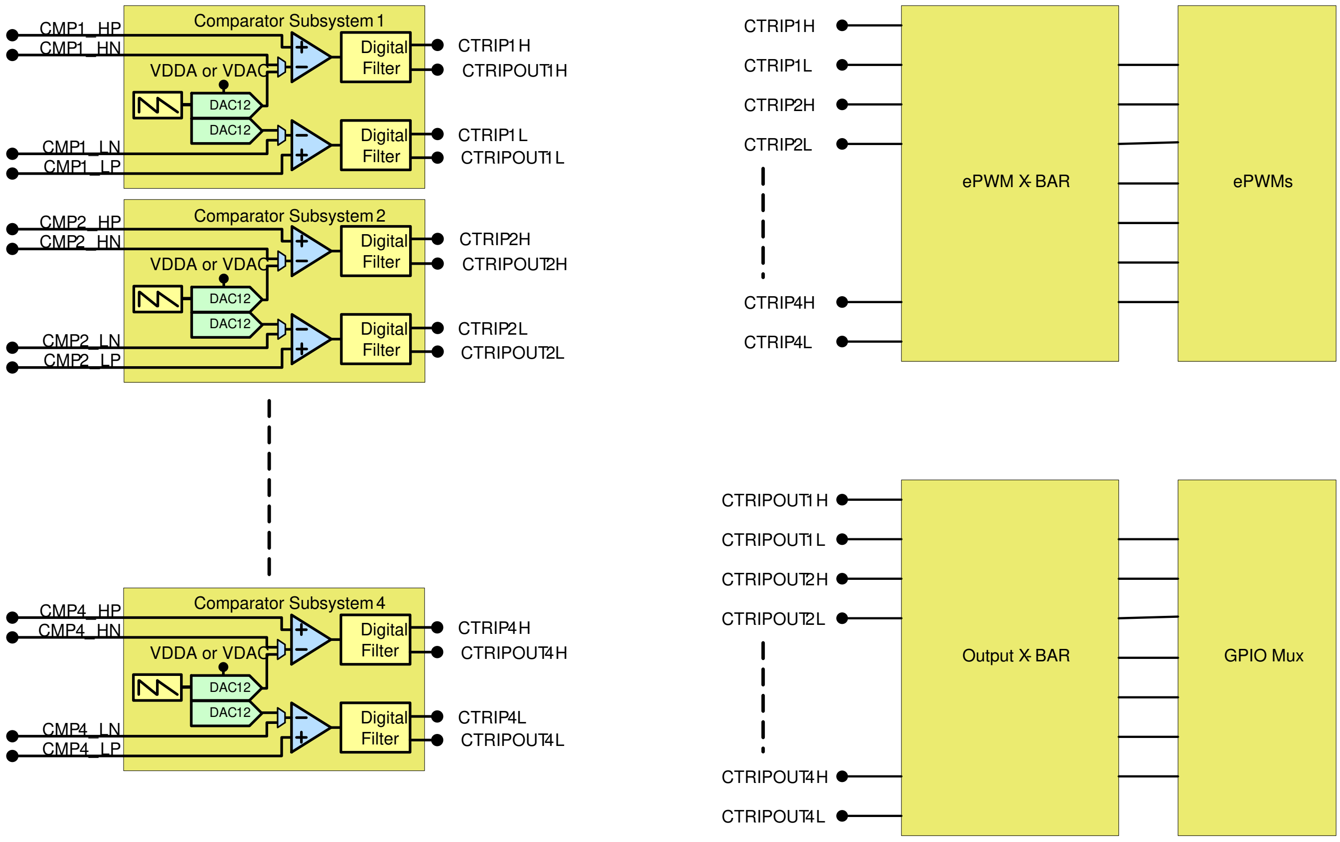


Figure 6-44. CMPSS Connectivity

6.12.5.1 CMPSS Electrical Data and Timing

Section 6.12.5.1.1 lists the comparator electrical characteristics. Figure 6-45 shows the CMPSS comparator input referred offset. Figure 6-46 shows the CMPSS comparator hysteresis.

6.12.5.1.1 Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPU	Power-up time				500	µs
Comparator input (CMPINxx) range			0		VDDA	V
Input referred offset error		Low common mode, inverting input set to 50mV	–20		20	mV
Hysteresis[1]		1x	4	12	20	LSB
		2x	17	24	33	
		3x	25	36	50	
		4x	30	48	67	
Response time (delay from CMPINx input change to output on ePWM X-BAR or Output X-BAR)		Step response		21	60	ns
		Ramp response (1.65V/µs)		26		
		Ramp response (8.25mV/µs)		30		ns
PSRR	Power Supply Rejection Ratio	Up to 250 kHz		46		dB
CMRR	Common Mode Rejection Ratio		40			dB

(1) The CMPSS DAC is used as the reference to determine how much hysteresis to apply. Therefore, hysteresis will scale with the CMPSS DAC reference voltage. Hysteresis is available for all comparator input source configurations.

CMPSS Comparator Input Referred Offset and Hysteresis

Note

The CMPSS inputs must be kept below VDDA + 0.3 V to ensure proper functional operation. If a CMPSS input exceeds this level, an internal blocking circuit isolates the internal comparator from the external pin until the external pin voltage returns below VDDA + 0.3 V. During this time, the internal comparator input is floating and can decay below VDDA within approximately 0.5 µs. After this time, the comparator could begin to output an incorrect result depending on the value of the other comparator input.

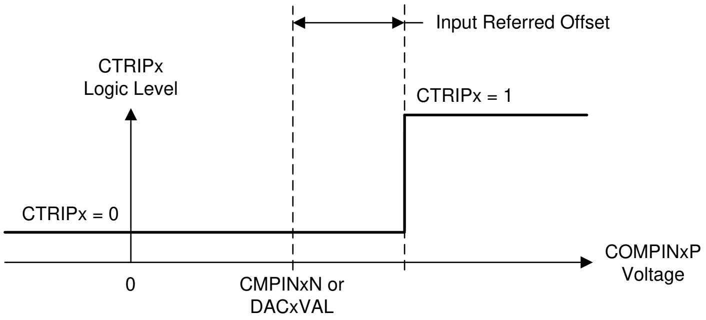


Figure 6-45. CMPSS Comparator Input Referred Offset

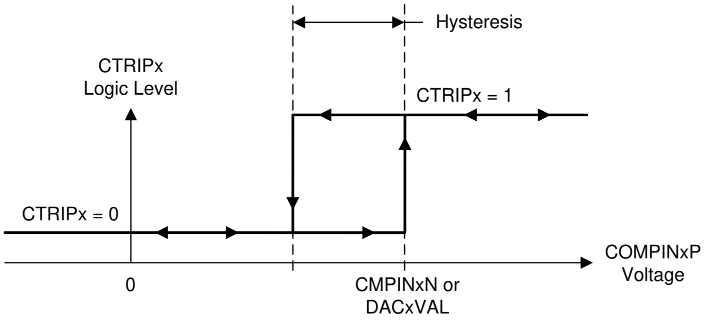


Figure 6-46. CMPSS Comparator Hysteresis

Section 6.12.5.1.2 lists the CMPSS DAC static electrical characteristics.

6.12.5.1.2 CMPSS DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMPSS DAC output range	Internal reference	0		VDDA	V
	External reference	0		VDAC(4)	
Static offset error(1)		–25		25	mV
Static gain error(1)		–2		2	% of FSR
Static DNL	Endpoint corrected	>–1		4	LSB
Static INL	Endpoint corrected	–16		16	LSB
Settling time	Settling to 1LSB after full-scale output change			1	µs
Resolution			12		bits
CMPSS DAC output disturbance(2)	Error induced by comparator trip or CMPSS DAC code change within the same CMPSS module	–100		100	LSB
CMPSS DAC disturbance time(2)				200	ns
VDAC reference voltage	When VDAC is reference	2.4	2.5 or 3.0	VDDA	V
VDAC load(3)	When VDAC is reference	6	8	10	kΩ

(1) Includes comparator input referred errors.
(2) Disturbance error may be present on the CMPSS DAC output for a certain amount of time after a comparator trip.
(3) Per active CMPSS module.
(4) The maximum output voltage is VDDA when VDAC > VDDA.

6.12.5.1.3 CMPSS Illustrative Graphs

Figure 6-47 shows the CMPSS DAC static offset. Figure 6-48 shows the CMPSS DAC static gain. Figure 6-49 shows the CMPSS DAC static linearity.

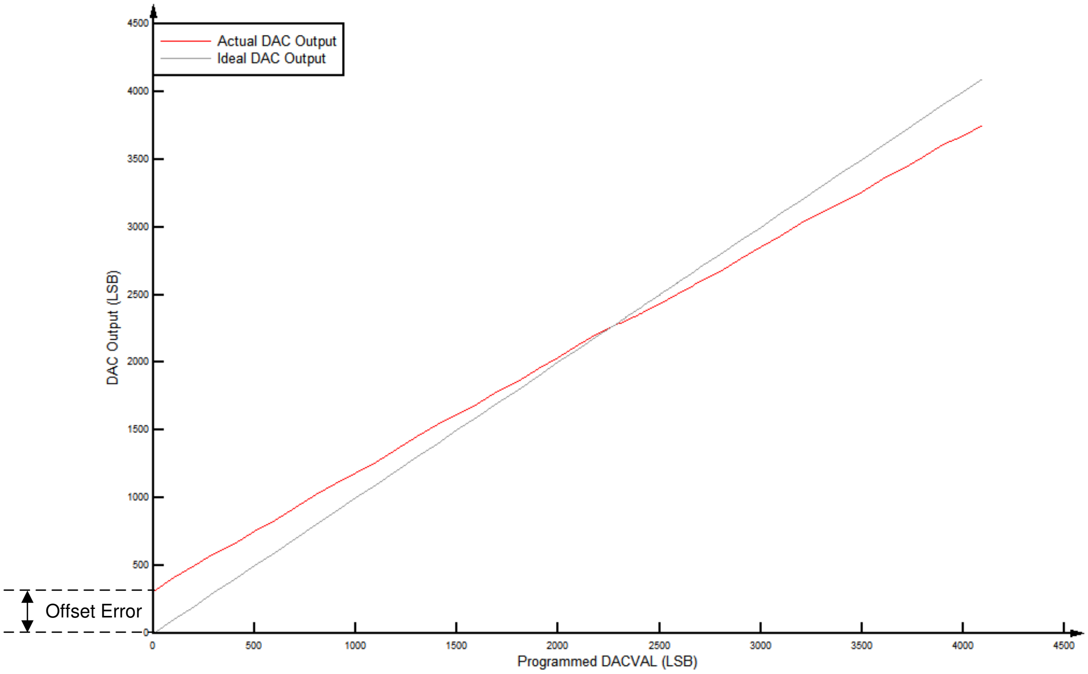


Figure 6-47. CMPSS DAC Static Offset

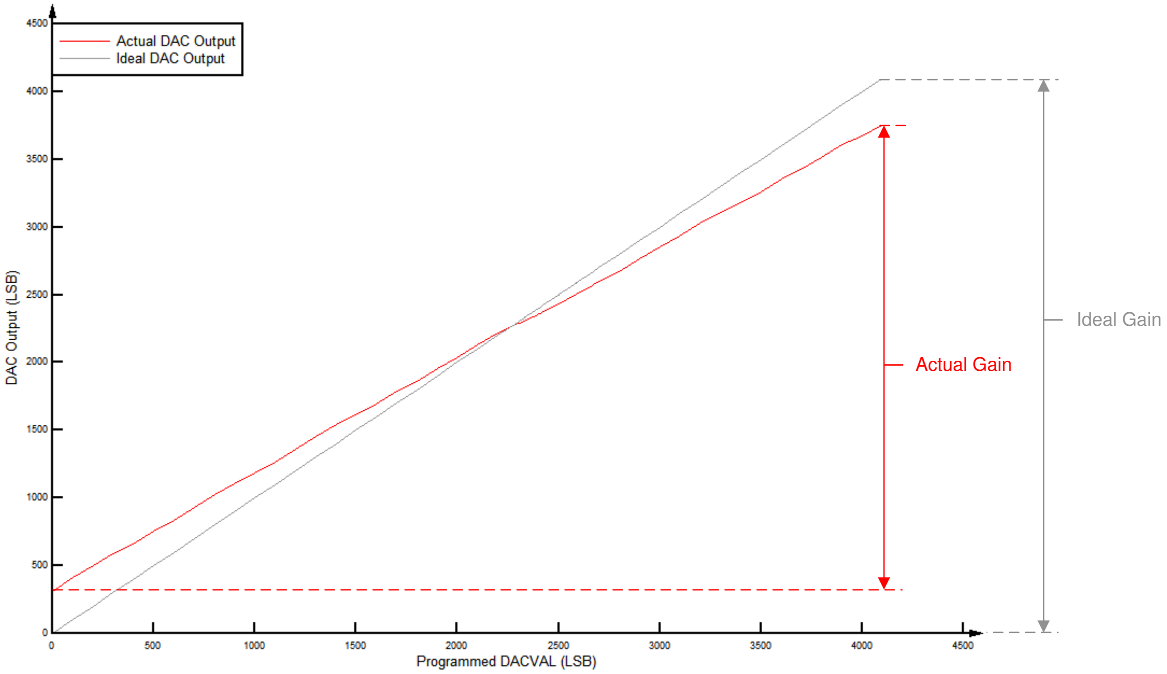


Figure 6-48. CMPSS DAC Static Gain

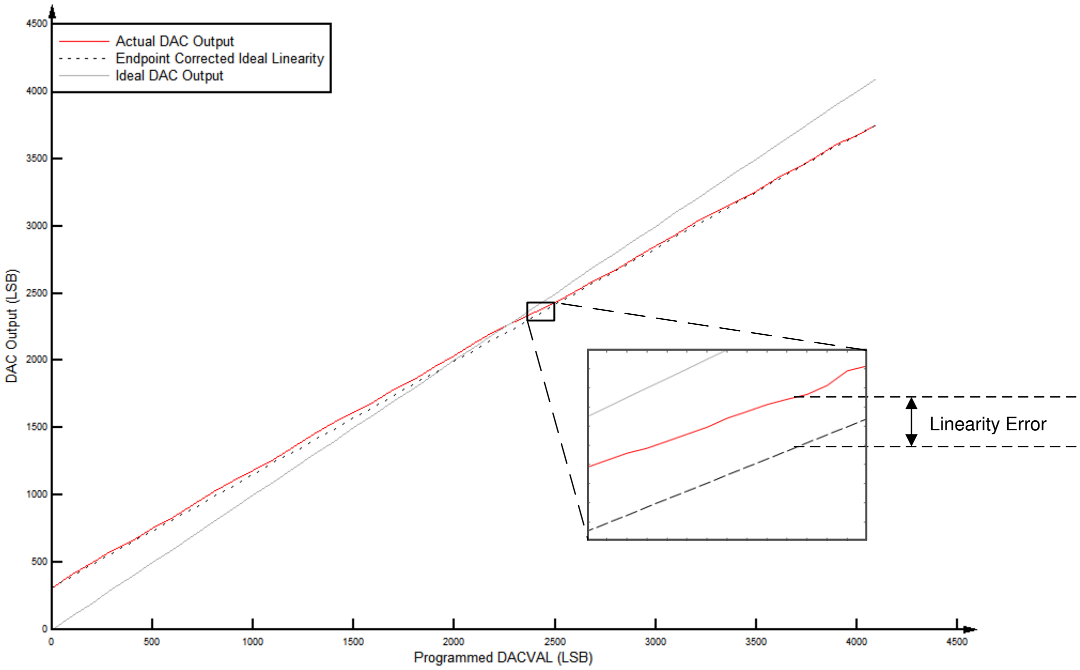


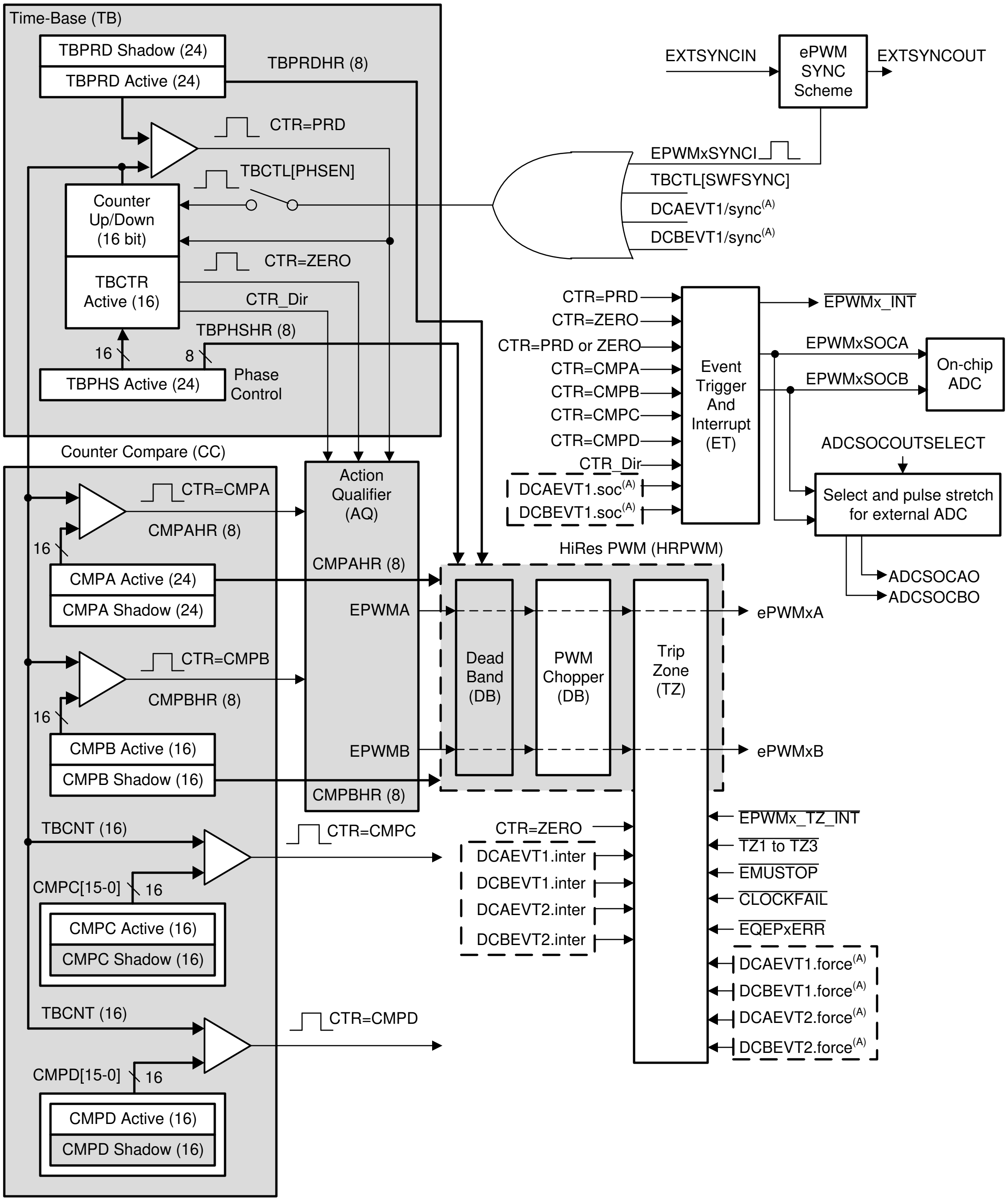
Figure 6-49. CMPSS DAC Static Linearity

6.13 Control Peripherals

6.13.1 Enhanced Pulse Width Modulator (ePWM)

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type-4 module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the ePWM type-4 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

Figure 6-50 shows the ePWM module. Figure 6-51 shows the ePWM trip input connectivity.



A. These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs.

Figure 6-50. ePWM Submodules and Critical Internal Signal Interconnects

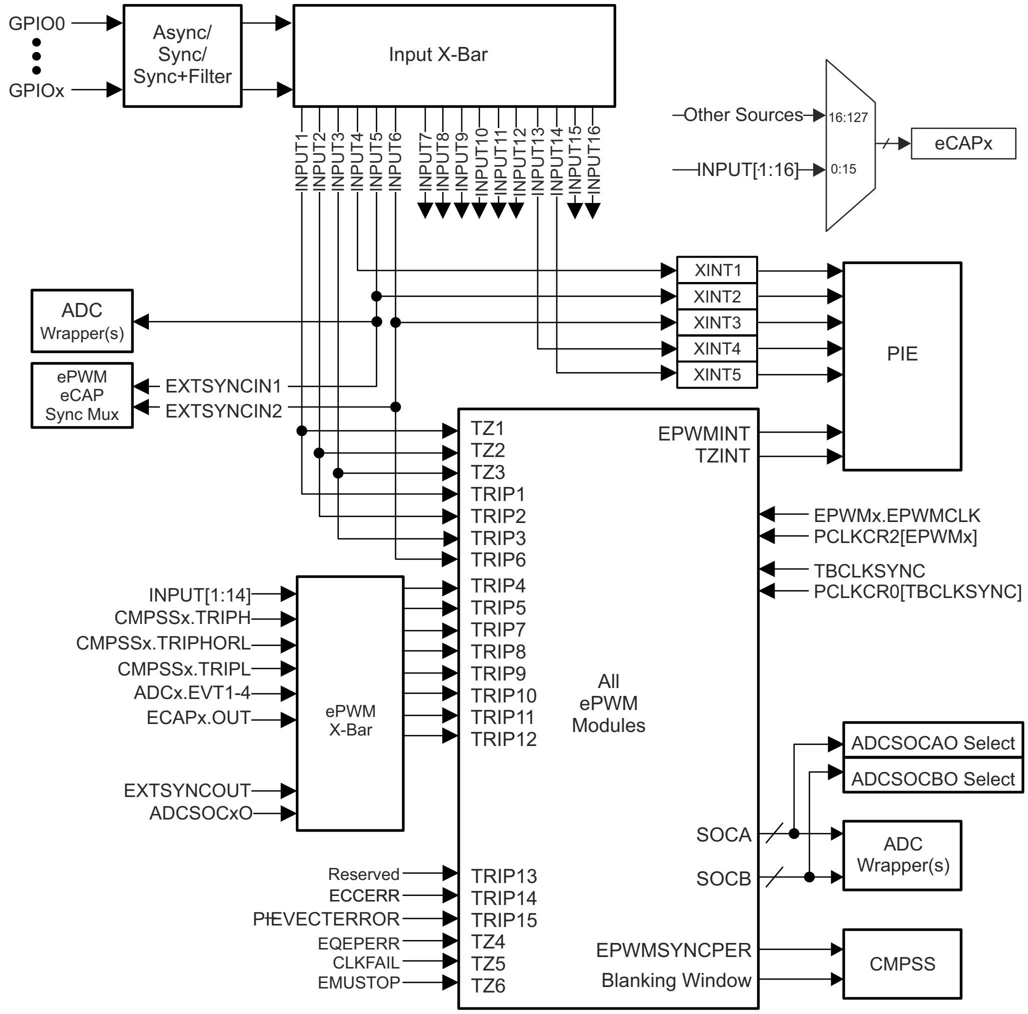
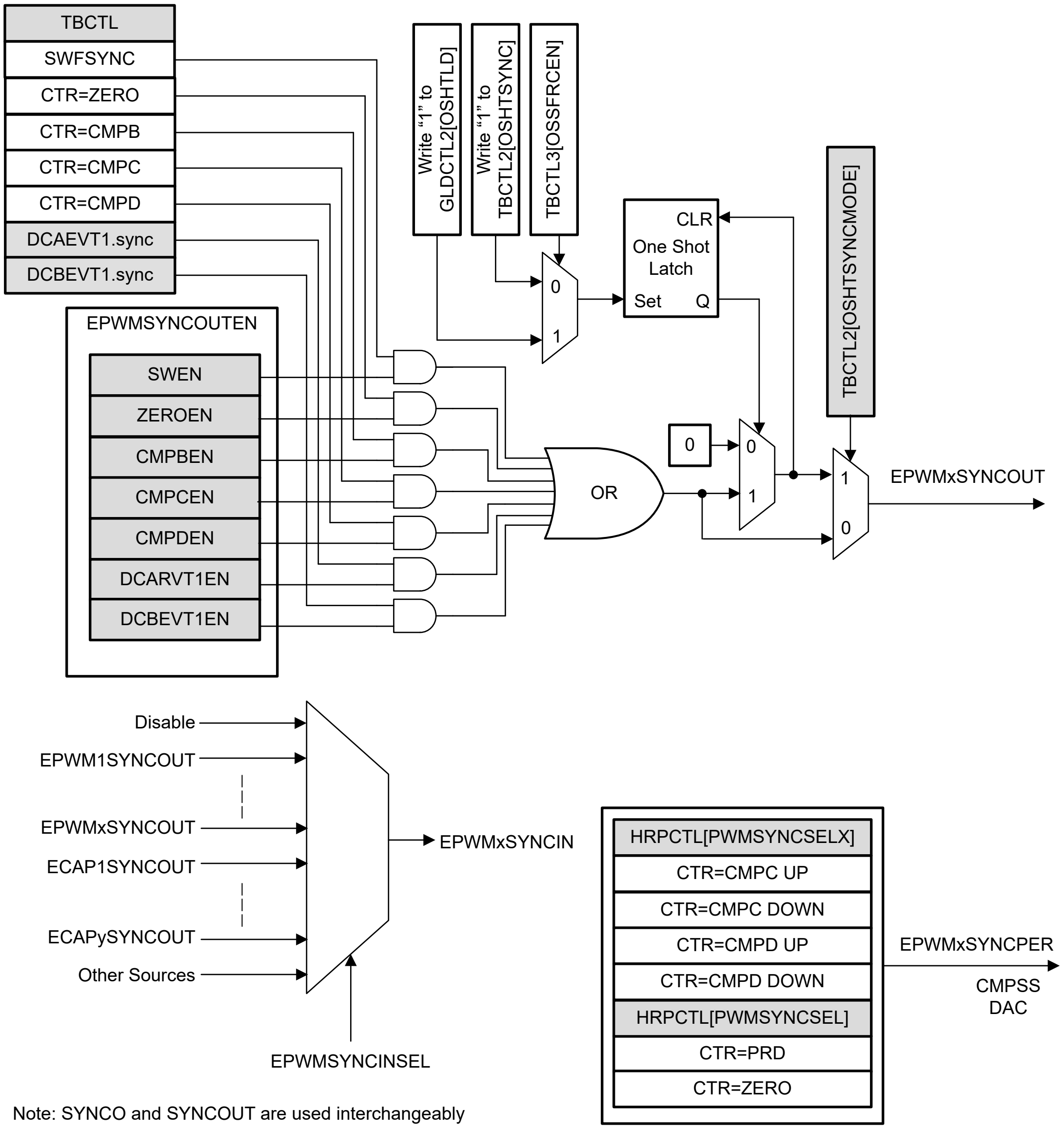


Figure 6-51. ePWM Trip Input Connectivity

6.13.1.1 Control Peripherals Synchronization

The ePWM and eCAP synchronization scheme on the device provides flexibility in partitioning the ePWM and eCAP modules and allows localized synchronization within the modules. Like the other peripherals, the partitioning of the ePWM and eCAP modules needs to be done using the CPUSELx registers. Figure 6-52 shows the synchronization scheme.



Note: SYNCO and SYNCOUT are used interchangeably

Figure 6-52. Synchronization Chain Architecture

6.13.1.2 ePWM Electrical Data and Timing

Section 6.13.1.2.1 lists the ePWM timing requirements and Section 6.13.1.2.2 lists the ePWM switching characteristics. For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.13.1.2.1 ePWM Timing Requirements

			MIN	MAX	UNIT
$t_{w(SYNCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		

6.13.1.2.2 ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

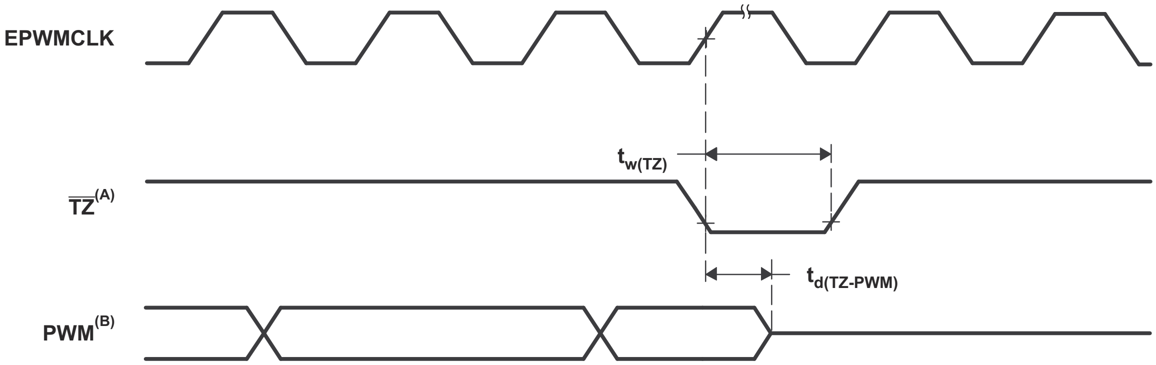
PARAMETER		MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low	20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width	$8t_{c(SYSCLK)}$		cycles
$t_{d(TZ\text{-}PWM)}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low Delay time, trip input active to PWM Hi-Z		25	ns

6.13.1.2.3 Trip-Zone Input Timing

Section 6.13.1.2.3.1 lists the trip-zone input timing requirements. Figure 6-53 shows the PWM Hi-Z characteristics. For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.13.1.2.3.1 Trip-Zone Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZx}$ input low	Asynchronous	$1t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		cycles
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		cycles



A. $\overline{TZ}$: $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, TRIP1–TRIP12

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 6-53. PWM Hi-Z Characteristics

6.13.1.3 External ADC Start-of-Conversion Electrical Data and Timing

Section 6.13.1.3.1 lists the external ADC start-of-conversion switching characteristics. Figure 6-54 shows the $\overline{\text{ADCSOCAO}}$ or $\overline{\text{ADCSOCBO}}$ timing.

6.13.1.3.1 External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCL)}$	Pulse duration, $\overline{\text{ADCSOCxO}}$ low	$32t_{c(SYSCLK)}$		cycles

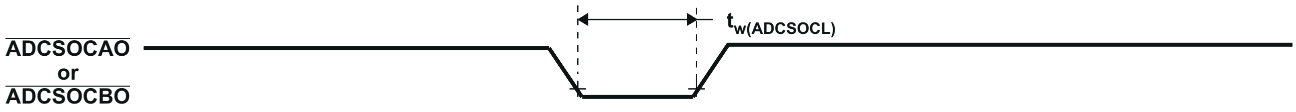


Figure 6-54. $\overline{\text{ADCSOCAO}}$ or $\overline{\text{ADCSOCBO}}$ Timing

6.13.2 High-Resolution Pulse Width Modulator (HRPWM)

The HRPWM combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module, there are two HR outputs:

- HR Duty and Deadband control on Channel A
- HR Duty and Deadband control on Channel B

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A, B, phase, period and deadband registers of the ePWM module.

Note

The minimum HRPWMCLK frequency allowed for HRPWM is 60 MHz.

6.13.2.1 HRPWM Electrical Data and Timing

Section 6.13.2.1.1 lists the high-resolution PWM switching characteristics.

6.13.2.1.1 High-Resolution PWM Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(1)		150	310	ps

(1) The MEP step size will be largest at high temperature and minimum voltage on V_{DD}. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO functions in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

6.13.3 Enhanced Capture and High-Resolution Capture (eCAP, HRCAP)

The eCAP module can be used in systems where accurate timing of external events is important. eCAP/HRCAP on this device is Type-2.

Applications for eCAP include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed through Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module includes the following features:

- 4-event time-stamp registers (each 32 bits)
- Edge-polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single shot capture of up to four event timestamps
- Continuous mode capture of timestamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All of the above resources dedicated to a single input pin
- When not used in capture mode, the eCAP module can be configured as a single-channel PWM output (APWM).

The capture functionality of the Type-1 eCAP is enhanced from the Type-0 eCAP with the following added features:

- Event filter reset bit
  - Writing a 1 to ECCTL2[CTRFILTRESET] will clear the event filter, the modulo counter, and any pending interrupts flags. Resetting the bit is useful for initialization and debug.
- Modulo counter status bits
  - The modulo counter (ECCTL2 [MODCTRSTS]) indicates which capture register will be loaded next. In the Type-0 eCAP, it was not possible to know current state of modulo counter.
- DMA trigger source
  - eCAPxDMA is added as a DMA trigger. CEVT[1–4] can be configured as the source for eCAPxDMA.
- Input multiplexer
  - ECCTL0 [INPUTSEL] selects one of 128 input signals.
- EALLOW protection
  - EALLOW protection is added to critical registers. To maintain software compatibility with the Type-0 eCAP, configure DEV_CFG_REGS.ECAPTYPE to make these registers unprotected.

The capture functionality of the Type-2 eCAP is enhanced from the Type-1 eCAP with the following added features:

- ECAPxSYNCINSEL register
  - The ECAPSxYNCINSEL register is added for each eCAP to select an external SYNCIN. Every eCAP can have a separate SYNCIN signal.

The eCAP inputs connect to any GPIO input through the Input X-BAR. The APWM outputs connect to GPIO pins through the Output X-BAR to OUTPUTx positions in the GPIO mux. See Section 5.4.3 and Section 5.4.4.

The eCAP module is clocked by PERx.SYSCLK.

The clock enable bits (ECAP1–ECAP3) in the PCLKCR3 register turn off the eCAP module individually (for low-power operation). Upon reset, ECAP1ENCLK is set to low, indicating that the peripheral clock is off.

6.13.3.1 High-Resolution Capture (HRCAP)

The eCAP3 module can be configured as high-resolution capture (HRCAP) submodules. The HRCAP submodule measures the difference, in time, between pulses asynchronously to the system clock. This submodule is new to the eCAP Type 1 module, and features many enhancements over the Type 0 HRCAP module.

Applications for the HRCAP include:

- Capacitive touch applications
- High-resolution period and duty-cycle measurements of pulse train cycles
- Instantaneous speed measurements
- Instantaneous frequency measurements
- Voltage measurements across an isolation boundary
- Distance/sonar measurement and scanning
- Flow measurements

The HRCAP submodule includes the following features:

- Pulse-width capture in either non-high-resolution or high-resolution modes
- Absolute mode pulse-width capture
- Continuous or "one-shot" capture
- Capture on either falling or rising edge
- Continuous mode capture of pulse widths in 4-deep buffer
- Hardware calibration logic for precision high-resolution capture
- All of the resources in this list are available on any pin using the Input X-BAR.

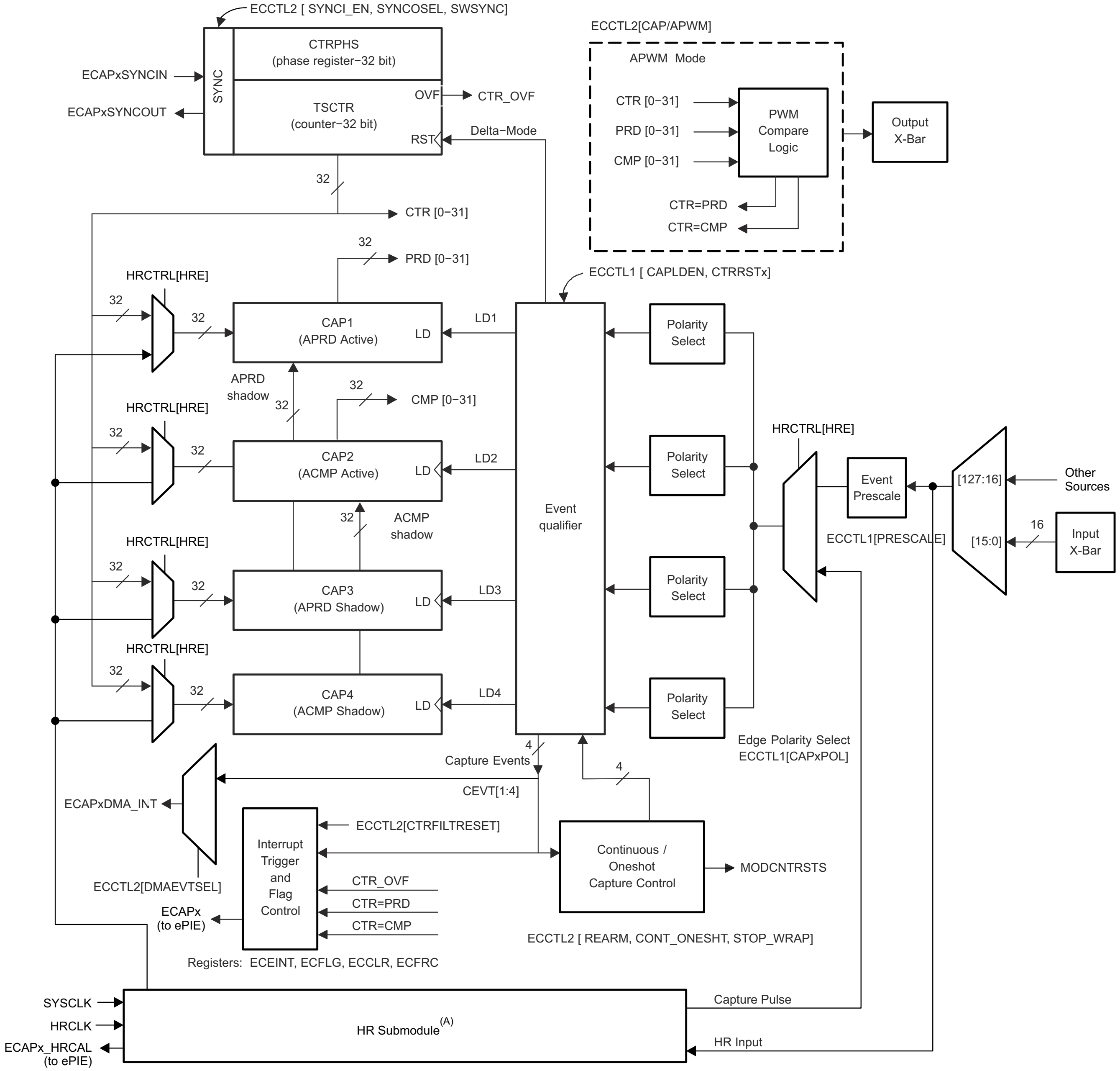
The HRCAP submodule includes one high-resolution capture channel in addition to a calibration block. The calibration block allows the HRCAP submodule to be continually recalibrated, at a set interval, with no “down time”. Because the HRCAP submodule now uses the same hardware as its respective eCAP, if the HRCAP is used, the corresponding eCAP will be unavailable.

Each high-resolution-capable channel has the following independent key resources.

- All hardware of the respective eCAP
- High-resolution calibration logic
- Dedicated calibration interrupt

6.13.3.2 eCAP and HRCAP Block Diagram

Figure 6-55 shows the eCAP and HRCAP block diagram.



A. The HRCAP submodule is not available on all eCAP modules; in this case, the high-resolution muxes and hardware are not implemented.

Figure 6-55. eCAP and HRCAP Block Diagram

6.13.3.3 eCAP/HRCAP Synchronization

The eCAP modules can be synchronized with each other by selecting a common SYNCIN source. SYNCIN source for eCAP can be either software sync-in or external sync-in. The external sync-in signal can come from EPWM, eCAP, or X-Bar. The SYNC signal is defined by the selection in the ECAPxSYNCINSEL[SEL] bit for ECAPx as shown in Figure 6-56.

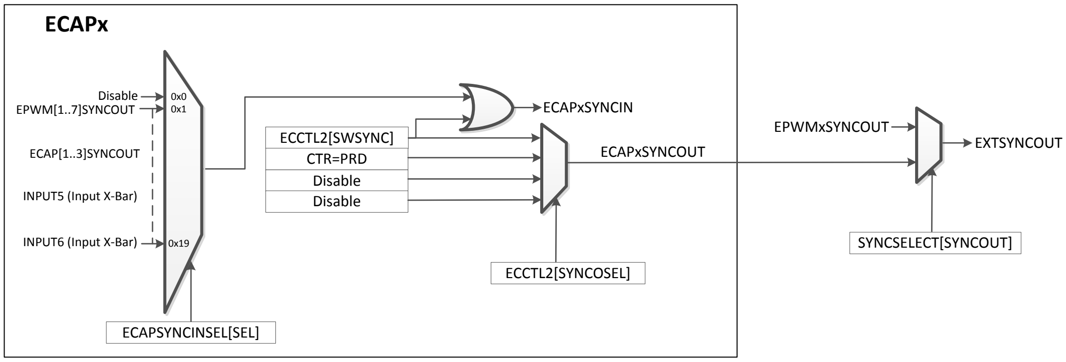


Figure 6-56. eCAPSynchronization Scheme

6.13.3.4 eCAP Electrical Data and Timing

Section 6.13.3.4.1 lists the eCAP timing requirements and Section 6.13.3.4.2 lists the eCAP switching characteristics.

6.13.3.4.1 eCAP Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SYSCLK)}$			ns
		Synchronous	$2t_{c(SYSCLK)}$			
		With input qualifier	$1t_{c(SYSCLK)} + t_{w\_(IQSW)}$			

6.13.3.4.2 eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low	20			ns

6.13.3.5 HRCAP Electrical Data and Timing

Section 6.13.3.5.1 lists the HRCAP switching characteristics. Figure 6-57 shows the HRCAP accuracy precision and resolution. Figure 6-58 shows the HRCAP standard deviation characteristics.

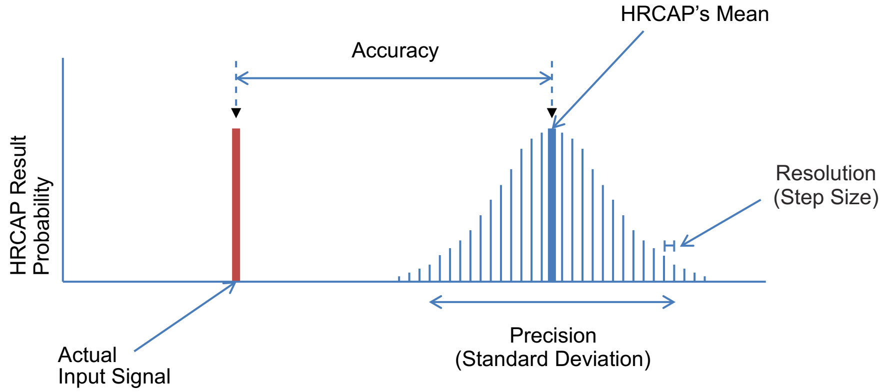
6.13.3.5.1 HRCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input pulse width		110			ns
Accuracy(1) (2) (3) (4)	Measurement length ≤ 5 µs		±390	540	ps
	Measurement length > 5 µs		±450	1450	ps
Standard deviation			See HRCAP Standard Deviation Characteristics figure		
Resolution			300		ps

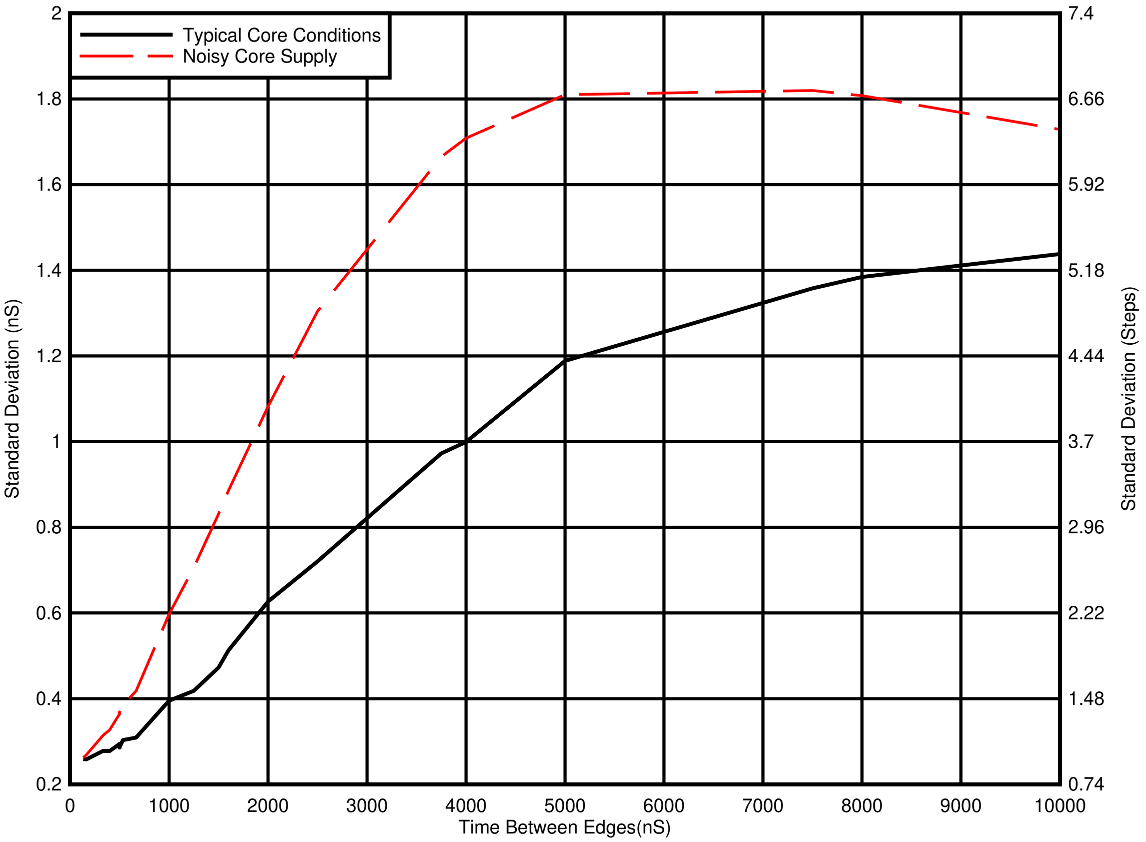
(1) Value obtained using an oscillator of 100 PPM, oscillator accuracy directly affects the HRCAP accuracy.
(2) Measurement is completed using rising-rising or falling-falling edges
(3) Opposite polarity edges will have an additional inaccuracy due to the difference between V_{IH} and V_{IL}. This effect is dependent on the signal's slew rate.
(4) Accuracy only applies to time-converted measurements.

6.13.3.5.2 HRCAP Figure and Graph



A. The HRCAP has some variation in performance, this results in a probability distribution which is described using the following terms:
  - Accuracy: The time difference between the input signal and the mean of the HRCAP's distribution.
  - Precision: The width of the HRCAP's distribution, this is given as a standard deviation.
  - Resolution: The minimum measurable increment.

Figure 6-57. HRCAP Accuracy Precision and Resolution



A. Typical core conditions: All peripheral clocks are enabled.

B. Noisy core supply: All core clocks are enabled and disabled with a regular period during the measurement.

C. Fluctuations in current and voltage on the 1.2-V rail cause the standard deviation of the HRCAP to rise. Care should be taken to ensure that the 1.2-V supply is clean, and that noisy internal events, such as enabling and disabling clock trees, have been minimized while using the HRCAP.

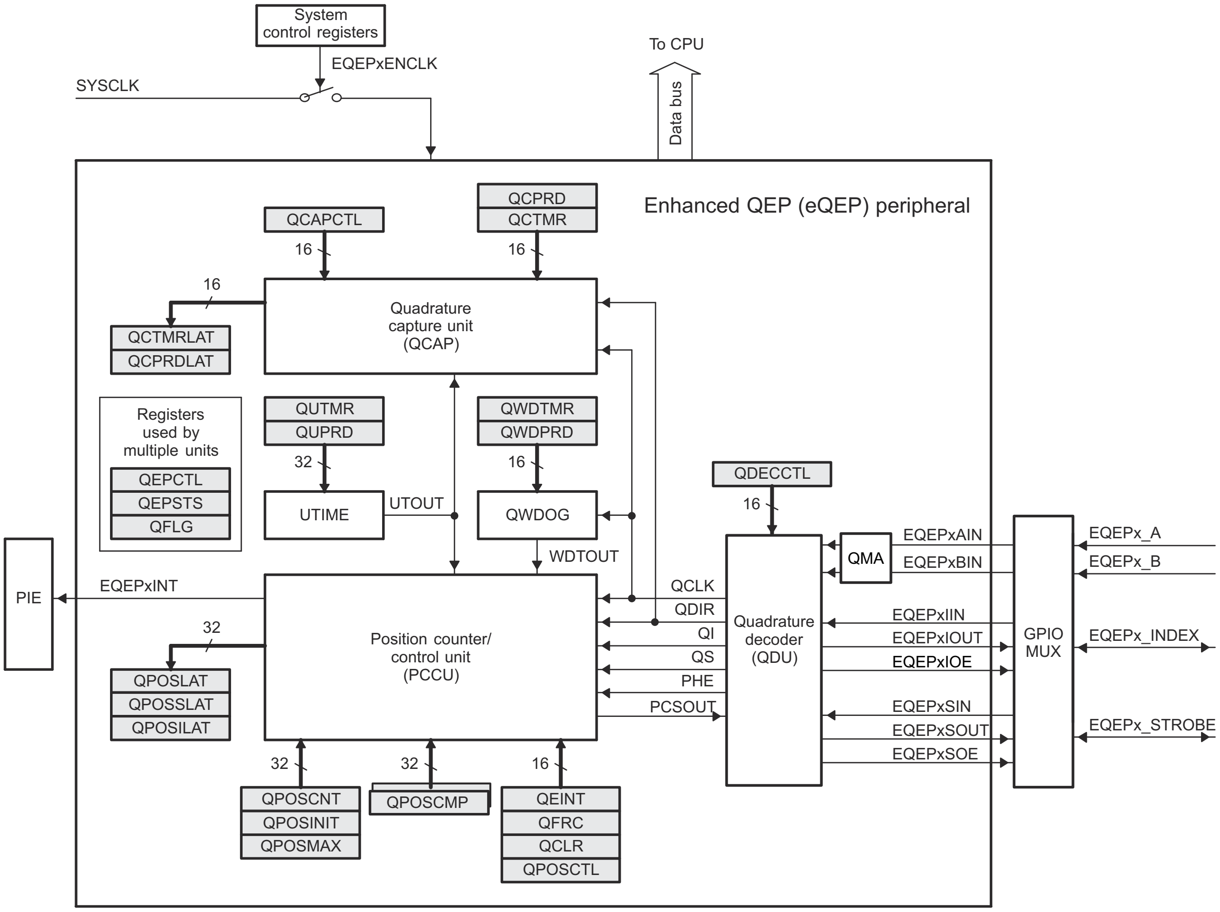
Figure 6-58. HRCAP Standard Deviation Characteristics

6.13.4 Enhanced Quadrature Encoder Pulse (eQEP)

The eQEP module on this device is Type-2. The eQEP interfaces directly with linear or rotary incremental encoders to obtain position, direction, and speed information from rotating machines used in high-performance motion and position control systems.

The eQEP peripheral contains the following major functional units (see Figure 6-59):

- Programmable input qualification for each pin (part of the GPIO MUX)
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)
- Quadrature Mode Adapter (QMA)



Copyright © 2017, Texas Instruments Incorporated

Figure 6-59. eQEP Block Diagram

6.13.4.1 eQEP Electrical Data and Timing

Section 6.13.4.1.1 lists the eQEP timing requirements and Section 6.13.4.1.2 lists the eQEP switching characteristics. For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.13.4.1.1 eQEP Timing Requirements

			MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Synchronous[1]	$2t_{c(SYSCLK)}$		cycles
		Synchronous with input qualifier	$2[1t_{c(SYSCLK)} + t_{w(IQSW)}]$		
$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous[1]	$2t_{c(SYSCLK)}$		cycles
		Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		
$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous[1]	$2t_{c(SYSCLK)}$		cycles
		Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		
$t_{w(STROBH)}$	QEP Strobe High time	Synchronous[1]	$2t_{c(SYSCLK)}$		cycles
		Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		
$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous[1]	$2t_{c(SYSCLK)}$		cycles
		Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		

(1) The GPIO GPxQSELn Asynchronous mode should not be used for eQEP module input pins.

6.13.4.1.2 eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		$5t_{c(SYSCLK)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		$7t_{c(SYSCLK)}$	cycles

6.14 Communications Peripherals

6.14.1 Controller Area Network (CAN)

Note

The CAN module uses the IP known as *DCAN*. This document uses the names *CAN* and *DCAN* interchangeably to reference this peripheral.

The CAN module implements the following features:

- Complies with ISO11898-1 (Bosch® CAN protocol specification 2.0 A and B)
- Bit rates up to 1 Mbps
- Multiple clock sources
- 32 message objects (mailboxes), each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard (11-bit) or extended (29-bit) identifier
  - Supports programmable identifier receive mask
  - Supports data and remote frames
  - Holds 0 to 8 bytes of data
  - Parity-checked configuration and data RAM
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loopback modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus on after bus-off state by a programmable 32-bit timer
- Two interrupt lines
- DMA support

Note

For a CAN bit clock of 100 MHz, the smallest bit rate possible is 3.90625 kbps.

Note

The accuracy of the on-chip zero-pin oscillator is in Section 6.11.3.5.1. Depending on parameters such as the CAN bit timing settings, bit rate, bus length, and propagation delay, the accuracy of this oscillator may not meet the requirements of the CAN protocol. In this situation, an external clock source must be used.

Figure 6-60 shows the CAN block diagram.

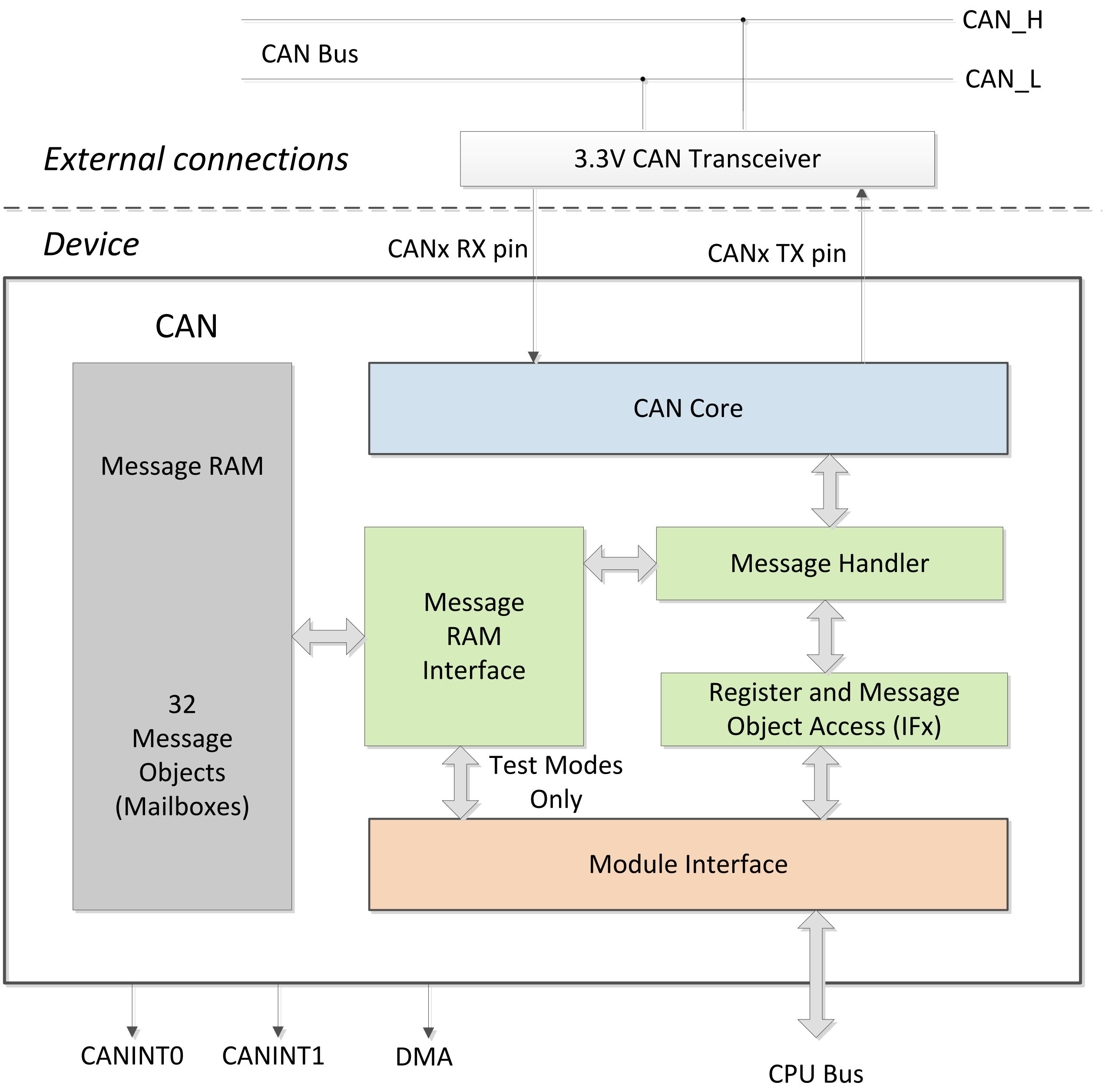


Figure 6-60. CAN Block Diagram

6.14.2 Inter-Integrated Circuit (I2C)

The I2C module has the following features:

- Compliance with the NXP Semiconductors I^{2}C-bus specification (version 2.1):
  - Support for 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate from 10 kbps up to 400 kbps (Fast-mode)
- One 16-byte receive FIFO and one 16-byte transmit FIFO
- Supports two ePIE interrupts
  - I2Cx interrupt – Any of the below conditions can be configured to generate an I2Cx interrupt:
    - Transmit Ready
    - Receive Ready
    - Register-Access Ready
    - No-Acknowledgment
    - Arbitration-Lost
    - Stop Condition Detected
    - Addressed-as-Slave
  - I2Cx_FIFO interrupts:
    - Transmit FIFO interrupt
    - Receive FIFO interrupt
- Module enable and disable capability
- Free data format mode

Figure 6-61 shows how the I2C peripheral module interfaces within the device.

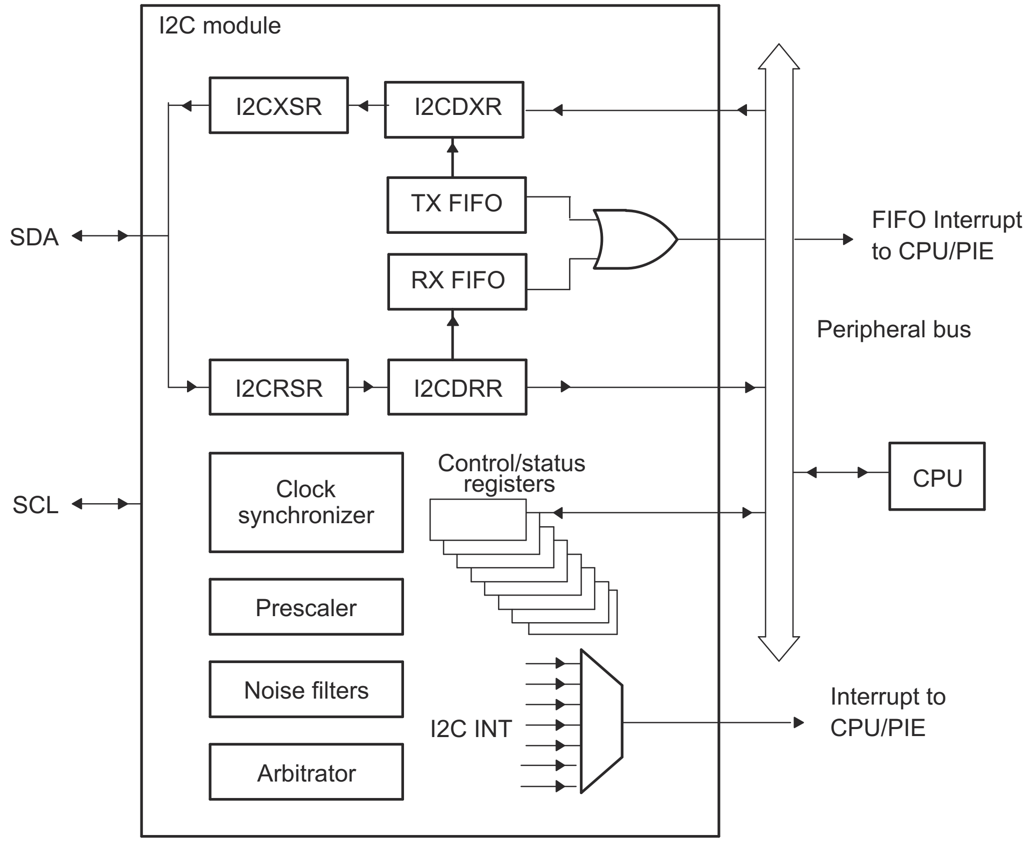


Figure 6-61. I2C Peripheral Module Interfaces

6.14.2.1 I2C Electrical Data and Timing

Section 6.14.2.1.1 lists the I2C timing requirements. Section 6.14.2.1.2 lists the I2C switching characteristics. Figure 6-62 shows the I2C timing diagram.

Note

To meet all of the I2C protocol timing specifications, the I2C module clock must be configured in the range from 7 MHz to 12 MHz.

6.14.2.1.1 I2C Timing Requirements

NO.			MIN	MAX	UNIT
Standard mode					
T0	f_{mod}	I2C module frequency	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	4.0		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	4.7		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	250 (2)		ns
T5	$t_{r(SDA)}$	Rise time, SDA		1000 (1)	ns
T6	$t_{r(SCL)}$	Rise time, SCL		1000 (1)	ns
T7	$t_{f(SDA)}$	Fall time, SDA		300	ns
T8	$t_{f(SCL)}$	Fall time, SCL		300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	4.0		µs
T10	$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by filter	0	50	ns
T11	C_b	capacitance load on each bus line		400	pF
Fast mode					
T0	f_{mod}	I2C module frequency	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	0.6		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	0.6		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	100		ns
T5	$t_{r(SDA)}$	Rise time, SDA	20	300	ns
T6	$t_{r(SCL)}$	Rise time, SCL	20	300	ns
T7	$t_{f(SDA)}$	Fall time, SDA	11.4	300	ns
T8	$t_{f(SCL)}$	Fall time, SCL	11.4	300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	0.6		µs
T10	$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by filter	0	50	ns
T11	C_b	capacitance load on each bus line		400	pF

(1) In order to minimize the rise time, TI recommends using a strong pullup on both the SDA and SCL bus lines on the order of 2.2-kΩ net pullup resistance. It is also recommended that the value of the pullup resistance used on both SCL and SDA pins be matched.
(2) The C2000 I2C is a Fast-mode device. There is a limitation when using the I2C as a target transmitter with a standard mode host. For more information, see the *TMS320F28002x Real-Time MCUs Silicon Errata*.

6.14.2.1.2 I2C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
Standard mode						
S1	f_{SCL}	SCL clock frequency		0	100	kHz
S2	T_{SCL}	SCL clock period		10		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		4.7		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		4.0		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		4.7		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			3.45	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			3.45	µs
S8	I_I	Input current on pins	$0.1\ V_{bus} < V_i < 0.9\ V_{bus}$	–10	10	µA
Fast mode						
S1	f_{SCL}	SCL clock frequency		0	400	kHz
S2	T_{SCL}	SCL clock period		2.5		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		1.3		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		0.6		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		1.3		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			0.9	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			0.9	µs
S8	I_I	Input current on pins	$0.1\ V_{bus} < V_i < 0.9\ V_{bus}$	–10	10	µA

6.14.2.1.3 I2C Timing Diagram

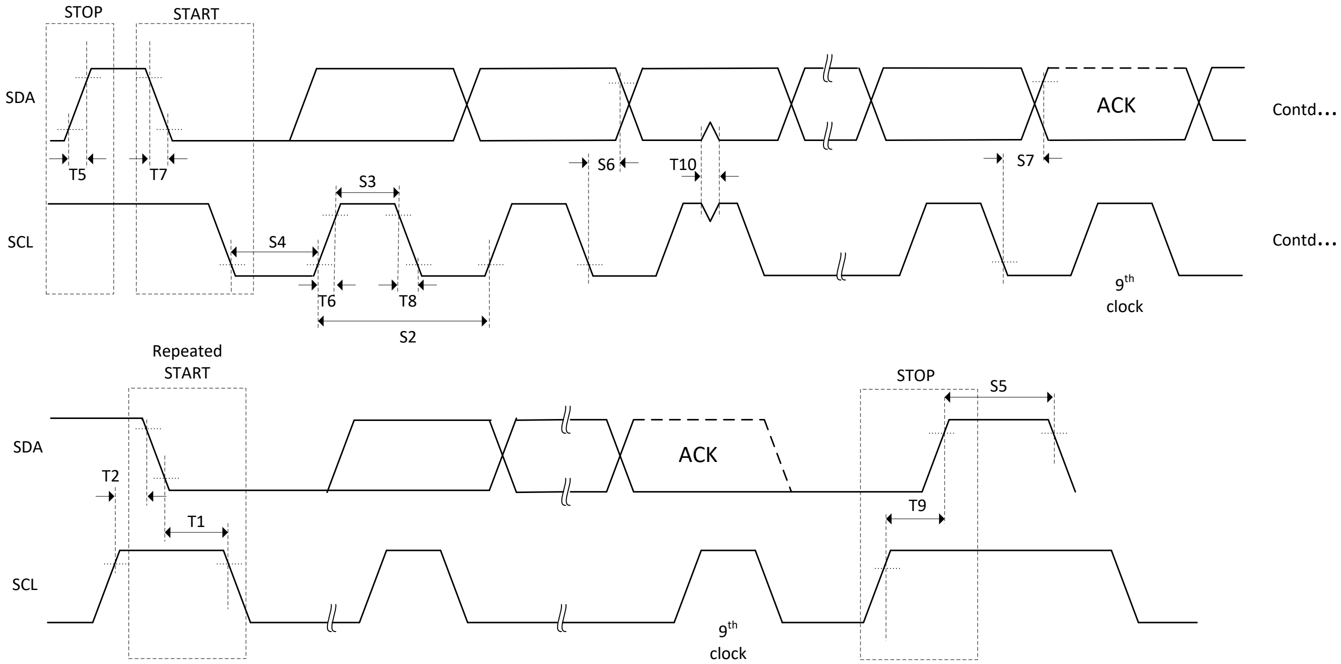


Figure 6-62. I2C Timing Diagram

6.14.3 Power Management Bus (PMBus) Interface

The PMBus module has the following features:

- Compliance with the SMI Forum PMBus Specification (Part I v1.0 and Part II v1.1)
- Support for master and slave modes
- Support for I2C mode
- Support for two speeds:
  - Standard Mode: Up to 100 kHz
  - Fast Mode: 400 kHz
- Packet error checking
- CONTROL and ALERT signals
- Clock high and low time-outs
- Four-byte transmit and receive buffers
- One maskable interrupt, which can be generated by several conditions:
  - Receive data ready
  - Transmit buffer empty
  - Slave address received
  - End of message
  - ALERT input asserted
  - Clock low time-out
  - Clock high time-out
  - Bus free

Figure 6-63 shows the PMBus block diagram.

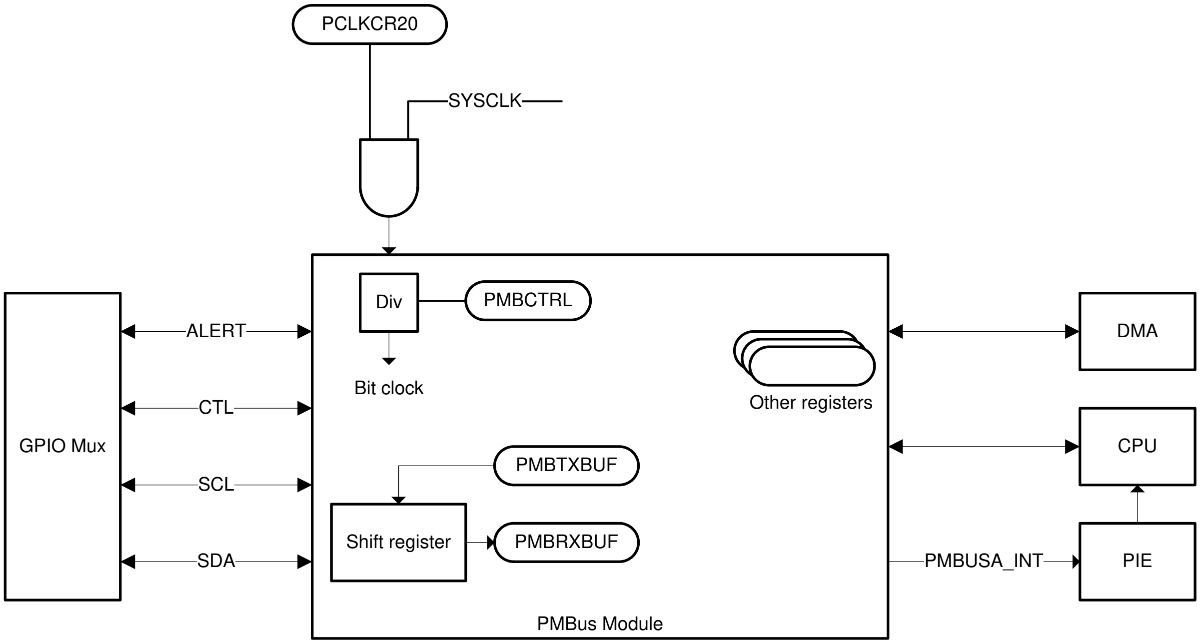


Figure 6-63. PMBus Block Diagram

6.14.3.1 PMBus Electrical Data and Timing

Section 6.14.3.1.1 lists the PMBus electrical characteristics. Section 6.14.3.1.2 lists the PMBUS fast mode switching characteristics. Section 6.14.3.1.3 lists the PMBUS standard mode switching characteristics.

6.14.3.1.1 PMBus Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Valid low-level input voltage				0.8	V
V_{IH}	Valid high-level input voltage		2.1		VDDIO	V
V_{OL}	Low-level output voltage	At I_{pullup} = 4 mA			0.4	V
I_{OL}	Low-level output current	$V_{OL} \leq 0.4$ V	4			mA
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0		50	ns
I_i	Input leakage current on each pin	0.1 Vbus < Vi < 0.9 Vbus	–10		10	µA
C_i	Capacitance on each pin				10	pF

6.14.3.1.2 PMBus Fast Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{mod} (1)	PMBus module frequency		SYSCLK / 32		10	MHz
f_{SCL}	SCL clock frequency		10		400	kHz
t_{BUF}	Bus free time between STOP and START conditions		1.3			µs
$t_{HD;STA}$	START condition hold time -- SDA fall to SCL fall delay		0.6			µs
$t_{SU;STA}$	Repeated START setup time -- SCL rise to SDA fall delay		0.6			µs
$t_{SU;STO}$	STOP condition setup time -- SCL rise to SDA rise delay		0.6			µs
$t_{HD;DAT}$	Data hold time after SCL fall		300			ns
$t_{SU;DAT}$	Data setup time before SCL rise		100			ns
$t_{Timeout}$	Clock low time-out		25		35	ms
t_{LOW}	Low period of the SCL clock		1.3			µs
t_{HIGH}	High period of the SCL clock		0.6		50	µs
$t_{LOW;SEXT}$	Cumulative clock low extend time (slave device)	From START to STOP			25	ms
$t_{LOW;MEXT}$	Cumulative clock low extend time (master device)	Within each byte			10	ms
t_r	Rise time of SDA and SCL	5% to 95%	20		300	ns
t_f	Fall time of SDA and SCL	95% to 5%	20		300	ns

(1) Supports only Standard and Fast mode.

6.14.3.1.3 PMBus Standard Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{mod} (1)	PMBus module frequency		SYSCLK / 32		10	MHz
f_{SCL}	SCL clock frequency		10		100	kHz
t_{BUF}	Bus free time between STOP and START conditions		4.7			µs
$t_{HD;STA}$	START condition hold time -- SDA fall to SCL fall delay		4			µs
$t_{SU;STA}$	Repeated START setup time -- SCL rise to SDA fall delay		4.7			µs
$t_{SU;STO}$	STOP condition setup time -- SCL rise to SDA rise delay		4			µs
$t_{HD;DAT}$	Data hold time after SCL fall		300			ns
$t_{SU;DAT}$	Data setup time before SCL rise		250			ns
$t_{Timeout}$	Clock low time-out		25		35	ms
t_{LOW}	Low period of the SCL clock		4.7			µs
t_{HIGH}	High period of the SCL clock		4		50	µs
$t_{LOW;SEXT}$	Cumulative clock low extend time (slave device)	From START to STOP			25	ms
$t_{LOW;MEXT}$	Cumulative clock low extend time (master device)	Within each byte			10	ms
t_r	Rise time of SDA and SCL				1000	ns
t_f	Fall time of SDA and SCL				300	ns

(1) Supports only Standard and Fast mode.

6.14.4 Serial Communications Interface (SCI)

The SCI is a 2-wire asynchronous serial port, commonly known as a UART. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format

The SCI receiver and transmitter each have a 16-level-deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication. To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register.

Features of the SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin
  - Baud rate programmable to 64K different rates
- Data-word format
  - 1 start bit
  - Data-word length programmable from 1 to 8 bits
  - Optional even/odd/no parity bit
  - 1 or 2 stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ format
- Auto baud-detect hardware logic
- 16-level transmit and receive FIFO

Note

All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte (bits 7–0), and the upper byte (bits 15–8) is read as zeros. Writing to the upper byte has no effect.

Figure 6-64 shows the SCI block diagram.

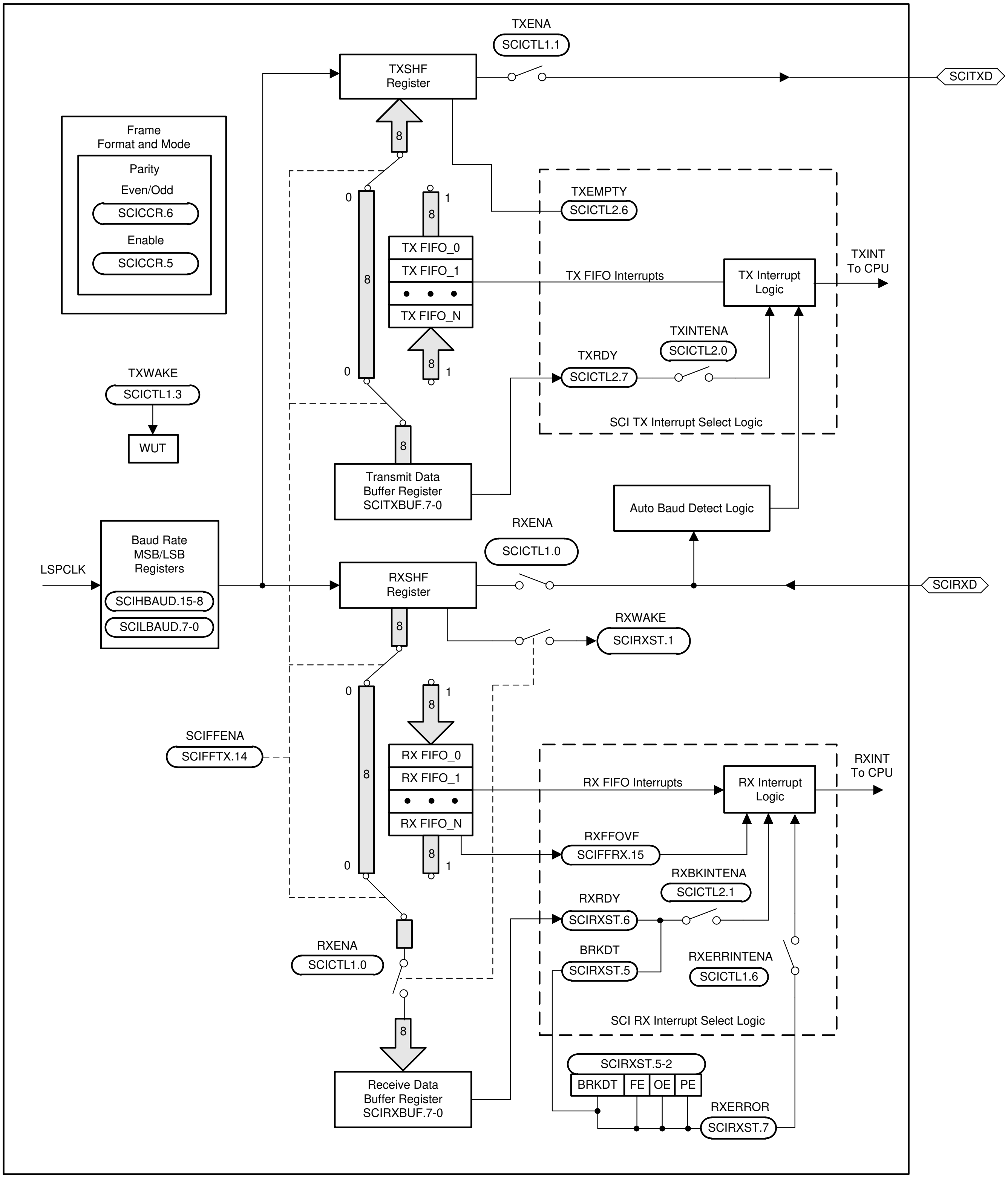


Figure 6-64. SCI Block Diagram

6.14.5 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a high-speed synchronous serial input and output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the MCU controller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and analog-to-digital converters (ADCs). Multidevice communications are supported by the master or slave operation of the SPI. The port supports a 16-level, receive and transmit FIFO for reducing CPU servicing overhead.

The SPI module features include:

- SPISOMI: SPI slave-output/master-input pin
- SPISIMO: SPI slave-input/master-output pin
- $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
- SPICLK: SPI serial-clock pin
- Two operational modes: Master and Slave
- Baud rate: 125 different programmable rates. The maximum baud rate that can be employed is limited by the maximum speed of the I/O buffers used on the SPI pins.
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithm
- 16-level transmit/receive FIFO
- DMA support
- High-speed mode
- Delayed transmit control
- 3-wire SPI mode
- $\overline{\text{SPISTE}}$ inversion for digital audio interface receive mode on devices with two SPI modules

Figure 6-65 shows the SPI CPU interfaces.

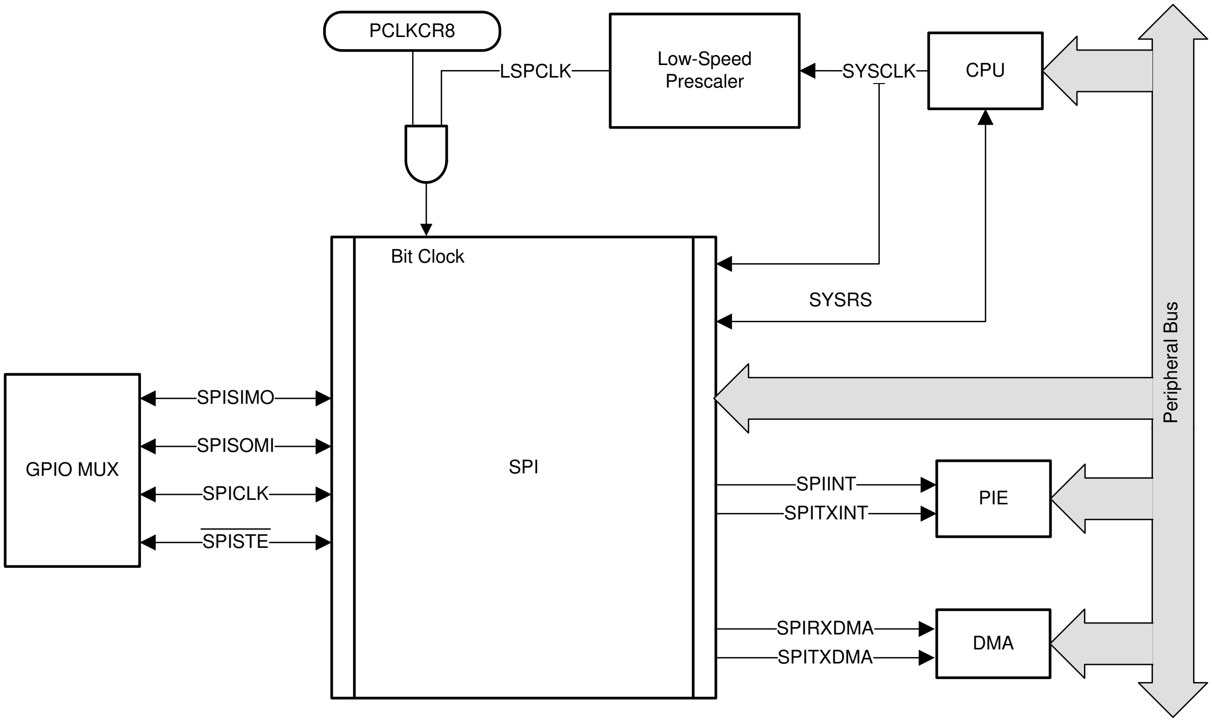


Figure 6-65. SPI CPU Interface

6.14.5.1 SPI Master Mode Timings

The following section contains the SPI Master Mode Timings. For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.

Section 6.14.5.1.1 lists the SPI master mode timing requirements.

Section 6.14.5.1.2 lists the SPI master mode switching characteristics where the clock phase = 0. Figure 6-66 shows the SPI master mode external timing where the clock phase = 0.

Section 6.14.5.1.3 lists the SPI master mode switching characteristics where the clock phase = 1. Figure 6-67 shows the SPI master mode external timing where the clock phase = 1.

Note

All timing parameters for SPI High-Speed Mode assume a load capacitance of 5 pF on SPICLK, SPISIMO, and SPISOMI.

6.14.5.1.1 SPI Master Mode Timing Requirements

NO.			(BRR + 1) (1)	MIN	MAX	UNIT
High-Speed Mode						
8	$t_{su(SOMI)M}$	Setup time, SPISOMI valid before SPICLK	Even, Odd	1		ns
9	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	Even, Odd	5		ns
Normal Mode						
8	$t_{su(SOMI)M}$	Setup time, SPISOMI valid before SPICLK	Even, Odd	15		ns
9	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	Even, Odd	0		ns

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

6.14.5.1.2 SPI Master Mode Switching Characteristics (Clock Phase = 0)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		(BRR + 1)(1)	MIN	MAX	UNIT
General						
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} – 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} – 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} – 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} – 0.5t_{c(LSPCLK)} – 1$	$0.5t_{c(SPC)M} – 0.5t_{c(LSPCLK)} + 1$	
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPISTE}}$ active to SPICLK	Even	$1.5t_{c(SPC)M} – 3t_{c(SYSCLK)} – 3$	$1.5t_{c(SPC)M} – 3t_{c(SYSCLK)} + 3$	ns
			Odd	$1.5t_{c(SPC)M} – 4t_{c(SYSCLK)} – 3$	$1.5t_{c(SPC)M} – 4t_{c(SYSCLK)} + 3$	
24	$t_{v(STE)M}$	Valid time, SPICLK to $\overline{\text{SPISTE}}$ inactive	Even	$0.5t_{c(SPC)M} – 3$	$0.5t_{c(SPC)M} + 3$	ns
			Odd	$0.5t_{c(SPC)M} – 0.5t_{c(LSPCLK)} – 3$	$0.5t_{c(SPC)M} – 0.5t_{c(LSPCLK)} + 3$	
High-Speed Mode						
4	$t_{d(SIMO)M}$	Delay time, SPICLK to SPISIMO valid	Even, Odd		1	ns
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} – 3$		ns
			Odd	$0.5t_{c(SPC)M} – 0.5t_{c(LSPCLK)} – 3$		
Normal Mode						
4	$t_{d(SIMO)M}$	Delay time, SPICLK to SPISIMO valid	Even, Odd		1	ns
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} – 3$		ns
			Odd	0.5tc(SPC)M – 0.5tc(LSPCLK) – 3		

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

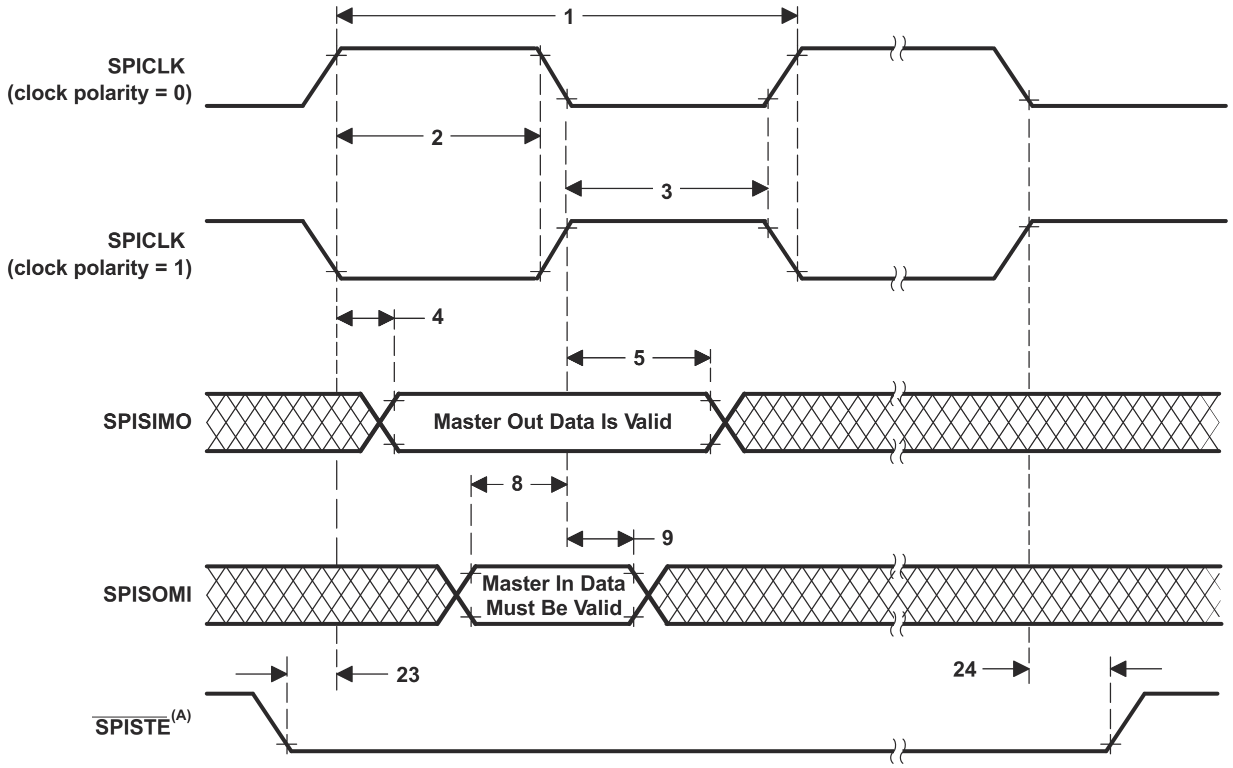
6.14.5.1.3 SPI Master Mode Switching Characteristics (Clock Phase = 1)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		(BRR + 1) [1]	MIN	MAX	UNIT
General						
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPISTE}}$ valid to SPICLK	Even, Odd	$2t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$	$2t_{c(SPC)M} - 3t_{c(SYSCLK)} + 2$	ns
24	$t_{d(STE)M}$	Delay time, SPICLK to $\overline{\text{SPISTE}}$ invalid	Even	–3	2	ns
			Odd	–3	2	
High-Speed Mode						
4	$t_{d(SIMO)M}$	Delay time, SPISIMO valid to SPICLK	Even	$0.5t_{c(SPC)M} - 2$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 2$		
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		
Normal Mode						
4	$t_{d(SIMO)M}$	Delay time, SPISIMO valid to SPICLK	Even	$0.5t_{c(SPC)M} - 2$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 2$		
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		

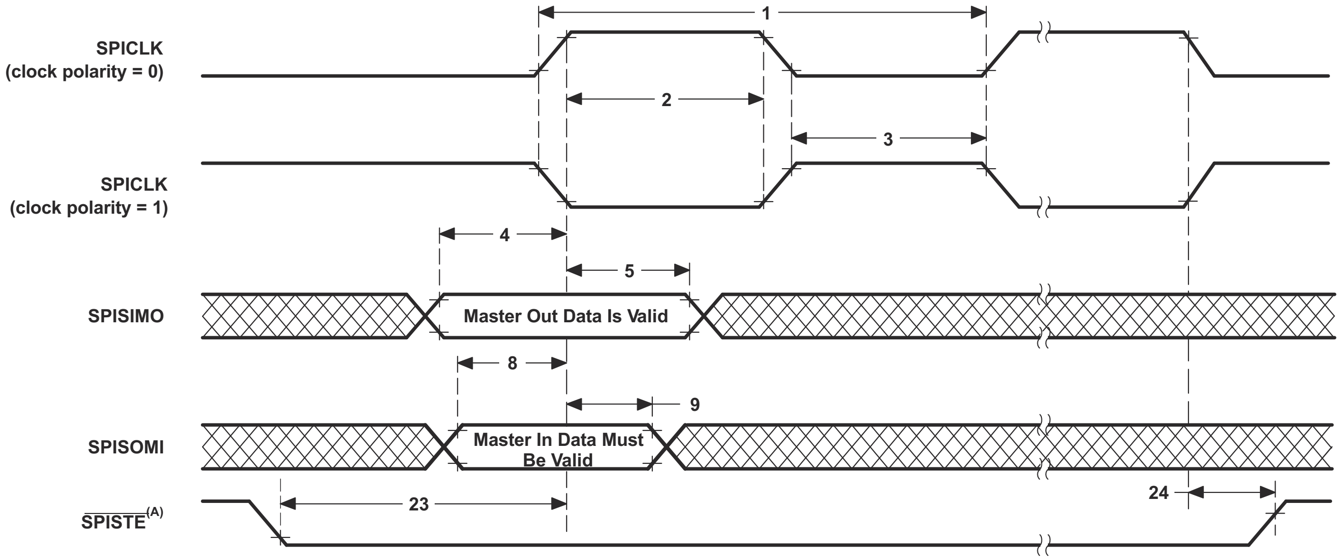
(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

6.14.5.1.4 SPI Master Mode Timing Diagrams



A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-66. SPI Master Mode External Timing (Clock Phase = 0)



A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-67. SPI Master Mode External Timing (Clock Phase = 1)

6.14.5.2 SPI Slave Mode Timings

The following section contains the SPI Slave Mode Timings. For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.

Section 6.14.5.2.1 lists the SPI slave mode timing requirements. Section 6.14.5.2.2 lists the SPI slave mode switching characteristics.

Figure 6-68 shows the SPI slave mode external timing where the clock phase = 0. Figure 6-69 shows the SPI slave mode external timing where the clock phase = 1.

6.14.5.2.1 SPI Slave Mode Timing Requirements

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK, first pulse	$2t_{c(SYSCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK, second pulse	$2t_{c(SYSCLK)} - 1$		ns
19	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
20	$t_{h(SIMO)S}$	Hold time, SPISIMO valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK (Clock Phase = 0)	$2t_{c(SYSCLK)} + 3$		ns
		Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK (Clock Phase = 1)	$2t_{c(SYSCLK)} + 23$		ns
26	$t_{h(STE)S}$	Hold time, $\overline{\text{SPISTE}}$ invalid after SPICLK	$1.5t_{c(SYSCLK)}$		ns

6.14.5.2.2 SPI Slave Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
15	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		12	ns
16	$t_{v(SOMI)S}$	Valid time, SPISOMI valid after SPICLK	0		ns

6.14.5.2.3 SPI Slave Mode Timing Diagrams

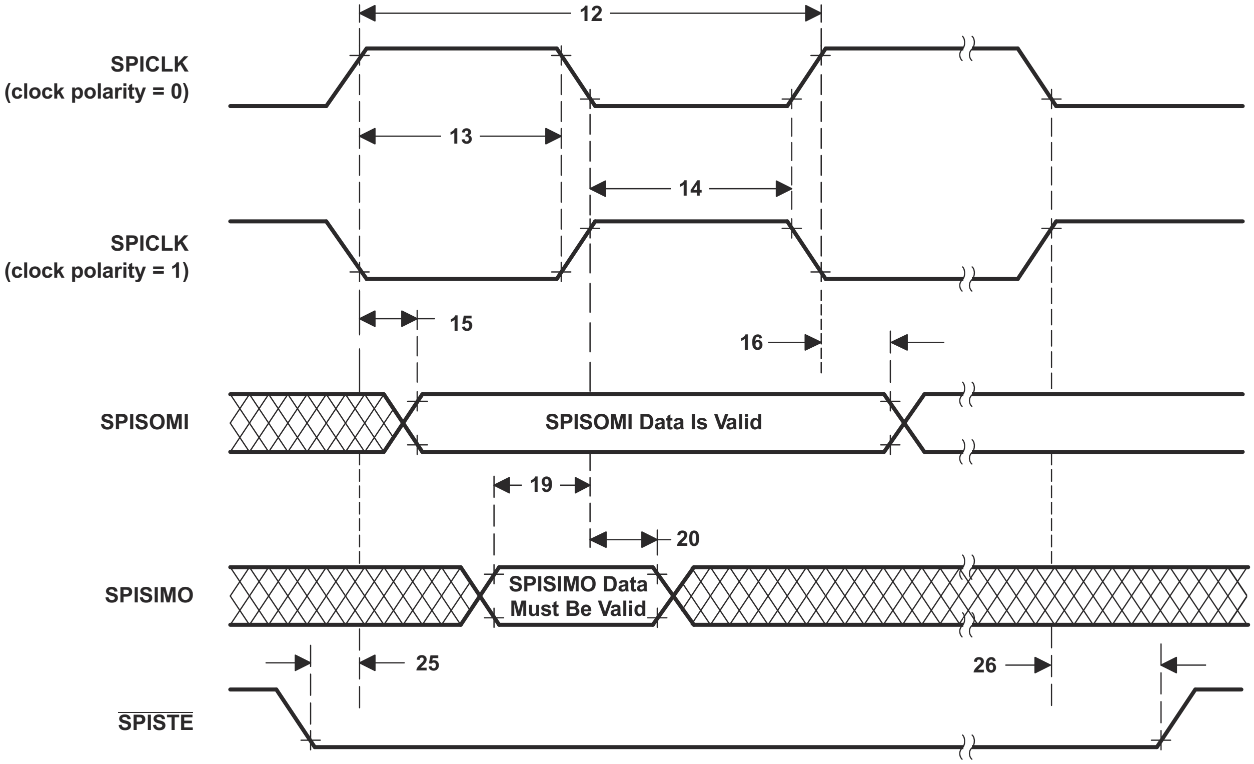


Figure 6-68. SPI Slave Mode External Timing (Clock Phase = 0)

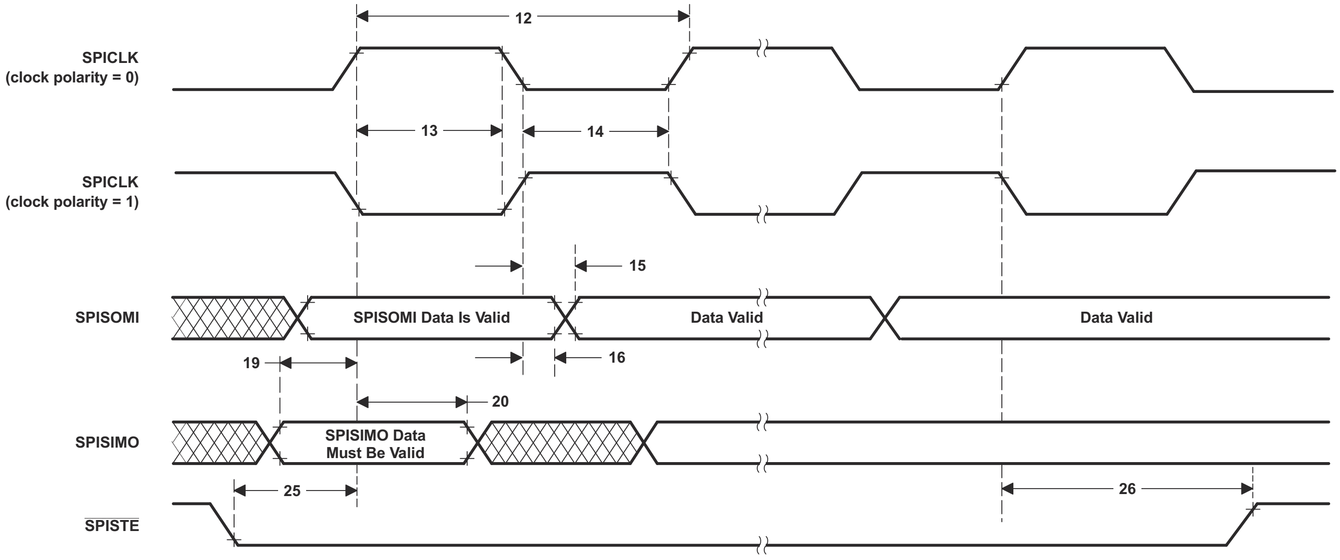


Figure 6-69. SPI Slave Mode External Timing (Clock Phase = 1)

6.14.6 Local Interconnect Network (LIN)

This device contains one Local Interconnect Network (LIN) module. The LIN module adheres to the LIN 2.1 standard as defined by the *LIN Specification Package Revision 2.1*. The LIN is a low-cost serial interface designed for applications where the CAN protocol may be too expensive to implement, such as small subnetworks for cabin comfort functions like interior lighting or window control in an automotive application.

The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-master and multiple-slave with a message identification for multicast transmission between any network nodes.

The LIN module can be programmed to work either as an SCI or as a LIN as the core of the module is an SCI. The hardware features of the SCI are augmented to achieve LIN compatibility. The SCI module is a universal asynchronous receiver-transmitter (UART) that implements the standard non-return-to-zero format.

Though the registers are common for LIN and SCI, the register descriptions have notes to identify the register/bit usage in different modes. Because of this, code written for this module cannot be directly ported to the stand-alone SCI module and vice versa.

The LIN module has the following features:

- Compatibility with LIN 1.3, 2.0 and 2.1 protocols
- Configurable baud rate up to 20 kbps (as per LIN 2.1 protocol)
- Two external pins: LINRX and LINTX
- Multibuffered receive and transmit units
- Identification masks for message filtering
- Automatic master header generation
  - Programmable synchronization break field
  - Synchronization field
  - Identifier field
- Slave automatic synchronization
  - Synchronization break detection
  - Optional baud rate update
  - Synchronization validation
- 2^{31} programmable transmission rates with 7 fractional bits
- Wakeup on LINRX dominant level from transceiver
- Automatic wakeup support
  - Wakeup signal generation
  - Expiration times on wakeup signals
- Automatic bus idle detection
- Error detection
  - Bit error
  - Bus error
  - No-response error
  - Checksum error
  - Synchronization field error
  - Parity error
- Capability to use direct memory access (DMA) for transmit and receive data
- Two interrupt lines with priority encoding for:
  - Receive
  - Transmit
  - ID, error, and status
- Support for LIN 2.0 checksum
- Enhanced synchronizer finite state machine (FSM) support for frame processing
- Enhanced handling of extended frames
- Enhanced baud rate generator
- Update wakeup/go to sleep

Figure 6-70 shows the LIN block diagram.

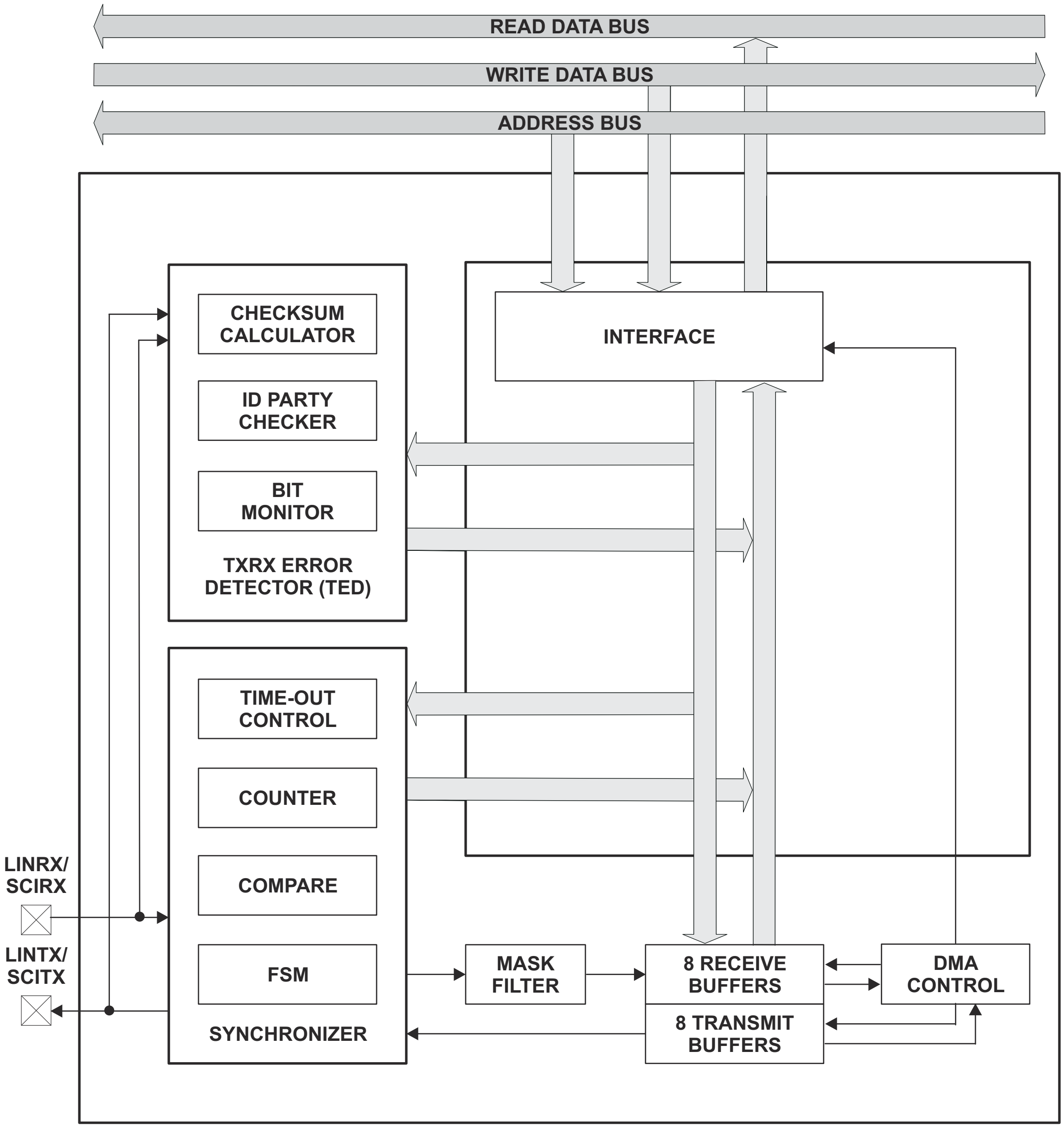


Figure 6-70. LIN Block Diagram

6.14.7 Fast Serial Interface (FSI)

The Fast Serial Interface (FSI) module is a serial communication peripheral capable of reliable and robust high-speed communications. The FSI is designed to ensure data robustness across many system conditions such as chip-to-chip as well as board-to-board across an isolation barrier. Payload integrity checks such as CRC, start- and end-of-frame patterns, and user-defined tags, are encoded before transmit and then verified after receipt without additional CPU interaction. Line breaks can be detected using periodic transmissions, all managed and monitored by hardware. The FSI is also tightly integrated with other control peripherals on the device. To ensure that the latest sensor data or control parameters are available, frames can be transmitted on every control loop period. An integrated skew-compensation block has been added on the receiver to handle skew that may occur between the clock and data signals due to a variety of factors, including trace-length mismatch and skews induced by an isolation chip. With embedded data robustness checks, data-link integrity checks, skew compensation, and integration with control peripherals, the FSI can enable high-speed, robust communication in any system. These and many other features of the FSI follow.

The FSI module includes the following features:

- Independent transmitter and receiver cores
- Source-synchronous transmission
- Dual data rate (DDR)
- One or two data lines
- Programmable data length
- Skew adjustment block to compensate for board and system delay mismatches
- Frame error detection
- Programmable frame tagging for message filtering
- Hardware ping to detect line breaks during communication (ping watchdog)
- Two interrupts per FSI core
- Externally triggered frame generation
- Hardware- or software-calculated CRC
- Embedded ECC computation module
- Register write protection
- DMA support
- SPI compatibility mode (limited features available)

Operating the FSI at maximum speed (50 MHz) at dual data rate (100 Mbps) may require the integrated skew compensation block to be configured according to the specific operating conditions on a case-by-case basis. The *Fast Serial Interface (FSI) Skew Compensation* Application Report provides example software on how to configure and set up the integrated skew compensation block on the Fast Serial Interface.

The FSI consists of independent transmitter (FSITX) and receiver (FSIRX) cores. The FSITX and FSIRX cores are configured and operated independently. The features available on the FSITX and FSIRX are described in Section 6.14.7.1 and Section 6.14.7.2, respectively.

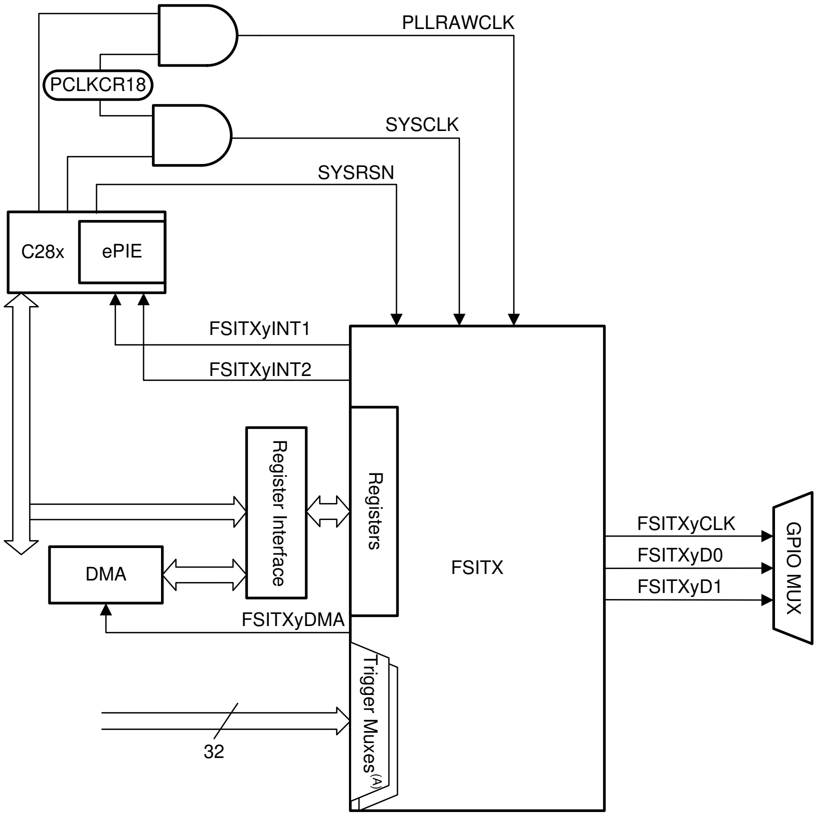
6.14.7.1 FSI Transmitter

The FSI transmitter module handles the framing of data, CRC generation, signal generation of TXCLK, TXD0, and TXD1, as well as interrupt generation. The operation of the transmitter core is controlled and configured through programmable control registers. The transmitter control registers let the CPU program, control, and monitor the operation of the FSI transmitter. The transmit data buffer is accessible by the CPU and the DMA.

The transmitter has the following features:

- Automated ping frame generation
- Externally triggered ping frames
- Externally triggered data frames
- Software-configurable frame lengths
- 16-word data buffer
- Data buffer underrun and overrun detection
- Hardware-generated CRC on data bits
- Software ECC calculation on select data
- DMA support

Figure 6-71 shows the FSITX CPU interface. Figure 6-72 shows the high-level block diagram of the FSITX. Not all data paths and internal connections are shown. This diagram provides a high-level overview of the internal modules present in the FSITX.



A. The signals connected to the trigger muxes are described in the External Frame Trigger Mux section of the Fast Serial Interface (FSI) chapter in the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.

Figure 6-71. FSITX CPU Interface

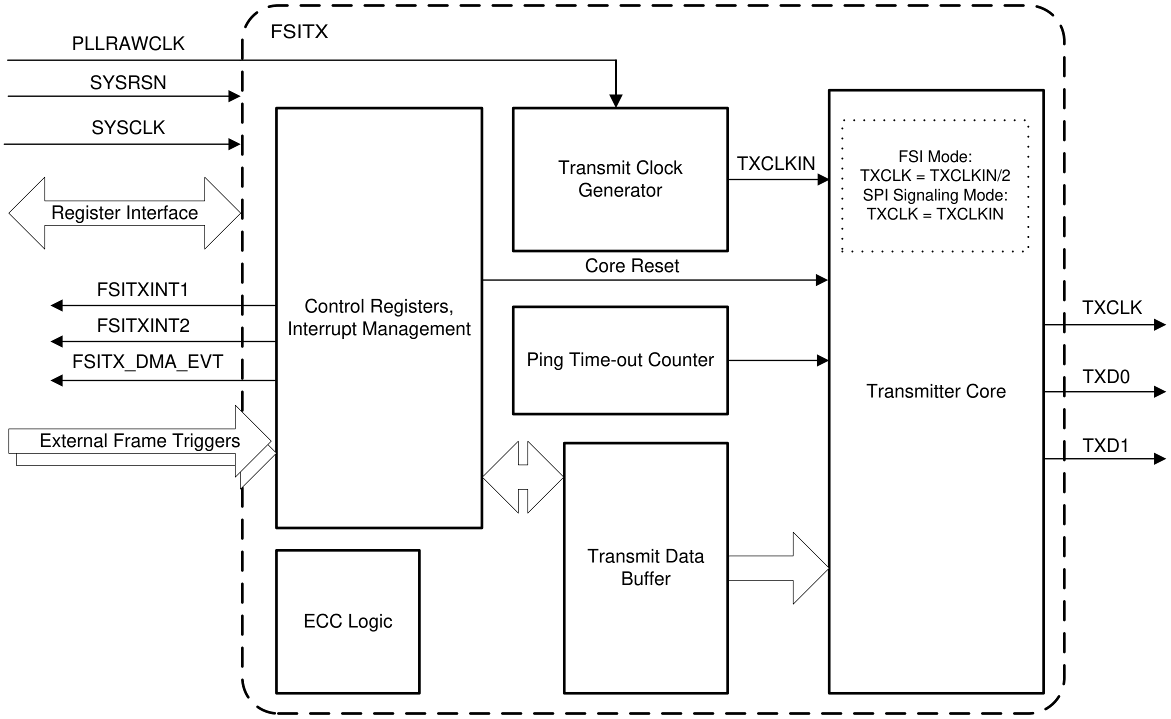


Figure 6-72. FSITX Block Diagram

6.14.7.1.1 FSITX Electrical Data and Timing

Section 6.14.7.1.1.1 lists the FSITX switching characteristics. Figure 6-73 shows the FSITX timings.

6.14.7.1.1.1 FSITX Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(TXCLK)}$	Cycle time, TXCLK	20		ns
2	$t_{w(TXCLK)}$	Pulse width, TXCLK low or TXCLK high	$(0.5t_{c(TXCLK)}) – 1$	$(0.5t_{c(TXCLK)}) + 1$	ns
3	$t_{d(TXCLK–TXD)}$	Delay time, TXCLK rising or falling toTXD valid	$(0.25t_{c(TXCLK)}) – 2$	$(0.25t_{c(TXCLK)}) + 2$	ns
TDM1	$t_{skew(TDM\_CLK-TDM\_Dx\ )}$	Delay skew introduced between TXCLK-TDM_CLK delay and TXDx-TDM_Dx delays	-2	2	ns

6.14.7.1.1.2 FSITX Timings

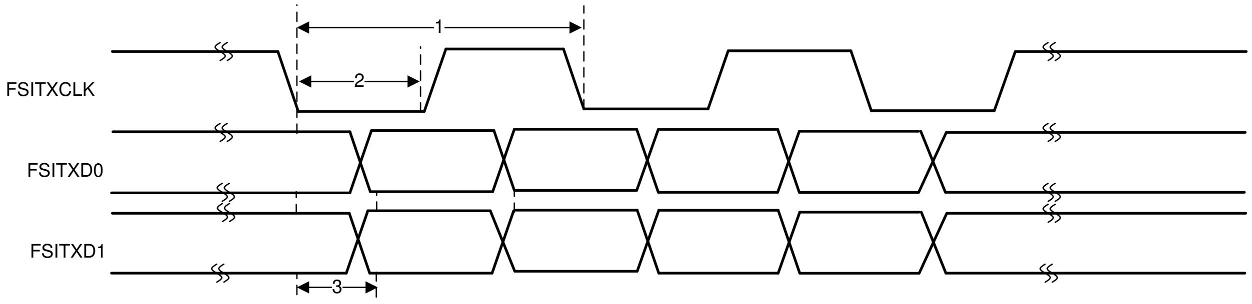


Figure 6-73. FSITX Timings

6.14.7.2 FSI Receiver

The receiver module interfaces to the FSI clock (RXCLK), and data lines (RXD0 and RXD1) after they pass through an optional programmable delay line. The receiver core handles the data framing, CRC computation, and frame-related error checking. The receiver bit clock and state machine are run by the RXCLK input, which is asynchronous to the device system clock.

The receiver control registers let the CPU program, control, and monitor the operation of the FSIRX. The receive data buffer is accessible by the CPU, HIC, and the DMA.

The receiver core has the following features:

- 16-word data buffer
- Multiple supported frame types
- Ping frame watchdog
- Frame watchdog
- CRC calculation and comparison in hardware
- ECC detection
- Programmable delay line control on incoming signals
- DMA support
- SPI compatibility mode

Figure 6-74 shows the FSIRX CPU interface. Figure 6-75 provides a high-level overview of the internal modules present in the FSIRX. Not all data paths and internal connections are shown.

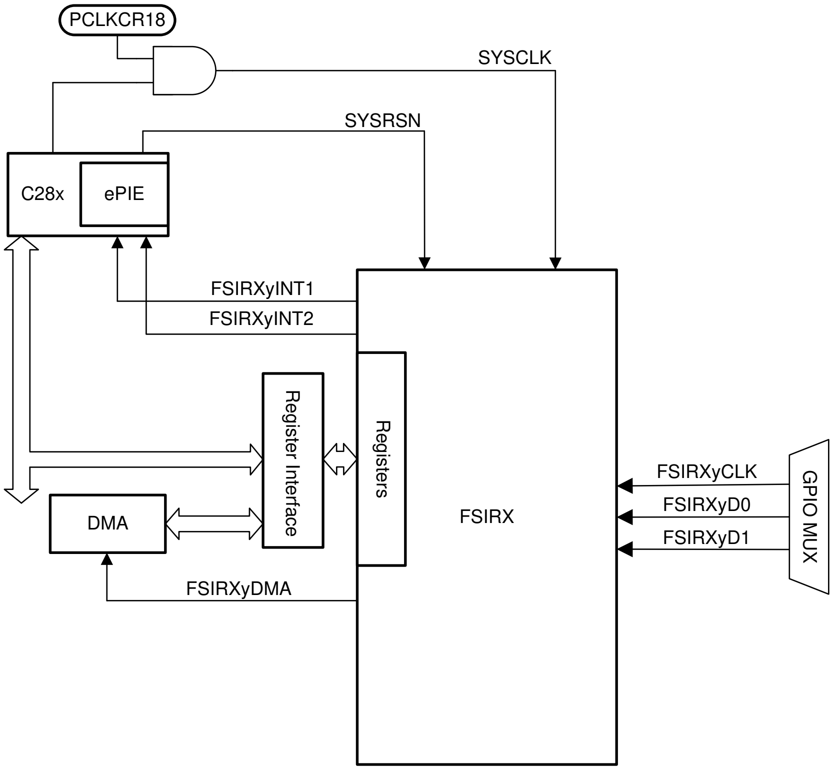


Figure 6-74. FSIRX CPU Interface

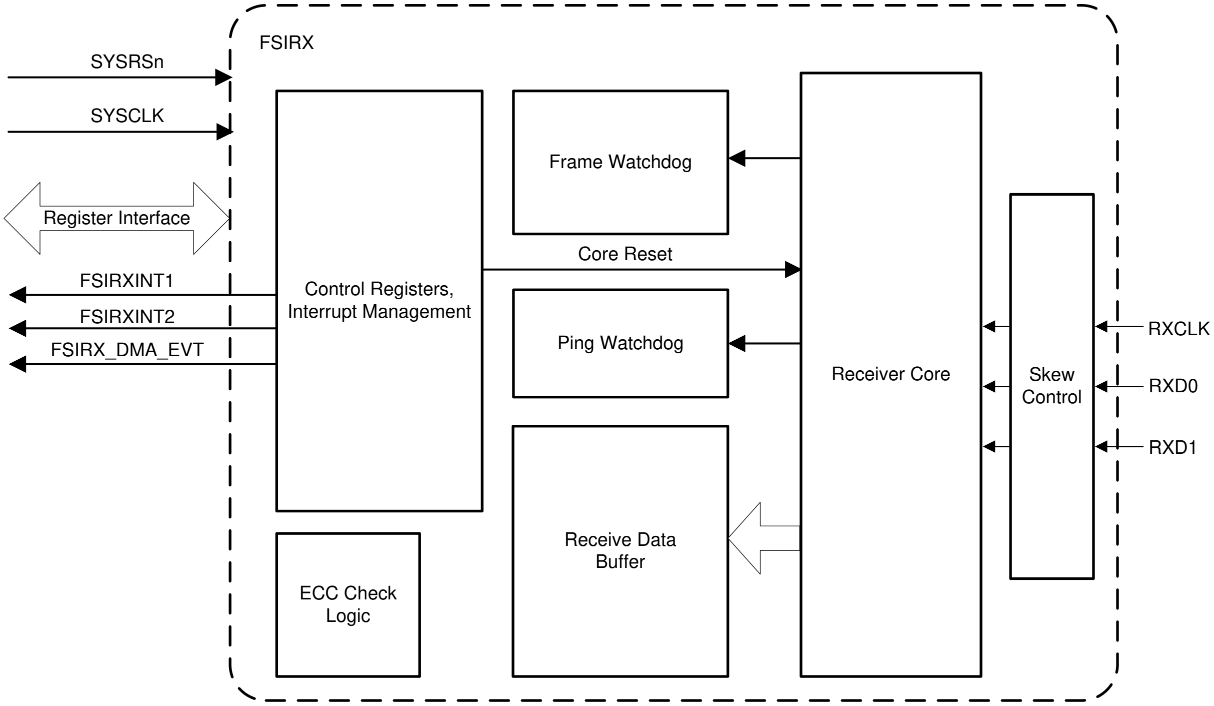


Figure 6-75. FSIRX Block Diagram

6.14.7.2.1 FSIRX Electrical Data and Timing

Section 6.14.7.2.1.1 lists the FSIRX timing requirements. Section 6.14.7.2.1.2 lists the FSIRX switching characteristics. Figure 6-76 shows the FSIRX Timings.

6.14.7.2.1.1 FSIRX Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(RXCLK)}$	Cycle time, RXCLK	20		ns
2	$t_{w(RXCLK)}$	Pulse width, RXCLK low or RXCLK high.	$0.35t_{c(RXCLK)}$	$0.65t_{c(RXCLK)}$	ns
3	$t_{su(RXCLK–RXD)}$	Setup time with respect to RXCLK, applies to both edges of the clock	1.7		ns
4	$t_{h(RXCLK–RXD)}$	Hold time with respect to RXCLK, applies to both edges of the clock	2		ns

6.14.7.2.1.2 FSIRX Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{d(RXCLK)}$	RXCLK delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31	10	30	ns
2	$t_{d(RXD0)}$	RXD0 delay compensation at RX_DLYLINE_CTRL[RXD0_DLY]=31	10	30	ns
3	$t_{d(RXD1)}$	RXD1 delay compensation at RX_DLYLINE_CTRL[RXD1_DLY]=31	10	30	ns
4	$t_{d(DELAY\_ELEMENT)}$	Incremental delay of each delay line element for RXCLK, RXD0, and RXD1	0.3	1	ns

6.14.7.2.1.3 FSIRX Timings

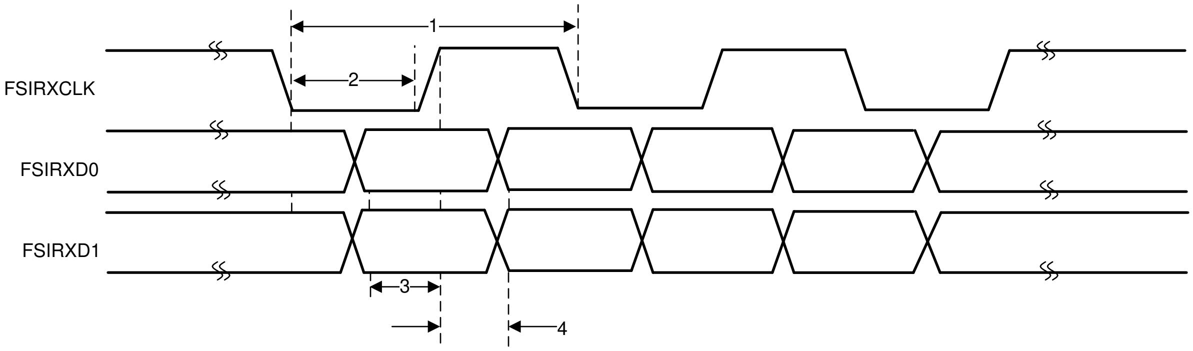


Figure 6-76. FSIRX Timings

6.14.7.3 FSI SPI Compatibility Mode

The FSI supports a SPI compatibility mode to enable communication with programmable SPI devices. In this mode, the FSI transmits its data in the same manner as a SPI in a single clock configuration mode. While the FSI is able to physically interface with a SPI in this mode, the external device must be able to encode and decode an FSI frame to communicate successfully. This is because the FSI transmits all SPI frame phases with the exception of the preamble and postamble. The FSI provides the same data validation and frame checking as if it was in standard FSI mode, allowing for more robust communication without consuming CPU cycles. The external SPI is required to send all relevant information and can access standard FSI features such as the ping frame watchdog on the FSIRX, frame tagging, or custom CRC values. The list of features of SPI compatibility mode follows:

- Data will transmit on rising edge and receive on falling edge of the clock.
- Only 16-bit word size is supported.
- TXD1 will be driven like an active-low chip-select signal. The signal will be low for the duration of the full frame transmission.
- No receiver chip-select input is required. RXD1 is not used. Data is shifted into the receiver on every active clock edge.
- No preamble or postamble clocks will be transmitted. All signals return to the idle state after the frame phase is finished.
- It is not possible to transmit in the SPI slave configuration because the FSI TXCLK cannot take an external clock source.

6.14.7.3.1 FSITX SPI Signaling Mode Electrical Data and Timing

Section 6.14.7.3.1.1 lists the FSITX SPI signaling mode switching characteristics. Figure 6-77 shows the FSITX SPI signaling mode timings. Special timings are not required for the FSIRX in SPI signaling mode. FSIRX timings listed in Section 6.14.7.2.1.1 are applicable in SPI compatibility mode. Setup and Hold times are only valid on the falling edge of FSIRXCLK because this is the active edge in SPI signaling mode.

6.14.7.3.1.1 FSITX SPI Signaling Mode Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(TXCLK)}$	Cycle time, TXCLK	20		ns
2	$t_{w(TXCLK)}$	Pulse width, TXCLK low or TXCLK high	$(0.5t_{c(TXCLK)}) - 1$	$(0.5t_{c(TXCLK)}) + 1$	ns
3	$t_{d(TXCLKH–TXD0)}$	Delay time, TXD0 valid after TXCLK high		3	ns
4	$t_{d(TXD1-TXCLK)}$	Delay time, TXCLK high after TXD1 low	$t_{w(TXCLK)} - 3$		ns
5	$t_{d(TXCLK-TXD1)}$	Delay time, TXD1 high after TXCLK low	$t_{w(TXCLK)}$		ns

6.14.7.3.1.2 FSITX SPI Signaling Mode Timings

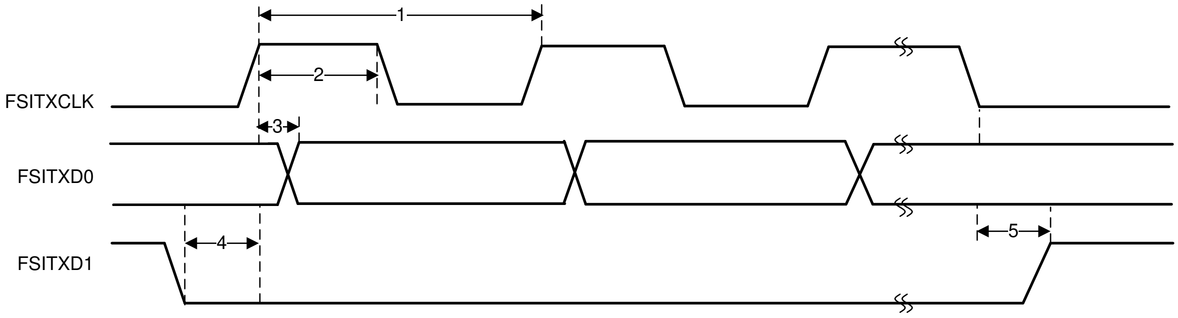


Figure 6-77. FSITX SPI Signaling Mode Timings

6.14.8 Host Interface Controller (HIC)

The HIC module allows an external host controller to directly access resources of the device by emulating the ASRAM protocol. It has two modes of operation: direct access and mailbox access. In direct access mode, device resources is written to and read from directly by the external host. In mailbox access mode, external host and device write to and read from a buffer and notify each other when the buffer write/read is complete. For security reasons, the HIC has to be enabled by the device before the external host can access it. Figure 6-78 shows the block diagram of the HIC.

Features of the HIC include:

- Configurable I/O data lines of 8 bits and 16 bits
- Direct and mailbox access modes
- 8 address lines and 8 configurable base addresses for a total of 2048 possible addressable regions
- Two 64-byte buffers for external host and device when using mailbox access mode
- Interrupt generation on buffer full/empty
- High throughput
- Trigger HIC activity from other peripherals
- Error indicators to the system or interface

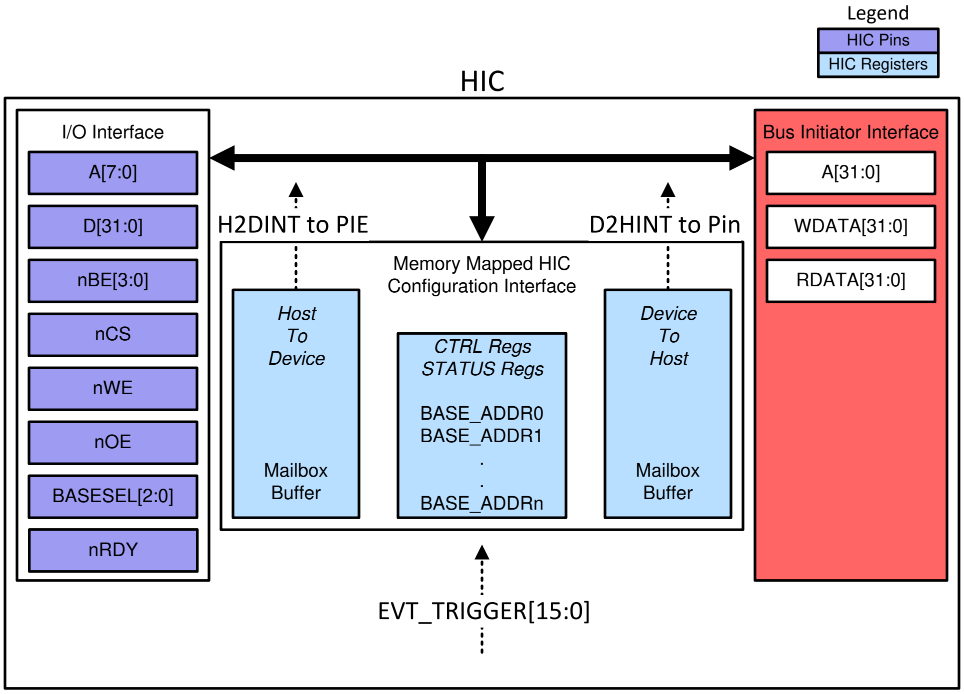


Figure 6-78. HIC Block Diagram

6.14.8.1 HIC Electrical Data and Timing

Section 6.14.8.1.1 lists the HIC timing requirements. Section 6.14.8.1.2 lists the HIC switching characteristics. Figure 6-79 shows the read/write operation with nOE and nWE pins. Figure 6-80 shows the read/write operation with RnW pin.

6.14.8.1.1 HIC Timing Requirements

over operating free-air temperature range (unless otherwise noted)

REFID			MIN	MAX	UNIT
Read/Write Parameters with nOE and nWE pins - Dual Read/Write pins					
T1	$t_{\text{su(ABBV-OEV)}}$	Setup time, A/BASESEL/nBE before nOE active	0		ns
T2	$t_{\text{su(ABBV-WEV)}}$	Setup time, A/BASESEL/nBE before nWE active	0		ns
T3	$t_{\text{su(CSV-OEV)}}$	Setup time, nCS active before nOE active	$0.5t_{\text{c(SYSCLK)}}$		ns
T4	$t_{\text{su(CSV-WEV)}}$	Setup time, nCS active before nWE active	$0.5t_{\text{c(SYSCLK)}}$		ns
T5	$t_{\text{h(ABBV-OEIV)}}$	Hold time, A/BASESEL/nBE/nCS after nOE inactive	6		ns
T6	$t_{\text{h(ABBV-WEIV)}}$	Hold time, A/BASESEL/nBE/nCS after nWE inactive	6		ns
T7	$t_{\text{w(OEV)}}$	Active pulse width of nOE (Read)(1)	$4t_{\text{c(SYSCLK)}}$		ns
T8	$t_{\text{w(WEV)}}$	Active pulse width of nWE (Write)	$4t_{\text{c(SYSCLK)}}$		ns
T9	$t_{\text{w(CSIV)}}$	Inactive pulse width of nCS(2)	$3t_{\text{c(SYSCLK)}}$		ns
T10	$t_{\text{w(OEIV)}}$	Inactive Read pulse width of nOE(2)	$3t_{\text{c(SYSCLK)}}$		ns
T11	$t_{\text{w(WEIV)}}$	Inactive Write pulse width of nWE(2)	$3t_{\text{c(SYSCLK)}}$		ns
T12	$t_{\text{su(DV-WEV)}}$	Setup time, D before nWE active	0		ns
T13	$t_{\text{h(DV-WEIV)}}$	Hold time, D after nWE inactive	6		ns
Read/Write Parameters with RnW pin - Single Read/Write pin					
T14	$t_{\text{su(ABBV-CSV)}}$	Setup time, A/BASESEL/nBE before nCS active	0		ns
T15	$t_{\text{su(RNWV-CSV)}}$	Setup time, RnW before nCS active	$0.5t_{\text{c(SYSCLK)}}$		ns
T16	$t_{\text{h(ABBV-CSIV)}}$	Hold time, A/BASESEL/nBE/RnW after nCS inactive	6		ns
T17	$t_{\text{w(CSV\_RD)}}$	Active pulse width of nCS for read operation(1)	$4t_{\text{c(SYSCLK)}}$		ns
T18	$t_{\text{w(CSV\_WR)}}$	Active pulse width of nCS for write operation	$4t_{\text{c(SYSCLK)}}$		ns
T19	$t_{\text{w(CSIV)}}$	Inactive pulse width of nCS(2)	$3t_{\text{c(SYSCLK)}}$		ns
T20	$t_{\text{w(RNWIV)}}$	Inactive pulse width of RnW(2)	$3t_{\text{c(SYSCLK)}}$		ns
T21	$t_{\text{su(DV-CSV)}}$	Setup time, D before nCS active	0		ns
T22	$t_{\text{h(DV-CSIV)}}$	Hold time, D after nCS inactive	5		ns

(1) For accesses to the device region, additional 2 SYSCLK cycles are required.
(2) For accesses to the device region with nRDY pin, additional SYSCLK cycle is required.

6.14.8.1.2 HIC Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

REFID	PARAMETER		MIN	MAX	UNIT
Read/Write Parameters with nOE and nWE pins					
S1	$t_{d(OEV-DV)}$	Output data delay time : nOE to D output valid (1)	$3t_{c(SYSCLK)}$	$4t_{c(SYSCLK)} + 14$	ns
S2	$t_{d(OEIV-DIV)}$	Output data hold time : nOE invalid to D output invalid (tri-state)	$1t_{c(SYSCLK)}$	$2t_{c(SYSCLK)} + 14$	ns
S3	$t_{d(OEV-RDYV)}$	Read Ready delay time : nOE to nRDY output valid	0	11	ns
S4	$t_{d(WEV-RDYV)}$	Write Ready delay time : nWE to nRDY output valid	0	11	ns
S5	$t_{d(RDYV-DV)}$	Ready to Data delay time : nRDY output valid to D output valid	-3	3	ns
S6	$t_{w(RDYACT)}$	Active pulse width of nRDY output	$2t_{c(SYSCLK)}$		ns
Read/Write Parameters with RnW pin					
S7	$t_{d(CSV-DV)}$	Output delay time : nCS active to D output valid (1)	$3t_{c(SYSCLK)}$	$4t_{c(SYSCLK)} + 14$	ns
S8	$t_{d(CSIV-DIV)}$	Output hold time : nCS inactive to D output invalid (tri-state)	$1t_{c(SYSCLK)}$	$2t_{c(SYSCLK)} + 14$	ns
S9	$t_{d(CSV-RDYV)}$	Output delay time : nCS to nRDY output valid	0	11	ns
S10	$t_{d(RDYV-DV)}$	Ready to Data delay time : nRDY output valid to D output valid	-3	3	ns
S11	$t_{w(RDYACT)}$	Active pulse width of nRDY output	$2t_{c(SYSCLK)}$		ns

(1) Applicable to mailbox accesses only. Direct memory map (Device) accesses are qualified with nRDY pin.

6.14.8.1.3 HIC Timing Diagrams

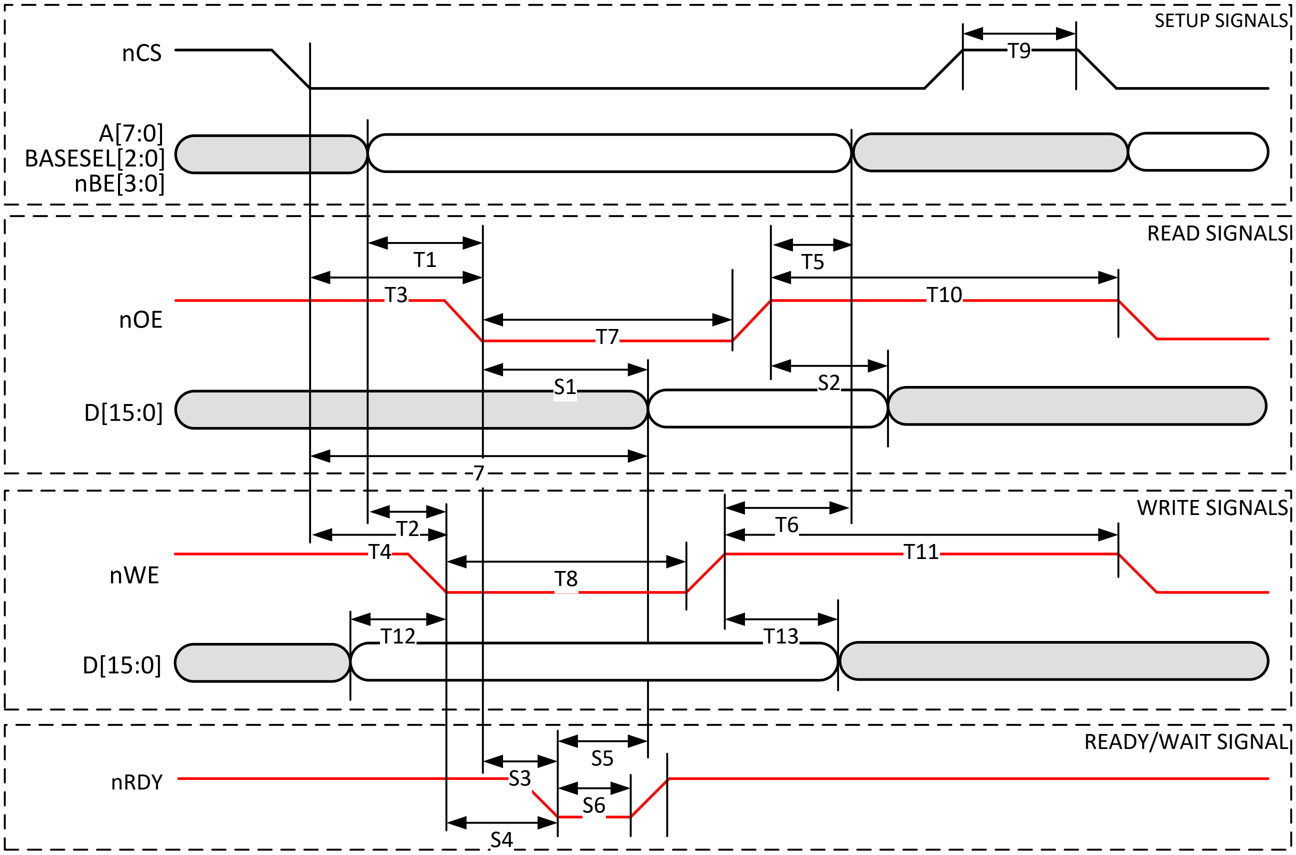


Figure 6-79. Read/Write Operation With nOE and nWE Pins

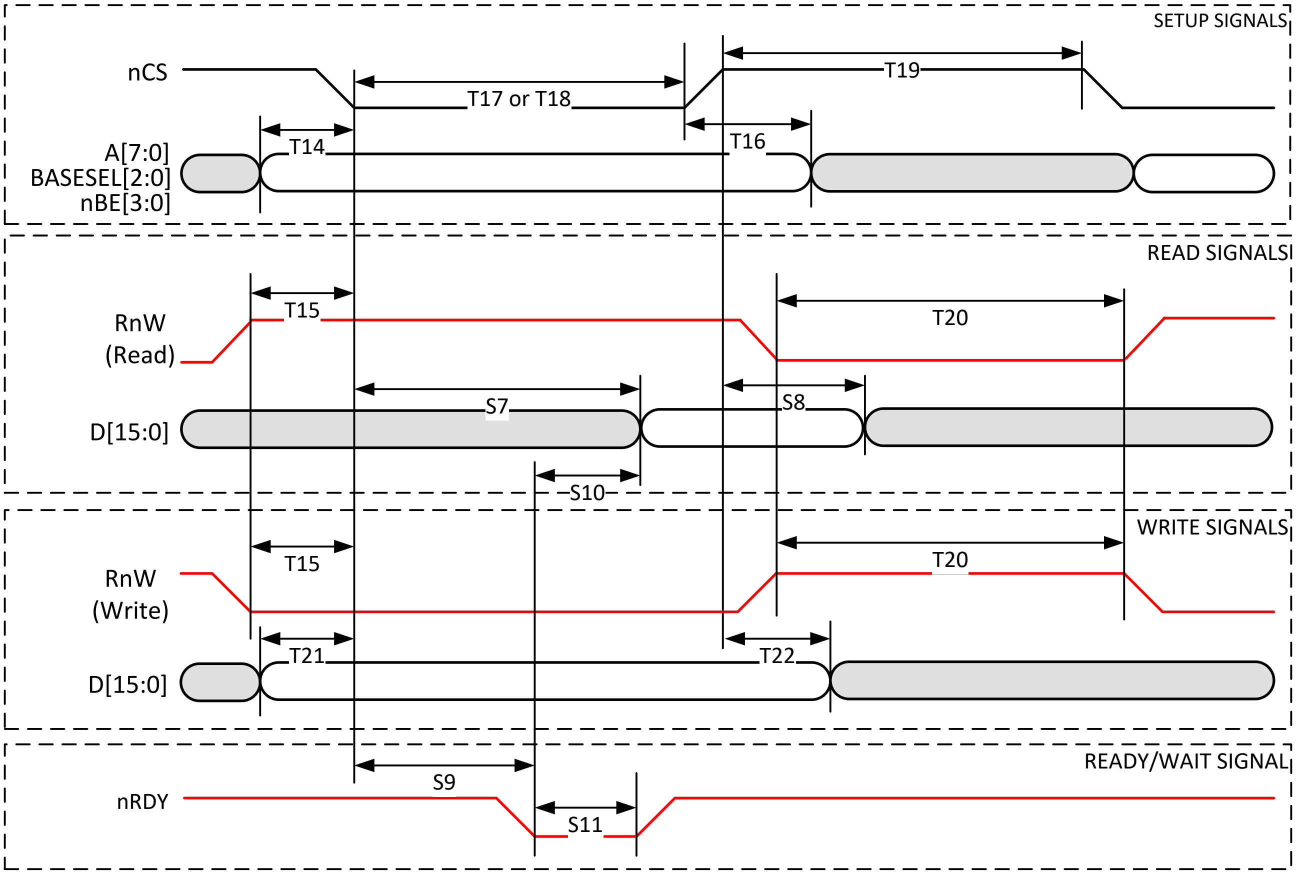


Figure 6-80. Read/Write Operation With RnW Pin

7 Detailed Description

7.1 Overview

C2000™ 32-bit microcontrollers are optimized for processing, sensing, and actuation to improve closed-loop performance in real-time control applications such as industrial motor drives; solar inverters and digital power; electrical vehicles and transportation; motor control; and sensing and signal processing.

The TMS320F28002x (F28002x) is a powerful 32-bit floating-point microcontroller unit (MCU) that lets designers incorporate crucial control peripherals, differentiated analog, and nonvolatile memory on a single device.

The real-time control subsystem is based on TI's 32-bit C28x CPU, which provides 100 MHz of signal processing performance. The C28x CPU is further boosted by the new TMU extended instruction set, which enables fast execution of algorithms with trigonometric operations commonly found in transforms and torque loop calculations; and the VCRC extended instruction set, which reduces the latency for complex math operations commonly found in encoded applications.

The F28002x supports up to 128KB (64KW) of flash memory in one bank. Up to 24KB (12KW) of on-chip SRAM is also available in blocks of 4KB (2KW) for efficient system partitioning. Flash ECC, SRAM ECC/parity, and dual-zone security are also supported.

High-performance analog blocks are integrated on the F28002x real-time MCU to further enable system consolidation. Two separate 12-bit ADCs provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. Four analog comparator modules provide continuous monitoring of input voltage levels for trip conditions.

The TMS320C2000™ devices contain industry-leading control peripherals with frequency-independent ePWM/HRPWM and eCAP allow for a best-in-class level of control to the system.

Connectivity is supported through various industry-standard communication ports (such as SPI, SCI, I2C, PMBus, LIN, and CAN) and offers multiple muxing options for optimal signal placement in a variety of applications. New to the C2000™ platform is Host Interface Controller (HIC), a high throughput interface that allows an external host to access resources of the TMS320F28002x. Additionally, in an industry first, the FSI enables high-speed, robust communication to complement the rich set of peripherals that are embedded in the device.

A specially enabled device variant, TMS320F28002xC, allows access to the Configurable Logic Block (CLB) for additional interfacing features and allows access to the secure ROM, which includes a library to enable InstaSPIN-FOC™. See the Device Comparison table for more information.

The Embedded Real-Time Analysis and Diagnostic (ERAD) module enhances the debug and system analysis capabilities of the device by providing additional hardware breakpoints and counters for profiling.

To learn more about the C2000 real-time MCUs, visit the C2000™ real-time control MCUs page.

7.2 Functional Block Diagram

Figure 7-1 shows the CPU system and associated peripherals.

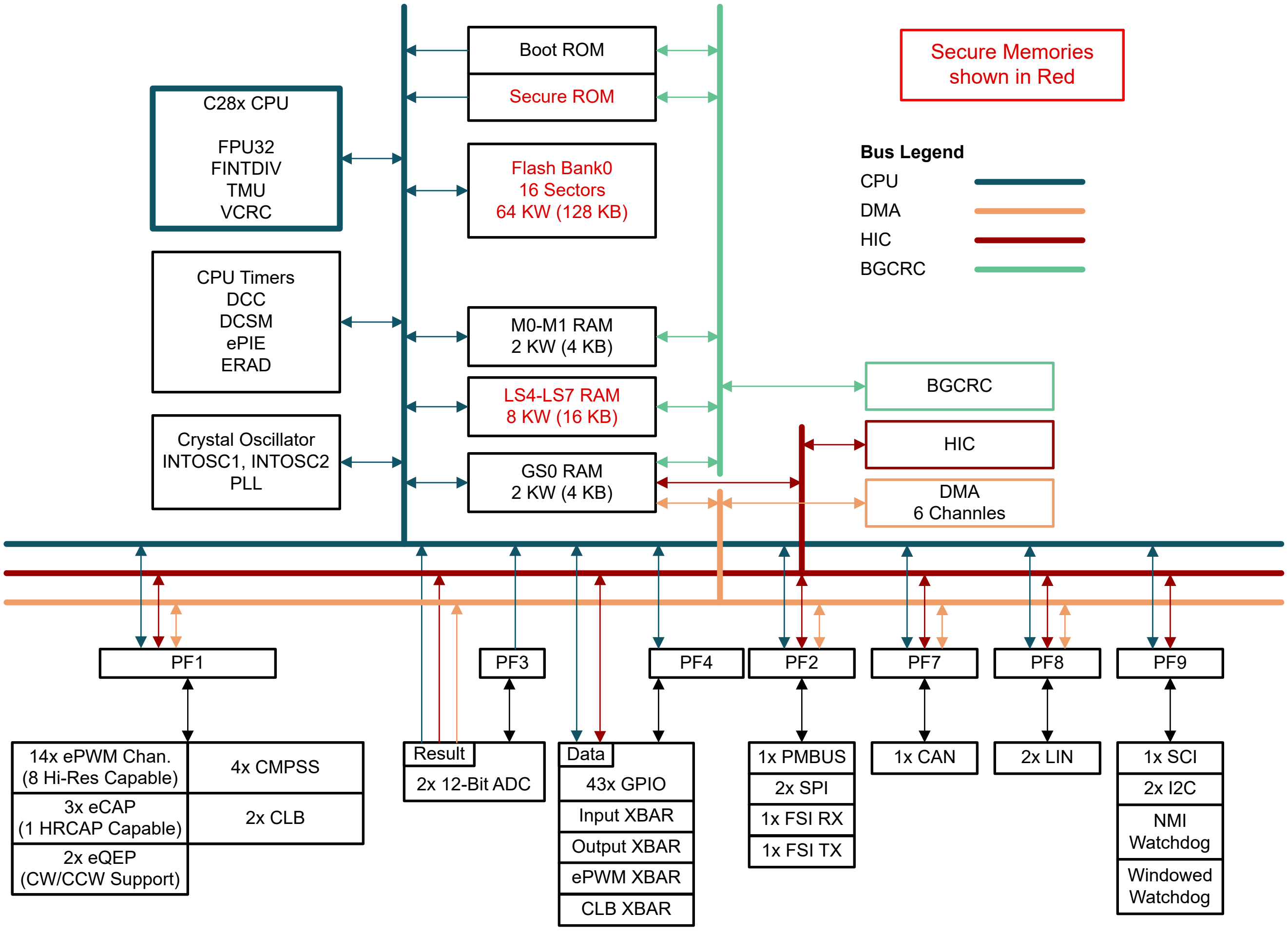


Figure 7-1. Functional Block Diagram

7.3 Memory

7.3.1 Memory Map

The Memory Map table describes the memory map. See the Memory Controller Module section of the System Control chapter in the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.

Table 7-1. Memory Map

MEMORY	SIZE	START ADDRESS	END ADDRESS	HIC ACCESS	DMA ACCESS	ECC/ PARITY	ACCESS PROTECTION	SECURITY
M0 RAM	1K x 16	0x0000 0000	0x0000 03FF	-	-	ECC	Yes	-
M1 RAM	1K x 16	0x0000 0400	0x0000 07FF	-	-	ECC	Yes	-
PieVectTable	512 x 16	0x0000 0D00	0x0000 0EFF	-	-	-	-	-
LS4 RAM	2K x 16	0x0000 A000	0x0000 A7FF	-	-	ECC	Yes	Yes
LS5 RAM	2K x 16	0x0000 A800	0x0000 AFFF	-	-	ECC	Yes	Yes
LS6 RAM	2K x 16	0x0000 B000	0x0000 B7FF	-	-	ECC	Yes	Yes
LS7 RAM	2K x 16	0x0000 B800	0x0000 BFFF	-	-	ECC	Yes	Yes
GS0 RAM	2K x 16	0x0000 C000	0x0000 C7FF	Yes	Yes	Parity	Yes	-
CAN A Message RAM	2K x 16	0x0004 9000	0x0004 97FF	-	-	Parity	-	-
TI OTP(1)	1K x 16	0x0007 0000	0x0007 03FF	-	-	ECC	-	-
User OTP	1K x 16	0x0007 8000	0x0007 83FF	-	-	ECC	-	Yes
Flash	64K x 16	0x0008 0000	0x0008 FFFF	-	-	ECC	-	Yes
Secure ROM	32K x 16	0x003E 8000	0x003E FFFF	-	-	Parity	-	Yes
Boot ROM	64K x 16	0x003F 0000	0x003F FFFF	-	-	Parity	-	-
Pie Vector Fetch Error (part of Boot ROM)	1 x 16	0x003F FFBE	0x003F FFBF	-	-	Parity	-	-
Default Vectors (part of Boot ROM)	64 x 16	0x003F FFC0	0x003F FFFF	-	-	Parity	-	-

(1) TI OTP is for TI internal use only.

7.3.1.1 Dedicated RAM (Mx RAM)

The CPU subsystem has two dedicated ECC-capable RAM blocks: M0 and M1. These memories are small nonsecure blocks that are tightly coupled with the CPU (that is, only the CPU has access to them).

7.3.1.2 Local Shared RAM (LSx RAM)

Local shared RAMs (LSx RAMs) are accessible to the CPU, HIC, and BGCRC. All LSx RAM blocks have ECC. These memories are secure and have CPU access protection (CPU write/CPU fetch).

7.3.1.3 Global Shared RAM (GSx RAM)

Global shared RAMs (GSx RAMs) are accessible from the CPU, HIC, and DMA. The CPU, HIC, and DMA have full read and write access to these memories. All GSx RAM blocks have parity. The GSx RAMs have access protection (CPU write/CPU fetch/DMA write/HIC write).

7.3.2 Flash Memory Map

On the F28002x devices one flash bank (128KB [64KW]) is available. Code to program the flash should be executed out of RAM, there should not be any kind of access to the flash bank when an erase or program operation is in progress. Table 7-2 lists the addresses of flash sectors available for each part number.

7.3.2.1 Addresses of Flash Sectors

Table 7-2. Addresses of Flash Sectors

PART NUMBER	SECTOR	ADDRESS			ECC ADDRESS		
		SIZE	START	END	SIZE	START	END
OTP Sectors							
All F28002x	TI OTP	1K x 16	0x0007 0000	0x0007 03FF	128 x 16	0x0107 0000	0x0107 007F
	DCSM OTP	1K x 16	0x0007 8000	0x0007 83FF	128 x 16	0x0107 1000	0x0107 107F
Bank 0 Sectors							
All F28002x	Sector 0	4K x 16	0x0008 0000	0x0008 0FFF	512 x 16	0x0108 0000	0x0108 01FF
	Sector 1	4K x 16	0x0008 1000	0x0008 1FFF	512 x 16	0x0108 0200	0x0108 03FF
	Sector 2	4K x 16	0x0008 2000	0x0008 2FFF	512 x 16	0x0108 0400	0x0108 05FF
	Sector 3	4K x 16	0x0008 3000	0x0008 3FFF	512 x 16	0x0108 0600	0x0108 07FF
F280025, F280023	Sector 4	4K x 16	0x0008 4000	0x0008 4FFF	512 x 16	0x0108 0800	0x0108 09FF
	Sector 5	4K x 16	0x0008 5000	0x0008 5FFF	512 x 16	0x0108 0A00	0x0108 0BFF
	Sector 6	4K x 16	0x0008 6000	0x0008 6FFF	512 x 16	0x0108 0C00	0x0108 0DFF
	Sector 7	4K x 16	0x0008 7000	0x0008 7FFF	512 x 16	0x0108 0E00	0x0108 0FFF
F280025	Sector 8	4K x 16	0x0008 8000	0x0008 8FFF	512 x 16	0x0108 1000	0x0108 11FF
	Sector 9	4K x 16	0x0008 9000	0x0008 9FFF	512 x 16	0x0108 1200	0x0108 13FF
	Sector 10	4K x 16	0x0008 A000	0x0008 AFFF	512 x 16	0x0108 1400	0x0108 15FF
	Sector 11	4K x 16	0x0008 B000	0x0008 BFFF	512 x 16	0x0108 1600	0x0108 17FF
	Sector 12	4K x 16	0x0008 C000	0x0008 CFFF	512 x 16	0x0108 1800	0x0108 19FF
	Sector 13	4K x 16	0x0008 D000	0x0008 DFFF	512 x 16	0x0108 1A00	0x0108 1BFF
	Sector 14	4K x 16	0x0008 E000	0x0008 EFFF	512 x 16	0x0108 1C00	0x0108 1DFF
	Sector 15	4K x 16	0x0008 F000	0x0008 FFFF	512 x 16	0x0108 1E00	0x0108 1FFF

7.3.3 Peripheral Registers Memory Map

The Peripheral Registers Memory Map (C28x) table lists the peripheral registers.

Table 7-3. Peripheral Registers Memory Map (C28x)

Bit Field Name		DriverLib Name	Base Address	Pipeline Protected	DMA Access	HIC Access
Instance	Structure					
Peripheral Frame 0 (PF0)						
AdcaResultRegs	ADC_RESULT_REGS	ADCARESULT_BASE	0x0000_0B00	-	YES	YES
AdccResultRegs	ADC_RESULT_REGS	ADCCRESULT_BASE	0x0000_0B40	-	YES	YES
CpuTimer0Regs	CPUTIMER_REGS	CPUTIMER0_BASE	0x0000_0C00	-	-	-
CpuTimer1Regs	CPUTIMER_REGS	CPUTIMER1_BASE	0x0000_0C08	-	-	-
CpuTimer2Regs	CPUTIMER_REGS	CPUTIMER2_BASE	0x0000_0C10	-	-	-
PieCtrlRegs	PIE_CTRL_REGS	PIECTRL_BASE	0x0000_0CE0	-	-	-
DmaRegs	DMA_REGS	DMA_BASE	0x0000_1000	-	-	-
Dmach1Regs	DMA_CH_REGS	DMA_CH1_BASE	0x0000_1020	-	-	-
Dmach2Regs	DMA_CH_REGS	DMA_CH2_BASE	0x0000_1040	-	-	-
Dmach3Regs	DMA_CH_REGS	DMA_CH3_BASE	0x0000_1060	-	-	-
Dmach4Regs	DMA_CH_REGS	DMA_CH4_BASE	0x0000_1080	-	-	-
Dmach5Regs	DMA_CH_REGS	DMA_CH5_BASE	0x0000_10A0	-	-	-
Dmach6Regs	DMA_CH_REGS	DMA_CH6_BASE	0x0000_10C0	-	-	-
Peripheral Frame 1 (PF1)						
Clb1LogicCfgRegs	CLB_LOGIC_CONFIG_REGS	CLB1_LOGICCFG_BASE	0x0000_3000	-	YES	YES
Clb1LogicCtrlRegs	CLB_LOGIC_CONTROL_REGS	CLB1_LOGICCTRL_BASE	0x0000_3100	-	YES	YES
Clb1DataExchRegs	CLB_DATA_EXCHANGE_REGS	CLB1_DATAEXCH_BASE	0x0000_3180	-	YES	YES
Clb2LogicCfgRegs	CLB_LOGIC_CONFIG_REGS	CLB2_LOGICCFG_BASE	0x0000_3200	-	YES	YES
Clb1DataExchRegs	CLB_DATA_EXCHANGE_REGS	CLB1_DATAEXCH_BASE	0x0000_3300	-	YES	YES
Clb2LogicCfgRegs	CLB_LOGIC_CONFIG_REGS	CLB2_LOGICCFG_BASE	0x0000_3380	-	YES	YES
EPwm1Regs	EPWM_REGS	EPWM1_BASE	0x0000_4000	YES	YES	YES
EPwm2Regs	EPWM_REGS	EPWM2_BASE	0x0000_4100	YES	YES	YES
EPwm3Regs	EPWM_REGS	EPWM3_BASE	0x0000_4200	YES	YES	YES
EPwm4Regs	EPWM_REGS	EPWM4_BASE	0x0000_4300	YES	YES	YES
EPwm5Regs	EPWM_REGS	EPWM5_BASE	0x0000_4400	YES	YES	YES
EPwm6Regs	EPWM_REGS	EPWM6_BASE	0x0000_4500	YES	YES	YES
EPwm7Regs	EPWM_REGS	EPWM7_BASE	0x0000_4600	YES	YES	YES
EQep1Regs	EQEP_REGS	EQEP1_BASE	0x0000_5100	YES	YES	YES
EQep2Regs	EQEP_REGS	EQEP2_BASE	0x0000_5140	YES	YES	YES
ECap1Regs	ECAP_REGS	ECAP1_BASE	0x0000_5200	YES	YES	YES
ECap2Regs	ECAP_REGS	ECAP2_BASE	0x0000_5240	YES	YES	YES
ECap3Regs	ECAP_REGS	ECAP3_BASE	0x0000_5280	YES	YES	YES
Hrcap3Regs	HRCAP_REGS	HRCAP3_BASE	0x0000_52A0	YES	YES	YES
Cmpss1Regs	CMPSS_REGS	CMPSS1_BASE	0x0000_5C80	YES	YES	YES

Table 7-3. Peripheral Registers Memory Map (C28x) (continued)

Bit Field Name		DriverLib Name	Base Address	Pipeline Protected	DMA Access	HIC Access
Instance	Structure					
Cmpss2Regs	CMPSS_REGS	CMPSS2_BASE	0x0000_5CA0	YES	YES	YES
Cmpss3Regs	CMPSS_REGS	CMPSS3_BASE	0x0000_5CC0	YES	YES	YES
Cmpss4Regs	CMPSS_REGS	CMPSS4_BASE	0x0000_5CE0	YES	YES	YES
Peripheral Frame 2 (PF2)						
SpiaRegs	SPI_REGS	SPIA_BASE	0x0000_6100	YES	YES	YES
SpibRegs	SPI_REGS	SPIB_BASE	0x0000_6110	YES	YES	YES
BgcrcCpuRegs	BGCRC_REGS	BGCRC_CPU_BASE	0x0000_6340	YES	YES	YES
PmbusaRegs	PMBUS_REGS	PMBUSA_BASE	0x0000_6400	YES	YES	YES
HicRegs	HIC_CFG_REGS	HIC_BASE	0x0000_6500	YES	YES	YES
FsiTxaRegs	FSI_TX_REGS	FSITXA_BASE	0x0000_6600	YES	YES	YES
FsiRxaRegs	FSI_RX_REGS	FSIRXA_BASE	0x0000_6680	YES	YES	YES
Peripheral Frame 3 (PF3)						
AdcaRegs	ADC_REGS	ADCA_BASE	0x0000_7400	YES	-	-
AdccRegs	ADC_REGS	ADCC_BASE	0x0000_7500	YES	-	-
Peripheral Frame 4 (PF4)						
InputXbarRegs	INPUT_XBAR_REGS	INPUTXBAR_BASE	0x0000_7900	YES	-	-
XbarRegs	XBAR_REGS	XBAR_BASE	0x0000_7920	YES	-	-
SyncSocRegs	SYNC_SOC_REGS	SYNCSOC_BASE	0x0000_7940	YES	-	-
InputXbar2Regs	INPUT_XBAR_REGS	INPUTXBAR2_BASE	0x0000_7960	YES	-	-
DmaClaSrcSelRegs	DMA_CLA_SRC_SEL_REGS	DMACLASRCSEL_BASE	0x0000_7980	YES	-	-
EPwmXbarRegs	EPWM_XBAR_REGS	EPWMXBAR_BASE	0x0000_7A00	YES	-	-
ClbXbarRegs	CLB_XBAR_REGS	CLBXBAR_BASE	0x0000_7A40	YES	-	-
OutputXbarRegs	OUTPUT_XBAR_REGS	OUTPUTXBAR_BASE	0x0000_7A80	YES	-	-
OutputXbar2Regs	OUTPUT_XBAR_REGS	OUTPUTXBAR2_BASE	0x0000_7BC0	YES	-	-
GpioCtrlRegs	GPIO_CTRL_REGS	GPIOCTRL_BASE	0x0000_7C00	YES	-	-
GpioDataRegs	GPIO_DATA_REGS	GPIODATA_BASE	0x0000_7F00	YES	-	-
GpioDataReadRegs	GPIO_DATA_READ_REGS	GPIODATAREAD_BASE	0x0000_7F80	YES	-	YES
Peripheral Frame 5 (PF5)						
DevCfgRegs	DEV_CFG_REGS	DEVCFG_BASE	0x0005_D000	YES	-	-
ClkCfgRegs	CLK_CFG_REGS	CLKCFG_BASE	0x0005_D200	YES	-	-
CpuSysRegs	CPU_SYS_REGS	CPUSYS_BASE	0x0005_D300	YES	-	-
PeriphAcRegs	PERIPH_AC_REGS	PERIPHAC_BASE	0x0005_D500	YES	-	-
AnalogSubsysRegs	ANALOG_SUBSYS_REGS	ANALOGSUBSYS_BASE	0x0005_D700	YES	-	-
DcsmBank0Z1Regs	DCSM_BANK0_Z1_REGS	DCSM_BANK0_Z1_BASE	0x0005_F000	YES	-	-
DcsmBank0Z2Regs	DCSM_BANK0_Z2_REGS	DCSM_BANK0_Z2_BASE	0x0005_F040	YES	-	-
DcsmCommonRegs	DCSM_COMMON_REGS	DCSMCOMMON_BASE	0x0005_F070	YES	-	-
DcsmCommon2Regs	DCSM_COMMON2_REGS	DCSMCOMMON2_BASE	0x0005_F080	YES	-	-

Table 7-3. Peripheral Registers Memory Map (C28x) (continued)

Bit Field Name		DriverLib Name	Base Address	Pipeline Protected	DMA Access	HIC Access
Instance	Structure					
Peripheral Frame 6 (PF6)						
MemCfgRegs	MEM_CFG_REGS	MEMCFG_BASE	0x0005_F400	YES	-	-
AccessProtectionRegs	ACCESSPROTECTION_REGS	ACCESSPROTECTION_BASE	0x0005_F500	YES	-	-
MemoryErrorRegs	MEMORY_ERROR_REGS	MEMORYERROR_BASE	0x0005_F540	YES	-	-
RomWaitStateRegs	ROM_WAIT_STATE_REGS	ROMWAITSTATE_BASE	0x0005_F580	YES	-	-
RomPrefetchRegs	ROM_PREFETCH_REGS	ROMPREFETCH_BASE	0x0005_F588	YES	-	-
Flash0CtrlRegs	FLASH_CTRL_REGS	FLASH0CTRL_BASE	0x0005_F800	YES	-	-
Flash0EccRegs	FLASH_ECC_REGS	FLASH0ECCREGS_BASE	0x0005_FB00	YES	-	-
Peripheral Frame 7 (PF7)						
CanaRegs	CAN_REGS	CANA_BASE	0x0004_8000	YES	YES	YES
CanaMboxRegs	CAN_MBOX	CANAMBOX_BASE	0x0004_9000	YES	YES	YES
HwbistRegs	HWBIST_REGS	HWBIST_BASE	0x0005_E000	YES	-	-
MpostRegs	MPOST_REGS	MPOST_BASE	0x0005_E200	YES	-	-
Dcc0Regs	DCC_REGS	DCC0_BASE	0x0005_E700	YES	-	-
Dcc1Regs	DCC_REGS	DCC1_BASE	0x0005_E740	YES	-	-
EradGlobalRegs	ERAD_GLOBAL_REGS	ERADGLOBAL_BASE	0x0005_E800	YES	-	-
EradHWBP1Regs	ERAD_HWBP_REGS	ERADHWBP1_BASE	0x0005_E900	YES	-	-
EradHWBP2Regs	ERAD_HWBP_REGS	ERADHWBP2_BASE	0x0005_E908	YES	-	-
EradHWBP3Regs	ERAD_HWBP_REGS	ERADHWBP3_BASE	0x0005_E910	YES	-	-
EradHWBP4Regs	ERAD_HWBP_REGS	ERADHWBP4_BASE	0x0005_E918	YES	-	-
EradHWBP5Regs	ERAD_HWBP_REGS	ERADHWBP5_BASE	0x0005_E920	YES	-	-
EradHWBP6Regs	ERAD_HWBP_REGS	ERADHWBP6_BASE	0x0005_E928	YES	-	-
EradHWBP7Regs	ERAD_HWBP_REGS	ERADHWBP7_BASE	0x0005_E930	YES	-	-
EradHWBP8Regs	ERAD_HWBP_REGS	ERADHWBP8_BASE	0x0005_E938	YES	-	-
EradCounter1Regs	ERAD_COUNTER_REGS	ERADCOUNTER1_BASE	0x0005_E980	YES	-	-
EradCounter2Regs	ERAD_COUNTER_REGS	ERADCOUNTER2_BASE	0x0005_E990	YES	-	-
EradCounter3Regs	ERAD_COUNTER_REGS	ERADCOUNTER3_BASE	0x0005_E9A0	YES	-	-
EradCounter4Regs	ERAD_COUNTER_REGS	ERADCOUNTER4_BASE	0x0005_E9B0	YES	-	-
EradCRCGlobalRegs	ERAD_CRC_GLOBAL_REGS	ERADCRCGLOBAL_BASE	0x0005_EA00	YES	-	-
EradCRC1Regs	ERAD_CRC_REGS	ERADCRC1_BASE	0x0005_EA10	YES	-	-
EradCRC2Regs	ERAD_CRC_REGS	ERADCRC2_BASE	0x0005_EA20	YES	-	-
EradCRC3Regs	ERAD_CRC_REGS	ERADCRC3_BASE	0x0005_EA30	YES	-	-
EradCRC4Regs	ERAD_CRC_REGS	ERADCRC4_BASE	0x0005_EA40	YES	-	-
EradCRC5Regs	ERAD_CRC_REGS	ERADCRC5_BASE	0x0005_EA50	YES	-	-
EradCRC6Regs	ERAD_CRC_REGS	ERADCRC6_BASE	0x0005_EA60	YES	-	-
EradCRC7Regs	ERAD_CRC_REGS	ERADCRC7_BASE	0x0005_EA70	YES	-	-
EradCRC8Regs	ERAD_CRC_REGS	ERADCRC8_BASE	0x0005_EA80	YES	-	-

Table 7-3. Peripheral Registers Memory Map (C28x) (continued)

Bit Field Name		DriverLib Name	Base Address	Pipeline Protected	DMA Access	HIC Access
Instance	Structure					
Peripheral Frame 8 (PF8)						
LinaRegs	LIN_REGS	LINA_BASE	0x0000_6A00	YES	YES	YES
LinbRegs	LIN_REGS	LINB_BASE	0x0000_6B00	YES	YES	YES
Peripheral Frame 9 (PF9)						
WdRegs	WD_REGS	WD_BASE	0x0000_7000	YES	-	YES
NmiIntruptRegs	NMI_INTRUPT_REGS	NMI_BASE	0x0000_7060	YES	-	YES
XintRegs	XINT_REGS	XINT_BASE	0x0000_7070	YES	-	YES
SciaRegs	SCI_REGS	SCIA_BASE	0x0000_7200	YES	-	YES
I2caRegs	I2C_REGS	I2CA_BASE	0x0000_7300	YES	-	YES
I2cbRegs	I2C_REGS	I2CB_BASE	0x0000_7340	YES	-	YES

7.4 Identification

Table 7-4 lists the Device Identification Registers. Additional information on these device identification registers can be found in the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual*.

Table 7-4. Device Identification Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION	
PARTIDH	0x0005 D00A	2	Device part identification number	
			TMS320F280025	0x04FF 0500
			TMS320F280025C	0x04FF 0500
			TMS320F280023	0x04FD 0500
			TMS320F280023C	0x04FD 0500
			TMS320F280021	0x04FB 0500
REVID	0x0005 D00C	2	Silicon revision number	
			Revision 0	0x0000 0000
			Revision A	0x0000 0001
UID_UNIQUE	0x0007 01F4	2	Unique identification number. This number is different on each individual device with the same PARTIDH. This unique number can be used as a serial number in the application. This number is present only on TMS devices.	

7.5 Bus Architecture – Peripheral Connectivity

The Peripheral Connectivity table lists a broad view of the peripheral and configuration register accessibility from each bus master.

Table 7-5. Peripheral Connectivity

PERIPHERAL	C28	DMA	HIC	BGCRC
SYSTEM PERIPHERALS				
CPU Timers	Y			
ERAD	Y			
GPIO Data	Y		Y	
GPIO Pin Mapping and Configuration	Y			
XBAR Configuration	Y			
System Configuration	Y			
DCC	Y			
MEMORY				
M0/M1	Y			Y
LSx	Y			Y
GS0	Y	Y	Y	Y
ROM	Y			Y
FLASH	Y			
CONTROL PERIPHERALS				
ePWM/HRPWM	Y	Y	Y	
eCAP	Y	Y	Y	
eQEP[1]	Y	Y	Y	
ANALOG PERIPHERALS				
CMPSS[1]	Y	Y	Y	
ADC Configuration	Y			
ADC Results[1]	Y	Y	Y	
COMMUNICATION PERIPHERALS				
CAN	Y	Y	Y	
FSITX/FSIRX	Y	Y	Y	
I2C	Y		Y	
LIN	Y	Y	Y	
PMBus	Y	Y	Y	
SCI	Y		Y	
SPI	Y	Y	Y	

[1] These modules are accessible from DMA but cannot trigger a DMA transfer.

7.6 C28x Processor

The CPU is a 32-bit fixed-point processor. This device draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets.

The CPU features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and modified Harvard architecture. The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over six separate address/data buses.

For more information on CPU architecture and instruction set, see the *TMS320C28x CPU and Instruction Set Reference Guide*. For more information on the C28x Floating Point Unit (FPU), Trigonometric Math Unit, and Cyclic Redundancy Check (VCRC) instruction sets, see the *TMS320C28x Extended Instruction Sets Technical Reference Manual*. A brief overview of the FPU, TMU, and VCRC are provided here.

7.6.1 Floating-Point Unit (FPU)

The C28x plus floating-point (C28x+FPU) processor extends the capabilities of the C28x fixed-point CPU by adding registers and instructions to support IEEE single-precision floating-point operations.

Devices with the C28x+FPU include the standard C28x register set plus an additional set of floating-point unit registers. The additional floating-point unit registers are the following:

- Eight floating-point result registers, RnH (where n = 0–7)
- Floating-point Status Register (STF)
- Repeat Block Register (RB)

All of the floating-point registers, except the RB, are shadowed. This shadowing can be used in high-priority interrupts for fast context save and restore of the floating-point registers.

7.6.2 Fast Integer Division Unit

The Fast Integer Division (FINTDIV) unit of the C28x CPU uniquely supports three types of integer division (Truncated, Modulus, Euclidean) of varying data type sizes (16/16, 32/16, 32/32, 64/32, 64/64) in unsigned or signed formats.

- Truncated integer division is naturally supported by C language (/, % operators).
- Modulus and Euclidean divisions are variants that are more efficient for control algorithms and are supported by C intrinsics.

All three types of integer division produce both a quotient and remainder component, are interruptible, and execute in a minimum number of deterministic cycles (10 cycles for a 32/32 division). In addition, the Fast Division capabilities of the C28x CPU uniquely support fast execution of floating-point 32-bit (in 5 cycles) and 64-bit (in 20 cycles) division.

For more information about fast integer division, see the *Fast Integer Division – A Differentiated Offering From C2000™ Product Family Application Report*.

7.6.3 Trigonometric Math Unit (TMU)

The TMU extends the capabilities of a C28x+FPU by adding instructions and leveraging existing FPU instructions to speed up the execution of common trigonometric and arithmetic operations listed in Table 7-6.

Table 7-6. TMU Supported Instructions

INSTRUCTIONS	C EQUIVALENT OPERATION	PIPELINE CYCLES
MPY2PIF32 RaH,RbH	a = b * 2pi	2/3
DIV2PIF32 RaH,RbH	a = b / 2pi	2/3
DIVF32 RaH,RbH,RcH	a = b/c	5
SQRTF32 RaH,RbH	a = sqrt(b)	5
SINPUF32 RaH,RbH	a = sin(b*2pi)	4
COSPUF32 RaH,RbH	a = cos(b*2pi)	4
ATANPUF32 RaH,RbH	a = atan(b)/2pi	4
QUADF32 RaH,RbH,RcH,RdH	Operation to assist in calculating ATANPU2	5

No changes have been made to existing instructions, pipeline or memory bus architecture. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out their operations.

Exponent instruction IEXP2F32 and logarithmic instruction LOG2F32 have been added to support computation of floating-point power function for the non-linear proportional integral derivative control (NLPID) component of the C2000 Digital Control Library. These two added instructions reduce the power function calculations from a typical of 300 cycles using library emulation to less than 10 cycles.

7.6.4 VCRC Unit

Cyclic redundancy check (CRC) algorithms provide a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. The C28x+VCRC can perform 8-bit, 16-bit, 24-bit, and 32-bit CRCs. For example, the VCRC can compute the CRC for a block length of 10 bytes in 10 cycles. A CRC result register contains the current CRC, which is updated whenever a CRC instruction is executed.

The following are the CRC polynomials used by the CRC calculation logic of the VCRC:

- CRC8 polynomial = 0x07
- CRC16 polynomial 1 = 0x8005
- CRC16 polynomial 2 = 0x1021
- CRC24 polynomial = 0x5d6dcb
- CRC32 polynomial 1 = 0x04c11db7
- CRC32 polynomial 2 = 0x1edc6f41

This module can calculate CRCs for a byte of data in a single cycle. The CRC calculation for CRC8, CRC16, CRC24, and CRC32 is done byte-wise (instead of computing on a complete 16-bit or 32-bit data read by the C28x core) to match the byte-wise computation requirement mandated by various standards.

The VCRC Unit also allows the user to provide the size (1b-32b) and value of any polynomial to fit custom CRC requirements. The CRC execution time increases to three cycles when using a custom polynomial.

7.7 Embedded Real-Time Analysis and Diagnostic (ERAD)

The ERAD module enhances the debug and system-analysis capabilities of the device. The debug and system-analysis enhancements provided by the ERAD module is done outside of the CPU. The ERAD module consists of the Enhanced Bus Comparator units and the System Event Counter units. The Enhanced Bus Comparator units are used to generate hardware breakpoints, hardware watch points, and other output events. The System Event Counter units are used to analyze and profile the system. The ERAD module is accessible by the debugger and by the application software, which significantly increases the debug capabilities of many real-time systems, especially in situations where debuggers are not connected. In the TMS320F28002x devices, the ERAD module contains eight Enhanced Bus Comparator units (which increases the number of Hardware breakpoints from two to ten) and four Benchmark System Event Counter units.

7.8 Background CRC-32 (BGCRC)

The Background CRC (BGCRC) module computes a CRC-32 on a configurable block of memory. It accomplishes this by fetching the specified block of memory during idle cycles (when the CPU, HIC, or DMA is not accessing the memory block). The calculated CRC-32 value is compared against a golden CRC-32 value to indicate a pass or fail. In essence, the BGCRC helps identify memory faults and corruption.

The BGCRC module has the following features:

- One cycle CRC-32 computation on 32 bits of data
- No CPU bandwidth impact for zero wait state memory
- Minimal CPU bandwidth impact for non-zero wait state memory
- Dual operation modes (CRC-32 mode and scrub mode)
- Watchdog timer to time CRC-32 completion
- Ability to pause and resume CRC-32 computation

7.9 Direct Memory Access (DMA)

The DMA module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as “ping-pong” data between buffers. These features are useful for structuring data into blocks for optimal CPU processing. Figure 7-2 shows a device-level block diagram of the DMA.

DMA features include:

- Six channels with independent PIE interrupts
- Peripheral interrupt trigger sources
  - ADC interrupts and EVT signals
  - External Interrupts
  - ePWM SOC signals
  - CPU timers
  - eCAP
  - SPI transmit and receive
  - CAN transmit and receive
  - LIN transmit and receive
- Data sources and destinations:
  - GSx RAM
  - ADC result registers
  - Control peripheral registers (ePWM, eQEP, eCAP)
  - SPI, LIN, CAN, and PMBus registers
- Word Size: 16-bit or 32-bit (SPI limited to 16-bit)
- Throughput: Four cycles per word without arbitration

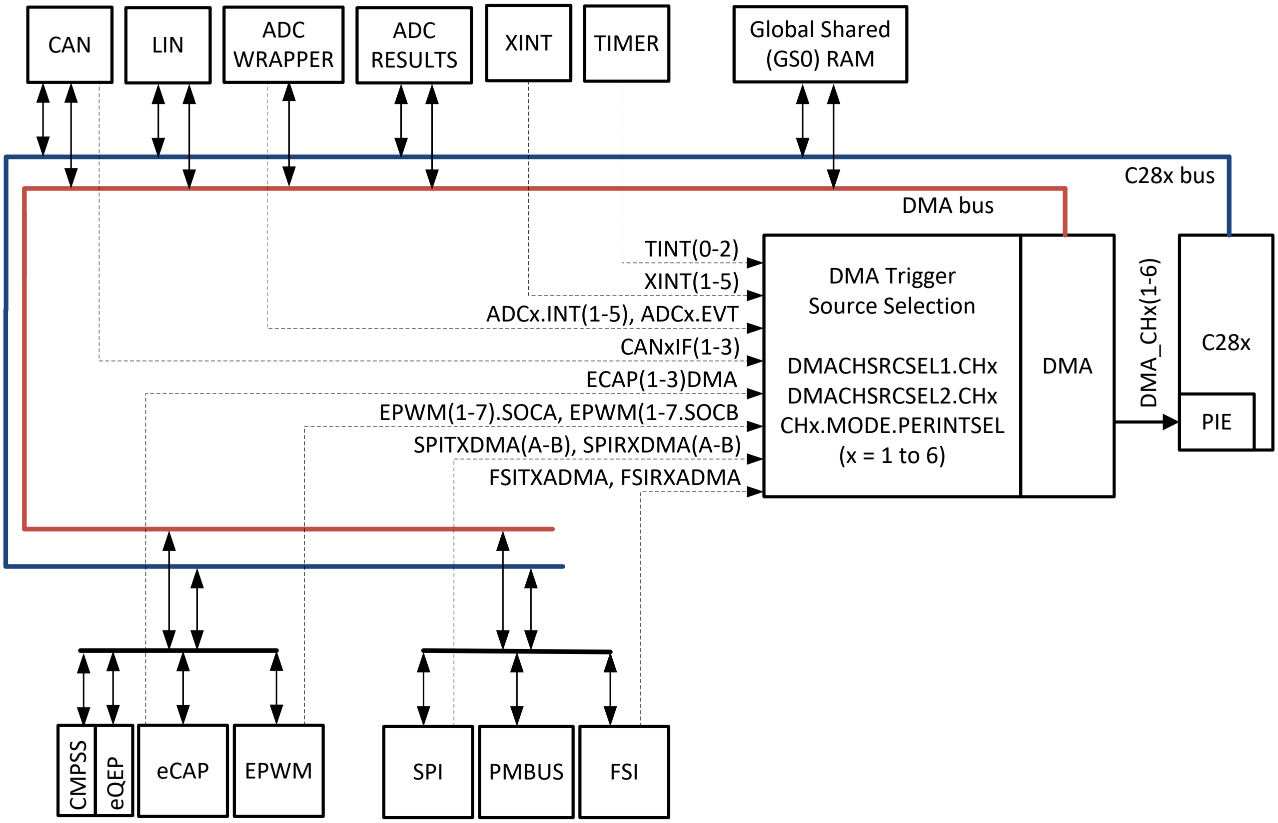


Figure 7-2. DMA Block Diagram

7.10 Device Boot Modes

This section explains the default boot modes, as well as all the available boot modes supported on this device. The boot ROM uses the boot mode select, general-purpose input/output (GPIO) pins to determine the boot mode configuration.

Table 7-7 shows the boot mode options available for selection by the default boot mode select pins. Users have the option to program the device to customize the boot modes selectable in the boot-up table as well as the boot mode select pin GPIOs used.

All the peripheral boot modes that are supported use the first instance of the peripheral module (SCIA, SPIA, I2CA, CANA, and so forth). Whenever these boot modes are referred to in this chapter, such as SCI boot, it is actually referring to the first module instance, which means the SCI boot on the SCIA port. The same applies to the other peripheral boots.

See Section 6.11.2.2.2 and Figure 6-11 for $t_{boot\text{-}flash}$, the boot ROM execution time to first instruction fetch in flash.

Table 7-7. Device Default Boot Modes

BOOT MODE	GPIO24 (DEFAULT BOOT MODE SELECT PIN 1)	GPIO32 (DEFAULT BOOT MODE SELECT PIN 0)
Parallel IO	0	0
SCI / Wait Boot(1)	0	1
CAN	1	0
Flash	1	1

(1) SCI boot mode can be used as a wait boot mode as long as SCI continues to wait for an 'A' or 'a' during the SCI autobaud lock process.

7.10.1 Device Boot Configurations

This section details what boot configurations are available and how to configure them. This device supports from 0 boot mode select pins up to 3 boot mode select pins as well as from 1 configured boot mode up to 8 configured boot modes.

To change and configure the device from the default settings to custom settings for your application, use the following process:

1. Determine all the various ways you want application to be able to boot. (For example: Primary boot option of Flash boot for your main application, secondary boot option of CAN boot for firmware updates, tertiary boot option of SCI boot for debugging, and so forth.)
2. Based on the number of boot modes needed, determine how many boot mode select pins (BMSPs) are required to select between your selected boot modes. (For example: 2 BMSPs are required to select between 3 boot mode options.)
3. Assign the required BMSPs to a physical GPIO pin. (For example, BMSP0 to GPIO10, BMSP1 to GPIO51, and BMSP2 left as default which is disabled). Refer to Section 7.10.1.1 for all the details on performing these configurations.
4. Assign the determined boot mode definitions to indexes in your custom boot table that correlate to the decoded value of the BMSPs. For example, BOOTDEF0=Boot to Flash, BOOTDEF1=CAN Boot, BOOTDEF2=SCI Boot; all other BOOTDEFx are left as default/nothing). Refer to Section 7.10.1.2 for all the details on setting up and configuring the custom boot mode table.

Additionally, the Boot Mode Example Use Cases section of the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual* provides some example use cases on how to configure the BMSPs and custom boot tables.

Note

The CAN boot mode turns on the XTAL. Be sure an XTAL is installed in the application before using CAN boot mode.

7.10.1.1 Configuring Boot Mode Pins

This section explains how the boot mode select pins can be customized by the user, by programming the BOOTPIN-CONFIG location (refer to Table 7-8) in the user-configurable dual-zone security module (DCSM) OTP. The location in the DCSM OTP is Z1-OTP-BOOTPIN-CONFIG or Z2-OTP-BOOTPIN-CONFIG. When debugging, EMU-BOOTPIN-CONFIG is the emulation equivalent of Z1-OTP-BOOTPIN-CONFIG/Z2-OTP-BOOTPIN-CONFIG, and can be programmed to experiment with different boot modes without writing to OTP. The device can be programmed to use 0, 1, 2, or 3 boot mode select pins as needed.

Note

When using Z2-OTP-BOOTPIN-CONFIG, the configurations programmed in this location will take priority over the configurations in Z1-OTP-BOOTPIN-CONFIG. It is recommended to use Z1-OTP-BOOTPIN-CONFIG first and then if OTP configurations need to be altered, switch to using Z2-OTP-BOOTPIN-CONFIG.

Table 7-8. BOOTPIN-CONFIG Bit Fields

BIT	NAME	DESCRIPTION
31:24	Key	Write 0x5A to these 8-bits to indicate the bits in this register are valid
23:16	Boot Mode Select Pin 2 (BMSP2)	Refer to BMSP0 description except for BMSP2
15:8	Boot Mode Select Pin 1 (BMSP1)	Refer to BMSP0 description except for BMSP1
7:0	Boot Mode Select Pin 0 (BMSP0)	Set to the GPIO pin to be used during boot (up to 255): - 0x0 = GPIO0 - 0x01 = GPIO1 - and so on Writing 0xFF disables BMSP0 and this pin is no longer used to select the boot mode.

The following GPIOs cannot be used as a BMSP. If selected for a particular BMSP, the boot ROM automatically selects the factory default GPIO (the factory default for BMSP2 is 0xFF, which disables the BMSP).

- GPIO 20 and GPIO 21
- GPIO 36 and GPIO 38
- GPIO 47 to GPIO 60
- GPIO 63 to GPIO 223

Table 7-9. Standalone Boot Mode Select Pin Decoding

BOOTPIN_CONFIG KEY	BMSP0	BMSP1	BMSP2	REALIZED BOOT MODE
!= 0x5A	Don't Care	Don't Care	Don't Care	Boot as defined by the factory default BMSPs
= 0x5A	0xFF	0xFF	0xFF	Boot as defined in the boot table for boot mode 0 (All BMSPs disabled)
	Valid GPIO	0xFF	0xFF	Boot as defined by the value of BMSP0 (BMSP1 and BMSP2 disabled)
	0xFF	Valid GPIO	0xFF	Boot as defined by the value of BMSP1 (BMSP0 and BMSP2 disabled)
	0xFF	0xFF	Valid GPIO	Boot as defined by the value of BMSP2 (BMSP0 and BMSP1 disabled)
	Valid GPIO	Valid GPIO	0xFF	Boot as defined by the values of BMSP0 and BMSP1 (BMSP2 disabled)
	Valid GPIO	0xFF	Valid GPIO	Boot as defined by the values of BMSP0 and BMSP2 (BMSP1 disabled)
	0xFF	Valid GPIO	Valid GPIO	Boot as defined by the values of BMSP1 and BMSP2 (BMSP0 disabled)
	Valid GPIO	Valid GPIO	Valid GPIO	Boot as defined by the values of BMSP0, BMSP1, and BMSP2
	Invalid GPIO	Valid GPIO	Valid GPIO	BMSP0 is reset to the factory default BMSP0 GPIO Boot as defined by the values of BMSP0, BMSP1, and BMSP2
	Valid GPIO	Invalid GPIO	Valid GPIO	BMSP1 is reset to the factory default BMSP1 GPIO Boot as defined by the values of BMSP0, BMSP1, and BMSP2
	Valid GPIO	Valid GPIO	Invalid GPIO	BMSP2 is reset to the factory default state, which is disabled Boot as defined by the values of BMSP0 and BMSP1

Note

When decoding the boot mode, BMSP0 is the least-significant-bit and BMSP2 is the most-significant-bit of the boot table index value. It is recommended when disabling BMSPs to start with disabling BMSP2. For example, in an instance when only using BMSP2 (BMSP1 and BMSP0 are disabled), then only the boot table indexes of 0 and 4 will be selectable. In the instance when using only BMSP0, then the selectable boot table indexes are 0 and 1.

7.10.1.2 Configuring Boot Mode Table Options

This section explains how to configure the boot definition table, BOOTDEF, for the device and the associated boot options. The 64-bit location is located in user-configurable DCSM OTP in the Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH locations. When debugging, EMU-BOOTDEF-LOW and EMU-BOOTDEF-HIGH are the emulation equivalents of Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH, and can be programmed to experiment with different boot mode options without writing to OTP. The range of customization to the boot definition table depends on how many boot mode select pins (BMSP) are being used. For example, 0 BMSPs equals to 1 table entry, 1 BMSP equals to 2 table entries, 2 BMSPs equals to 4 table entries, and 3 BMSPs equals to 8 table entries. Refer to the *TMS320F28002x Real-Time Microcontrollers Technical Reference Manual* for examples on how to set up the BOOTPIN_CONFIG and BOOTDEF values.

Note

The locations Z2-OTP-BOOTDEF-LOW and Z2-OTP-BOOTDEF-HIGH will be used instead of Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH locations when Z2-OTP-BOOTPIN-CONFIG is configured. Refer to Configuring Boot Mode Pins for more details on BOOTPIN_CONFIG usage.

Table 7-10. BOOTDEF Bit Fields

BOOTDEF NAME	BYTE POSITION	NAME	DESCRIPTION
BOOT_DEF0	7:0	BOOT_DEF0 Mode/Options	Set the boot mode for index 0 of the boot table. Different boot modes and their options can include, for example, a boot mode that uses different GPIOs for a specific bootloader or a different flash entry point address. Any unsupported boot mode will cause the device to either go to wait boot or boot to flash. Refer to *GPIO Assignments* for valid BOOTDEF values to set in the table.
BOOT_DEF1	15:8	BOOT_DEF1 Mode/Options	Refer to BOOT_DEF0 description
BOOT_DEF2	23:16	BOOT_DEF2 Mode/Options	
BOOT_DEF3	31:24	BOOT_DEF3 Mode/Options	
BOOT_DEF4	39:32	BOOT_DEF4 Mode/Options	
BOOT_DEF5	47:40	BOOT_DEF5 Mode/Options	
BOOT_DEF6	55:48	BOOT_DEF6 Mode/Options	
BOOT_DEF7	63:56	BOOT_DEF7 Mode/Options	

7.10.2 GPIO Assignments

This section details the GPIOs and boot option values used for boot mode set in the BOOT_DEF memory location located at Z1-OTP-BOOTDEF-LOW/ Z2-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH/ Z2-OTP-BOOTDEF-HIGH. Refer to Configuring Boot Mode Table Options on how to configure BOOT_DEF. When selecting a boot mode option, make sure to verify that the necessary pins are available in the pin mux options for the specific device package being used.

Table 7-11. SCI Boot Options

OPTION	BOOTDEF VALUE	SCITXDA GPIO	SCIRXDA GPIO
0 (default)	0x01	GPIO29	GPIO28
1	0x21	GPIO16	GPIO17
2	0x41	GPIO8	GPIO9
3	0x61	GPIO2	GPIO3
4	0x81	GPIO16	GPIO3

Table 7-12. CAN Boot Options

OPTION	BOOTDEF VALUE	CANTXA GPIO	CANRXA GPIO
0 (default)	0x02	GPIO4	GPIO5
1	0x22	GPIO32	GPIO33
2	0x42	GPIO2	GPIO3

Table 7-13. I2C Boot Options

OPTION	BOOTDEF VALUE	SDAA GPIO	SCLA GPIO
0	0x07	GPIO32	GPIO33
1	0x27	GPIO0	GPIO1
2	0x47	GPIO10	GPIO8

Table 7-14. RAM Boot Options

OPTION	BOOTDEF VALUE	RAM ENTRY POINT (ADDRESS)
0	0x05	0x0000 0000

Table 7-15. Flash Boot Options

OPTION	BOOTDEF VALUE	FLASH ENTRY POINT (ADDRESS)	FLASH SECTOR
0 (default)	0x03	0x0008 0000	Bank0 Sector 0
1	0x23	0x0008 4000	Bank 0 Sector 4
2	0x43	0x0008 8000	Bank 0 Sector 8
3	0x63	0x0008 EFF0	Bank 0, End of Sector 14

Table 7-16. Wait Boot Options

OPTION	BOOTDEF VALUE	WATCHDOG
0	0x04	Enabled
1	0x24	Disabled

Table 7-17. SPI Boot Options

OPTION	BOOTDEF VALUE	SPISIMOA	SPISOMIA	SPICLKA	SPISTEA
0	0x06	GPIO2	GPIO1	GPIO3	GPIO5
1	0x26	GPIO16	GPIO1	GPIO3	GPIO0
2	0x46	GPIO8	GPIO10	GPIO9	GPIO11
3	0x66	GPIO8	GPIO17	GPIO9	GPIO11

Table 7-18. Parallel Boot Options

OPTION	BOOTDEF VALUE	D0-D7 GPIO	28x(DSP) CONTROL GPIO	HOST CONTROL GPIO
0 (default)	0x00	D0 - GPIO28	GPIO16	GPIO29
		D1 - GPIO1		
		D2 - GPIO2		
		D3 - GPIO3		
		D4 - GPIO4		
		D5 - GPIO5		
		D6 - GPIO6		
		D7 - GPIO7		
1	0x20	D0 - GPIO0	GPIO16	GPIO11
		D1 - GPIO1		
		D2 - GPIO2		
		D3 - GPIO3		
		D4 - GPIO4		
		D5 - GPIO5		
		D6 - GPIO6		
		D7 - GPIO7		

7.11 Dual Code Security Module

The dual code security module (DCSM) prevents access to on-chip secure memories. The term “secure” means access to secure memories and resources is blocked. The term “unsecure” means access is allowed; for example, through a debugging tool such as Code Composer Studio™ (CCS).

The code security mechanism offers protection for two zones, Zone 1 (Z1) and Zone 2 (Z2). The security implementation for both the zones is identical. Each zone has its own dedicated secure resource (OTP memory and secure ROM) and allocated secure resource (LSx RAM and flash sectors).

The security of each zone is ensured by its own 128-bit password (CSM password). The password for each zone is stored in an OTP memory location based on a zone-specific link pointer. The link pointer value can be changed to program a different set of security settings (including passwords) in OTP.

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

7.12 Watchdog

The watchdog module is the same as the one on previous TMS320C2000 devices, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backward-compatible.

The watchdog generates either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

Figure 7-3 shows the various functional blocks within the watchdog module.

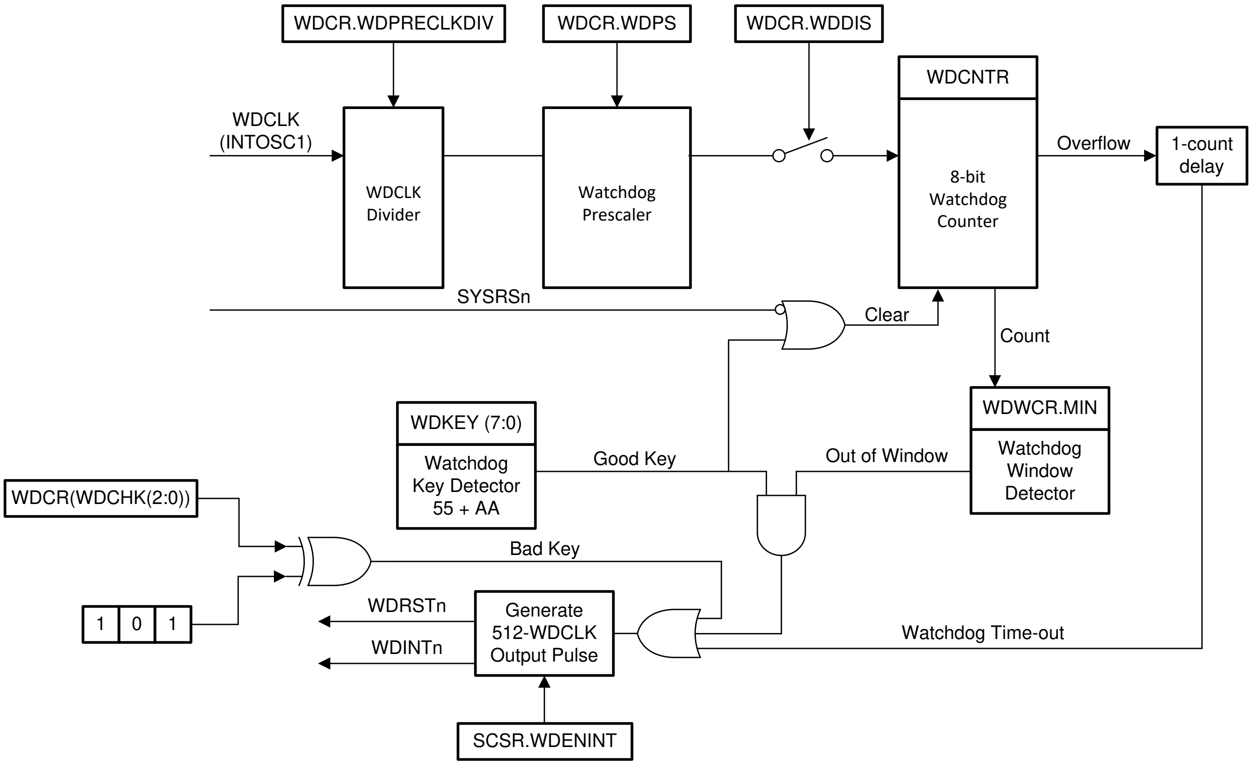


Figure 7-3. Windowed Watchdog

7.13 C28x Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register that generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and is connected to INT13 of the CPU. CPU-Timer 2 is reserved for TI-RTOS. It is connected to INT14 of the CPU. If TI-RTOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:
- SYSCLK (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTOSC2)
- X1 (XTAL)

7.14 Dual-Clock Comparator (DCC)

There are three Dual-Clock Comparators (DCC0 and DCC1) on the device. All three DCCs are only accessible through CPU1. The DCC module is used for evaluating and monitoring the clock input based on a second clock, which can be a more accurate and reliable version. This instrumentation is used to detect faults in clock source or clock structures, thereby enhancing the system's safety metrics.

7.14.1 Features

The DCC has the following features:
- Allows the application to ensure that a fixed ratio is maintained between frequencies of two clock signals.
- Supports the definition of a programmable tolerance window in terms of the number of reference clock cycles.
- Supports continuous monitoring without requiring application intervention.
- Supports a single-sequence mode for spot measurements.
- Allows the selection of a clock source for each of the counters, resulting in several specific use cases.

7.14.2 Mapping of DCCx (DCC0 and DCC1) Clock Source Inputs

Table 7-19. DCCx Clock Source0 Table

DCCxCLKSRC0[3:0]	CLOCK NAME
0x0	XTAL/X1
0x1	INTOSC1
0x2	INTOSC2
0x5	CPU1.SYSCLK
0xC	INPUT XBAR (Output16 of input-xbar)
others	Reserved

Table 7-20. DCCx Clock Source1 Table

DCCxCLKSRC1[4:0]	CLOCK NAME
0x0	PLLRAWCLK
0x2	INTOSC1
0x3	INTOSC2
0x6	CPU1.SYSCLK
0x9	Input XBAR (Output15 of the input-xbar)
0xB	EPWMCLK
0xC	LSPCLK
0xD	ADCCLK
0xE	WDCLK
0xF	CAN0BITCLK
others	Reserved

7.15 Configurable Logic Block (CLB)

The C2000 configurable logic block (CLB) is a collection of blocks that can be interconnected using software to implement custom digital logic functions or enhance existing on-chip peripherals. The CLB is able to enhance existing peripherals through a set of crossbar interconnections, which provide a high level of connectivity to existing control peripherals such as enhanced pulse width modulators (ePWM), enhanced capture modules (eCAP), and enhanced quadrature encoder pulse modules (eQEP). The crossbars also allow the CLB to be connected to external GPIO pins. In this way, the CLB can be configured to interact with device peripherals to perform small logical functions such as comparators, or to implement custom serial data exchange protocols. Through the CLB, functions that would otherwise be accomplished using external logic devices can now be implemented inside the MCU.

The CLB peripheral is configured through the CLB tool. For more information on the CLB tool, available examples, application reports and users guide, please refer to the following location in your C2000Ware package (C2000Ware_2_00_00_03 and higher):

- **C2000WARE_INSTALL_LOCATION\utilities\clb_tool\clb_syscfg\doc**
- *CLB Tool User's Guide*
- *Designing With the C2000™ Configurable Logic Block (CLB) Application Report*
- *How to Migrate Custom Logic From an FPGA/CPLD to C2000™ Microcontrollers Application Report*

The CLB module and its interconnections are shown in Figure 7-4.

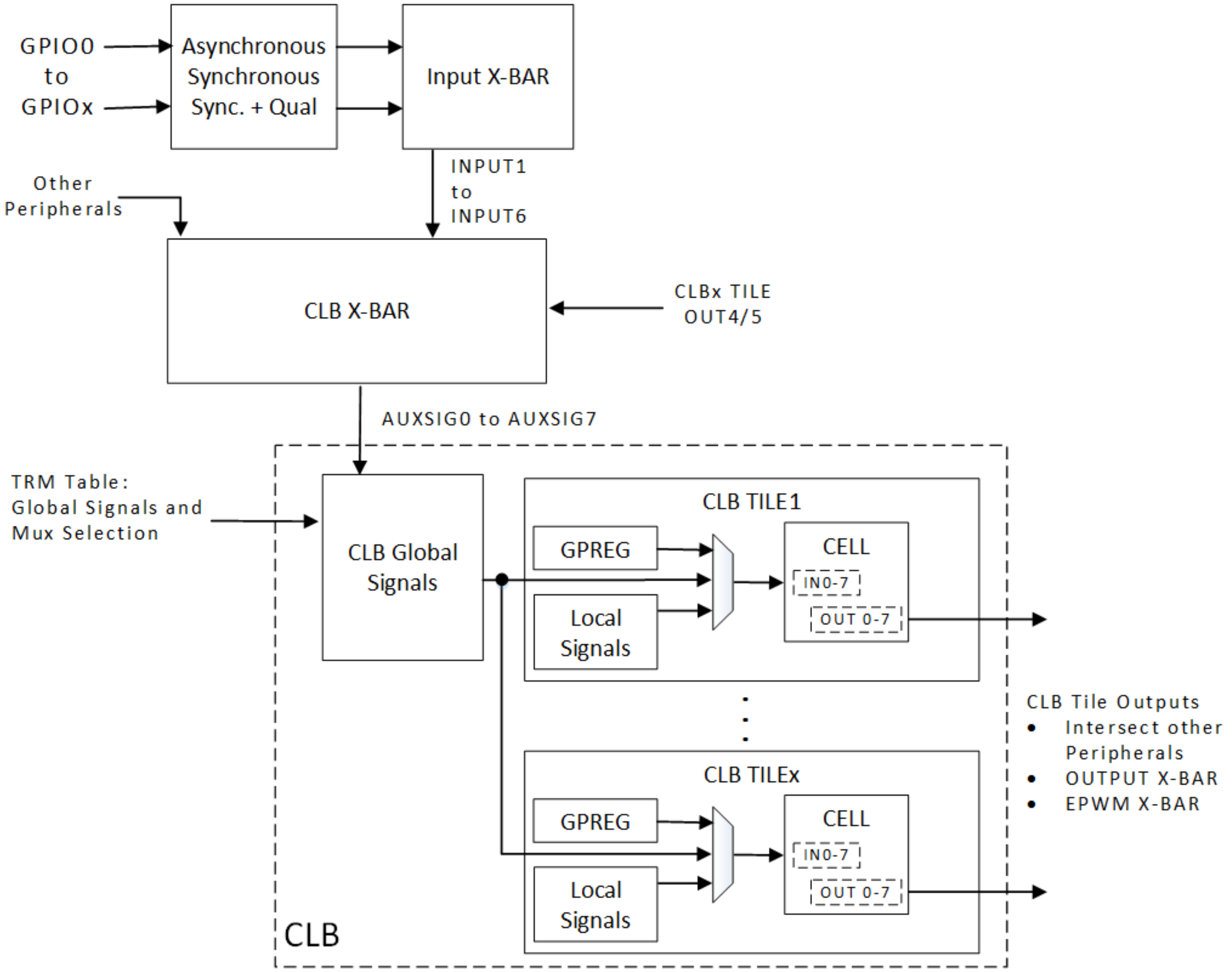


Figure 7-4. CLB Overview

Absolute encoder protocol interfaces are now provided as Position Manager solutions in the C2000Ware MotorControl SDK. Configuration files, application programmer interface (API), and use examples for such solutions are provided with C2000Ware MotorControl SDK. In some solutions, the TI-configured CLB is used with other on-chip resources, such as the SPI port or the C28x CPU, to perform more complex functionality.

8 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

The *Hardware Design Guide for F2800x C2000™ Real-Time MCU Series Application Note* is an essential guide for hardware developers using C2000 devices, and helps to streamline the design process while mitigating the potential for faulty designs. Key topics discussed include: power requirements; general-purpose input/output (GPIO) connections; analog inputs and ADC; clocking generation and requirements; and JTAG debugging among many others.

8.1 Key Device Features

Table 8-1. Key Device Features

MODULE	FEATURE	SYSTEM BENEFIT
	PROCESSING	
Real-time control CPUs	Up to 200 MIPS C28x: 100 MIPS CLA: 100 MIPS Flash: Up to 256KB RAM : Up to 100KB 32-bit Floating-Point Unit (FPU32) Trigonometric Math Unit (TMU) Vertibi Complex Math Unit (VCU)	TI's 32-bit C28x DSP core, provides 100 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM Provides 100 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. **FPU32:** Native hardware support for IEEE-754 single-precision floating-point operations **TMU:** Accelerators used to speed up execution of trigonometric and arithmetic operations for faster computation (such as PLL and DQ transform) optimized for control applications. Helps in achieving faster control loops, resulting in higher efficiency and better component sizing. Special instructions to support nonlinear PID control algorithms **VCU:** Reduces the latency for complex math operations commonly found in encoded applications Real-time Benchmarks Showcasing C2000™ControlMCU's Optimized Signal Chain
	SENSING	
Analog-to-Digital Converter (ADC) (12-bit)	Up to 3 ADC modules 3.45 MSPS Up to 21 channels	ADC provides precise and concurrent sampling of all three-phase currents and DC bus with zero jitter. ADC post-processing – On-chip hardware reduces ADC ISR complexity and shortens current loop cycles. More ADCs help in multiphase applications. Provide better effective MSPS (oversampling) and typical ENOB for better control-loop performance.

Table 8-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
Comparator Subsystem (CMPSS)	**CMPSS** 2 windowed comparator Dual 12-bit DACs DAC ramp generation Low DAC output on external pin Digital filters 60-ns detection to trip time Slope compensation	**System protection without false alarms:** Comparator Subsystem (CMPSS) modules are useful for applications such as peak-current mode control, switched-mode power, power factor correction, and voltage trip monitoring. PWM trip-triggering and removal of unwanted noise are easy with blanking window and filtering features provided with the analog comparator subsystems. Provides better control accuracy. No need for further CPU configuration to control the PWM with the comparator and 12-bit DAC (CMPSS). Enables protection and control using the same pin.
Enhanced Quadrature Encoder Pulse (eQEP)	2 eQEP modules	Used for direct interface with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine used in a high-performance motion and position-control system. Also can be used in other applications to count input pulses from an external device (such as a sensor).
Enhanced Capture (eCAP) / High Resolution Enhanced Capture (HRCAP)	7 eCAP modules (2 with HRCAP capability) Measures elapsed time between events (up to 4 time-stamped events). Connects to any GPIO through the input X-BAR. When not used in capture mode, the eCAP module can be configured as a single-channel PWM output (APWM).	**Applications for eCAP include:** Speed measurements of rotating machinery (for example, toothed sprockets sensed through Hall sensors) Elapsed time measurements between position sensor pulses Period and duty cycle measurements of pulse train signals Decoding current or voltage amplitude derived from duty-cycle encoded current/voltage sensors
	2 HRCAP channels Provides the capability to measure the width of external pulses with a typical resolution of 300 ps.	**Applications for HRCAP include:** High-resolution period and duty-cycle measurements of pulse train cycles Instantaneous speed measurements Instantaneous frequency measurements Voltage measurements across an isolation boundary Distance/sonar measurement and scanning Flow measurements Capacitive touch applications

Table 8-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
ACTUATION		
Enhanced Pulse Width Modulation (ePWM) / High-Resolution Pulse Width Modulation (HRPWM)	Up to 16 ePWM channels Ability to generate high-side/low-side PWMs with deadband Supports Valley switching (ability to switch PWM output at valley point) and features like blanking window	Flexible PWM waveform generation with best power topology coverage. Shadowed deadband and shadowed action qualifier enable adaptive PWM generation and protection for improved control accuracy and reduced power loss. Enables improvement in Power Factor (PF) and Total Harmonic Distortion (THD), which is especially relevant in Power Factor Correction (PFC) applications. Improves light load efficiency.
	HRPWM capability: All the 16 channels provide high-resolution capability (150 ps) Provides 150-ps steps for duty cycle, period, deadband, and phase offsets for 99% greater precision	Beneficial for accurate control and enables better-performance high-frequency power conversion. Achieves cleaner waveforms and avoids oscillations/limit cycle at output.
	One-shot and global reload feature	Critical for variable-frequency and multiphase DC-DC applications and helps in attaining high-frequency control loops (>2 MHz). Enables control of interleaved LLC topologies at high frequencies
	Independent PWM action on a Cycle-by-Cycle (CBC) trip event and an One-Shot Trip (OST) trip event	Provides cycle-by-cycle protection and complete shutoff of PWM under fault condition. Helps implement multiphase PFC or DC-DC control.
	Load on SYNC (support for shadow-to-active load on a SYNC event)	Enables variable-frequency applications (allows LLC control in power conversion).
	Ability to shut down the PWMs without software intervention (no ISR latency)	Fast protection under fault condition
	Delayed Trip Functionality	Helps implement the deadband with Peak Current Mode Control (PCMC) Phase- Shifted Full Bride (PSFB) DC-DC easily without occupying much CPU resources (even on trigger events based on comparator, trip, or sync-in events).
	Deadband Generator (DB) submodule	Prevents simultaneous ON conditions of High and Low side gates by adding programmable delay to rising (RED) and falling (FED) PWM signal edges.
	Flexible PWM Phase Relationships and Timer Synchronization	Each ePWM module can be synchronized with other ePWM modules or other peripherals. Keeps PWM edges in synchronization with each other or with certain events. Supports flexible ADC scheduling with specific sampling window in synchronization with power device switching.
CONNECTIVITY		
Serial Peripheral Interface (SPI)	2 high-speed SPI port	Supports 25 MHz
Serial Communication Interface (SCI)	2 SCI (UART) modules	Interfaces with controllers
Local Interconnect Network (LIN)	1 LIN	Provides a low-cost solution where the bandwidth and fault tolerance of a Controller Area Network (CAN) are not required. Can also be used as SCI to communication with other controllers.
Controller Area Network (CAN/ DCAN)	1 DCAN module	Provides compatibility with classic CAN modules
Inter-Integrated Circuit (I2C)	1 I2C modules	Interfaces with external EEPROMs, sensors, or controllers

Table 8-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
Power-Management Bus (PMBus)	1 PMBus module Compliance with the SMI Forum PMBus Specification (Part I v1.0 and Part II v1.1)	Seamless HW-based host communication
Fast Serial Interface (FSI) with a transmitter and receiver	Up to 1 FSI transmitters and 1 FSI receivers Serial communication peripheral capable of reliable high-speed communication (up to 100 MHz) across isolation devices	Fast serial interface (FSI) can be useful for low-pin count, high-speed communication even across isolation boundary at up to 100Mbps.
OTHER SYSTEM FEATURES		
Security enhancers	Dual-zone Code Security Module (DCSM) Watchdog Write Protection on Register Missing Clock Detection Logic (MCD) Error Correction Code (ECC) and parity	**DCSM:** Prevents duplication and reverse-engineering of proprietary code **Watchdog:** Generates reset if CPU gets stuck in endless loops of execution **Write Protection on Registers:** LOCK protection on system configuration registers Protection against spurious CPU writes **MCD:** Automatic clock failure detection **ECC and parity:** Single-bit error correction and double-bit error detection
Crossbars (XBARs)	Provides flexibility to connect device inputs, outputs, and internal resources in a variety of configurations. • Input X-BAR • Output X-BAR • ePWM X-BAR • CLB X-BAR	**Enhances hardware design versatility:** **Input X-BAR:** Routes signals from any GPIO to multiple IP blocks within the chip **Output XBAR:** Routes internal signals onto designated GPIO pins **ePWM X-BAR:** Routes internal signals from various IP blocks to EPWM **CLB X-BAR:** Allows user to bring signals from various IP blocks to CLB

8.2 Application Information

8.2.1 Typical Application

The *Typical Applications* section details *some* applications of this device. For a more extensive list of applications, see the *Applications* section of this data sheet.

8.2.1.1 Servo Drive Control Module

Servo drives require high precision current and voltage sensing for accurate torque control and often supports interfaces for multiple encoder types along with communication interfaces. This C2000 device can be used either as single chip solution for standalone servo drive (shown in Figure 8-1) or can be used in decentralized systems (shown in Figure 8-2). In the later case, the F2838x C2000 device functions as the controller which samples all the voltage and current inputs and generates the correct PWM signals for inverter. Each C2000 device serves as real-time controller for a target axis, running motor current control loop. Using the Fast Serial Interface (FSI) peripheral, up to 16 axes can be managed with one C2000 device. As an outer loop controller, the C2000 device executes main axis motor control, controls data exchange with all secondary axis over FSI and communicates with a host or PLC through EtherCAT.

8.2.1.1.1 System Block Diagram

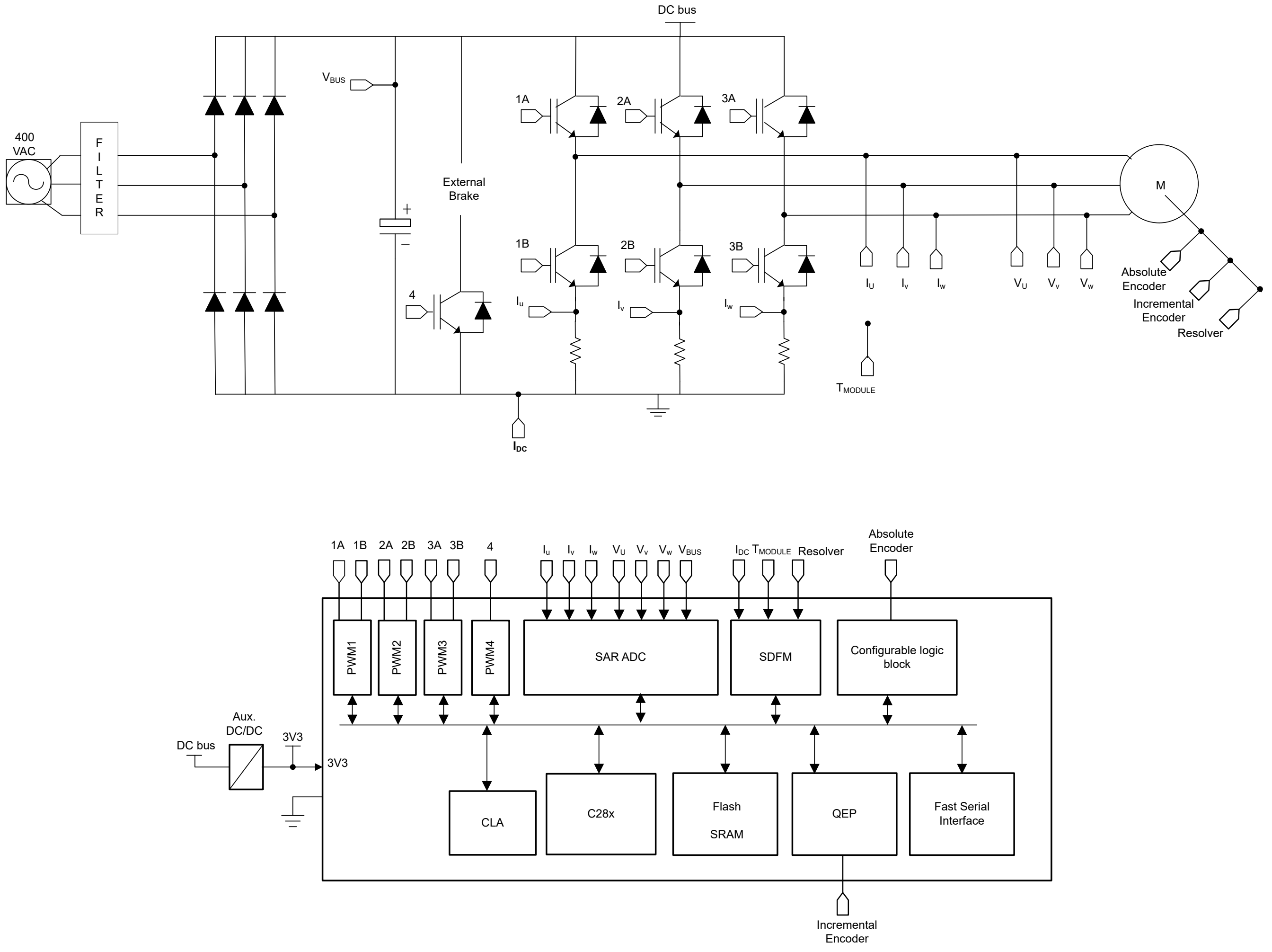


Figure 8-1. Servo Drive Control Module

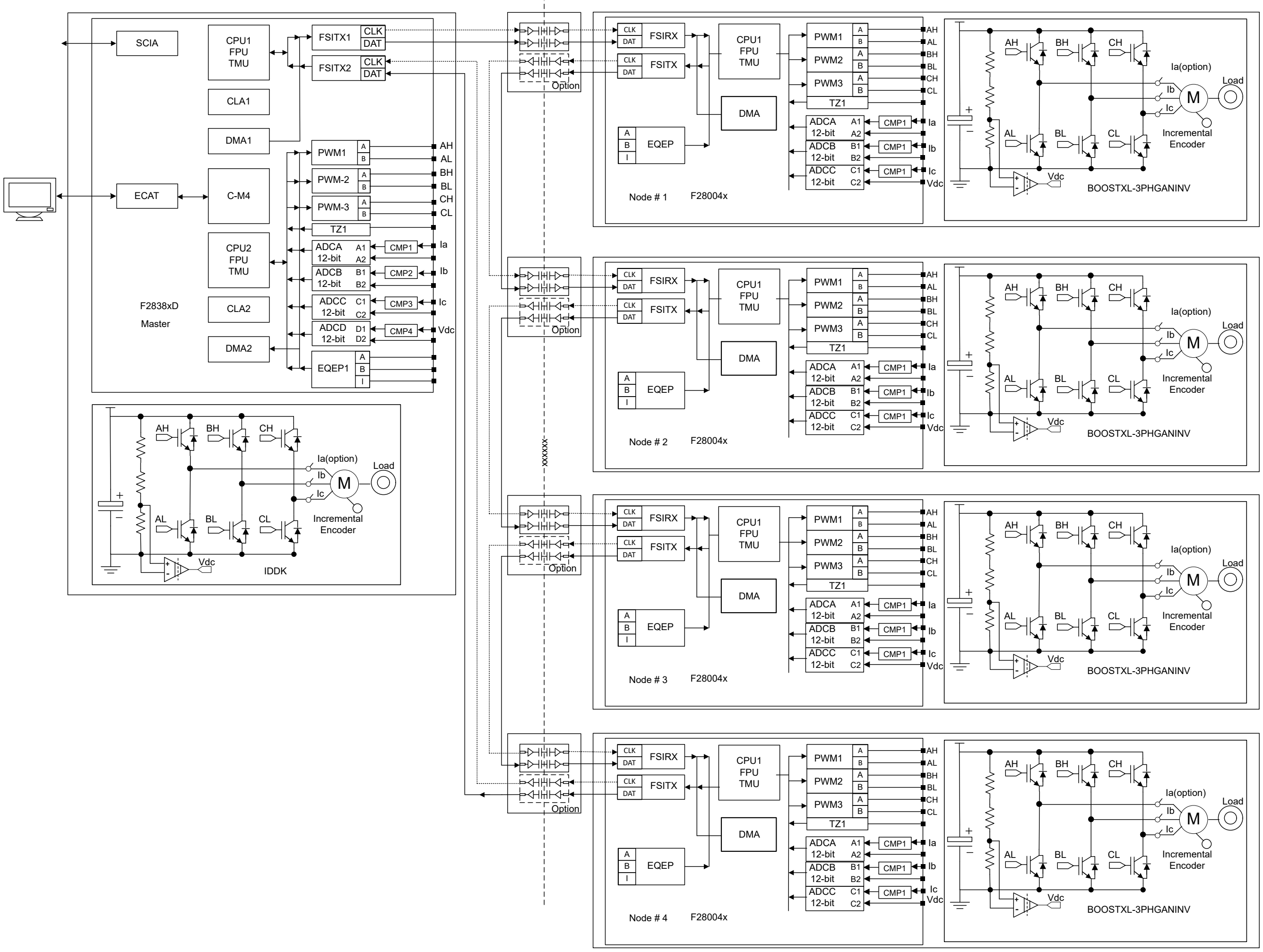


Figure 8-2. Distributed Multi-Axis Servo Drive

8.2.1.1.2 Servo Drive Control Module Resources

Reference Designs and Associated Training Videos

48-V Three-Phase Inverter With Shunt-Based In-Line Motor Phase Current Sensing Evaluation Module

The BOOSTXL-3PHGANINV evaluation module features a 48-V/10-A three-phase GaN inverter with precision in-line shunt-based phase current sensing for accurate control of precision drives such as servo drives.

C2000 DesignDRIVE Development Kit for Industrial Motor Control

The DesignDRIVE Development Kit (IDDK) hardware offers an integrated servo drive design with full power stage to drive a high voltage three-phase motor and eases the evaluation of a range of position feedback, current sensing and control topologies.

C2000 DesignDRIVE position manager BoosterPack™ plug-in module

The PositionManager BoosterPack is a flexible low voltage platform intended for evaluating interfaces to absolute encoders and analog sensors like resolvers and SinCos transducers. When combined with the DesignDRIVE Position Manager software solutions this low-cost evaluation module becomes a powerful tool for interfacing many popular position encoder types such as EnDat, BiSS and T-format with C2000 Real-Time Control devices. C2000 Position Manager technology integrates interfaces to the most popular digital and analog position sensors onto C2000 Real-Time Controller, thus eliminating the need for external FPGAs for these functions.

C2000Ware MotorControl SDK
MotorControl SDK for C2000™ microcontrollers (MCU) is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 real-time controller based motor control system development time targeted for various three-phase motor control applications. The software includes firmware that runs on C2000 motor control evaluation modules (EVMs) and TI designs (TIDs) which are targeted for industrial drives, robotics, appliances, and automotive applications. MotorControl SDK provides all the needed resources at every stage of development and evaluation for high performance motor control applications.

TIDM-02006 Distributed multi-axis servo drive over fast serial interface (FSI) reference design
This reference design presents an example distributed or decentralized multi-axis servo drive over Fast Serial Interface (FSI) using C2000™ real-time controllers. Multi-axis servo drives are used in many applications such as factory automation and robots. The cost per axis, performance and ease of use are always high concerns for such systems. FSI is a cost-optimized and reliable high speed communication interface with low jitter that can daisy-chain multiple C2000 microcontrollers. In this design, each TMS320F280049 or TMS320F280025 real-time controller serves as a real-time controller for a distributed axis, running motor current control loop. A single TMS320F28388D runs position and speed control loops for all axes. The same F2838x also executes a centralized motor control axis plus EtherCAT communication, leveraging its multiple cores. The design uses our existing EVM kits, the software is released within C2000WARE MotorControl SDK.

8.2.1.2 Server or Telecom Power Supply Unit (PSU)

A server or telecom power supply unit (PSU) consists of a power factor correction (PFC) stage and a DC-DC converter stage. The Totem pole PFC is widely used as the PFC stage. For the DC-DC stage, LLC and phase-shifted full bridge (PSFB) are the two most popular topologies. Usually, current server PSU is based on a two-chip architecture, as shown in Figure 8-3. Telecom PSU is more likely to have a single-chip architecture, as shown in Figure 8-4.

The PFC stage draws sine-wave current from the AC mains in phase with the AC voltage, and maintains a steady DC bus voltage (VDC, typically +400 V) across its output. This output voltage is applied to the input of DC-DC stage, which converts it to an isolated low-output voltage Vout (12 V/48 V for server, 48 V for telecom).

8.2.1.2.1 System Block Diagram

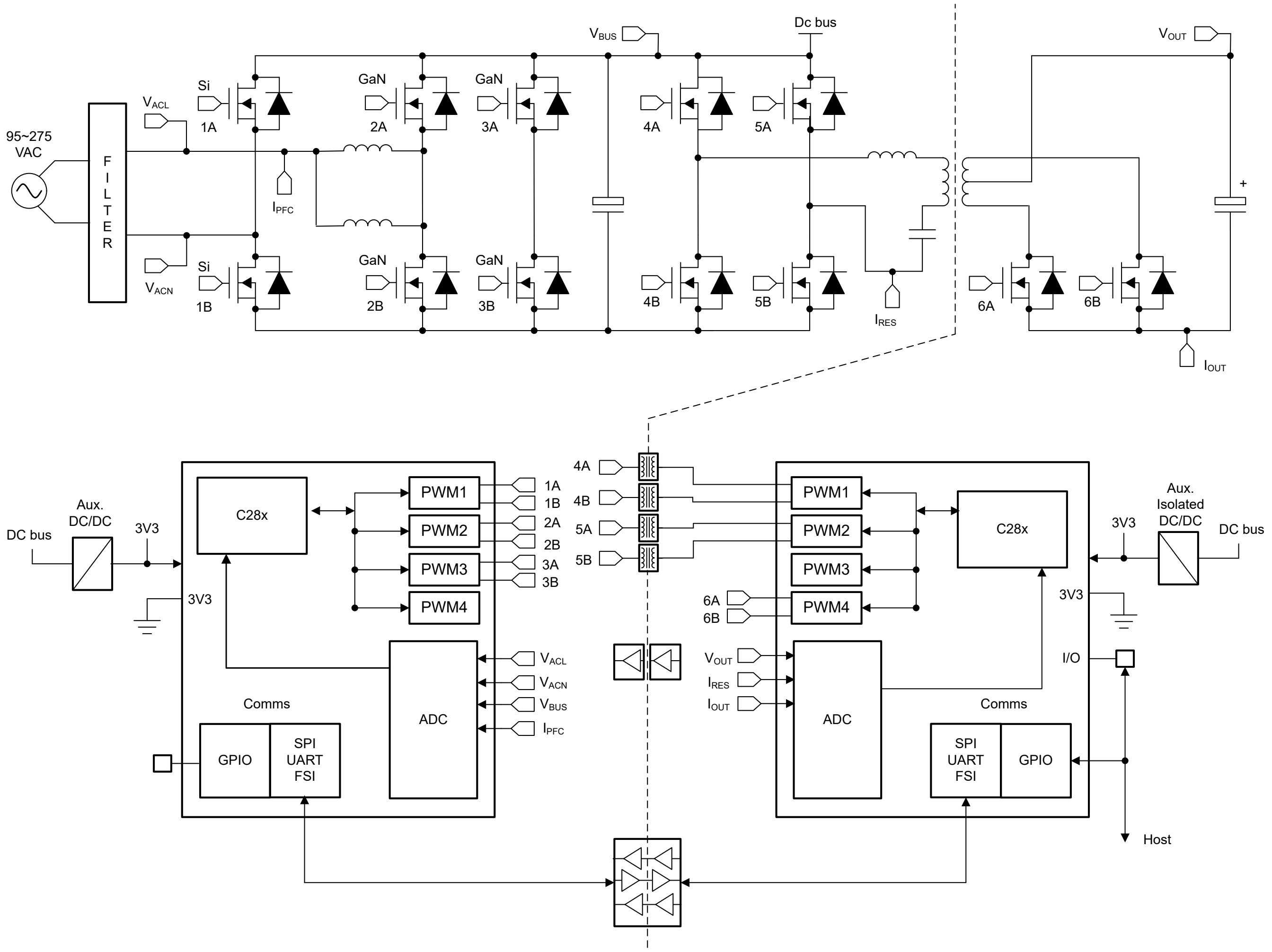


Figure 8-3. Typical Server PSU Architecture

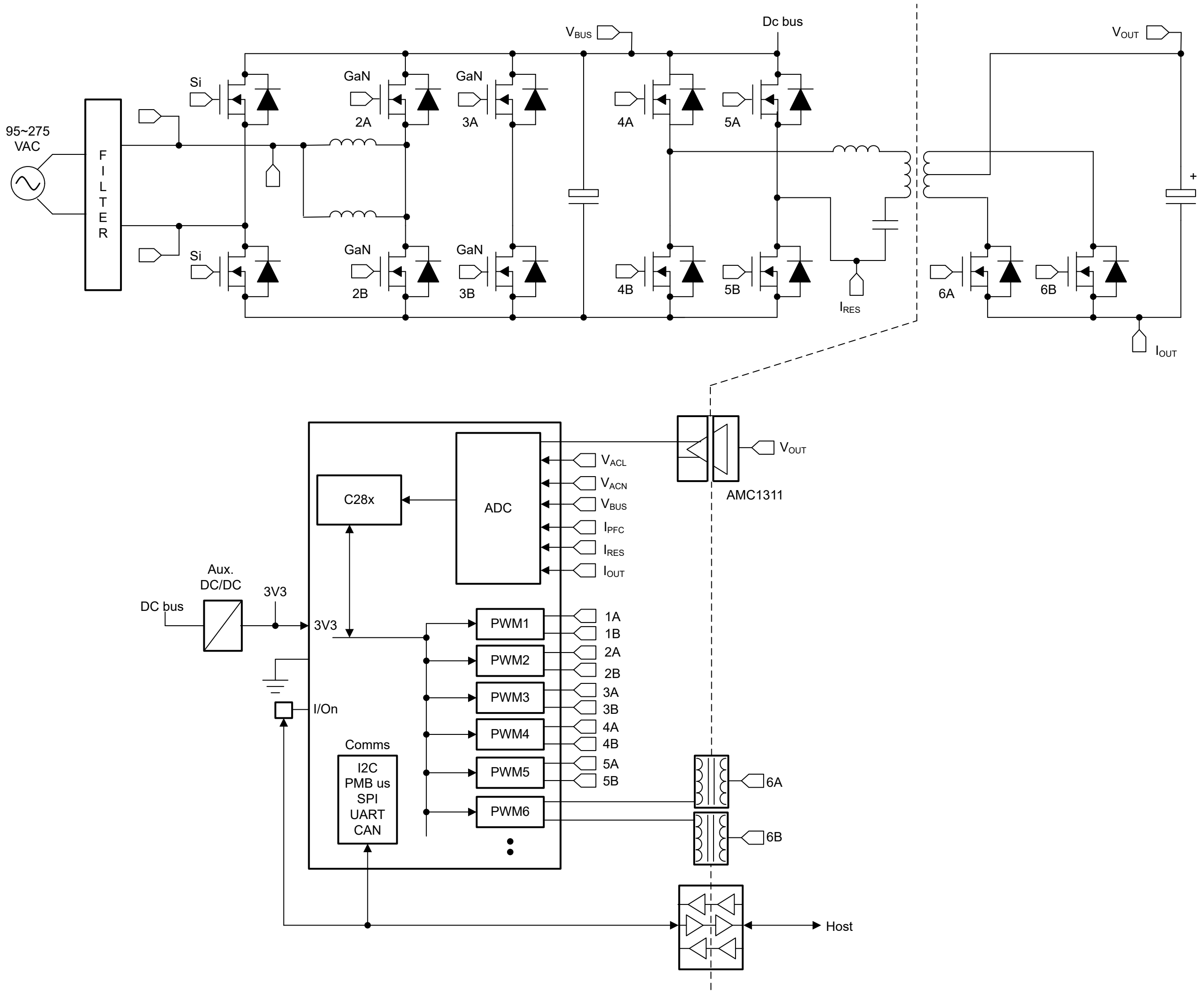


Figure 8-4. Typical Telecom PSU Architecture

8.2.1.2.2 Server and Telecom PSU Resources

Reference Designs and Associated Training Videos

PMP41081 1-kW, 12-V HHC LLC reference design using C2000™ real-time microcontroller
This reference design is a 1-kW, 400-V to 12-V half-bridge resonant DC/DC platform used to evaluate the load transient performance of hybrid-hysteretic control (HHC) with a C2000™ microcontroller.

3-kW phase-shifted full bridge with active clamp reference design with > 270-W/in3 power density
This reference design is a GaN-based 3-kW phase-shifted full bridge (PSFB) targeting maximum power density. The design has an active clamp to minimize voltage stress on the secondary synchronous rectifier MOSFETs enabling use of lower voltage-rating MOSFETs with better figure-of-merit (FoM). PMP23126 uses our 30mΩ GaN on the primary side and silicon MOSFETs on the secondary side. The LMG3522 top-side cooled GaN with integrated driver and protection enables higher efficiency by maintaining ZVS over a wider range of operation compared to Si MOSFET. The PSFB operates at 100 kHz and achieves a peak efficiency of 97.74%.

PMP23069 3.6-kW single-phase totem-pole bridgeless PFC reference design with a > 180-W/in³ power density
This reference design is a GaN-based 3.6-kW single-phase continuous conduction mode (CCM) totem-pole power factor correction (PFC) converter targeting maximum power density. The power stage is followed by a

small boost converter, which helps to reduce the size of the bulk capacitor. The LMG3522 top-side cooled GaN with integrated driver and protection enables higher efficiency and reduces power supply size and complexity. The F28004x or F28002x C2000™ controller is used for all the advanced controls that includes fast relay control; baby boost operation during AC dropout event; reverse-current-flow protection; and communication between the PFC and the housekeeping controller. The PFC operates at a switching frequency of 65 kHz and achieves peak efficiency of 98.7%.

PMP41017 3kW two-phase interleaved half-bridge LLC reference design with GaN and C2000™ MCU
This reference design is a 3-kW, two-phase, interleaved half-bridge inductor-inductor-capacitor (LLC) using the LMG3422 and C2000™ devices.

Digitally Controlled High Efficiency and High Power Density PFC Circuits - Part 2 (Video)
This presentation will introduce two bridgeless PFC designs using C2000 MCU. TI high voltage GaN is used to implement a 3.3kW interleaved CCM totem-pole PFC and a 1.6kW interleaved TRM totem-pole PFC designs. Detailed design considerations are provided to minimize switching loss, current crossover distortion, input current THD and improve efficiency and PF.

TIDA-010062 1-kW, 80 Plus titanium, GaN CCM totem pole bridgeless PFC and half-bridge LLC reference design
This reference design is a digitally controlled, compact 1-kW AC/DC power supply design for server power supply unit (PSU) and telecom rectifier applications. The highly efficient design supports two main power stages, including a front-end continuous conduction mode (CCM) totem-pole bridgeless power factor correction (PFC) stage. The PFC stage features an LMG341x GaN FET with integrated driver to provide enhanced efficiency across a wide load range and meet 80-plus titanium requirements. The design also supports a half-bridge LLC isolated DC/DC stage to achieve a +12-V DC output at 1-kW. Two control cards use C2000™ Entry-Performance MCUs to control both power stages.

TIDM-1007 Interleaved CCM Totem Pole PFC Reference Design (Video)
This video covers the hardware aspects, the control aspects, and the software design that are required to control a totem-pole PFC using a C2000 microcontroller. The test results achieved on this reference design are also presented as part of this presentation.

Variable-frequency, ZVS, 5-kW, GaN-based, two-phase totem-pole PFC reference design
This reference design is a high-density and high-efficiency 5-kW totem-pole power factor correction (PFC) design. The design uses a two-phase totem-pole PFC operating with variable frequency and zero voltage switching (ZVS). The control uses a new topology and improved triangular current mode (iTCM) to achieve both small size and high efficiency. The design uses a high performance processing core inside a TMS320F280049C microcontroller to maintain efficiency over a wide operating range. The PFC operates with variable frequency between 100 kHz and 800 kHz. A peak system efficiency of 99% was achieved with an open-frame power density of 120 W/in3.

8.2.1.3 Merchant Telecom Rectifiers

Merchant telecom rectifier consists of a power factor correction (PFC) stage and a DC-DC converter stage. The Totem pole PFC is widely used as the PFC stage. For the DC-DC stage, LLC and phase-shifted full bridge (PSFB) are the two most popular topologies. Single-chip and two-chip architecture can be used in merchant telecom rectifier, as shown in Figure 8-5 and Figure 8-6.

The PFC stage draws sine-wave current from the AC mains in phase with the AC voltage, and maintains a steady DC bus voltage (VDC, typically +400 V) across its output. This output voltage is applied to the input of DC-DC stage, which converts it to an isolated low-output voltage Vout (usually 48 V).

8.2.1.3.1 System Block Diagram

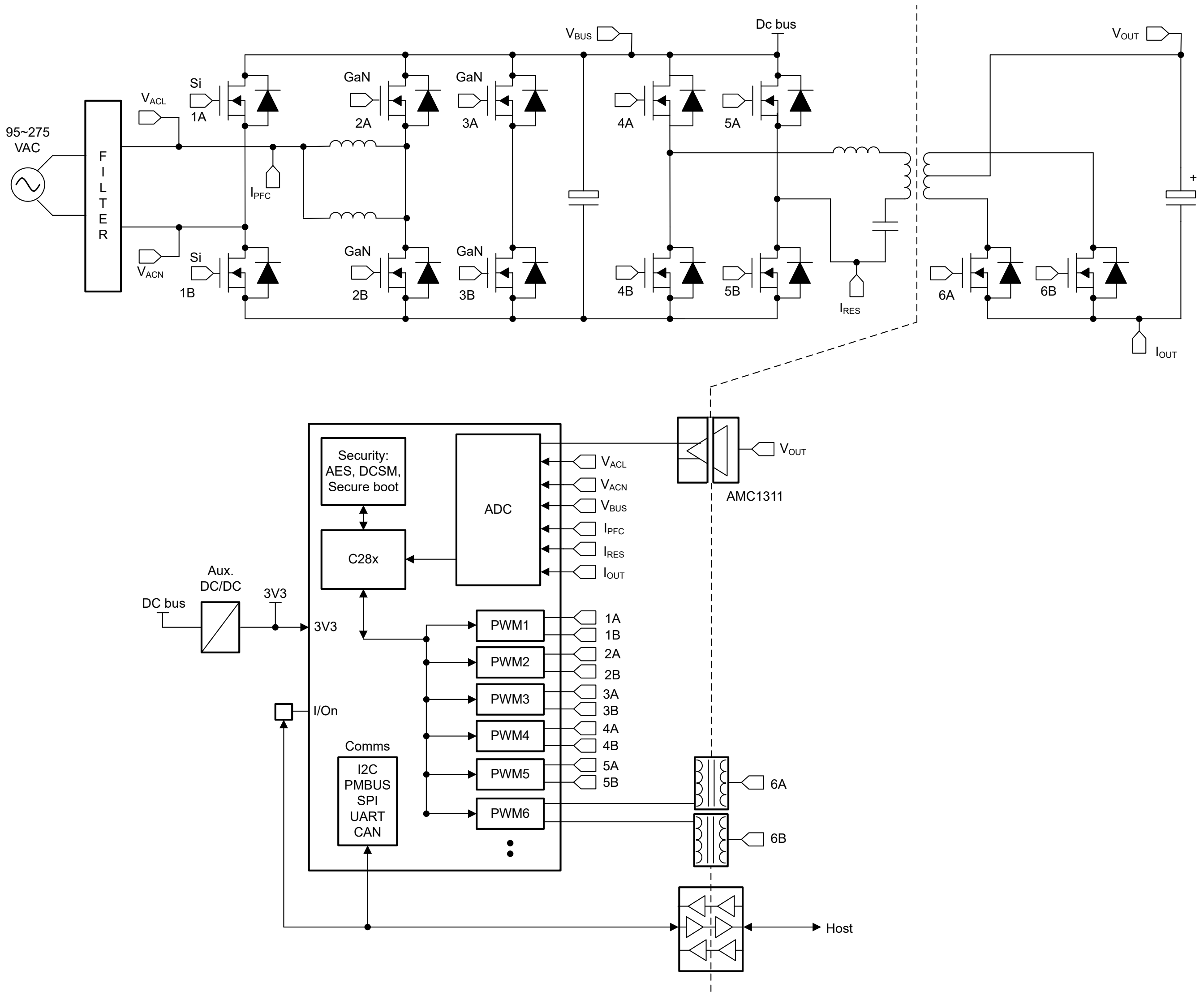


Figure 8-5. Merchant Telecom Rectifier Single-chip Architecture

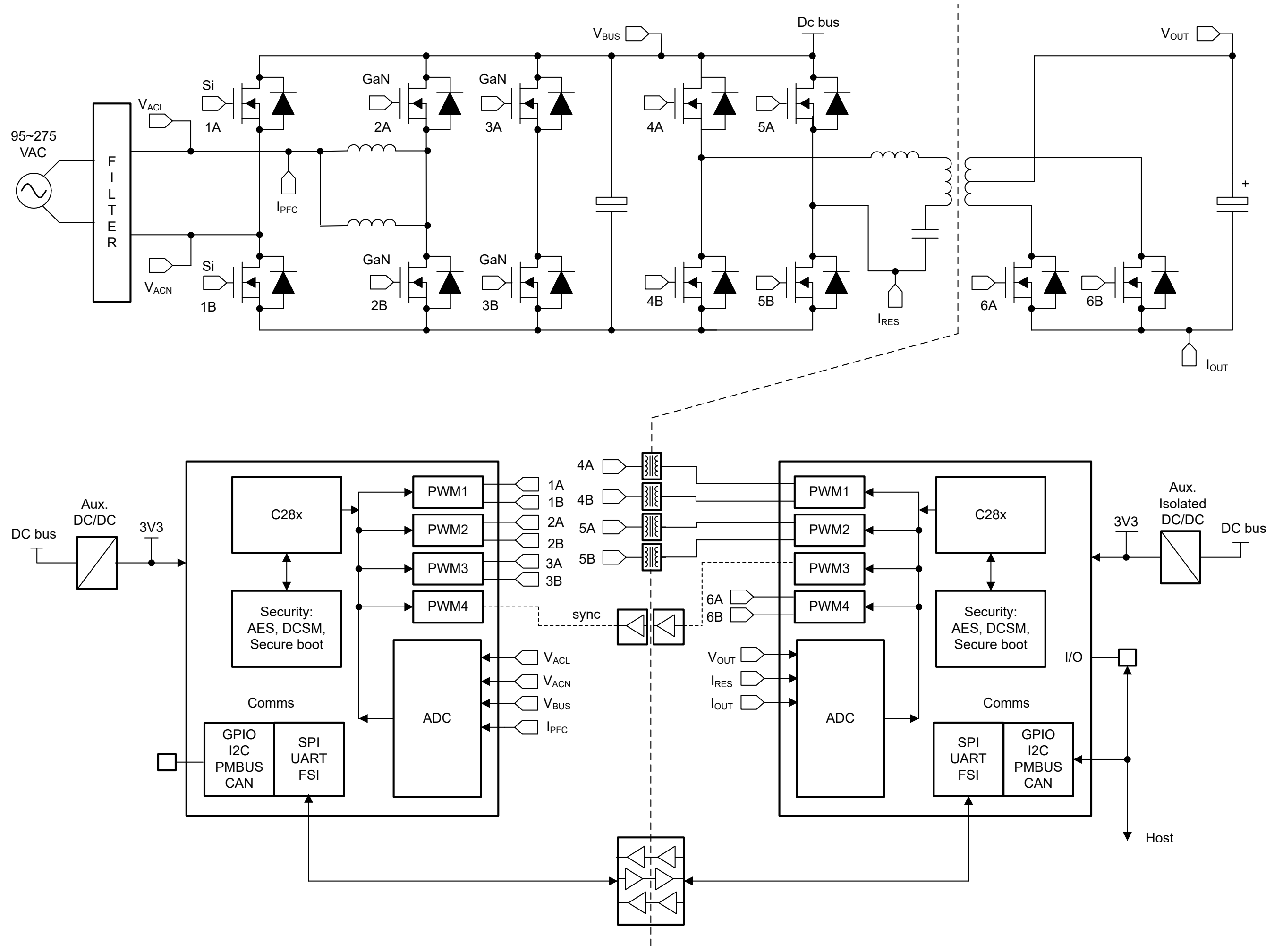


Figure 8-6. Merchant Telecom Rectifier Dual-chip Architecture

8.2.1.3.2 Merchant Telecom Rectifiers Resources

Reference Designs and Associated Training Videos

PMP41081 1-kW, 12-V HHC LLC reference design using C2000™ real-time microcontroller
This reference design is a 1-kW, 400-V to 12-V half-bridge resonant DC/DC platform used to evaluate the load transient performance of hybrid-hysteretic control (HHC) with a C2000™ microcontroller.

3-kW phase-shifted full bridge with active clamp reference design with > 270-W/in3 power density
This reference design is a GaN-based 3-kW phase-shifted full bridge (PSFB) targeting maximum power density. The design has an active clamp to minimize voltage stress on the secondary synchronous rectifier MOSFETs enabling use of lower voltage-rating MOSFETs with better figure-of-merit (FoM). PMP23126 uses our 30mΩ GaN on the primary side and silicon MOSFETs on the secondary side. The LMG3522 top-side cooled GaN with integrated driver and protection enables higher efficiency by maintaining ZVS over a wider range of operation compared to Si MOSFET. The PSFB operates at 100 kHz and achieves a peak efficiency of 97.74%.

PMP23069 3.6-kW single-phase totem-pole bridgeless PFC reference design with a > 180-W/in³ power density
This reference design is a GaN-based 3.6-kW single-phase continuous conduction mode (CCM) totem-pole power factor correction (PFC) converter targeting maximum power density. The power stage is followed by a small boost converter, which helps to reduce the size of the bulk capacitor. The LMG3522 top-side cooled GaN with integrated driver and protection enables higher efficiency and reduces power supply size and complexity. The F28004x or F28002x C2000™ controller is used for all the advanced controls that includes fast relay control;

baby boost operation during AC dropout event; reverse-current-flow protection; and communication between the PFC and the housekeeping controller. The PFC operates at a switching frequency of 65 kHz and achieves peak efficiency of 98.7%.

PMP41017 3kW two-phase interleaved half-bridge LLC reference design with GaN and C2000™ MCU
This reference design is a 3-kW, two-phase, interleaved half-bridge inductor-inductor-capacitor (LLC) using the LMG3422 and C2000™ devices.

Digitally Controlled High Efficiency and High Power Density PFC Circuits - Part 2 (Video)
This presentation will introduce two bridgeless PFC designs using C2000 MCU. TI high voltage GaN is used to implement a 3.3kW interleaved CCM totem-pole PFC and a 1.6kW interleaved TRM totem-pole PFC designs. Detailed design considerations are provided to minimize switching loss, current crossover distortion, input current THD and improve efficiency and PF.

TIDA-010062 1-kW, 80 Plus titanium, GaN CCM totem pole bridgeless PFC and half-bridge LLC reference design
This reference design is a digitally controlled, compact 1-kW AC/DC power supply design for server power supply unit (PSU) and telecom rectifier applications. The highly efficient design supports two main power stages, including a front-end continuous conduction mode (CCM) totem-pole bridgeless power factor correction (PFC) stage. The PFC stage features an LMG341x GaN FET with integrated driver to provide enhanced efficiency across a wide load range and meet 80-plus titanium requirements. The design also supports a half-bridge LLC isolated DC/DC stage to achieve a +12-V DC output at 1-kW. Two control cards use C2000™ Entry-Performance MCUs to control both power stages.

TIDM-1007 Interleaved CCM Totem Pole PFC Reference Design (Video)
This video covers the hardware aspects, the control aspects, and the software design that are required to control a totem-pole PFC using a C2000 microcontroller. The test results achieved on this reference design are also presented as part of this presentation.

Variable-frequency, ZVS, 5-kW, GaN-based, two-phase totem-pole PFC reference design
This reference design is a high-density and high-efficiency 5-kW totem-pole power factor correction (PFC) design. The design uses a two-phase totem-pole PFC operating with variable frequency and zero voltage switching (ZVS). The control uses a new topology and improved triangular current mode (iTCM) to achieve both small size and high efficiency. The design uses a high performance processing core inside a TMS320F280049C microcontroller to maintain efficiency over a wide operating range. The PFC operates with variable frequency between 100 kHz and 800 kHz. A peak system efficiency of 99% was achieved with an open-frame power density of 120 W/in3.

8.2.1.4 EV Charging Station Power Module

The power module in a DC charging station consists of AC/DC power stage and DC/DC power stage. Each converter associated with its power stage comprises of power switches and gate driver, current and voltage sensing, and a real-time micro-controller. On the input side it has three-phase AC mains which are connected to the AC/DC power stage. This block converts the incoming AC voltage into a fixed DC voltage of around 800 V. This voltage serves as input to the DC/DC power stage which processes power and interfaces directly with the battery on the electric vehicle. Each power stage has a separate real-time micro-controller which is responsible for the processing of analog signals and providing fast control action.

The AC/DC stage (also known as the PFC stage) is the first level of power conversion in an EV charging station. It converts the incoming AC power from the grid (380–415 VAC) into a stable DC link voltage of around 800 V. The PFC stage maintains sinusoidal input currents, with typically a THD < 5%, and provides controlled DC output voltage higher than the amplitude of the line-to-line input voltage. The DC/DC stage is the second level of power conversion in an EV charging station. It converts the incoming DC link voltage of 800 V (in case of three-phase systems) to a lower DC voltage to charge the battery of an electric vehicle. The DC/DC converter must be capable of delivering rated power to the battery over a wide range with the capability of charging the battery at constant current or at constant voltage modes, depending on the State Of Charge (SOC) of the battery.

8.2.1.4.1 System Block Diagram

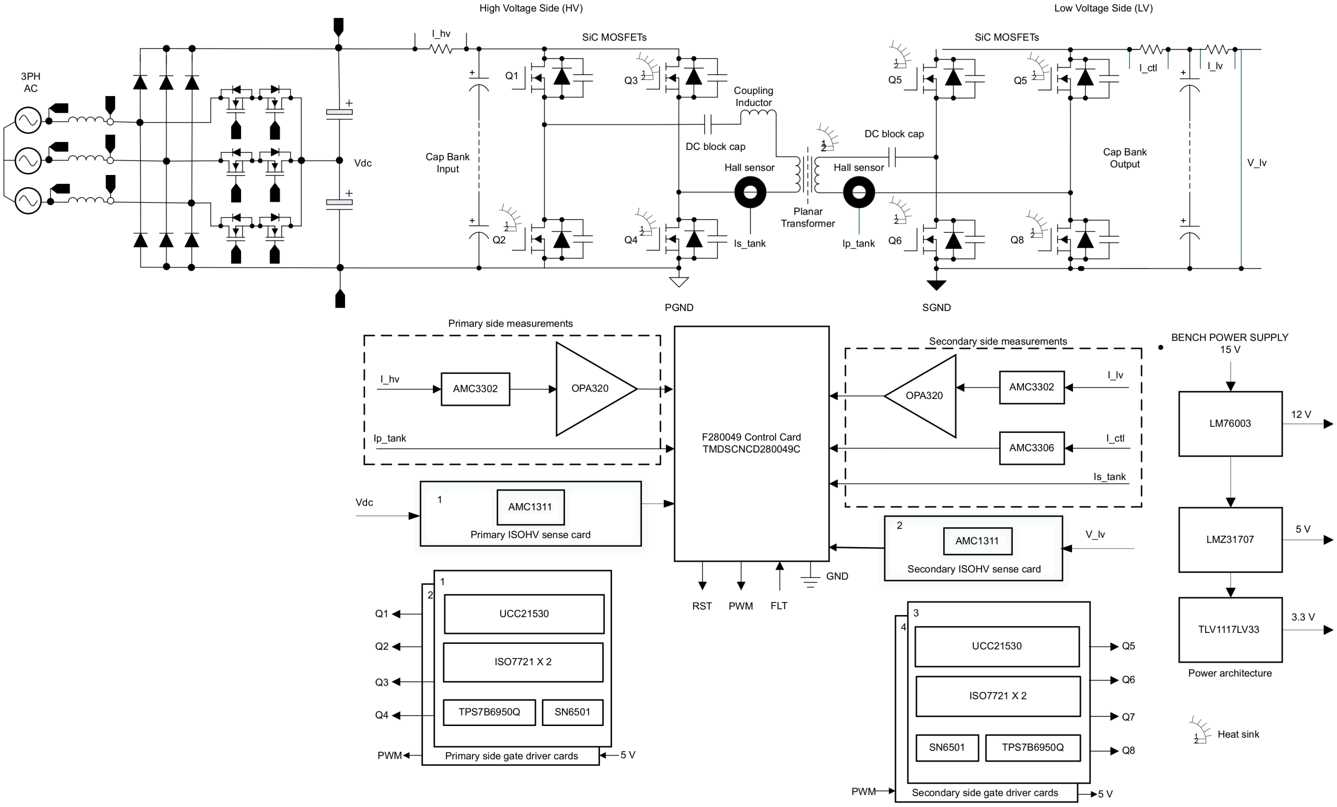


Figure 8-7. Dual-active-bridge DC/DC converter

8.2.1.4.2 EV Charging Station Power Module Resources

Reference Designs and Associated Training Videos

TIDA-01606 10-kW, bidirectional three-phase three-level (T-type) inverter and PFC reference design

This reference design provides an overview on how to implement a bidirectional three-level, three-phase, SiC-based active front end (AFE) inverter and PFC stage. The design uses a switching frequency of 50 kHz and a LCL output filter to reduce the size of the magnetics. A peak efficiency of 99% is achieved. The design shows how to implement a complete three phase AFE control in the DQ domain. The control and software is validated on the actual hardware and on hardware in the loop (HIL) setup.

TIDA-010210 11-kW, bidirectional, three-phase ANPC based on GaN reference design

This reference design provides a design template for implementing a three-level, three-phase, gallium nitride (GaN) based ANPC inverter power stage. The use of fast switching power devices makes it possible to switch at a higher frequency of 100 kHz, reducing the size of magnetics for the filter and increasing the power density of the power stage. The multilevel topology allows the use of 600-V rated power devices at higher DC bus voltages of up to 1000 V. The lower switching voltage stress reduces switching losses, resulting in a peak efficiency of 98.5%

TIDA-010054 Bi-directional, dual active bridge reference design for level 3 electric vehicle charging stations

This reference design provides an overview on the implementation of a single-phase Dual Active Bridge (DAB) DC/DC converter. DAB topology offers advantages like soft-switching commutations, a decreased number of devices and high efficiency. The design is beneficial where power density, cost, weight, galvanic isolation, high-voltage conversion ratio, and reliability are critical factors, making it ideal for EV charging stations and energy storage applications. Modularity and symmetrical structure in the DAB allow for stacking converters to achieve high power throughput and facilitate a bidirectional mode of operation to support battery charging and discharging applications.

C2000™ MCUs - Electric vehicle (EV) training videos (Video)
This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

Maximizing power for Level 3 EV charging stations
This explains how C2000's rich portfolio provide optimal solutions that help engineers solve design challenges and implement advanced power topologies.

Power Topology Considerations for Electric Vehicle Charging Stations Application Report
This Application Report discusses the topology consideration for designing power modules that acts as a building block for design of these fast DC Charging Station.

TIDM-02000 Peak current-mode controlled phase-shifted full-bridge reference design using C2000™ real-time MCU
This design implements a digitally peak current mode-controlled (PCMC) phase-shifted full bridge (PSFB) DC-DC converter that converts a 400-V DC input to a regulated 12-V DC output. Novel PCMC waveform generation based on the type-4 PWM and internal slope compensation; and simple PCMC implementation are the highlights of this design. A TMS320F280049C MCU from the C2000 real-time microcontroller family is used.

TIDUEG2C TIDM-02002 Bidirectional CLLLC resonant dual active bridge (DAB) reference design for HEV/EV onboard charger
The CLLLC resonant DAB with bidirectional power flow capability and soft switching characteristics is an ideal candidate for Hybrid Electric Vehicle/Electric Vehicle (HEV/EV) on-board chargers and energy storage applications. This design illustrates control of this power topology using a C2000™ MCU in closed voltage and closed current-loop mode. The hardware and software available with this design help accelerate your time to market.

8.2.1.5 Air-conditioner Outdoor Unit

Air-conditioner outdoor unit design considerations include maximizing power efficiency; minimizing acoustics; and cost. Variable-speed air-conditioners enable continuous temperature regulation and are more efficient than fixed-speed air-conditioners. The air-conditioner’s outdoor unit (ODU) consists of a power factor correction (PFC) stage, compressor motor drive, and fan motor drive. A sensorless Field-Oriented Control (FOC)-based Permanent Magnet Synchronous Motor (PMSM) drive is used in the ODU compressor and fan motors to control motor speed and torque by varying the input frequency and voltage of the motors. PFC ensures that the current waveform follows the voltage waveform, improving the line-side power factor, and regulates the output DC voltage to a constant value, regardless of any changes in load or input conditions.

8.2.1.5.1 System Block Diagram

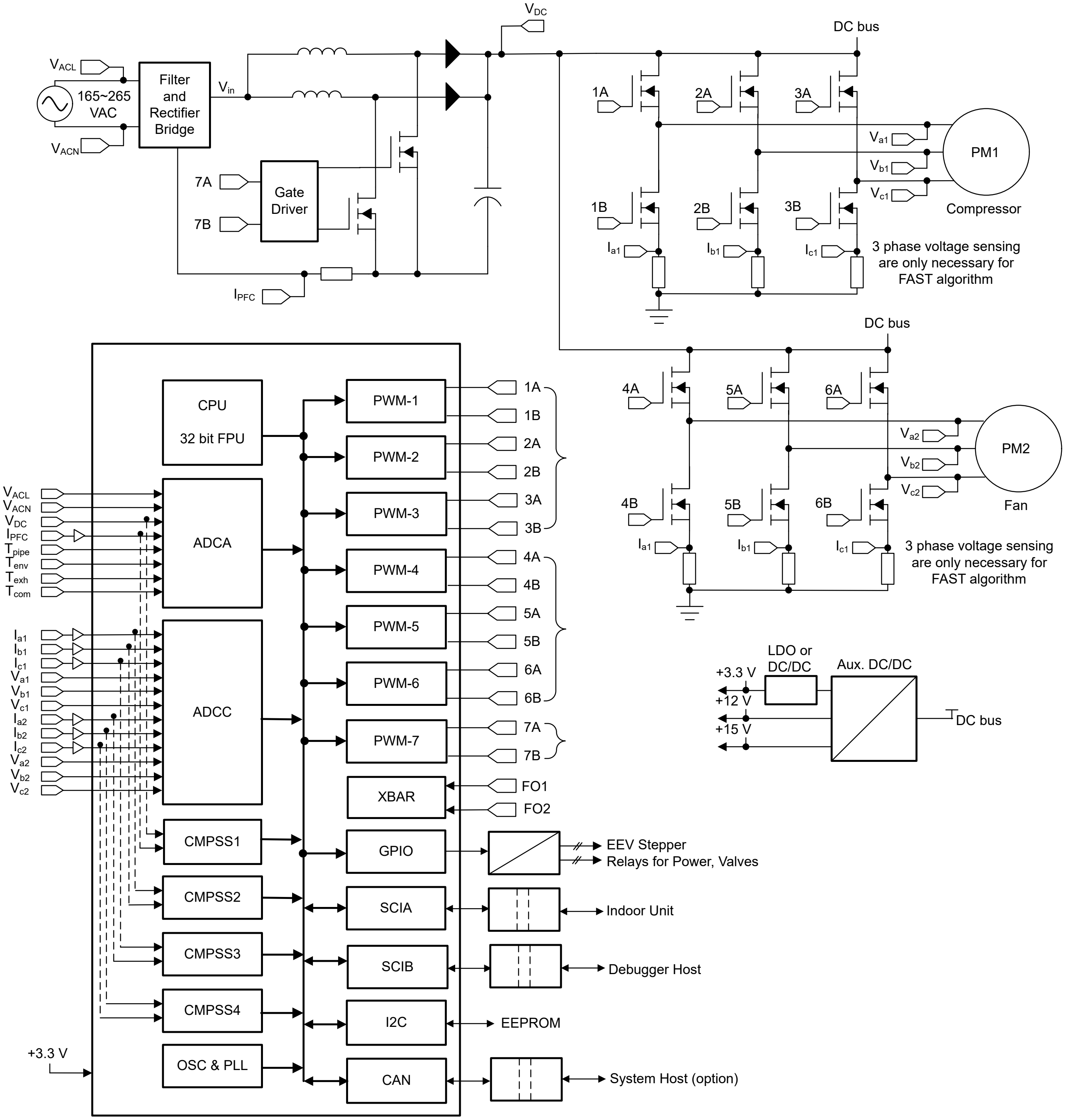


Figure 8-8. Typical Variable-Frequency Air-Conditioner with Dual-Motor Control Using Three-Shunt Plus Interleave PFC

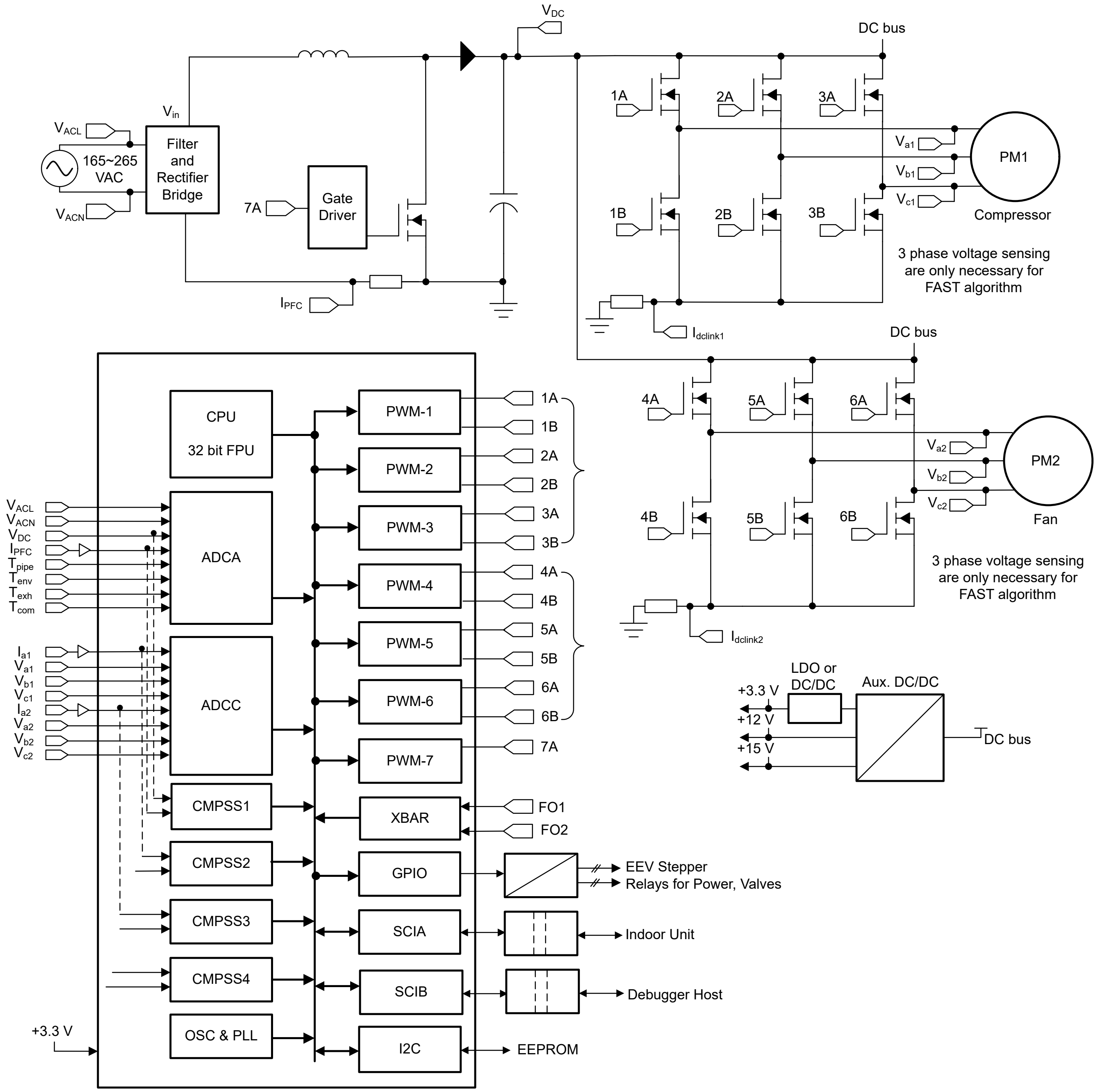


Figure 8-9. Typical Variable-Frequency Air-Conditioner with Dual-Motor Control Using Single Shunt Plus Single-Phase PFC

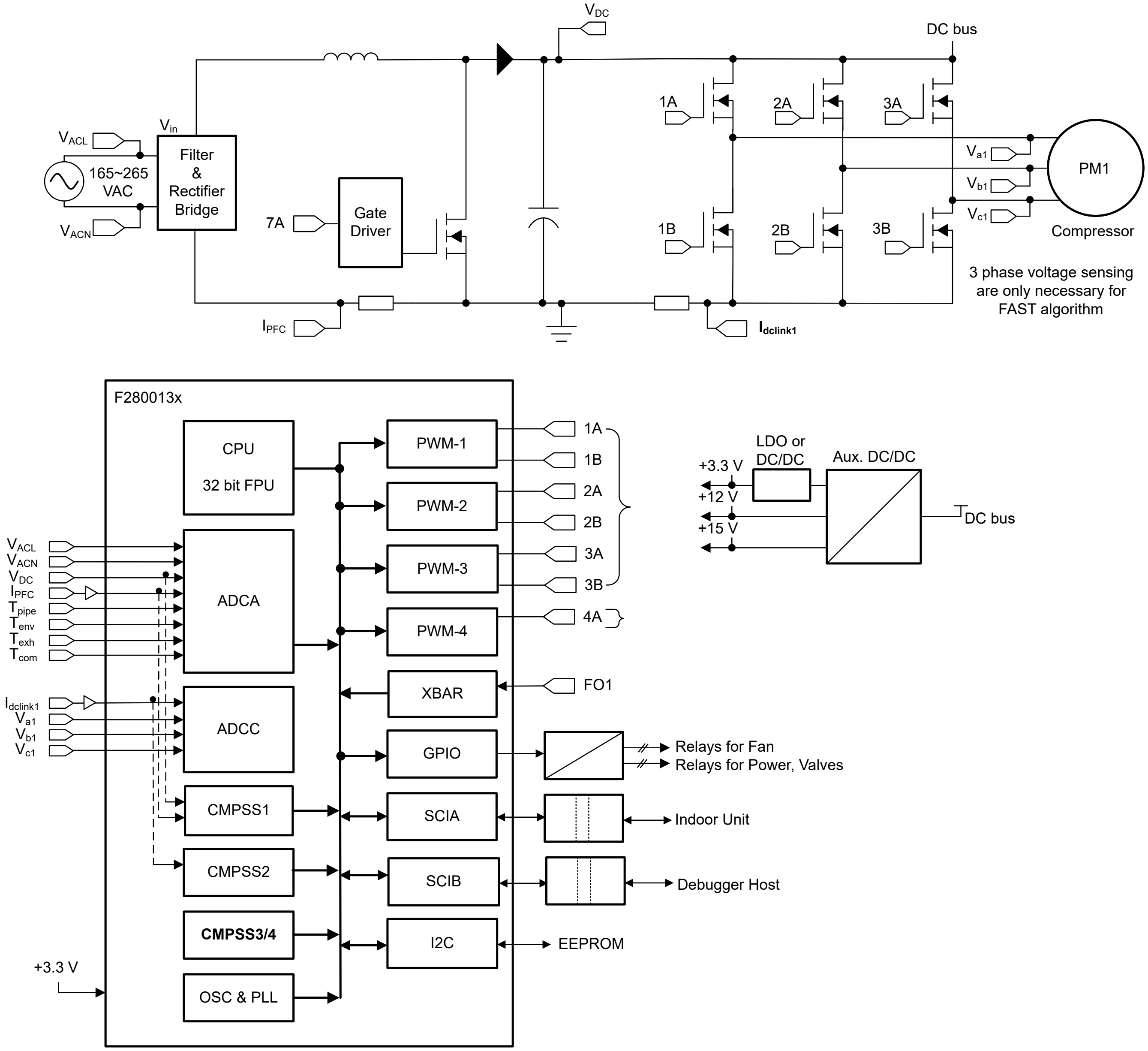


Figure 8-10. Typical Variable-Frequency Air-Conditioner with Single-Motor Control Using Single Shunt Plus Single-Phase PFC

8.2.1.5.2 Air Conditioner Outdoor Unit Resources

Reference Designs and Associated Training Videos

TIDM-02010: Dual motor control with digital interleaved PFC for HVAC reference design

The TIDM-02010 reference design is a 1.5-kW dual-motor drive and power factor correction (PFC) control reference design for a variable-frequency air-conditioner outdoor unit controller in HVAC applications. This reference design illustrates a method to implement sensorless 3-phase PMSM vector control for compressor and fan motor drive, and digital interleaved boost PFC for meeting new efficiency standards with a single C2000™ microcontroller. The hardware and software available with this reference design are tested and ready to use to help accelerate development time to market. The reference design includes hardware design files and software codes.

Variable speed air conditioner (HVAC) reference design demo (Video)
This video introduces dual-motor control with interleaved PFC for HVAC application design using a single C2000 MCU. The test results achieved on this reference design are also presented as part of this presentation.

9 Device and Documentation Support

9.1 Getting Started and Next Steps

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

For a quick overview of the TMS320F28002x device, features, roadmap, comparisons to other devices, and package details, see *C2000™ real-time microcontrollers: F28002x series*.

9.2 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320 MCU devices and support tools. Each TMS320™ MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS**320F280025C). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (with TMX for devices and TMDX for tools) through fully qualified production devices and tools (with TMS for devices and TMDS for tools).

Device development evolutionary flow:

TMX	Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
TMP	Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
TMS	Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX	Development-support product that has not yet completed Texas Instruments internal qualification testing.
TMDS	Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

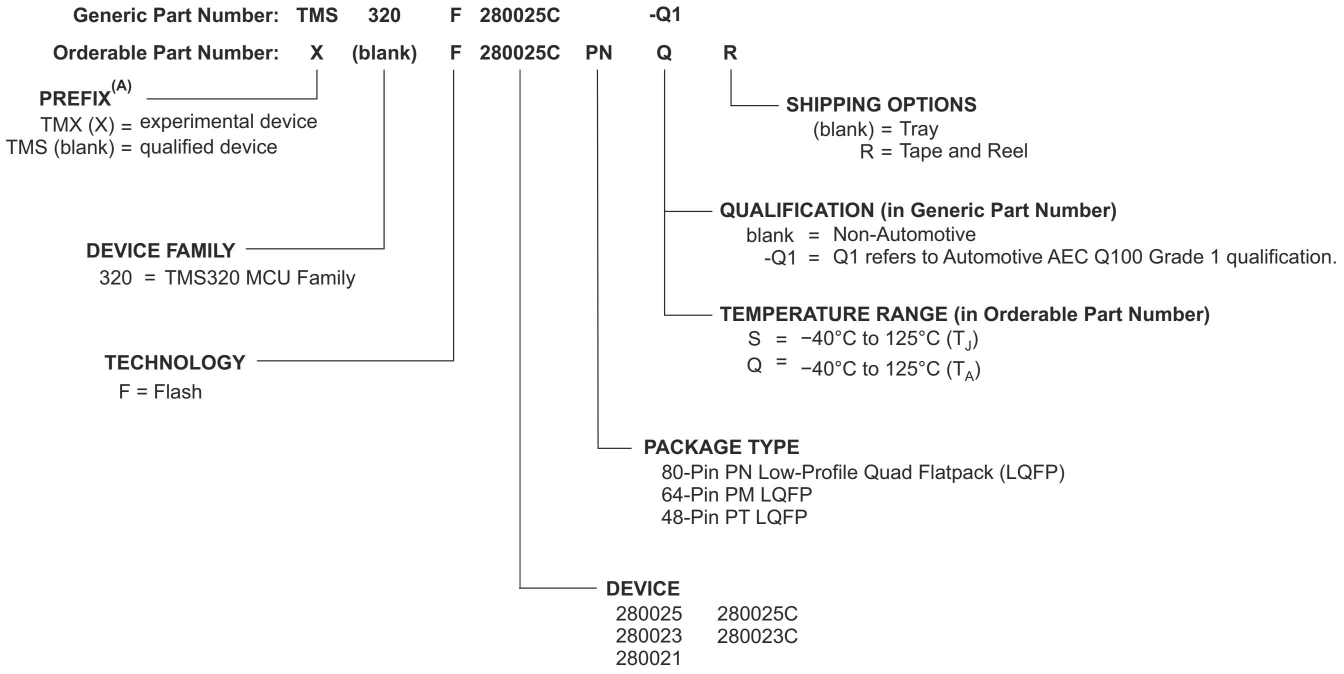
Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PN) and temperature range (for example, S).

For device part numbers and further ordering information, see the TI website (www.ti.com) or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *TMS320F28002x Real-Time MCUs Silicon Errata*.

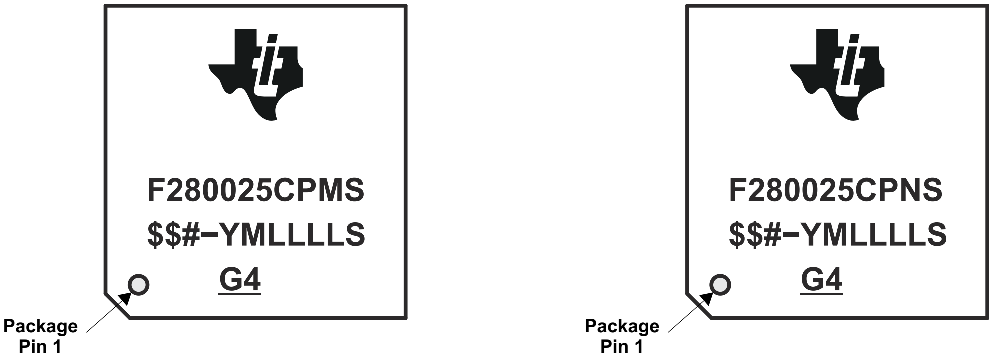


A. Prefix X is used in orderable part numbers.

Figure 9-1. Device Nomenclature

9.3 Markings

Figure 9-2 and Figure 9-3 show the package symbolization. Table 9-1 lists the silicon revision codes.

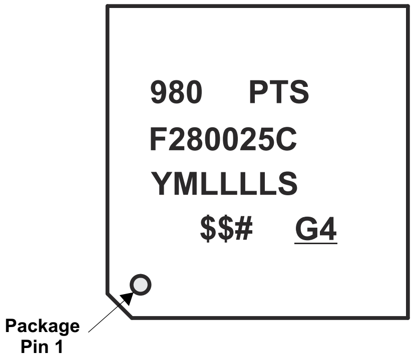


YMLLLLS = Lot Trace Code

YM = 2-Digit Year/Month Code
LLLL = Assembly Lot
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
= Silicon Revision Code

G4 = Green (Low Halogen and RoHS-compliant)

Figure 9-2. Package Symbolization for PM and PN Packages



YMLLLLS = Lot Trace Code

YM = 2-Digit Year/Month Code
LLLL = Assembly Lot
S = Assembly Site Code
980 = TI E.I.A. Code
$$ = Wafer Fab Code (one or two characters) as applicable
 # = Silicon Revision Code

G4 = Green (Low Halogen and RoHS-compliant)

Figure 9-3. Package Symbolization for PT Package

Table 9-1. Revision Identification

SILICON REVISION CODE	SILICON REVISION	REVID(1) ADDRESS: 0x5D00C	COMMENTS
Blank	0	0x0000 0000	This silicon revision is available as TMX.
A	A	0x0000 0001	This silicon revision is available as TMX and TMS.

(1) Silicon Revision ID

9.4 Tools and Software

TI offers an extensive line of development tools. Some of the tools and software to evaluate the performance of the device, generate code, and develop solutions follow. To view all available tools and software for C2000™ real-time control MCUs, visit the C2000 real-time control MCUs – Design & development page.

Development Tools

LAUNCHXL-F280025C
LAUNCHXL-F280025C is a low-cost development board for TI C2000™ Real-Time Controllers series of F28002x devices. Ideal for initial evaluation and prototyping, it provides a standardized and easy-to-use platform to develop your next application. This extended version LaunchPad™ development kit offers extra pins for evaluation and supports the connection of two BoosterPack™ plug-in modules.

F280025 controlCARD
The F280025 controlCARD is an HSEC180 controlCARD based evaluation and development tool for the C2000™ F28002x series of microcontroller products. controlCARDs are ideal to use for initial evaluation and system prototyping. controlCARDs are complete board-level modules that utilize one of two standard form factors (100-pin DIMM or 180-pin HSEC) to provide a low-profile single-board controller solution. For first evaluation controlCARDs are typically purchased bundled with a baseboard or bundled in an application kit.

TI Resource Explorer
To enhance your experience, be sure to check out the TI Resource Explorer to browse examples, libraries, and documentation for your applications.

Software Tools

C2000Ware for C2000 MCUs
C2000Ware for C2000™ MCUs is a cohesive set of software and documentation created to minimize development time. It includes device-specific drivers, libraries, and peripheral examples.

Digital Power SDK
Digital Power SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based digital power system development time targeted for various AC-DC, DC-DC and DC-AC power supply applications. The software includes firmware that runs on C2000 digital power evaluation modules (EVMs) and TI designs (TIDs), which are targeted for solar, telecom, server, electric vehicle chargers and industrial power delivery applications. Digital Power SDK provides all the needed resources at every stage of development and evaluation in a digital power applications.

Motor Control SDK
Motor Control SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based motor control system development time targeted for various three-phase motor control applications. The software includes firmware that runs on C2000 motor control evaluation modules (EVMs) and TI designs (TIDs), which are targeted for industrial drive and other motor control, Motor Control SDK provides all the needed resources at every stage of development and evaluation for high-performance motor control applications.

Code Composer Studio™ (CCS) Integrated Development Environment (IDE) for C2000 microcontrollers
Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking the user through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

SysConfig System configuration tool
SysConfig is a comprehensive collection of graphical utilities for configuring pins, peripherals, radios, subsystems, and other components. SysConfig helps you manage, expose and resolve conflicts visually so that you have more time to create differentiated applications. The tool's output includes C header and code files that can be used with software development kit (SDK) examples or used to configure custom software. The SysConfig tool automatically selects the pinmux settings that satisfy the entered requirements. The SysConfig tool is delivered integrated in CCS, as a standalone installer, or can be used via the dev.ti.com cloud tools portal. For more information about the SysConfig system configuration tool, visit the System configuation tool page.

C2000 Third-party search tool TI has partnered with multiple companies to offer a wide range of solutions and services for TI C2000 devices. These companies can accelerate your path to production using C2000 devices. Download this search tool to quickly browse third-party details and find the right third-party to meet your needs.

Models

Various models are available for download from the product Design & development pages. These models include I/O Buffer Information Specification (IBIS) Models and Boundary-Scan Description Language (BSDL) Models. To view all available models, visit the Design tools & simulation section of the Design & development page for each device.

Training

To help assist design engineers in taking full advantage of the C2000 microcontroller features and performance, TI has developed a variety of training resources. Utilizing the online training materials and downloadable hands-on workshops provides an easy means for gaining a complete working knowledge of the C2000 microcontroller family. These training resources have been designed to decrease the learning curve, while reducing development time, and accelerating product time to market. For more information on the various training resources, visit the C2000™ real-time control MCUs – Support & training site.

The architecture and many of the peripherals of the F28002x are similar to those of the F28004x. The following Workshop material and the *Migration Between TMS320F28004x and TMS320F28002x Application Report* will cover the technical details of the TMS320F28004x architecture and highlight the device differences, which will be helpful to users of the F28002x device.

Specific TMS320F28004x hands-on training resources can be found at C2000™ MCU Device Workshops.

Technical Introduction to the New C2000 TMS320F28004x Device Family

Many of the peripherals and architecture of the F28002x are similar to the F28004x. This presentation will cover the technical details of the TMS320F28004x architecture and highlight the new improvements to various key peripherals which will be helpful to users of the F28002x device.

9.5 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral follows.

Errata

TMS320F28002x Real-Time MCUs Silicon Errata describes known advisories on silicon and provides workarounds.

Technical Reference Manual

TMS320F28002x Real-Time Microcontrollers Technical Reference Manual details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the F28002x real-time microcontrollers.

CPU User's Guides

TMS320C28x CPU and Instruction Set Reference Guide describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

TMS320C28x Extended Instruction Sets Technical Reference Manual describes the architecture, pipeline, and instruction set of the TMU, VCU-II, and FPU accelerators.

Peripheral Guides

C2000 Real-Time Control Peripherals Reference Guide describes the peripheral reference guides of the 28x DSPs.

Tools Guides

TMS320C28x Assembly Language Tools v22.6.0.LTS User's Guide describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

TMS320C28x Optimizing C/C++ Compiler v22.6.0.LTS User's Guide describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

Application Reports

The SMT & packaging application notes website lists documentation on TI’s surface mount technology (SMT) and application notes on a variety of packaging-related topics.

Semiconductor Packing Methodology describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

Calculating Useful Lifetimes of Embedded Processors provides a methodology for calculating the useful lifetime of TI embedded processors (EPs) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement.

An Introduction to IBIS (I/O Buffer Information Specification) Modeling discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures, and future trends.

Serial Flash Programming of C2000™ Microcontrollers discusses using a flash kernel and ROM loaders for serial programming a device.

Fast Integer Division – A Differentiated Offering From C2000™ Product Family provides an overview of the different division and modulo (remainder) functions and its associated properties.

C2000™ Key Technology Guide provides a deeper look into the components that differentiate the C2000 Microcontroller Unit (MCU) as it pertains to Real-Time Control Systems.

Migration Between TMS320F28004x and TMS320F28002x describes the hardware and software differences to be aware of when moving between F28004x and F28002x C2000™ MCUs.

TMS320F2802x/TMS320F2803x to TMS320F28002x Migration Overview describes the differences between the Texas Instruments TMS320F2802x/TMS320F2803x and the TMS320F28002x microcontrollers for the purpose of assisting with application migration.

9.6 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.7 Trademarks

C2000™, TMS320C2000™, InstaSPIN-FOC™, Code Composer Studio™, TMS320™, LaunchPad™, BoosterPack™, and TI E2E™ are trademarks of Texas Instruments.
Bosch® is a registered trademark of Robert Bosch GmbH Corporation.
All trademarks are the property of their respective owners.

9.8 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.9 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from December 18, 2020 to April 4, 2024 (from Revision B (December 2020) to Revision C (April 2024)) Page

- *Features* section: Changed "**On-chip** crystal oscillator or external clock input" to "Crystal oscillator or external clock input". Changed the number of individually programmable multiplexed General-Purpose Input/Output (GPIO) pins from 39 to 43.......... 1
- *Features* section: Added Functional Safety bullet.......... 1
- *Applications* section: Updated "Hybrids, electric & powertrain systems" applications.......... 2
- *Description* section: Added reference to *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide*.......... 2
- *Package Information* table: Added table.......... 2
- *Functional Block Diagram* figure: Removed connection between BGCRC and Flash Bank0. Changed "39x GPIO" to "43x GPIO".......... 5
- *Device Comparison* table: Updated pin counts of GPIO pins. Added Note to "Additional GPIO". Updated "eCAP/HRCAP modules – Type 1". Updated "ePWM/HRPWM channels – Type 4". 7
- *Device Comparison* table: Updated high resolution module numbers for eCAP and ePWM.......... 7
- *Pin Attributes* table: Updated descriptions of VDD, VDDA, and VDDIO.......... 9
- *Power and Ground* table: Updated descriptions of VDD, VDDA, and VDDIO.......... 27
- *Specifications* section: Removed paragraph.......... 48
- *Absolute Maximum Ratings* table: Updated "Input clamp current". Updated "Continuous clamp current per pin is ±2 mA …" footnote. Added "Applying a V_{IN} greater than VDDIO/VDDA or less than VSS/VSSA ..." footnote. Added "Input clamp current must also be observed" footnote.......... 48
- *Absolute Maximum Ratings* table: Added "Stresses beyond those listed under *Absolute Maximum Ratings* …" footnote and "All voltage values are with respect to VSS, unless otherwise noted" footnote.......... 48
- *Recommended Operating Conditions* table: Removed MIN and MAX SR_{SUPPLY} values. Removed SR_{SUPPLY} unit. Updated its associated footnote.......... 48
- *Recommended Operating Conditions* table: Removed $t_{VDDIO-RAMP}$ row.......... 48
- *Recommended Operating Conditions* table: Updated T_J and T_A.......... 48
- *Recommended Operating Conditions* table: Added "Applying a V_{IN} greater than VDDIO/VDDA or less than VSS/VSSA ..." footnote.......... 48
- *ESD Ratings – Commercial* table: Removed JEDEC specification JESD22-C101 from description of Charged-device model (CDM). Added corner pins.......... 48
- *Current Consumption Graphs* section: Added Note.......... 52
- *Power Management Module (PMM)* section: Updated section.......... 58
- *Delay Blocks* section: Removed reference to external VREG.......... 60
- *Internal 1.2-V LDO Voltage Regulator (VREG)* section: Removed "It is enabled by tying the VREGENZ pin low" sentence.......... 60
- *VDD Decoupling* section: Updated Configuration 1 and Configuration 2.......... 60
- *Reset Circuit* figure: Updated figure.......... 66
- *Crystal Oscillator* section: Removed section. Replaced by new *XTAL Oscillator* section.......... 70
- *Internal Clock Frequencies* table: Updated MIN $f_{(INTCLK)}$.......... 73
- *XTAL Oscillator* section: Added section.......... 75
- *INTOSC Characteristics* table: Updated table.......... 82
- *Flash Parameters* table: Updated MAX values of Erase Times.......... 83
- *Flash Parameters* table: Added "Each sector, by itself, can only be erased/programmed 20,000 times ..." footnote.......... 83
- *RAM Specifications* section: Added section.......... 85
- *ROM Specifications* section: Added section.......... 85
- *Connecting to the 14-Pin JTAG Header* figure: Updated figure.......... 86
- *Connecting to the 20-Pin JTAG Header* figure: Updated figure.......... 86

- *External Interrupt Timing Requirements* table: Added "For an explanation of the input qualifier parameters ..." footnote........ 94
- *External Interrupt Switching Characteristics* table: Added "For an explanation of the input qualifier parameters ..." footnote........ 94
- *Analog Pins and Internal Connections* table: Updated High Positive, High Negative, Low Positive, and Low Negative columns........ 103
- *ADC Electrical Data and Timing* section: Updated "The ADC inputs should be kept below VDDA + 0.3 V" Note........ 109
- *ADC Operating Conditions* table: Updated VREFHI - VREFLO TEST CONDITIONS........ 109
- *ADC Characteristics* table: Updated ENOB TEST CONDITIONS and values........ 109
- *ADC INL and DNL* figure: Added figure........ 111
- *ADC Input Model* section: Added references to the *Charge-Sharing Driving Circuits for C2000 ADCs Application Report* and the *ADC Input Circuit Evaluation for C2000 MCUs Application Report*........ 112
- *Comparator Subsystem (CMPSS)* section: Added Note about the muxing of CMPSS pins........ 116
- *Comparator Electrical Characteristics* table: Updated Hysteresis values........ 117
- *Synchronization Chain Architecture* figure: Updated figure........ 124
- *I2C Timing Requirements* table: Added footnotes........ 140
- *PMBus Fast Mode Switching Characteristics* table: Added f_{mod} (PMBus module frequency) and footnote........ 143
- *PMBus Standard Mode Switching Characteristics* table: Added f_{mod} (PMBus module frequency) and footnote........ 143
- *SPI Master Mode Switching Characteristics (Clock Phase = 1)* table: Added footnote........ 149
- *HIC Block Diagram*: Updated figure........ 164
- *Functional Block Diagram* figure: Removed connection between BGCRC and Flash Bank0. Changed "39x GPIO" to "43x GPIO"........ 169
- *Applications, Implementation, and Layout* section: Updated section........ 194
- *Merchant Telecom Rectifier Single-chip Architecture* figure: Corrected EPWM labels of lower FETs........ 204
- *Merchant Telecom Rectifier Dual-chip Architecture* figure: Corrected EPWM labels of lower FETs........ 204
- *Getting Started and Next Steps* section: Updated section........ 213
- *Tools and Software* section: Added "C2000 Third-party search tool" to **Software Tools** section........ 216

11 Mechanical, Packaging, and Orderable Information

11.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

To learn more about TI packaging, visit the Packaging information website.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
F280021PTQR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280021 PTQ	Samples
F280021PTSR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280021 PTS	Samples
F280021PTSRG4	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280021 PTS	Samples
F280023CPMSR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280023CPMS	Samples
F280023CPNSR	ACTIVE	LQFP	PN	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280023CPNS	Samples
F280023CPTSR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280023C PTS	Samples
F280023CPTSRG4	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280023C PTS	Samples
F280023PMQR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280023PMQ	Samples
F280023PMSR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280023PMS	Samples
F280023PNQR	ACTIVE	LQFP	PN	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280023PNQ	Samples
F280023PNSR	ACTIVE	LQFP	PN	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280023PNS	Samples
F280023PTQR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280023 PTQ	Samples
F280023PTSR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280023 PTS	Samples
F280023PTSRG4	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280023 PTS	Samples
F280025CPMQR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025CPMQ	Samples
F280025CPMS	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025CPMS	Samples
F280025CPMSR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025CPMS	Samples
F280025CPNQR	ACTIVE	LQFP	PN	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025CPNQ	Samples

PACKAGE OPTION ADDENDUM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
F280025CPNSR	ACTIVE	LQFP	PN	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025CPNS	Samples
F280025CPTQR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025C PTQ	Samples
F280025CPTSR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025C PTS	Samples
F280025CPTSRG4	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025C PTS	Samples
F280025PMQR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025PMQ	Samples
F280025PMS	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025PMS	Samples
F280025PMSR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025PMS	Samples
F280025PNQR	ACTIVE	LQFP	PN	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025PNQ	Samples
F280025PNS	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025PNS	Samples
F280025PNSR	ACTIVE	LQFP	PN	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025PNS	Samples
F280025PTQR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025 PTQ	Samples
F280025PTS	ACTIVE	LQFP	PT	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025 PTS	Samples
F280025PTSR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025 PTS	Samples
F280025PTSRG4	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F280025 PTS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMS320F280021, TMS320F280021-Q1, TMS320F280023, TMS320F280023-Q1, TMS320F280025, TMS320F280025-Q1, TMS320F280025C, TMS320F280025C-Q1 :

- Catalog : TMS320F280021, TMS320F280023, TMS320F280025, TMS320F280025C

- Automotive : TMS320F280021-Q1, TMS320F280023-Q1, TMS320F280025-Q1, TMS320F280025C-Q1

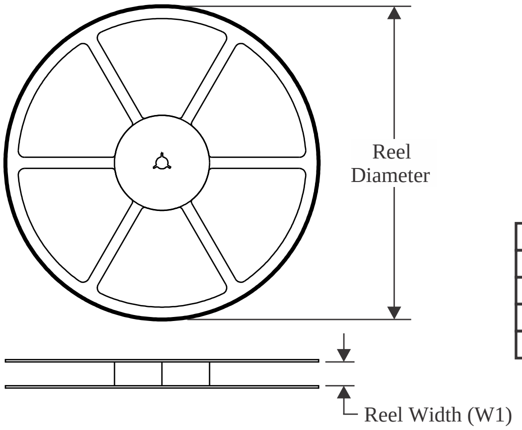
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

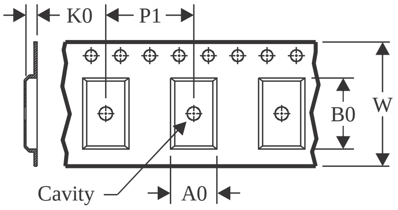
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

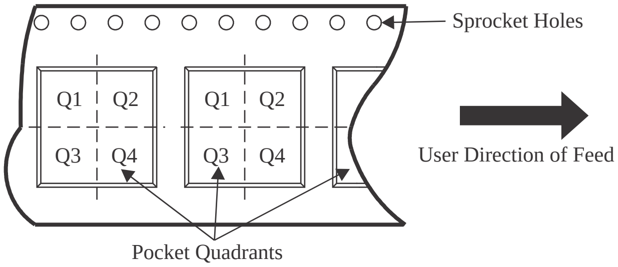


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

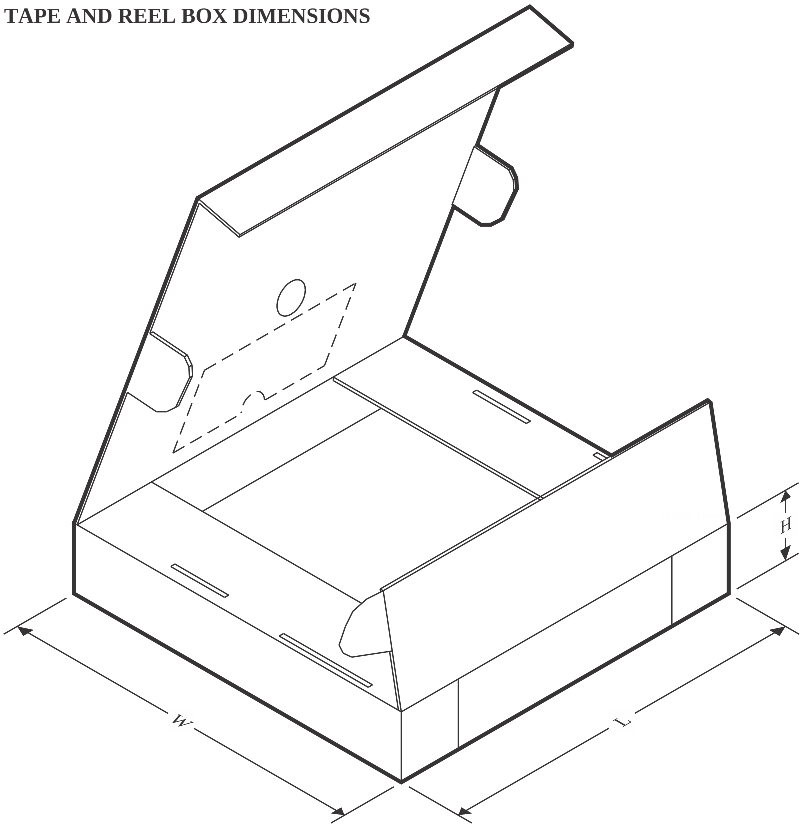


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
F280021PTQR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F280021PTSR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F280021PTSRG4	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F280023CPMSR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
F280023CPNSR	LQFP	PN	80	1000	330.0	24.4	16.0	16.0	2.0	24.0	24.0	Q2
F280023CPTSR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F280023CPTSRG4	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F280023PMQR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
F280023PMSR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
F280023PNQR	LQFP	PN	80	1000	330.0	24.4	16.0	16.0	2.0	24.0	24.0	Q2
F280023PNSR	LQFP	PN	80	1000	330.0	24.4	16.0	16.0	2.0	24.0	24.0	Q2
F280023PTQR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F280023PTSR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F280023PTSRG4	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F280025CPMQR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
F280025CPMSR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
F280025CPNQR	LQFP	PN	80	1000	330.0	24.4	16.0	16.0	2.0	24.0	24.0	Q2
F280025CPNSR	LQFP	PN	80	1000	330.0	24.4	16.0	16.0	2.0	24.0	24.0	Q2
F280025CPTQR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F280025CPTSR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F280025CPTSRG4	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F280025PMQR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
F280025PMSR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
F280025PNQR	LQFP	PN	80	1000	330.0	24.4	16.0	16.0	2.0	24.0	24.0	Q2
F280025PNSR	LQFP	PN	80	1000	330.0	24.4	16.0	16.0	2.0	24.0	24.0	Q2
F280025PTQR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F280025PTSR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F280025PTSRG4	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

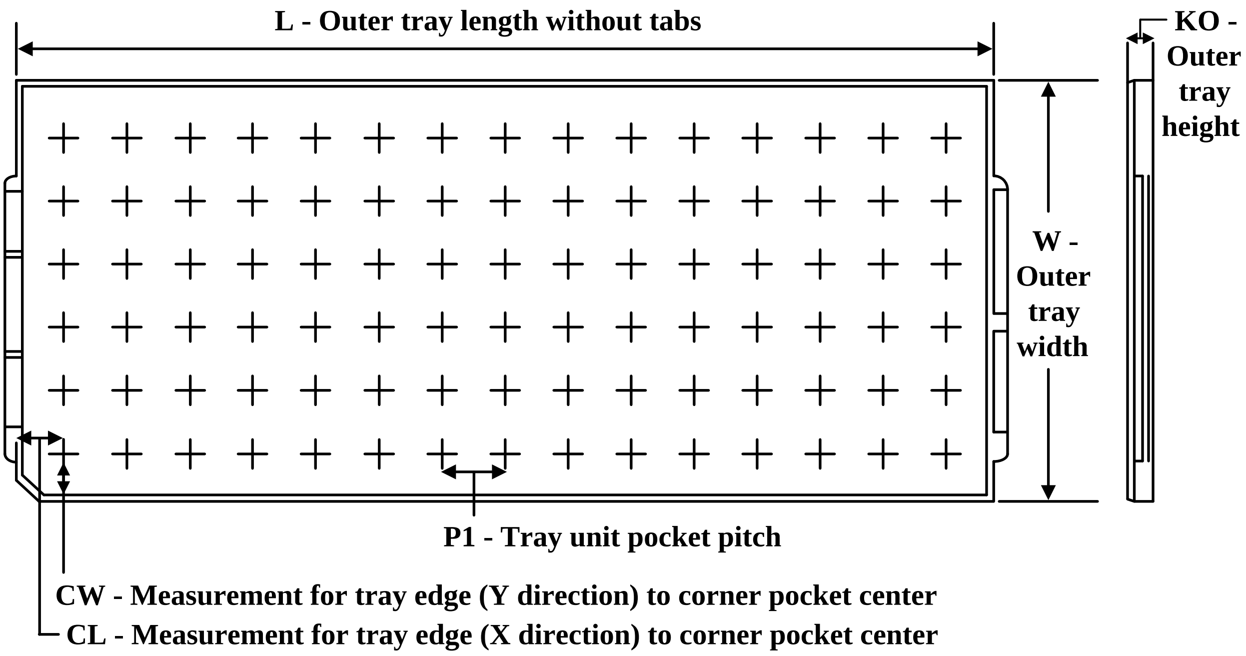


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
F280021PTQR	LQFP	PT	48	1000	336.6	336.6	31.8
F280021PTSR	LQFP	PT	48	1000	336.6	336.6	31.8
F280021PTSRG4	LQFP	PT	48	1000	336.6	336.6	31.8
F280023CPMSR	LQFP	PM	64	1000	336.6	336.6	41.3
F280023CPNSR	LQFP	PN	80	1000	367.0	367.0	55.0
F280023CPTSR	LQFP	PT	48	1000	336.6	336.6	31.8
F280023CPTSRG4	LQFP	PT	48	1000	336.6	336.6	31.8
F280023PMQR	LQFP	PM	64	1000	336.6	336.6	41.3
F280023PMSR	LQFP	PM	64	1000	336.6	336.6	41.3
F280023PNQR	LQFP	PN	80	1000	367.0	367.0	55.0
F280023PNSR	LQFP	PN	80	1000	367.0	367.0	55.0
F280023PTQR	LQFP	PT	48	1000	336.6	336.6	31.8
F280023PTSR	LQFP	PT	48	1000	336.6	336.6	31.8
F280023PTSRG4	LQFP	PT	48	1000	336.6	336.6	31.8
F280025CPMQR	LQFP	PM	64	1000	336.6	336.6	41.3
F280025CPMSR	LQFP	PM	64	1000	336.6	336.6	41.3
F280025CPNQR	LQFP	PN	80	1000	367.0	367.0	55.0
F280025CPNSR	LQFP	PN	80	1000	367.0	367.0	55.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
F280025CPTQR	LQFP	PT	48	1000	336.6	336.6	31.8
F280025CPTSR	LQFP	PT	48	1000	336.6	336.6	31.8
F280025CPTSRG4	LQFP	PT	48	1000	336.6	336.6	31.8
F280025PMQR	LQFP	PM	64	1000	336.6	336.6	41.3
F280025PMSR	LQFP	PM	64	1000	336.6	336.6	41.3
F280025PNQR	LQFP	PN	80	1000	367.0	367.0	55.0
F280025PNSR	LQFP	PN	80	1000	367.0	367.0	55.0
F280025PTQR	LQFP	PT	48	1000	336.6	336.6	31.8
F280025PTSR	LQFP	PT	48	1000	336.6	336.6	31.8
F280025PTSRG4	LQFP	PT	48	1000	336.6	336.6	31.8

TRAY

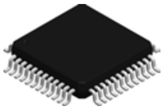


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
F280025CPMS	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
F280025PMS	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
F280025PNS	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95
F280025PTS	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

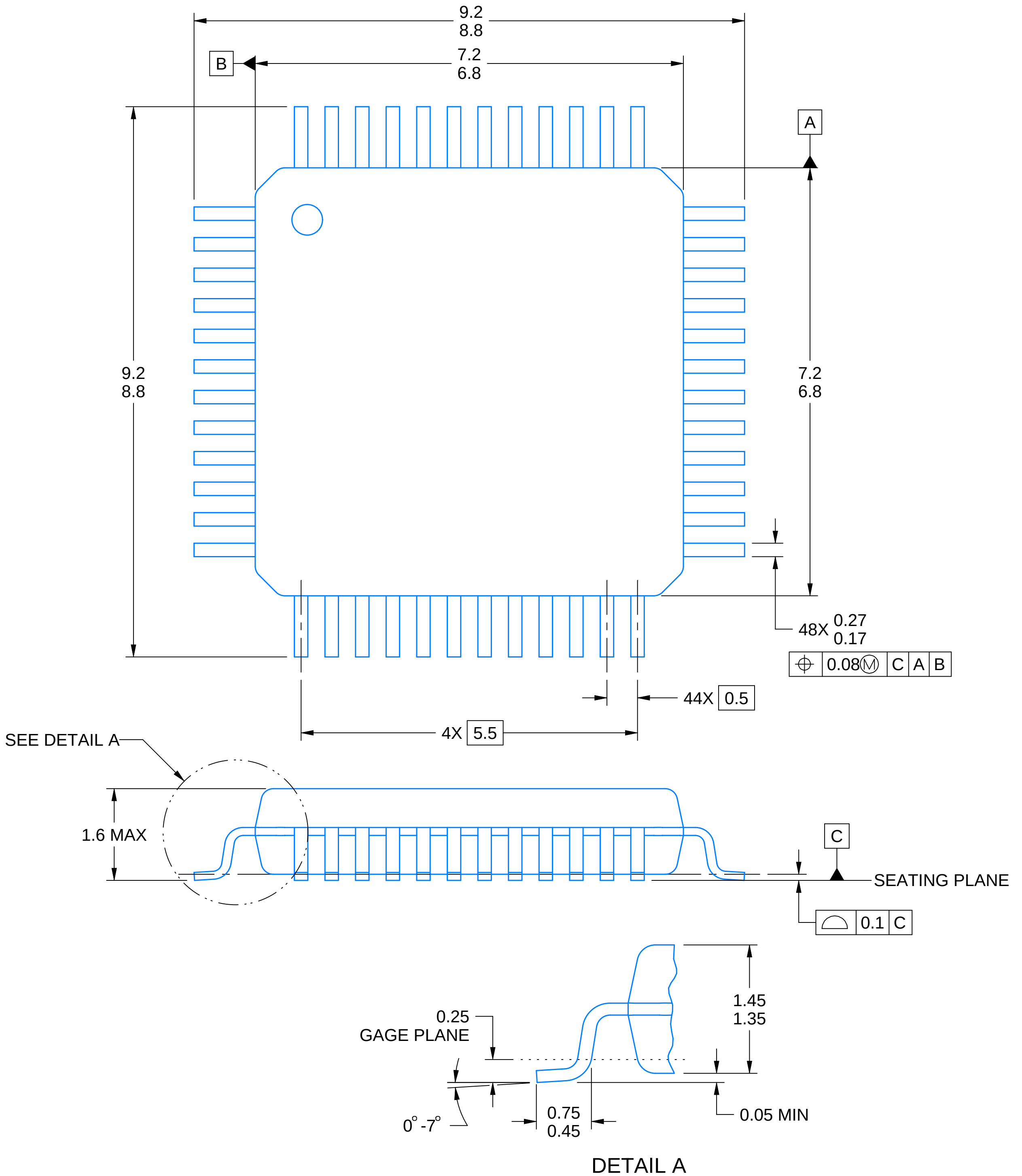
PT0048A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

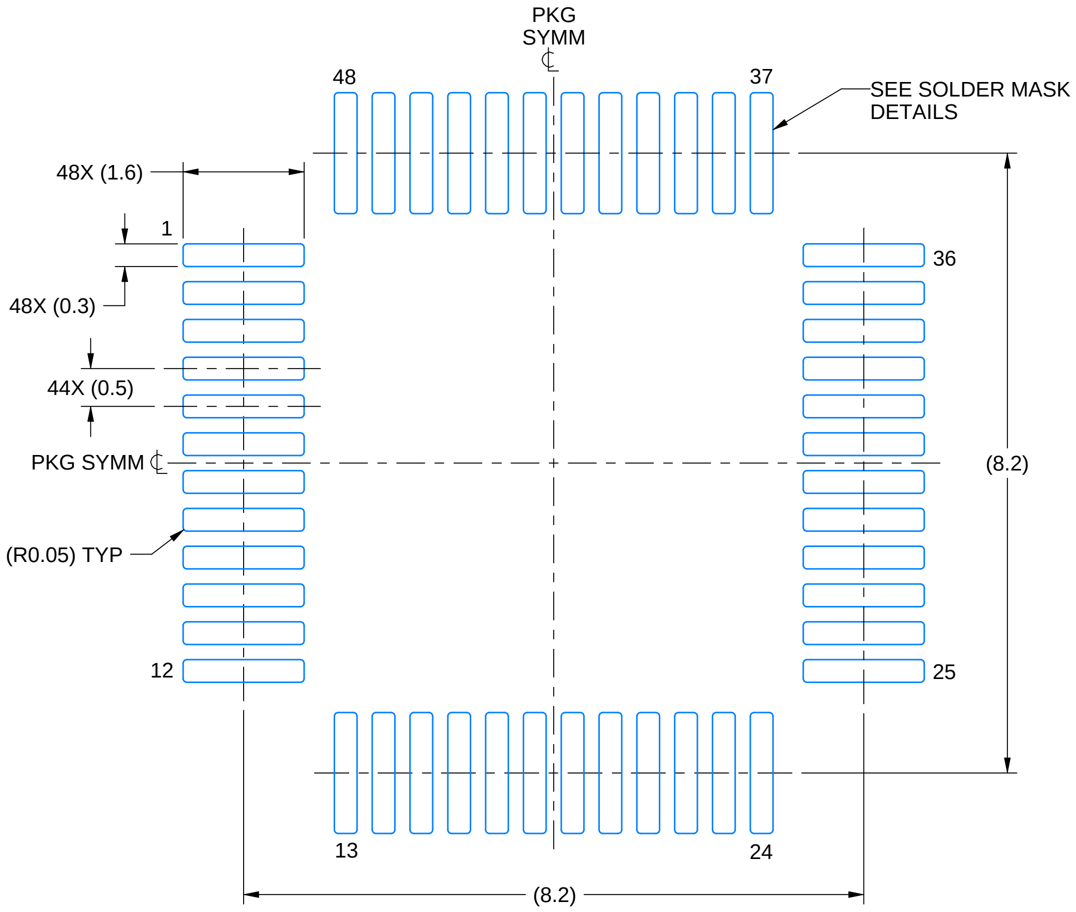
LOW PROFILE QUAD FLATPACK



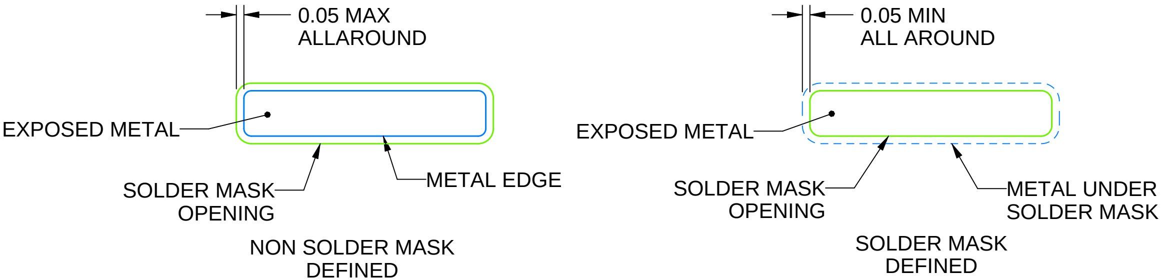
4215159/B 11/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000

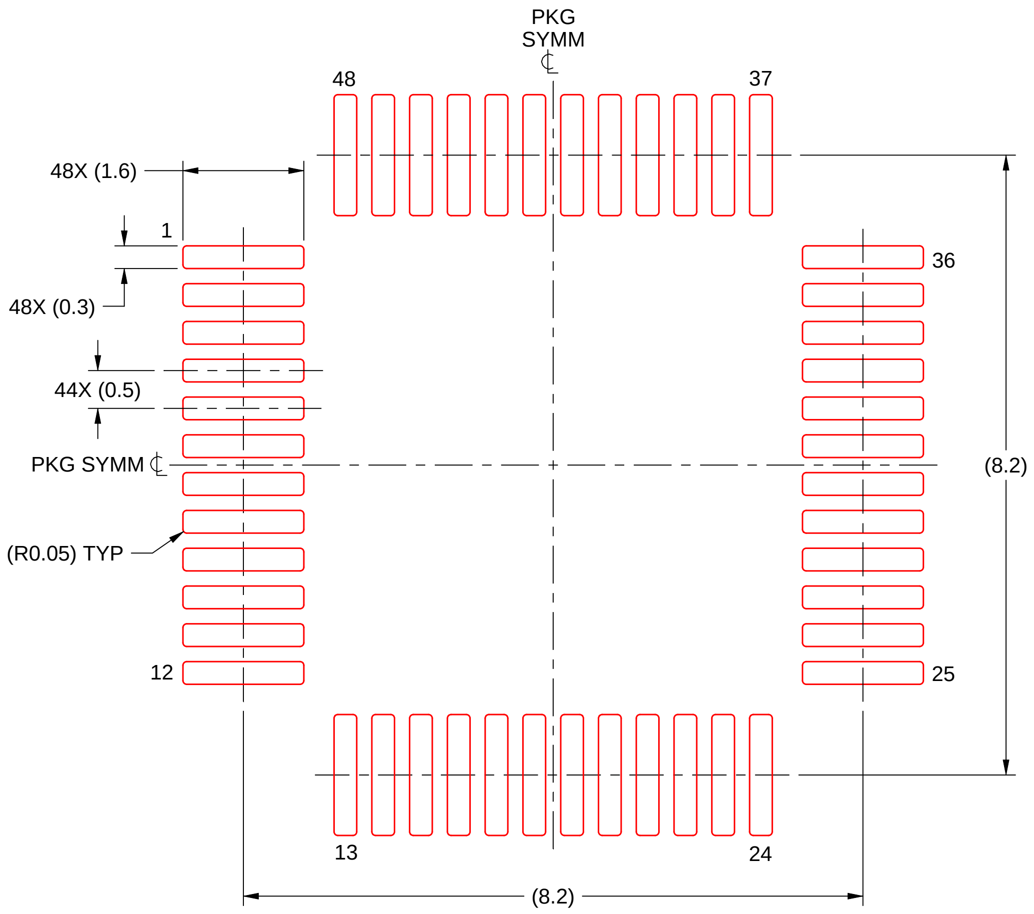


SOLDER MASK DETAILS

4215159/B 11/2023

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/B 11/2023

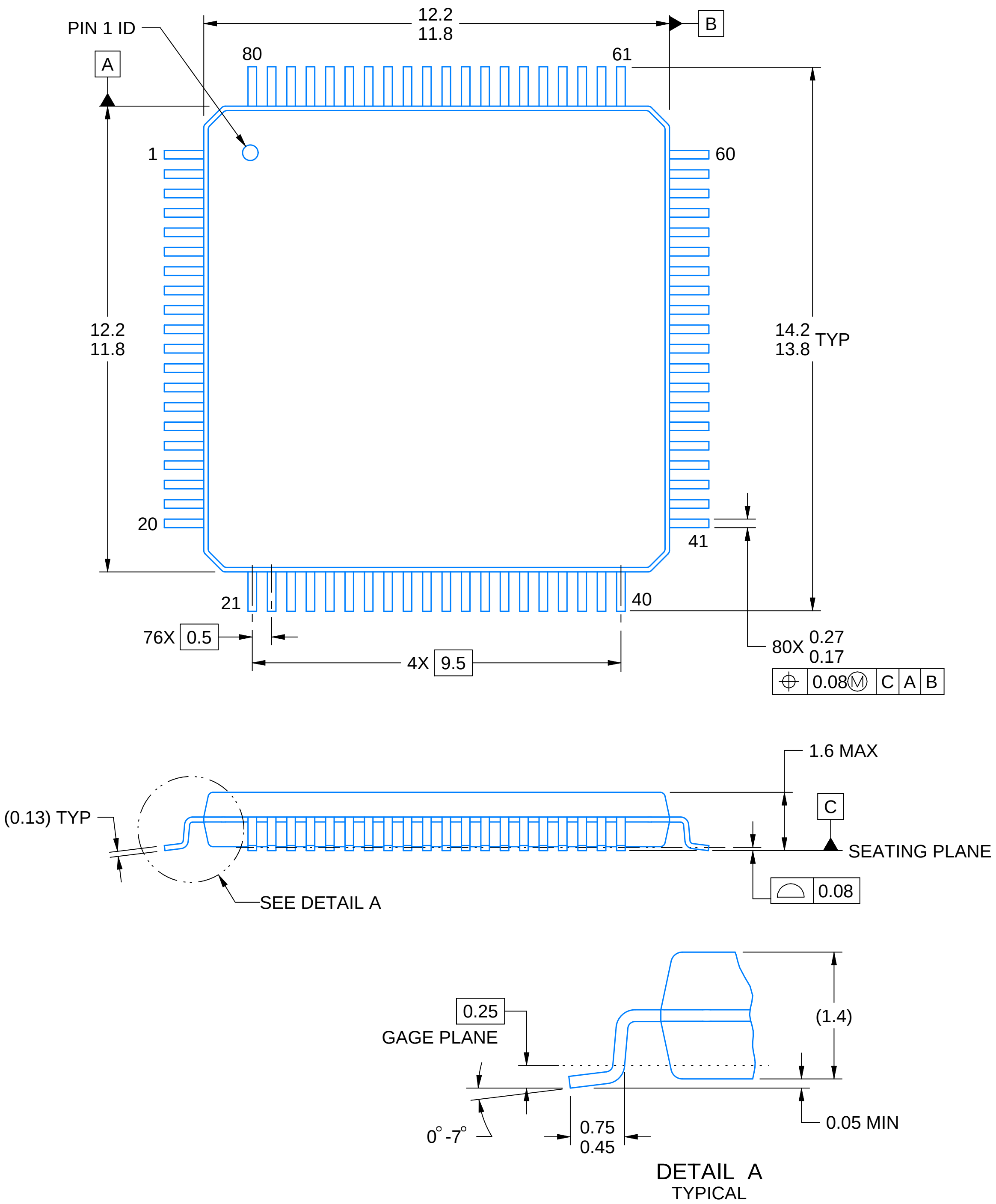
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

LQFP - 1.6 mm max height

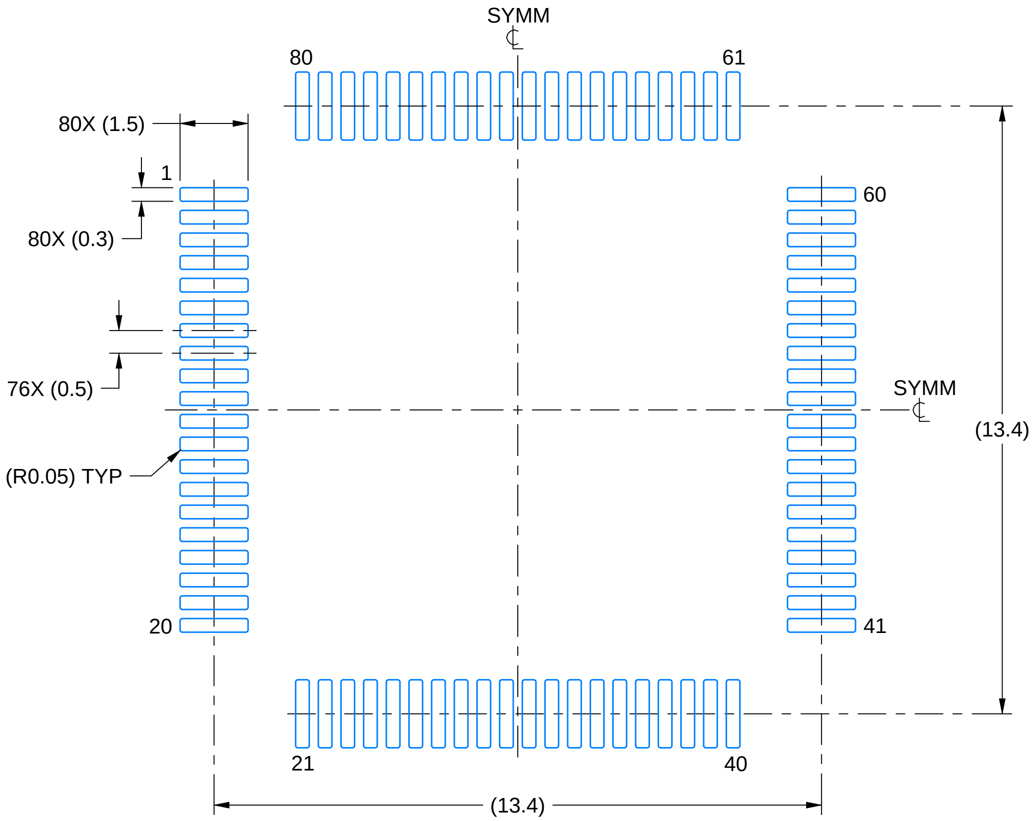
PLASTIC QUAD FLATPACK



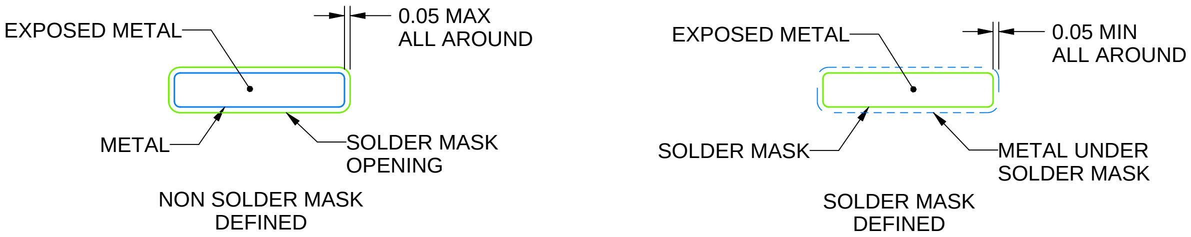
4215166/A 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

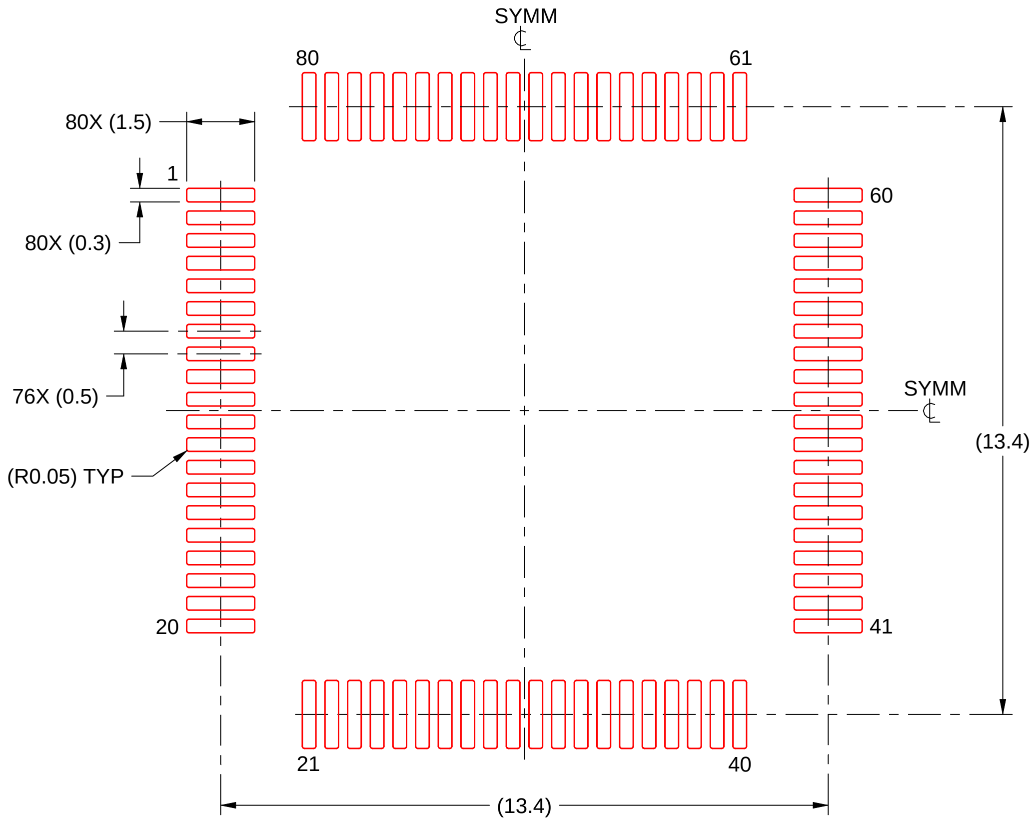


SOLDER MASK DETAILS

4215166/A 08/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215166/A 08/2022

NOTES: (continued)

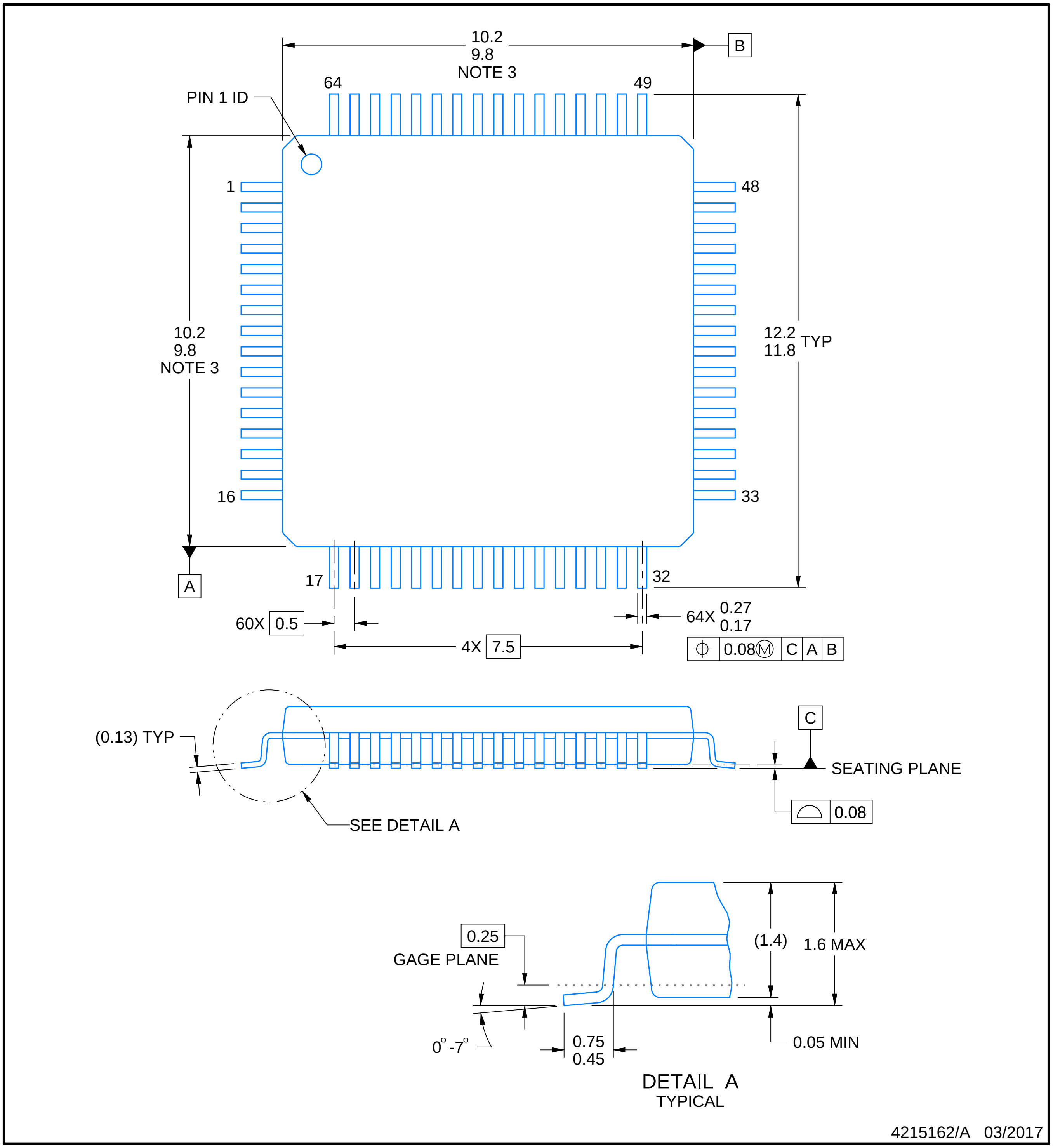
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PM0064A

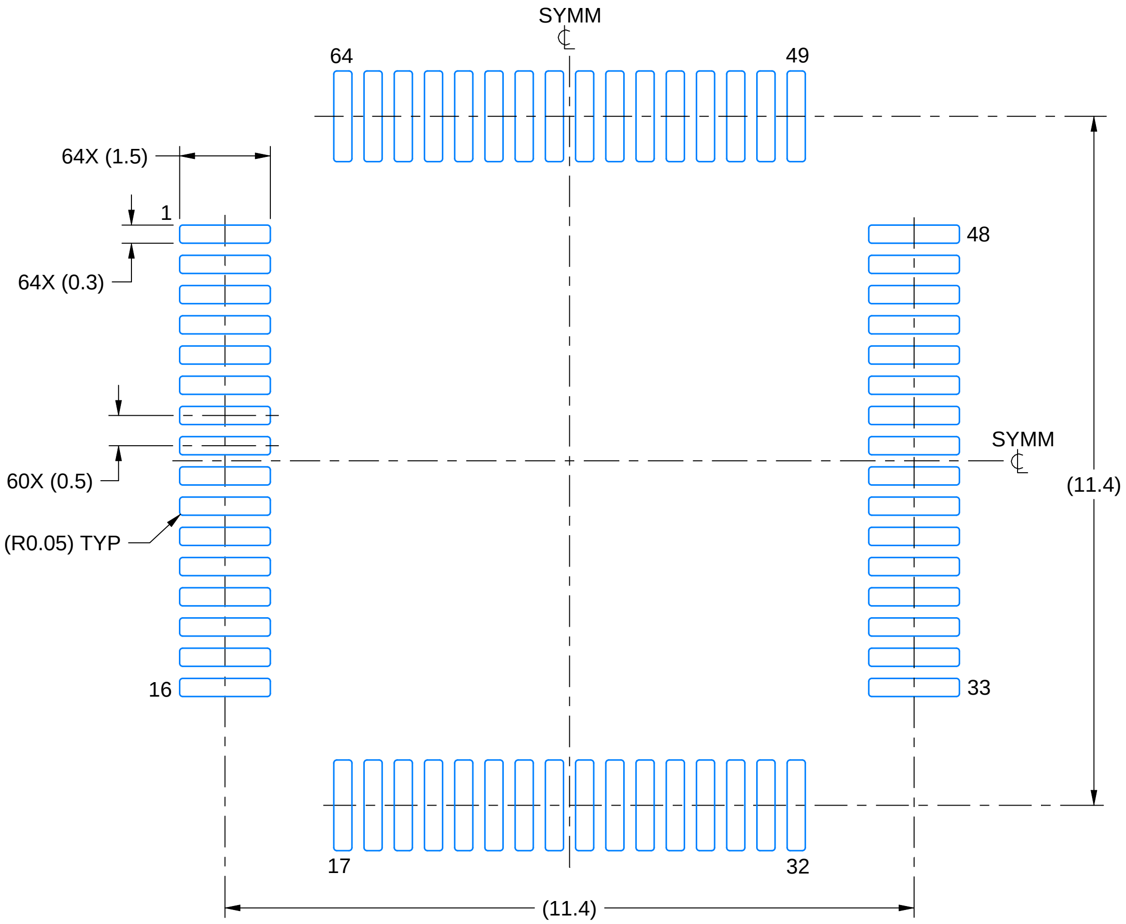
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

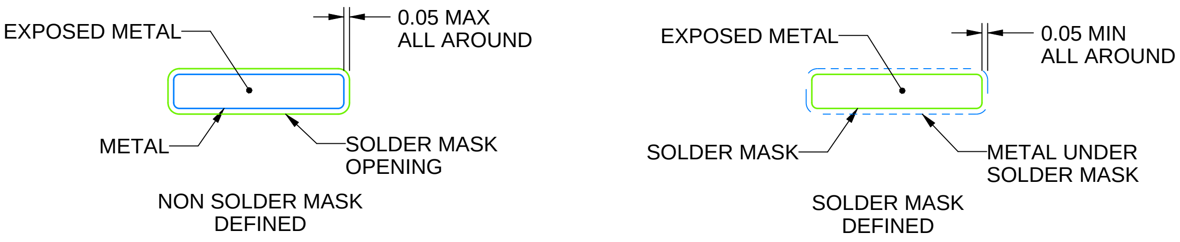


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

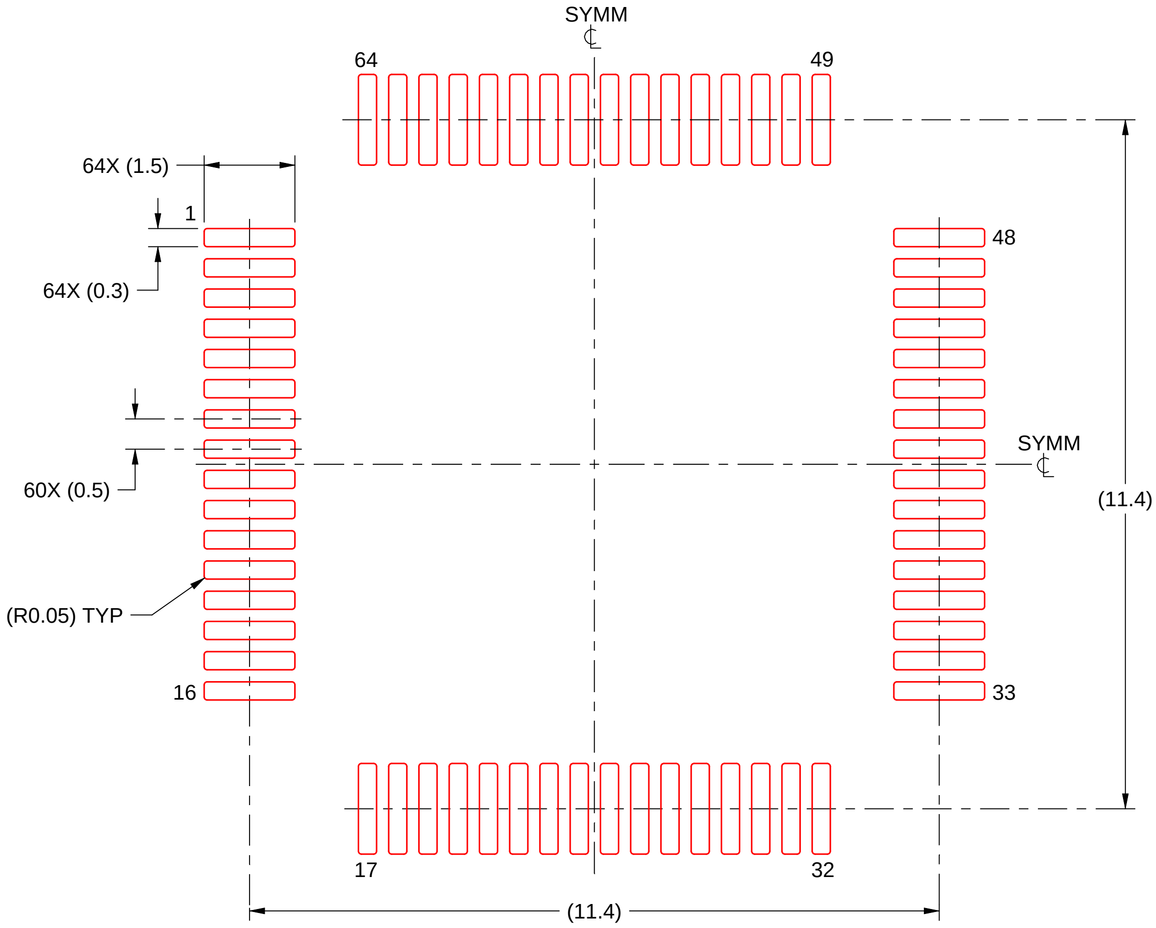


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated