COMPLETE DDR, DDR2, DDR3, AND LPDDR3 MEMORY POWER SOLUTION SYNCHRONOUS BUCK CONTROLLER, 1-A LDO, BUFFERED REFERENCE

Check for Samples: TPS51116-EP

FEATURES

- **Synchronous Buck Controller (VDDQ)**
  - **Wide-Input Voltage Range: 3.0-V to 28-V**
  - **D−CAP™ Mode with 100-ns Load Step Response**
  - **Current Mode Option Supports Ceramic Output Capacitors**
  - **Supports Soft-Off in S4/S5 States**
  - **Current Sensing from $R_{DS(on)}$ or Resistor**
  - **2.5-V (DDR), 1.8-V (DDR2), Adjustable to 1.5-V (DDR3) or 1.2-V (LPDDR3) or Output Range 0.75-V to 3.0-V**
  - **Equipped with Powergood, Overvoltage Protection and Undervoltage Protection**
- **1-A LDO (VTT), Buffered Reference (VREF)**
  - **Capable to Sink and Source 1 A**
  - **LDO Input Available to Optimize Power Losses**
  - **Requires only 20-µF Ceramic Output Capacitor**
  - **Buffered Low Noise 10-mA VREF Output**
  - **Accuracy ±20 mV for both VREF and VTT**
  - **Supports High-Z in S3 and Soft-Off in S4/S5**
  - **Thermal Shutdown**

APPLICATIONS

- **DDR/DDR2/DDR3/LPDDR3 Memory Power Supplies**
- **SSTL-2, SSTL-18, SSTL-15 and HSTL Termination**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C to 125°C) Temperature Range**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

DESCRIPTION

The TPS51116 provides a complete power supply for DDR/SSTL-2, DDR2/SSTL-18, DDR3/SSTL-15, and LPDDR3 memory systems. It integrates a synchronous buck controller with a 1-A sink/source tracking linear regulator and buffered low noise reference. The TPS51116 offers the lowest total solution cost in systems where space is at a premium. The TPS51116 synchronous controller runs fixed 400-kHz, pseudo-constant frequency PWM with an adaptive on-time control that can be configured in D-CAP™ Mode for ease of use and fastest transient response or in current mode to support ceramic output capacitors. The 1-A sink/source LDO maintains fast transient response only requiring 20-µF (2 × 10 µF) of ceramic output capacitance. In addition, the LDO supply input is available externally to significantly reduce the total power losses. The TPS51116 supports all of the sleep state controls placing VTT at high-Z in S3 (suspend to RAM) and discharging VDDQ, VTT and VTTREF (soft-off) in S4/S5 (suspend to disk). TPS51116 has all of the protection features including thermal shutdown and is offered in a 20-pin HTSSOP PowerPAD™ package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	Plastic HTSSOP PowerPAD (PWP)(2)	TPS51116MPWPREP	51116M	V62/12602-01XE
		TPS51116MPWPEP		V62/12602-01XE-T

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) With Cu NIPDAU lead/ball finish

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range unless otherwise noted

			MIN	MAX	UNIT
V_{IN}	Input voltage range	VBST	–0.3	36	V
		VBST wrt LL	–0.3	6	
		CS, MODE, S3, S5, VTTSNS, VDDQSNS, V5IN, VLDOIN, VDDQSET	–0.3	6	
		PGND, VTTGND	–0.3	0.3	
V_{OUT}	Output voltage range	DRVH	–1.0	36	V
		LL	–1.0	30	
		LL, pulse width < 20 ns	–5	30	
		COMP, DRVL, PGOOD, VTT, VTTREF	–0.3	6	
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS51116-EP PWP 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	41.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	27.4	
θ_{JB}	Junction-to-board thermal resistance(4)	23.9	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.1	
ψ_{JB}	Junction-to-board characterization parameter(6)	23.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	3.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, V5IN		4.75	5.25	V
Voltage range	VBST, DRVH	–0.1	34	V
	LL	–0.6	28	
	VLDOIN, VTT, VTTSNS, VDDQSNS	–0.1	3.6	
	VTTREF	–0.1	1.8	
	PGND, VTTGND	–0.1	0.1	
	S3, S5, MODE, VDDQSET, CS, COMP, PGOOD, DRVL	–0.1	5.25	
Operating temperature range, T_J		–55	125	°C

ELECTRICAL CHARACTERISTICS

T_J = −55°C to 125°C, $T_J = T_A$, V_{V5IN} = 5 V, VLDOIN is connected to VDDQ output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{V5IN1}	Supply current 1, V5IN	No load, $V_{S3} = V_{S5}$ = 5 V, COMP connected to capacitor		0.8	2	mA
I_{V5IN2}	Supply current 2, V5IN	No load, V_{S3} = 0 V, V_{S5} = 5 V, COMP connected to capacitor		300	610	µA
I_{V5IN3}	Supply current 3, V5IN	No load, V_{S3} = 0 V, V_{S5} = 5 V, V_{COMP} = 5 V		240	508	
$I_{V5INSDN}$	Shutdown current, V5IN	No load, $V_{S3} = V_{S5}$ = 0 V		0.1	1.81	
$I_{VLDOIN1}$	Supply current 1, VLDOIN	No load, $V_{S3} = V_{S5}$ = 5 V		1	10	
$I_{VLDOIN2}$	Supply current 2, VLDOIN	No load, V_{S3} = 5 V, V_{S5} = 0 V,		0.1	10.5	
$I_{VLDOINSDN}$	Standby current, VLDOIN	No load, $V_{S3} = V_{S5}$ = 0 V		0.1	1.5	

ELECTRICAL CHARACTERISTICS (continued)

T_J = −55°C to 125°C, T_J = T_A, V_{V5IN} = 5 V, VLDOIN is connected to VDDQ output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VTTREF OUTPUT						
V_{VTTREF}	Output voltage, VTTREF			$V_{VDDQSNS}$/2		V
$V_{VTTREFTOL}$	Output voltage tolerance	-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 2.5 V, Tolerance to $V_{VDDQSNS}$/2	-20		20	mV
		-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 1.8 V, Tolerance to $V_{VDDQSNS}$/2	-19		19	
		-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 1.5 V, Tolerance to $V_{VDDQSNS}$/2	-16		16	
		-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 1.2 V, Tolerance to $V_{VDDQSNS}$/2	–13		13	
$V_{VTTREFSRC}$	Source current	$V_{VDDQSNS}$ = 2.5 V, V_{VTTREF} = 0 V	-19	-40	-83.5	mA
$V_{VTTREFSNK}$	Sink current	$V_{VDDQSNS}$ = 2.5 V, V_{VTTREF} = 2.5 V	19	40	83.5	
VDDQ OUTPUT						
V_{VDDQ}	Output voltage, VDDQ	T_A = 25°C, $V_{VDDQSET}$ = 0 V, No load	2.465	2.500	2.535	V
		-55°C ≤ T_A ≤ 125°C, $V_{VDDQSET}$ = 0 V, No load	2.43	2.50	2.56	
		T_A = 25°C, $V_{VDDQSET}$ = 5 V, No load	1.776	1.800	1.830	
		-55°C ≤ T_A ≤ 125°C, $V_{VDDQSET}$ = 5 V, No load	1.762	1.800	1.838	
		-55°C ≤ T_A ≤ 125°C, Adjustable mode, No load	0.75		3.0	
$V_{VDDQSET}$	VDDQSET regulation voltage	T_A = 25°C, Adjustable mode	742.5	750	760.5	mV
		-55°C ≤ T_A ≤ 125°C, Adjustable mode	737	750	763	
$R_{VDDQSNS}$	Input impedance, VDDQSNS	$V_{VDDQSET}$ = 0 V		215		kΩ
		$V_{VDDQSET}$ = 5 V		180		
		Adjustable mode		460		
$I_{VDDQSET}$	Input current, VDDQSET	$V_{VDDQSET}$ = 0.78 V, COMP = Open		-0.04		µA
		$V_{VDDQSET}$ = 0.78 V, COMP = 5 V		-0.06		
$I_{VDDQDisch}$	Discharge current, VDDQ	V_{S3} = V_{S5} = 0 V, $V_{VDDQSNS}$ = 0.5 V, V_{MODE} = 0 V	10	40		mA
$I_{VLDOINDisch}$	Discharge current, VLDOIN	V_{S3} = V_{S5} = 0 V, $V_{VDDQSNS}$ = 0.5 V, V_{MODE} = 0.5 V		700		mA
VTT OUTPUT						
V_{VTTSNS}	Output voltage, VTT	V_{S3} = V_{S5} = 5 V, V_{VLDOIN} = $V_{VDDQSNS}$ = 2.5 V		1.25		V
		V_{S3} = V_{S5} = 5 V, V_{VLDOIN} = $V_{VDDQSNS}$ = 1.8 V		0.9		
		V_{S3} = V_{S5} = 5 V, V_{VLDOIN} = $V_{VDDQSNS}$ = 1.5 V		0.75		
$V_{VTTTOL25}$	VTT output voltage tolerance to VTTREF	$V_{VDDQSNS}$ = V_{VLDOIN} = 2.5 V, V_{S3} = V_{S5} = 5 V, I_{VTT} = 0 A	-21		21	mV
		$V_{VDDQSNS}$ = V_{VLDOIN} = 2.5 V, V_{S3} = V_{S5} = 5 V, $\|I_{VTT}\|$ < 1 A	-31		31	
$V_{VTTTOL18}$	VTT output voltage tolerance to VTTREF	$V_{VDDQSNS}$ = V_{VLDOIN} = 1.8 V, V_{S3} = V_{S5} = 5 V, I_{VTT} = 0 A	-21		21	mV
		$V_{VDDQSNS}$ = V_{VLDOIN} = 1.8 V, V_{S3} = V_{S5} = 5 V, $\|I_{VTT}\|$ < 1 A	-31		31	
$V_{VTTTOL15}$	VTT output voltage tolerance to VTTREF	$V_{VDDQSNS}$ = V_{VLDOIN} = 1.5 V, V_{S3} = V_{S5} = 5 V, I_{VTT} = 0 A	-21		21	mV
		$V_{VDDQSNS}$ = V_{VLDOIN} = 1.5 V, V_{S3} = V_{S5} = 5 V, $\|I_{VTT}\|$ < 1 A	-31		31	
$V_{VTTTOL12}$	VTT output voltage tolerance to VTTREF	$V_{VDDQSNS}$ = V_{VLDOIN} = 1.2 V, V_{S3} = V_{S5} = 5 V, I_{VTT} = 0 A	-21		21	mV
		$V_{VDDQSNS}$ = V_{VLDOIN} = 1.2 V, V_{S3} = V_{S5} = 5 V, $\|I_{VTT}\|$ < 1 A	-31		31	

ELECTRICAL CHARACTERISTICS (continued)

T_J = −55°C to 125°C, T_J = T_A, V_{V5IN} = 5 V, VLDOIN is connected to VDDQ output (unless otherwise noted)

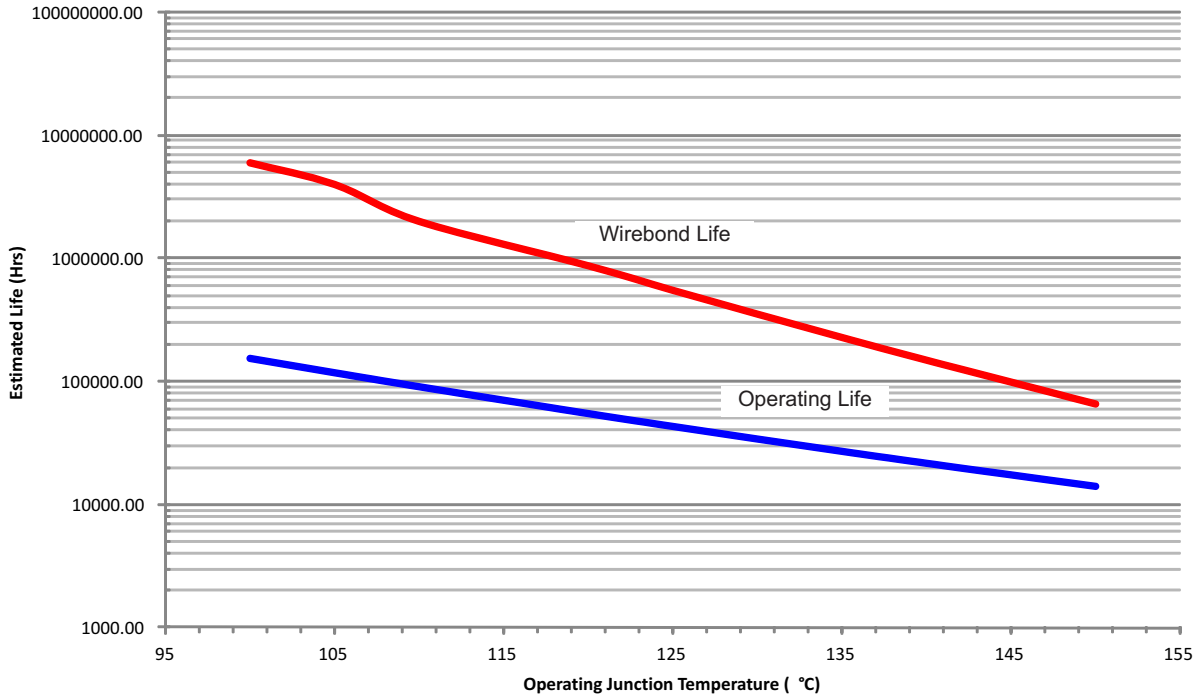
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VTTTOCLSRC}$	Source current limit, VTT	V_{VLDOIN} = $V_{VDDQSNS}$ = 2.5 V, V_{VTT} = V_{VTTSNS} = 1.19 V, PGOOD = HI	2.7	3.8	6.2	A
		V_{VLDOIN} = $V_{VDDQSNS}$ = 2.5 V, V_{VTT} = 0 V	1.4	2.2	3.2	
$I_{VTTTOCLSNK}$	Sink current limit, VTT	V_{VLDOIN} = $V_{VDDQSNS}$ = 2.5 V, V_{VTT} = V_{VTTSNS} = 1.31 V, PGOOD = HI	2.65	3.6	6	
		V_{VLDOIN} = $V_{VDDQSNS}$ = 2.5 V, V_{VTT} = V_{VDDQ}	1.4	2.2	3	
I_{VTTLK}	Leakage current, VTT	V_{S3} = 0 V, V_{S5} = 5 V, V_{VTT} = $V_{VDDQSNS}$ /2	-11		11	µA
$I_{VTTBIAS}$	Input bias current, VTTSNS	V_{S3} = 5 V, V_{VTTSNS} = $V_{VDDQSNS}$ /2	-1.1		1.1	
$I_{VTTSNSLK}$	Leakage current, VTTSNS	V_{S3} = 0 V, V_{S5} = 5 V, V_{VTT} = $V_{VDDQSNS}$ /2	-1		1	
$I_{VTTDisch}$	Discharge current, VTT	V_{S3} = V_{S5} = $V_{VDDQSNS}$ = 0 V, V_{VTT} = 0.5 V	9.5	17		mA
TRANSCONDUCTANCE AMPLIFIER						
gm	Gain		232	300	364	µS
$I_{COMPSNK}$	COMP maximum sink current	V_{S3} = 0 V, V_{S5} = 5 V, $V_{VDDQSET}$ = 0 V, $V_{VDDQSNS}$ = 2.7 V, V_{COMP} = 1.28 V		13		µA
$I_{COMPSRC}$	COMP maximum source current	V_{S3} = 0 V, V_{S5} = 5 V, $V_{VDDQSET}$ = 0 V, $V_{VDDQSNS}$ = 2.3 V, V_{COMP} = 1.28 V		-13		
V_{COMPHI}	COMP high clamp voltage	V_{S3} = 0 V, V_{S5} = 5 V, $V_{VDDQSET}$ = 0 V, $V_{VDDQSNS}$ = 2.3 V, V_{CS} = 0 V	1.3	1.34	1.38	V
V_{COMPLO}	COMP low clamp voltage	V_{S3} = 0 V, V_{S5} = 5 V, $V_{VDDQSET}$ = 0 V, $V_{VDDQSNS}$ = 2.7 V, V_{CS} = 0 V	1.17	1.21	1.25	
DUTY CONTROL						
t_{ON}	Operating on-time	V_{IN} = 12 V, $V_{VDDQSET}$ = 0 V		520		ns
t_{ON0}	Startup on-time	V_{IN} = 12 V, $V_{VDDQSNS}$ = 0 V		125		
$t_{ON(min)}$	Minimum on-time	T_A = 25°C		100		
$t_{OFF(min)}$	Minimum off-time	T_A = 25°C		350		
ZERO CURRENT COMPARATOR						
V_{ZC}	Zero current comparator offset		-6	0	6	mV
OUTPUT DRIVERS						
R_{DRVH}	DRVH resistance	Source, I_{DRVH} = –100 mA		3	6	Ω
		Sink, I_{DRVH} = 100 mA		0.9	3	
R_{DRVL}	DRVL resistance	Source, I_{DRVL} = –100 mA		3	6	
		Sink, I_{DRVL} = 100 mA		0.9	3	
t_D	Dead time	LL-low to DRVL-on		10		ns
		DRVL-off to DRVH-on		20		

ELECTRICAL CHARACTERISTICS (continued)

T_J = −55°C to 125°C, T_J = T_A, V_{V5IN} = 5 V, VLDOIN is connected to VDDQ output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL BST DIODE						
V_{FBST}	Forward voltage	$V_{V5IN-VBST}$, I_F = 10 mA	0.58	0.8	1.1	V
I_{VBSTLK}	VBST leakage current	V_{VBST} = 34 V, V_{LL} = 28 V, V_{VDDQ} = 2.6 V		0.1	1.11	µA
PROTECTIONS						
V_{OCL}	Current limit threshold	$V_{PGND-CS}$, PGOOD = HI, V_{CS} < 0.5 V	47	60	70	mV
		$V_{PGND-CS}$, PGOOD = LO, V_{CS} < 0.5 V	18	30	40	
I_{TRIP}	Current sense sink current	V_{CS} > 4.5 V, PGOOD = HI	4	10	20	µA
		V_{CS} > 4.5 V, PGOOD = LO	2	5	10	
TC_{ITRIP}	TRIP current temperature coefficient	$R_{DS(on)}$ sense scheme, On the basis of T_A = 25°C (1)		4500		ppm/°C
$V_{OCL(off)}$	Overcurrent protection COMP offset	($V_{V5IN-CS}$ - $V_{PGND-LL}$), $V_{V5IN-CS}$ = 60 mV, V_{CS} > 4.5 V	-7	0	7	mV
$V_{R(trip)}$	Current limit threshold setting range	$V_{V5IN-CS}$	30		150	
POWERGOOD COMPARATOR						
$V_{TVDDQPG}$	VDDQ powergood threshold	PG in from lower	92%	95%	98%	
		PG in from higher	102%	105%	108%	
		PG hysteresis		5%		
$I_{PG(max)}$	PGOOD sink current	V_{VTT} = 0 V, V_{PGOOD} = 0.5 V	2.3	7.5		mA
$t_{PG(del)}$	PGOOD delay time	Delay for PG in	78	130	205	µs
UNDERVOLTAGE LOCKOUT AND LOGIC THRESHOLD						
V_{UVV5IN}	V5IN UVLO threshold voltage	Wake up	3.6	4	4.4	V
		Hysteresis	0.19	0.3	0.41	
V_{THMODE}	MODE threshold	No discharge	4.7			
		Non-tracking discharge			0.08	
$V_{THVDDQSET}$	VDDQSET threshold voltage	2.5 V output	0.075	0.150	0.255	
		1.8 V output	3.45	4	4.55	
V_{IH}	High-level input voltage	S3, S5	2.2			
V_{IL}	Low-level input voltage	S3, S5			0.3	
V_{IHYST}	Hysteresis voltage	S3, S5		0.2		
V_{INLEAK}	Logic input leakage current	S3, S5, MODE	-1		1	µA
$V_{INVDDQSET}$	Input leakage/ bias current	VDDQSET	-1		1	
UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	VDDQ OVP trip threshold voltage	OVP detect	109%	115%	121%	
		Hysteresis		5%		
t_{OVPDEL}	VDDQ OVP propagation delay			1.5		µs
V_{UVP}	Output UVP trip threshold	UVP detect		70%		
		Hysteresis		10%		
t_{UVPDEL}	Output UVP propagation delay			32		cycle
t_{UVPEN}	Output UVP enable delay			1007		
THERMAL SHUTDOWN						
T_{SDN}	Thermal SDN threshold (1)	Shutdown temperature		160		°C
		Hysteresis		10		

(1) Specified by design. Not production tested.



(1) See datasheet for absolute maximum and minimum recommended operating conditions.

(2) Sillicon operating life design goal is 10 years at 110°C junction temperature.

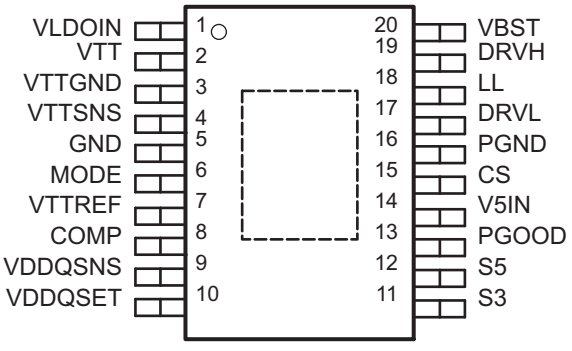
Figure 1. Operating and Wirebond Life Derating Chart

DEVICE INFORMATION

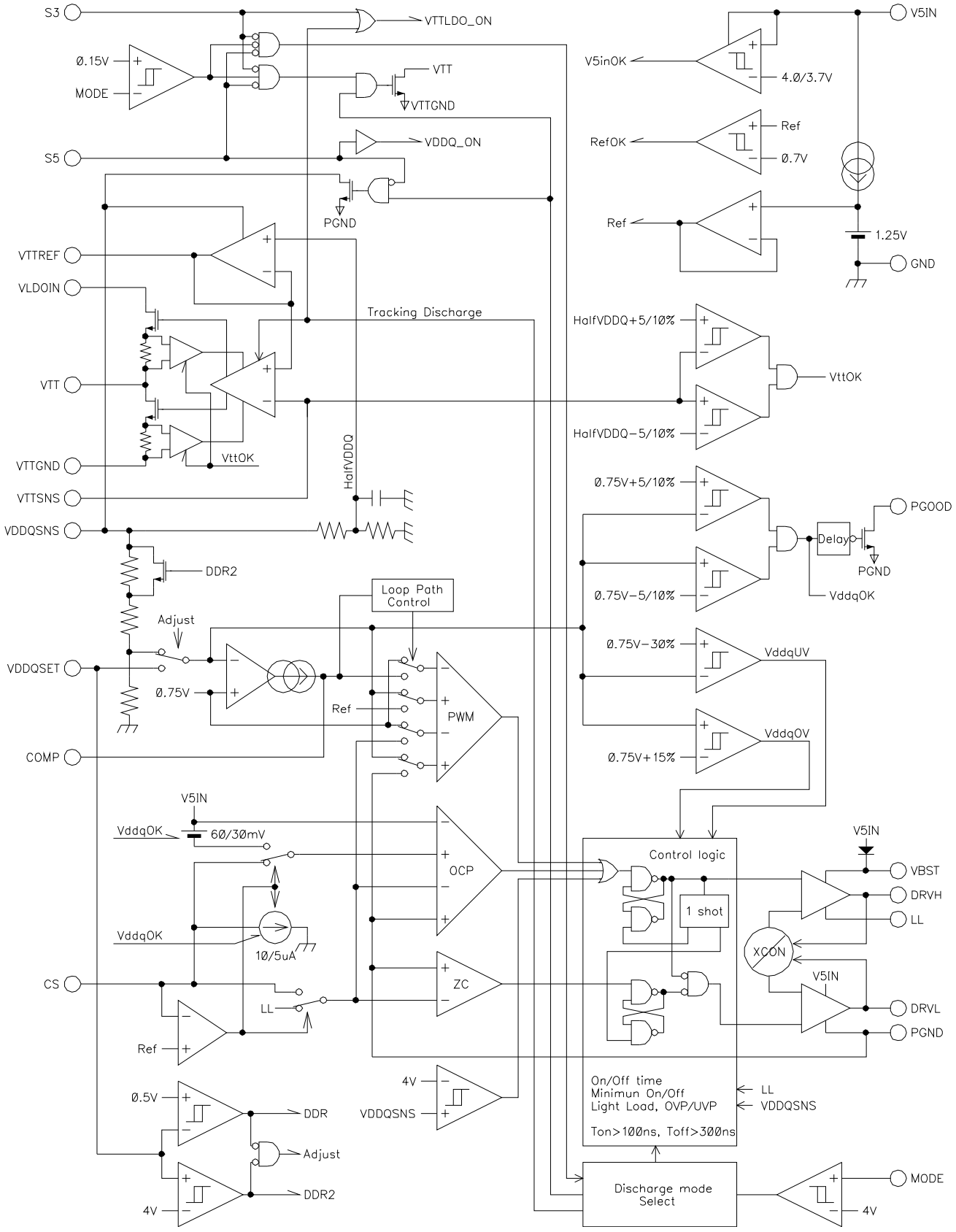
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO. PWP		
COMP	8	I/O	Output of the transconductance amplifier for phase compensation. Connect to V5IN to disable gm amplifier and use D-CAP™ mode.
CS	15	I/O	Current sense comparator input (-) for resistor current sense scheme. Or overcurrent trip voltage setting input for $R_{DS(on)}$ current sense scheme if connected to V5IN through the voltage setting resistor.
DRVH	19	O	Switching (top) MOSFET gate drive output.
DRVL	17	O	Rectifying (bottom) MOSFET gate drive output.
GND	5	-	Signal ground. Connect to minus terminal of the VTT LDO output capacitor.
LL	18	I/O	Switching (top) MOSFET gate driver return. Current sense comparator input (-) for $R_{DS(on)}$ current sense.
MODE	6	I	Discharge mode setting pin. See *VDDQ and VTT Discharge Control* section.
PGND	16	–	Ground for rectifying (bottom) MOSFET gate driver. Also current sense comparator input(+) and ground for powergood circuit.
PGOOD	13	O	Powergood signal open drain output, In HIGH state when VDDQ output voltage is within the target range.
S3	11	I	S3 signal input.
S5	12	I	S5 signal input.
V5IN	14	I	5-V power supply input for internal circuits and MOSFET gate drivers.
VBST	20	I/O	Switching (top) MOSFET driver bootstrap voltage input.
VDDQSET	10	I	VDDQ output voltage setting pin. See *VDDQ Output Voltage Selection* section.
VDDQSNS	9	I/O	VDDQ reference input for VTT and VTTREF. Power supply for the VTTREF. Discharge current sinking terminal for VDDQ Non-tracking discharge. Output voltage feedback input for VDDQ output if VDDQSET pin is connected to V5IN or GND.
VLDOIN	1	I	Power supply for the VTT LDO.
VTT	2	O	Power output for the VTT LDO.
VTTGND	3	–	Power ground output for the VTT LDO.
VTTREF	7	O	VTTREF buffered reference output.
VTTSNS	4	I	Voltage sense input for the VTT LDO. Connect to plus terminal of the VTT LDO output capacitor.

PWP PACKAGE
(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

The TPS51116 is an integrated power management solution which combines a synchronous buck controller, a 10-mA buffered reference and a high-current sink/source low-dropout linear regulator (LDO) in a small 20-pin HTSSOP package or a 24-pin QFN package. Each of these rails generates VDDQ, VTTREF and VTT that required with DDR/DDR2/DDR3/LPDDR3 memory systems. The switch mode power supply (SMPS) portion employs external N-channel MOSFETs to support high current for DDR/DDR2/DDR3/LPDDR3 memory VDD/VDDQ. The preset output voltage is selectable from 2.5 V or 1.8 V. User-defined output voltage is also possible and can be adjustable from 0.75 V to 3 V. Input voltage range of the SMPS is 3 V to 28 V. The SMPS runs an adaptive on-time PWM operation at high-load condition and automatically reduces frequency to keep excellent efficiency down to several mA. Current sensing scheme uses either $R_{DS(on)}$ of the external rectifying MOSFET for a low-cost, loss-less solution, or an optional sense resistor placed in series to the rectifying MOSFET for more accurate current limit. The output of the switcher is sensed by VDDQSNS pin to generate one-half VDDQ for the 10-mA buffered reference (VTTREF) and the VTT active termination supply. The VTT LDO can source and sink up to 1-A peak current with only 20-µF (two 10-µF in parallel) ceramic output capacitors. VTTREF tracks VDDQ/2 within ±1% of VDDQ. VTT output tracks VTTREF within ±20 mV at no load condition while ±40 mV at full load. The LDO input can be separated from VDDQ and optionally connected to a lower voltage by using VLDOIN pin. This helps reducing power dissipation in sourcing phase. TheTPS51116 is fully compatible to JEDEC DDR/DDR2 specifications at S3/S5 sleep state (see Table 2). The part has two options of output discharge function when both VTT and VDDQ are disabled. The tracking discharge mode discharges VDDQ and VTT outputs through the internal LDO transistors and then VTT output tracks half of VDDQ voltage during discharge. The non-tracking discharge mode discharges outputs using internal discharge MOSFETs which are connected to VDDQSNS and VTT. The current capability of these discharge FETs are limited and discharge occurs more slowly than the tracking discharge. These discharge functions can be disabled by selecting non-discharge mode.

VDDQ SMPS, Dual PWM Operation Modes

The main control loop of the SMPS is designed as an adaptive on-time pulse width modulation (PWM) controller. It supports two control schemes which are a current mode and a proprietary D-CAP™ mode. D-CAP™ mode uses internal compensation circuit and is suitable for low external component count configuration with an appropriate amount of ESR at the output capacitor(s). Current mode control has more flexibility, using external compensation network, and can be used to achieve stable operation with very low ESR capacitor(s) such as ceramic or specialty polymer capacitors.

These control modes are selected by the COMP terminal connection. If the COMP pin is connected to V5IN, TPS51116 works in the D-CAP™ mode, otherwise it works in the current mode. VDDQ output voltage is monitored at a feedback point voltage. If VDDQSET is connected to V5IN or GND, this feedback point is the output of the internal resistor divider inside VDDQSNS pin. If an external resistor divider is connected to VDDQSET pin, VDDQSET pin itself becomes the feedback point (see *VDDQ Output Voltage Selection* section).

At the beginning of each cycle, the synchronous high-side MOSFET is turned on, or becomes *ON* state. This MOSFET is turned off, or becomes *OFF* state, after internal one shot timer expires. This one shot is determined by V_{IN} and V_{OUT} to keep frequency fairly constant over input voltage range, hence it is called adaptive on-time control (see *PWM Frequency and Adaptive On-Time Control* section). The MOSFET is turned on again when feedback information indicates insufficient output voltage and inductor current information indicates below the overcurrent limit. Repeating operation in this manner, the controller regulates the output voltage. The synchronous bottom or the *rectifying* MOSFET is turned on each *OFF* state to keep the conduction loss minimum. The rectifying MOSFET is turned off when inductor current information detects zero level. This enables seamless transition to the reduced frequency operation at light load condition so that high efficiency is kept over broad range of load current.

In the current mode control scheme, the transconductance amplifier generates a target current level corresponding to the voltage difference between the feedback point and the internal 750 mV reference. During the *OFF* state, the PWM comparator monitors the inductor current signal as well as this target current level, and when the inductor current signal comes lower than the target current level, the comparator provides *SET* signal to initiate the next *ON* state. The voltage feedback gain is adjustable outside the controller device to support various types of output MOSFETs and capacitors. In the D-CAP™ mode, the transconductance amplifier is disabled and the PWM comparator compares the feedback point voltage and the internal 750 mV reference during the *OFF* state. When the feedback point comes lower than the reference voltage, the comparator provides *SET* signal to initiate the next *ON* state.

VDDQ SMPS, Light Load Condition

TPS51116 automatically reduces switching frequency at light load condition to maintain high efficiency. This reduction of frequency is achieved smoothly and without increase of V_{OUT}ripple or load regulation. Detail operation is described as follows. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its *valley* touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when this zero inductor current is detected. As the load current further decreased, the converter runs in discontinuous conduction mode and it takes longer and longer to discharge the output capacitor to the level that requires next *ON* cycle. The ON-time is kept the same as that in the heavy load condition. In reverse, when the output current increase from light load to heavy load, switching frequency increases to the constant 400 kHz as the inductor current reaches to the continuous conduction. The transition load point to the light load operation $I_{OUT(LL)}$ (i.e. the threshold between continuous and discontinuous conduction mode) can be calculated in Equation 1:

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

where

- *f* is the PWM switching frequency (400 kHz)

Switching frequency versus output current in the light load condition is a function of L, *f*, V_{IN} and V_{OUT}, but it decreases almost proportional to the output current from the $I_{OUT(LL)}$ given above. For example, it is 40 kHz at $I_{OUT(LL)}$/10 and 4 kHz at $I_{OUT(LL)}$/100.

Low-Side Driver

The low-side driver is designed to drive high-current, low-$R_{DS(on)}$, N-channel MOSFET(s). The drive capability is represented by the internal resistance, which is 3 Ω for V5IN to DRVL and 0.9 Ω for DRVL to PGND. A dead-time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on. 5-V bias voltage is delivered from V5IN supply. The instantaneous drive current is supplied by an input capacitor connected between V5IN and GND. The average drive current is equal to the gate charge at V_{GS} = 5 V times switching frequency. This gate drive current as well as the high-side gate drive current times 5 V makes the driving power which needs to be dissipated from TPS51116 package.

High-Side Driver

The high-side driver is designed to drive high-current, low on-resistance, N-channel MOSFET(s). When configured as a floating driver, 5-V bias voltage is delivered from V5IN supply. The average drive current is also calculated by the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between VBST and LL pins. The drive capability is represented by the internal resistance, which is 3 Ω for VBST to DRVH and 0.9 Ω for DRVH to LL.

Current Sensing Scheme

In order to provide both good accuracy and cost effective solution, TPS51116 supports both of external resistor sensing and MOSFET $R_{DS(on)}$ sensing. For resistor sensing scheme, an appropriate current sensing resistor should be connected between the source terminal of the low-side MOSFET and PGND. CS pin is connected to the MOSFET source terminal node. The inductor current is monitored by the voltage between PGND pin and CS pin. For $R_{DS(on)}$ sensing scheme, CS pin should be connected to V5IN through the trip voltage setting resistor, R_{TRIP}. In this scheme, CS terminal sinks 10-μA I_{TRIP} current and the trip level is set to the voltage across the R_{TRIP}. The inductor current is monitored by the voltage between PGND pin and LL pin so that LL pin should be connected to the drain terminal of the low-side MOSFET. I_{TRIP} has 4500ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. In either scheme, PGND is used as the positive current sensing node so that PGND should be connected to the proper current sensing device, i.e. the sense resistor or the source terminal of the low-side MOSFET.

PWM Frequency and Adaptive On-Time Control

TPS51116 includes an adaptive on-time control scheme and does not have a dedicated oscillator on board. However, the device runs with fixed 400-kHz pseudo-constant frequency by feed-forwarding the input and output voltage into the on-time one-shot timer. The on-time is controlled inverse proportional to the input voltage and proportional to the output voltage so that the duty ratio is kept as V_{OUT}/V_{IN} technically with the same cycle time. Although the TPS51116 does not have a pin connected to VIN, the input voltage is monitored at LL pin during the *ON* state. This helps pin count reduction to make the part compact without sacrificing its performance. In order to secure minimum ON-time during startup, feed-forward from the output voltage is enabled after the output becomes 750 mV or larger.

VDDQ Output Voltage Selection

TPS51116 can be used for both of DDR (V_{VDDQ} = 2.5 V) and DDR2 (V_{VDDQ} = 1.8 V) power supply and adjustable output voltage (0.75 V < V_{VDDQ} < 3 V) by connecting VDDQSET pin as shown in Table 1. Use the adjustable output voltage scheme for a DDR3 (V_{VDDQ}= 1.5 V) or LPDDR3 (V_{VDDQ}= 1.2 V) application.

Table 1. VDDQSET and Output Voltages

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	$V_{VDDQSNS}$/2	DDR
V5IN	1.8	$V_{VDDQSNS}$/2	DDR2
FB Resistors	Adjustable	$V_{VDDQSNS}$/2	0.75 V < V_{VDDQ} < 3 V(1) (2)

VTT Linear Regulator and VTTREF

TPS51116 integrates high performance low-dropout linear regulator that is capable of sourcing and sinking current up to 1 A. This VTT linear regulator employs ultimate fast response feedback loop so that small ceramic capacitors are enough to keep tracking the VTTREF within ±40 mV at all conditions including fast load transient. To achieve tight regulation with minimum effect of wiring resistance, a remote sensing terminal, VTTSNS, should be connected to the positive node of VTT output capacitor(s) as a separate trace from VTT pin. For stable operation, total capacitance of the VTT output terminal can be equal to or greater than 20 µF. It is recommended to attach two 10-µF ceramic capacitors in parallel to minimize the effect of ESR and ESL. If ESR of the output capacitor is greater than 2 mΩ, insert an RC filter between the output and the VTTSNS input to achieve loop stability. The RC filter time constant should be almost the same or slightly lower than the time constant made by the output capacitor and its ESR. VTTREF block consists of on-chip 1/2 divider, LPF and buffer. This regulator also has sink and source capability up to 10 mA. Bypass VTTREF to GND by a 0.033-µF ceramic capacitor for stable operation.

When VTT is not required in the design, following treatment is strongly recommended.

- Connect VLDOIN to VDDQSNS.
- Tie VTTSNS to VTT, and remove capacitors from VTT to float.
- Connect VTTGND and MODE to GND (Non-tracking discharge mode as shown in Table 3)
- Maintain a 0.033-µF capacitor connected at VTTREF.
- Pull down S3 to GND with 1 kΩ of resistance.

A typical circuit for this application is shown in Figure 2

(1) V_{VDDQ}≥ 1.2 V when used as VLDOIN.
(2) Including DDR3 and LPDDR3

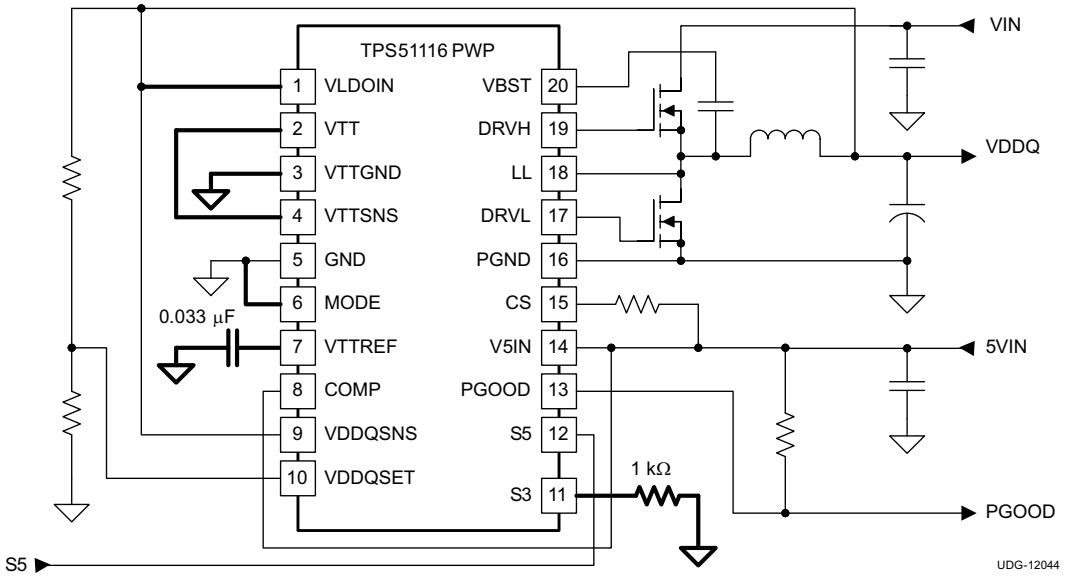


Figure 2. Application Circuit When VTT Is Not Required

Controling Outputs Using the S3 and S5 Pins

In the DDR/DDR2/DDR3/LPDDR3 memory applications, it is important to keep VDDQ always higher than VTT/VTTREF including both start-up and shutdown. TPS51116 provides this management by simply connecting both the S3 and S5 pins to the sleep-mode signals such as SLP_S3 and SLP_S5 in the notebook PC system. All of VDDQ, VTTREF and VTT are turned on at S0 state (S3 = S5 = high). In S3 state (S3 = low, S5 = high), VDDQ and VTTREF voltages are kept on while VTT is turned off and left at high impedance (high-Z) state. The VTT output is floated and does not sink or source current in this state. In S4/S5 states (S3 = S5 = low), all of the three outputs are disabled. Outputs are discharged to ground according to the discharge mode selected by MODE pin (see *VDDQ and VTT Discharge Control* section). Each state code represents as follow; S0 = full ON, S3 = suspend to RAM (STR), S4 = suspend to disk (STD), S5 = soft OFF. (See Table 2)

Table 2. Sleep Mode Control Using the S3 and S5 Pins

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF (High-Z)
S4/S5	LO	LO	OFF (Discharge)	Off (Discharge)	OFF (Discharge)

Soft-Start and Powergood

The soft start function of the SMPS is achieved by ramping up reference voltage and two-stage current clamp. At the starting point, the reference voltage is set to 650 mV (87% of its target value) and the overcurrent threshold is set half of the nominal value. When UVP comparator detects VDDQ become greater than 80% of the target, the reference voltage is raised toward 750 mV using internal 4-bit DAC. This takes approximately 85 µs. The overcurrent threshold is released to nominal value at the end of this period. The powergood signal waits another 45 µs after the reference voltage reaches 750 mV and the VDDQ voltage becomes good (above 95% of the target voltage), then turns off powergood open-drain MOSFET.

The soft-start function of the VTT LDO is achieved by current clamp. The current limit threshold is also changed in two stages using an internal powergood signal dedicated for LDO. During VTT is below the powergood threshold, the current limit level is cut into 60% (2.2 A).This allows the output capacitors to be charged with low and constant current that gives linear ramp up of the output. When the output comes up to the good state, the overcurrent limit level is released to normal value (3.8 A). TPS51116 has an independent counter for each output, but the PGOOD signal indicates only the status of VDDQ and does not indicate VTT powergood externally. See Figure 3.

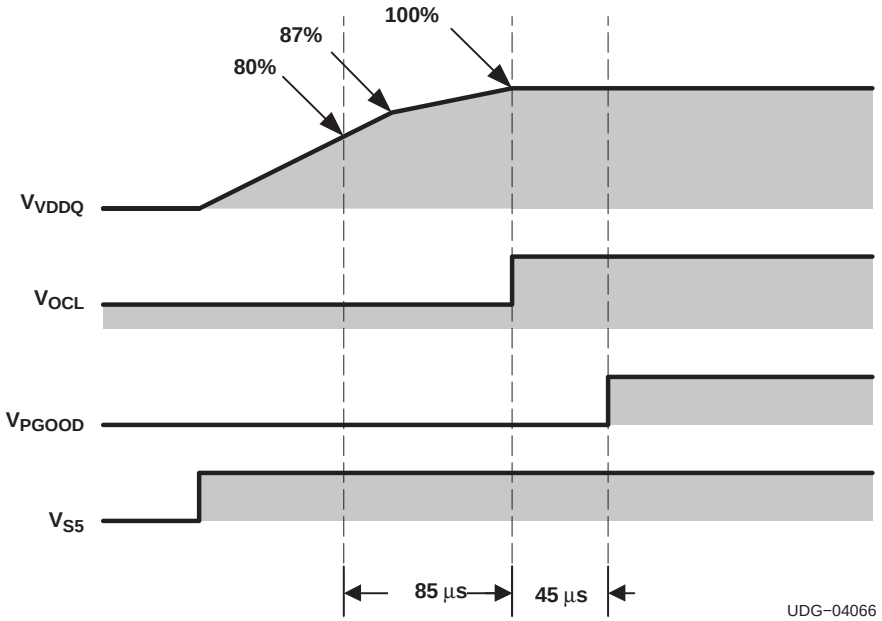


Figure 3. VDDQ Soft-Start and Powergood Timing

Soft-start duration, t_{VDDQSS}, t_{VTTSS} are functions of output capacitances.

$$t_{VDDQSS} = \frac{2 \times C_{VDDQ} \times V_{VDDQ} \times 0.8}{I_{VDDQOCP}} + 85\,\mu s \quad (2)$$

where

- $I_{VDDQOCP}$ is the current limit value for VDDQ switcher calculated by Equation 5

$$t_{VTTSS} = \frac{C_{VTT} \times V_{VTT}}{I_{VTTOCL}} \quad (3)$$

where

- I_{VTTOCL} = 2.2 A (typ)

In both Equation 2 and Equation 3 , no load current during start-up are assumed. Note that both switchers and the LDO do not start up with full load condition.

VDDQ and VTT Discharge Control

TPS51116 discharges VDDQ, VTTREF and VTT outputs when S3 and S5 are both low. There are two different discharge modes. The discharge mode can be set by connecting MODE pin as shown in Table 3.

Table 3. Discharge Selection

MODE	DISCHARGE MODE
V5IN	No discharge
VDDQ	Tracking discharge
GND	Non-tracking discharge

When in tracking-discharge mode, TPS51116 discharges outputs through the internal VTT regulator transistors and VTT output tracks half of VDDQ voltage during this discharge. Note that VDDQ discharge current flows via VLDOIN to LDOGND thus VLDOIN must be connected to VDDQ output in this mode. The internal LDO can handle up to 1 A and discharge quickly. After VDDQ is discharged down to 0.2 V, the internal LDO is turned off and the operation mode is changed to the non-tracking-discharge mode.

When in non-tracking-discharge mode, TPS51116 discharges outputs using internal MOSFETs which are connected to VDDQSNS and VTT. The current capability of these MOSFETs are limited to discharge slowly. Note that VDDQ discharge current flows from VDDQSNS to PGND in this mode. In no discharge mode, TPS51116 does not discharge any output charge.

Current Protection for VDDQ

The SMPS has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the *OFF* state and the controller keeps the OFF state during the inductor current is larger than the overcurrent trip level. The trip level and current sense scheme are determined by CS pin connection (see *Current Sensing Scheme* section). For resistor sensing scheme, the trip level, V_{TRIP}, is fixed value of 60 mV.

For $R_{DS(on)}$ sensing scheme, CS terminal sinks 10 µA and the trip level is set to the voltage across this R_{TRIP} resistor.

$$V_{TRIP}\,(mV) = R_{TRIP}\,(k\Omega) \times 10\,(\mu A) \tag{4}$$

As the comparison is done during the *OFF* state, V_{TRIP} sets valley level of the inductor current. Thus, the load current at overcurrent threshold, I_{OCP}, can be calculated as shown in Equation 5.

$$I_{OCP} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{I_{RIPPLE}}{2} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{2 \times L \times f} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}} \tag{5}$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down. If the output voltage becomes less than Powergood level, the V_{TRIP} is cut into half and the output voltage tends to be even lower. Eventually, it crosses the undervoltage protection threshold and shutdown.

Current Protection for VTT

The LDO has an internally fixed constant overcurrent limiting of 3.8 A while operating at normal condition. This trip point is reduced to 2.2 A before the output voltage comes within ±5% of the target voltage or goes outside of ±10% of the target voltage.

Overvoltage and Undervoltage Protection for VDDQ

TPS51116 monitors a resistor divided feedback voltage to detect overvoltage and undervoltage. If VDDQSET is connected to V5IN or GND, the feedback voltage is made by an internal resistor divider inside VDDQSNS pin. If an external resistor divider is connected to VDDQSET pin, the feedback voltage is VDDQSET voltage itself. When the feedback voltage becomes higher than 115% of the target voltage, the OVP comparator output goes high and the circuit latches as the high-side MOSFET driver OFF and the low-side MOSFET driver ON.

Also, TPS51116 monitors VDDQSNS voltage directly and if it becomes greater than 4 V TPS51116 turns off the high-side MOSFET driver. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 32 cycles, TPS51116 latches OFF both top and low-side MOSFETs. This function is enabled after 1007 cycles of SMPS operation to ensure startup.

V5IN Undervoltage Lockout (UVLO) Protection

TPS51116 has 5-V supply undervoltage lockout protection (UVLO). When the V5IN voltage is lower than UVLO threshold voltage, SMPS, VTTLDO and VTTREF are shut off. This is a non-latch protection.

V5IN Input Capacitor

Add a ceramic capacitor with a value between 1.0 µF and 4.7 µF placed close to the V5IN pin to stabilize 5 V from any parasitic impedance from the supply.

Thermal Shutdown

TPS51116 monitors the temperature of itself. If the temperature exceeds the threshold value, 160°C (typ), SMPS, VTTLDO and VTTREF are shut off. This is a non-latch protection and the operation is resumed when the device is cooled down by about 10°C.

APPLICATION INFORMATION

Loop Compensation and External Parts Selection

Current Mode Operation

A buck converter using TPS51116 current mode operation can be partitioned into three portions, a voltage divider, an error amplifier and a switching modulator. By linearizing the switching modulator, we can derive the transfer function of the whole system. Because current mode scheme directly controls the inductor current, the modulator can be linearized as shown in Figure 4.

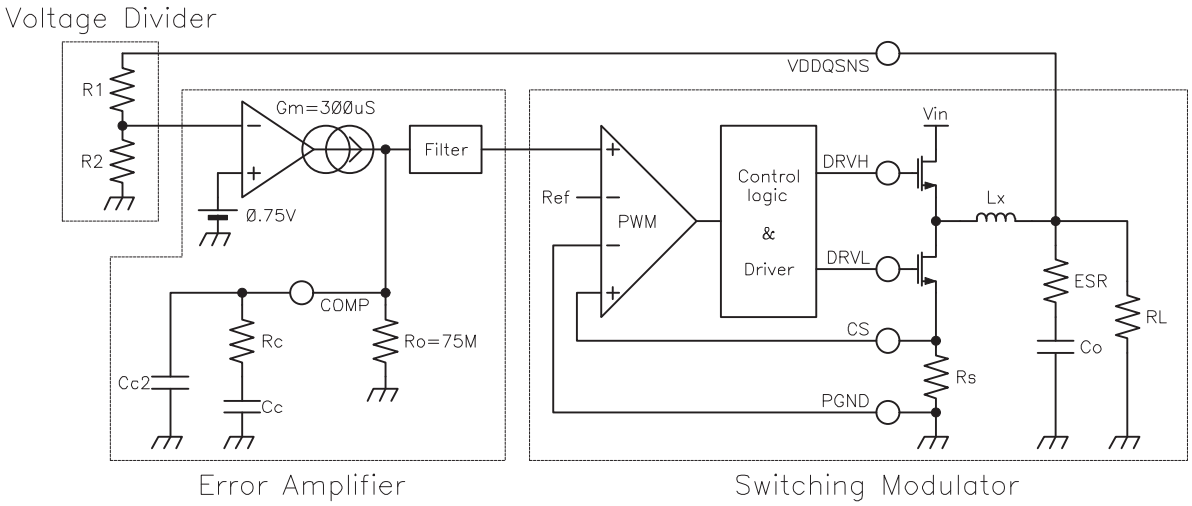


Figure 4. Linearizing the Modulator

Here, the inductor is located inside the local feedback loop and its inductance does not appear in the small signal model. As a result, a modulated current source including the power inductor can be modeled as a current source with its transconductance of $1/R_S$ and the output capacitor represent the modulator portion. This simplified model is applicable in the frequency space up to approximately a half of the switching frequency. One note is, although the inductance has no influence to small signal model, it has influence to the large signal model as it limits slew rate of the current source. This means the buck converter's load transient response, one of the large signal behaviors, can be improved by using smaller inductance without affecting the loop stability.

Total open loop transfer function of the whole system is given by Equation 6.

$$H(s) = H_1(s) \times H_2(s) \times H_3(s) \tag{6}$$

Assuming RL>>ESR, R_O>>R_C and C_C>>C_{C2}, each transfer function of the three blocks is shown starting with Equation 7.

$$H_1(s) = \frac{R2}{(R2 + R1)} \tag{7}$$

$$H_2(s) = -gm \times \frac{R_O\left(1 + s \times C_C \times R_C\right)}{\left(1 + s \times C_C \times R_O\right)\left(1 + s \times C_{C2} \times R_C\right)} \tag{8}$$

$$H_3(s) = \frac{(1 + s \times C_O \times ESR)}{\left(1 + s \times C_O \times RL\right)} \times \frac{RL}{R_S} \tag{9}$$

There are three poles and two zeros in H(s). Each pole and zero is given by the following five equations.

$$\omega_{P1} = \frac{1}{\left(C_C \times R_O\right)} \tag{10}$$

$$\omega_{P2} = \frac{1}{\left(C_O \times RL\right)} \tag{11}$$

$$\omega_{P3} = \frac{1}{\left(C_{C2} \times R_C\right)} \quad (12)$$

$$\omega_{Z1} = \frac{1}{\left(C_C \times R_C\right)} \quad (13)$$

$$\omega_{Z2} = \frac{1}{\left(C_O \times ESR\right)} \quad (14)$$

Usually, each frequency of those poles and zeros is lower than the 0 dB frequency, f_0. However, the f_0 should be kept under 1/3 of the switching frequency to avoid effect of switching circuit delay. The f_0 is given by Equation 15.

$$f_0 = \frac{1}{2\pi} \times \frac{R1}{R1 + R2} \times \frac{gm}{C_O} \times \frac{R_C}{R_S} = \frac{1}{2\pi} \times \frac{0.75}{V_{OUT}} \times \frac{gm}{C_O} \times \frac{R_C}{R_S} \quad (15)$$

Based on small signal analysis above, the external components can be selected by following manner.

1. **Choose the inductor.** The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current.

$$L = \frac{1}{I_{IND(ripple)} \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{2}{I_{OUT(max)} \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (16)$$

   The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated as shown in Equation 17.

$$I_{IND(peak)} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{L \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (17)$$

2. **Choose rectifying (bottom) MOSFET**. When $R_{DS(on)}$ sensing scheme is selected, the rectifying MOSFET's on-resistance is used as this R_S so that lower $R_{DS(on)}$ does not always promise better performance. In order to clearly detect inductor current, minimum R_S recommended is to give 15 mV or larger ripple voltage with the inductor ripple current. This promises smooth transition from CCM to DCM or vice versa. Upper side of the $R_{DS(on)}$ is of course restricted by the efficiency requirement, and usually this resistance affects efficiency more at high-load conditions. When using external resistor current sensing, there is no restriction for low $R_{DS(on)}$. However, the current sensing resistance R_S itself affects the efficiency
3. **Choose output capacitor(s).** When organic semiconductor capacitors (OS-CON) or specialty polymer capacitors (SP-CAP) are used, ESR to achieve required ripple value at stable state or transient load conditions determines the amount of capacitor(s) need, and capacitance is then enough to satisfy stable operation. The peak-to-peak ripple value can be estimated by ESR times the inductor ripple current for stable state, or ESR times the load current step for a fast transient load response. When ceramic capacitor(s) are used, the ESR is usually small enough to meet ripple requirement. In contrast, transient undershoot and overshoot driven by output capacitance becomes the key factor in determining the capacitor(s) required.
4. **Determine f_0 and calculate R_C** using Equation 18. Note that higher R_C shows faster transient response in cost of unstableness. If the transient response is not enough even with high R_C value, try increasing the out put capacitance. Recommended f_0 is $f_{OSC}/4$. Then R_C can be derived by Equation 19.

$$R_C \le 2\pi \times f_0 \times \frac{V_{OUT}}{0.75} \times \frac{C_O}{gm} \times R_S \quad (18)$$

$$R_C = 2.8 \times V_{OUT} \times C_O\,[\mu F] \times R_S\,[m\Omega] \quad (19)$$

5. **Calculate C_{C2}** . Purpose of this capacitance is to cancel zero caused by ESR of the output capacitor. When ceramic capacitor(s) are used, no need for C_{C2}.

$$\omega_{z2} = \frac{1}{\left(C_O \times ESR\right)} = \omega_{p3} = \frac{1}{\left(C_{C2} \times R_C\right)} \quad (20)$$

$$C_{C2} = \frac{C_O \times ESR}{R_C} \quad (21)$$

6. **Calculate C_C.** The purpose of C_C is to cut DC component to obtain high DC feedback gain. However, as it causes phase delay, another zero to cancel this effect at f_0 frequency is need. This zero, ωz1, is determined by Cc and Rc. Recommended ωz1 is 10 times lower to the f_0 frequency.

$$f_{z1} = \frac{1}{2\pi \times C_C \times R_C} = \frac{f_0}{10} \quad (22)$$

7. **When using adjustable mode, determine the value of R1 and R2.** .

$$R1 = \frac{V_{OUT} - 0.75}{0.75} \times R2 \quad (23)$$

D-CAP™ Mode Operation

A buck converter system using D-CAP™ Mode can be simplified as below.

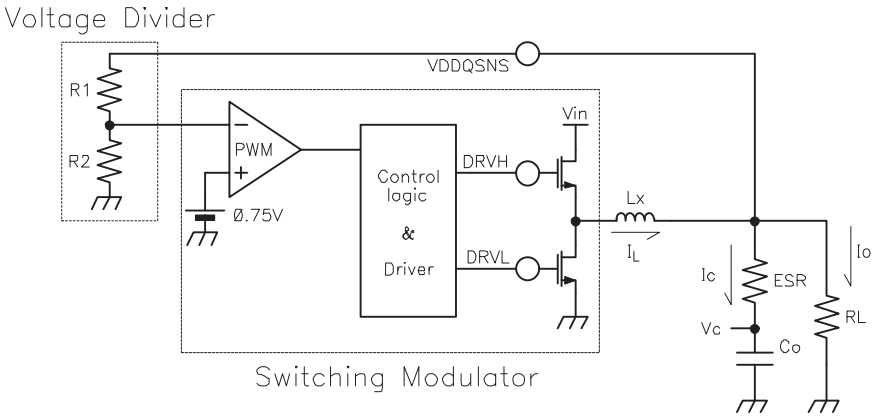


Figure 5. Linearizing the Modulator

The PWM comparator compares the VDDQSNS voltage divided by R1 and R2 with internal reference voltage, and determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator is high enough to keep the voltage at the beginning of each on cycle (or the end of off cycle) substantially constant. The DC output voltage may have line regulation due to ripple amplitude that slightly increases as the input voltage increase.

For the loop stability, the 0-dB frequency, f_0, defined below need to be lower than 1/3 of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_O} \le \frac{f_{SW}}{3} \quad (24)$$

As f_0 is determined solely by the output capacitor's characteristics, loop stability of D-CAP™ mode is determined by the capacitor's chemistry. For example, specialty polymer capacitors (SP-CAP) have C_O in the order of several 100 µF and ESR in range of 10 mΩ. These makes f_0 in the order of 100 kHz or less and the loop is then stable. However, ceramic capacitors have f_0 at more than 700 kHz, which is not suitable for this operational mode.

Although D-CAP™ mode provides many advantages such as ease-of-use, minimum external components configuration and extremely short response time, due to not employing an error amplifier in the loop, sufficient amount of feedback signal needs to be provided by external circuit to reduce jitter level.

The required signal level is approximately 15 mV at comparing point. This gives V_{RIPPLE} = (V_{OUT}/0.75) x 15 (mV) at the output node. The output capacitor's ESR should meet this requirement.

The external components selection is much simple in D-CAP™ mode.

1. **Choose inductor.** This section is the same as the current mode. Please refer to the instructions in the *Current Mode Operation* section.
2. **Choose output capacitor(s).**Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended. Determine ESR to meet required ripple voltage above. A quick approximation is shown in

Equation 25.

$$ESR = \frac{V_{OUT} \times 0.015}{I_{RIPPLE} \times 0.75} \approx \frac{VOUT}{I_{OUT(max)}} \times 60\ [m\Omega] \quad (25)$$

Thermal Design

Primary power dissipation of TPS51116 is generated from VTT regulator. VTT current flow in both source and sink directions generate power dissipation from the part. In the source phase, potential difference between VLDOIN and VTT times VTT current becomes the power dissipation, W_{DSRC}.

$$W_{DSRC} = \left(V_{VLDOIN} - V_{VTT}\right) \times I_{VTT} \quad (26)$$

In this case, if VLDOIN is connected to an alternative power supply lower than VDDQ voltage, power loss can be decreased.

For the sink phase, VTT voltage is applied across the internal LDO regulator, and the power dissipation, W_{DSNK}, is calculated by Equation 27:

$$W_{DSNK} = V_{VTT} \times I_{VTT} \quad (27)$$

Because this device does not sink AND source the current at the same time and I_{VTT} varies rapidly with time, actual power dissipation need to be considered for thermal design is an average of above value. Another power consumption is the current used for internal control circuitry from V5IN supply and VLDOIN supply. V5IN supports both the internal circuit and external MOSFETs drive current. The former current is in the VLDOIN supply can be estimated as 1.5 mA or less at normal operational conditions.

These powers need to be effectively dissipated from the package. Maximum power dissipation allowed to the package is calculated by Equation 28,

$$W_{PKG} = \frac{T_{J(max)} - T_{A(max)}}{\theta_{JA}} \quad (28)$$

where

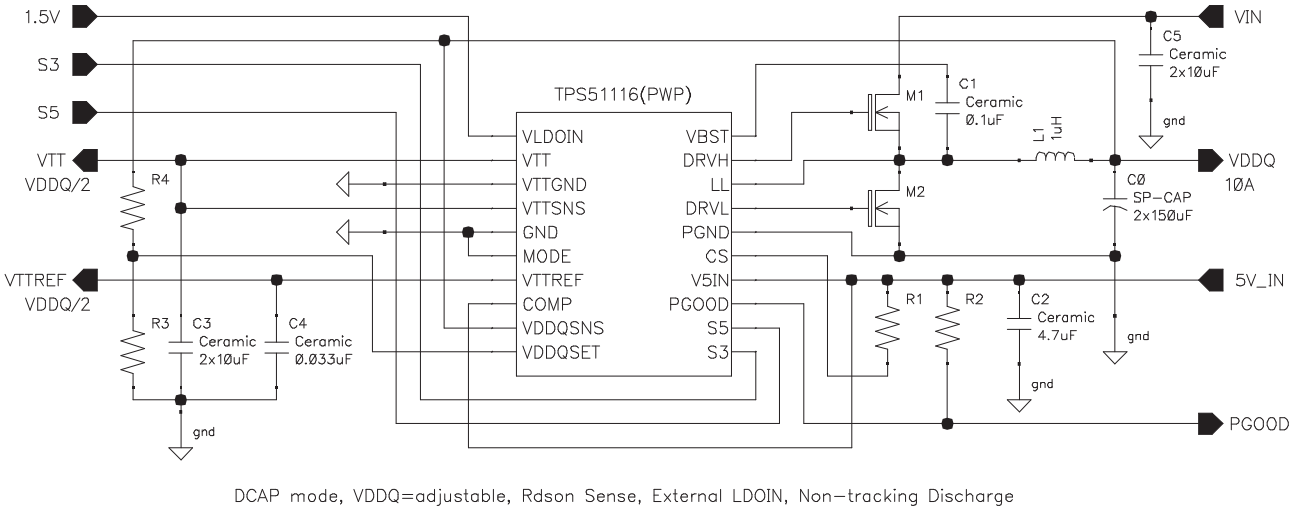
- $T_{J(max)}$ is 150°C
- $T_{A(max)}$ is the maximum ambient temperature in the system
- θ_{JA} is the thermal resistance from the silicon junction to the ambient

This thermal resistance strongly depends on the board layout. TPS51116 is assembled in a thermally enhanced PowerPAD™ package that has exposed die pad underneath the body. For improved thermal performance, this die pad needs to be attached to ground trace via thermal land on the PCB. This ground trace acts as a heat sink/spread. The typical thermal resistance, 41.2°C/W, is achieved based on a 6.5 mm × 3.4 mm thermal land with eight vias without air flow. It can be improved by using larger thermal land and/or increasing vias number. Further information about PowerPAD™ and its recommended board layout is described in (SLMA002). This document is available at http:\\www.ti.com.

Layout Considerations

Certain points must be considered before designing a layout using the TPS51116.

- PCB trace defined as LL node, which connects to source of switching MOSFET, drain of rectifying MOSFET and high-voltage side of the inductor, should be as short and wide as possible.
- Consider adding a small snubber circuit, consisting of a 3-Ω resitor and a 1-nF capacitor, between LL and PGND in case a high-frequency surge is observed on the LL voltage waveform.
- All sensitive analog traces such as VDDQSNS, VTTSNS and CS should placed away from high-voltage switching nodes such as LL, DRVL or DRVH nodes to avoid coupling.
- VLDOIN should be connected to VDDQ output with short and wide trace. If different power source is used for VLDOIN, an input bypass capacitor should be placed to the pin as close as possible with short and wide connection.
- The output capacitor for VTT should be placed close to the pin with short and wide connection in order to avoid additional ESR and/or ESL of the trace.
- VTTSNS should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current power line and is strongly recommended to avoid additional ESR and/or ESL. If it is needed to sense the voltage of the point of the load, it is recommended to attach the output capacitor(s) at that point. Also, it is recommended to minimize any additional ESR and/or ESL of ground trace between GND pin and the output capacitor(s).
- Consider adding LPF at VTTSNS when the ESR of the VTT output capacitor(s) is larger than 2 mΩ.
- VDDQSNS can be connected separately from VLDOIN. Remember that this sensing potential is the reference voltage of VTTREF. Avoid any noise generative lines.
- Negative node of VTT output capacitor(s) and VTTREF capacitor should be tied together by avoiding common impedance to the high current path of the VTT source/sink current.
- GND (Signal GND) pin node represents the reference potential for VTTREF and VTT outputs. Connect GND to negative nodes of VTT capacitor(s), VTTREF capacitor and VDDQ capacitor(s) with care to avoid additional ESR and/or ESL. GND and PGND (power ground) should be connected together at a single point.
- PGND is the return path for rectifying MOSFET gate drive. Use 0.65 mm (25mil) or wider trace. Connect to source of rectifying MOSFET with shortest possible path.
- The trace from the CS pin should avoid high-voltage switching nodes such as those for LL, VBST, DRVH, DRVL or PGOOD.
- In order to effectively remove heat from the package, prepare thermal land and solder to the package's thermal pad. Wide trace of the component-side copper, connected to this thermal land, helps heat spreading. Numerous vias with a 0.33-mm diameter connected from the thermal land to the internal/solder-side ground plane(s) should be used to help dissipation. **Do NOT connect PGND to this thermal land underneath the package.**



DCAP mode, VDDQ=adjustable, Rdson Sense, External LDOIN, Non−tracking Discharge

Figure 6. D-CAP™ Mode

Table 4. D-CAP™ Mode Schematic Components

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
R1	5.1 kΩ	-	
R2	100 kΩ	-	
R3	75 kΩ	-	
R4	(100 × V_{VDDQ} – 75) kΩ	-	
R5	5.1 Ω		
M1	30 V, 13 mΩ	International Rectifier	IRF7821
M2	30 V, 5 mΩ	International Rectifier	IRF7832

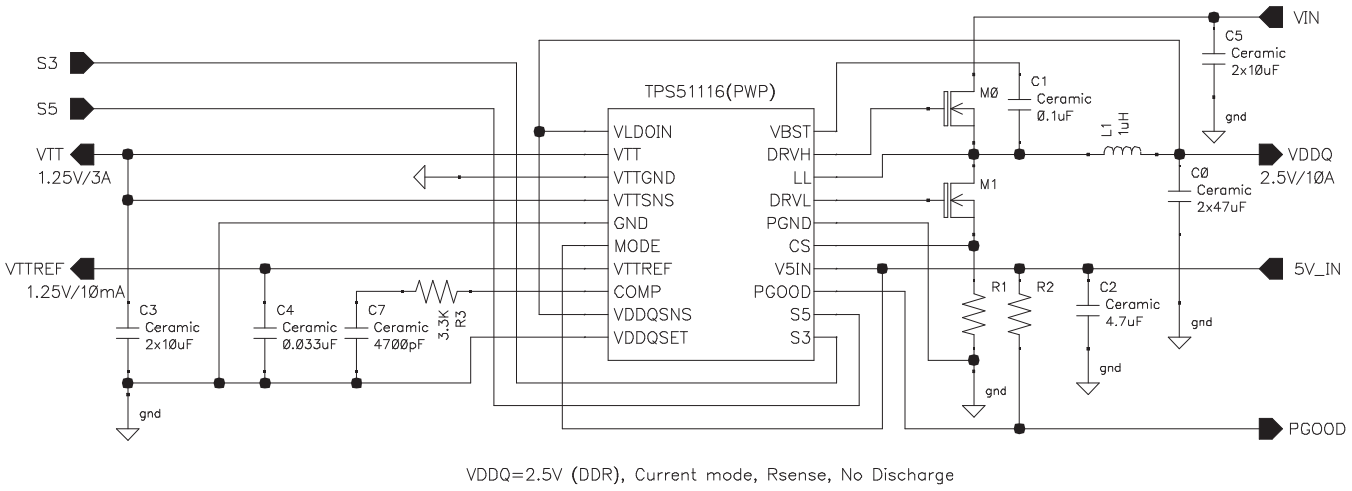


Figure 7. Current Mode

Table 5. Current Mode Schematic Components

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
R1	6 mΩ, 1%	Vishay	WSL-2521 0.006
R2	100 kΩ	-	-
R5	5.1 Ω		
M0	30 V, 13 mΩ	International Rectifier	IRF7821
M1	30 V, 5 mΩ	International Rectifier	IRF7832

TYPICAL CHARACTERISTICS

All data in the following graphs are measured from the PWP packaged device.

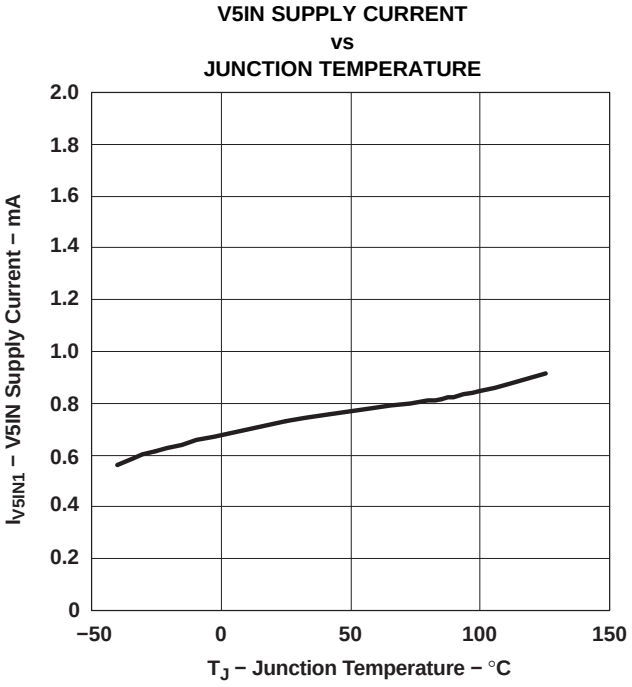


Figure 8.

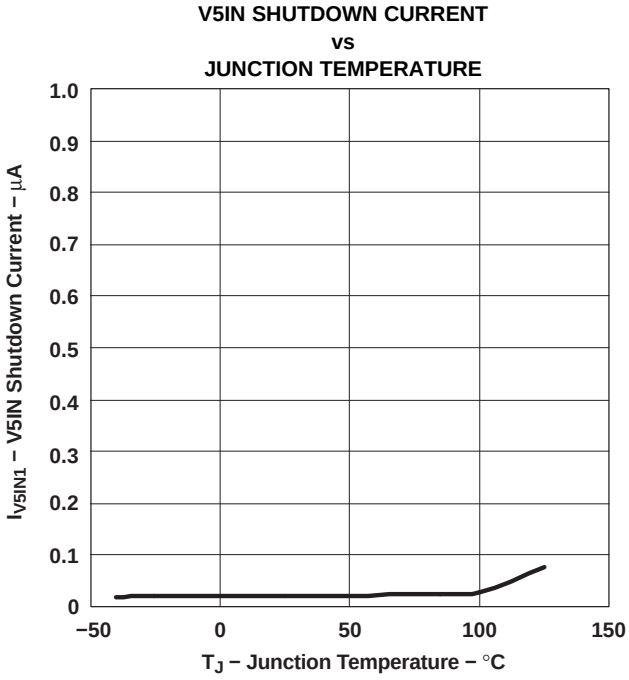


Figure 9.

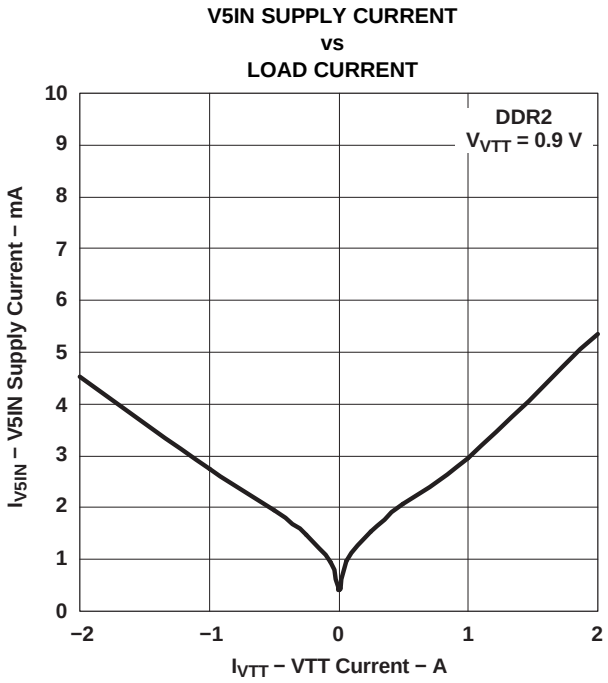


Figure 10.

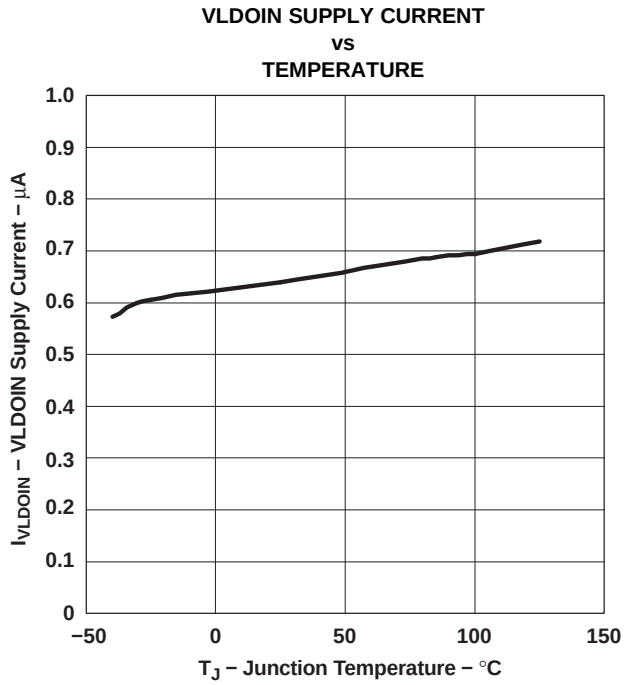


Figure 11.

TYPICAL CHARACTERISTICS (continued)

CS CURRENT
vs
JUNCTION TEMPERATURE

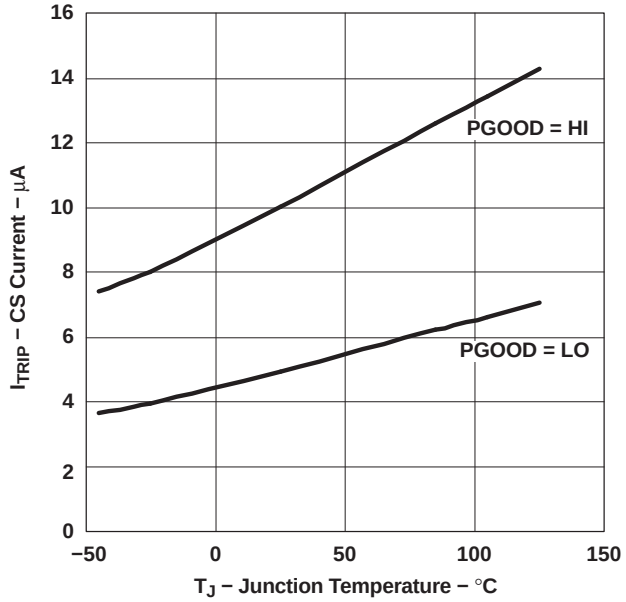


Figure 12.

VDDQ DISCHARGE CURRENT
vs
JUNCTION TEMPERATURE

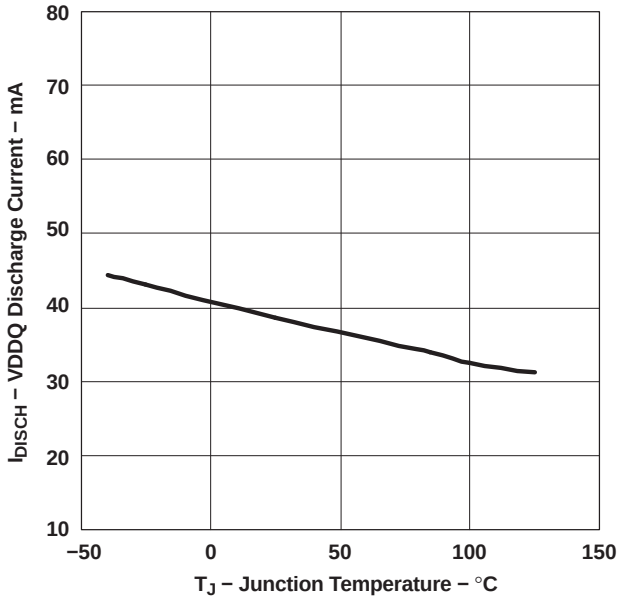


Figure 13.

VTT DISCHARGE CURRENT
vs
JUNCTION TEMPERATURE

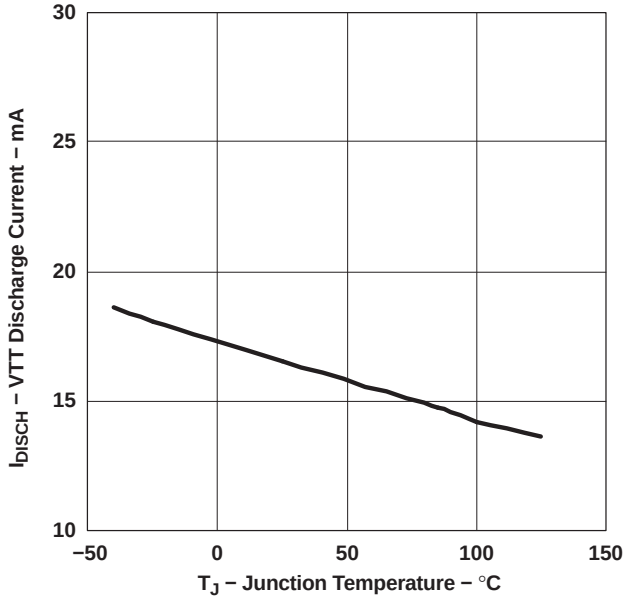


Figure 14.

OVERVOLTAGE AND UNDERVOLTAGE THRESHOLD
vs
JUNCTION TEMPERATURE

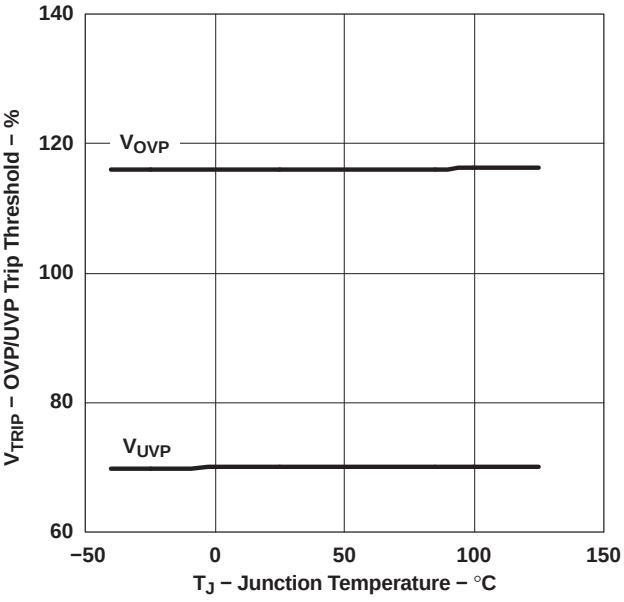


Figure 15.

TYPICAL CHARACTERISTICS (continued)

SWITCHING FREQUENCY vs INPUT VOLTAGE

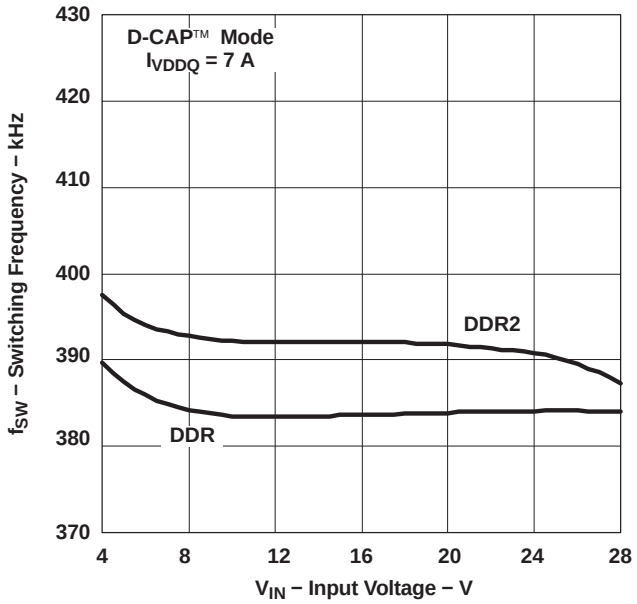


Figure 16.

SWITCHING FREQUENCY vs OUTPUT CURRENT

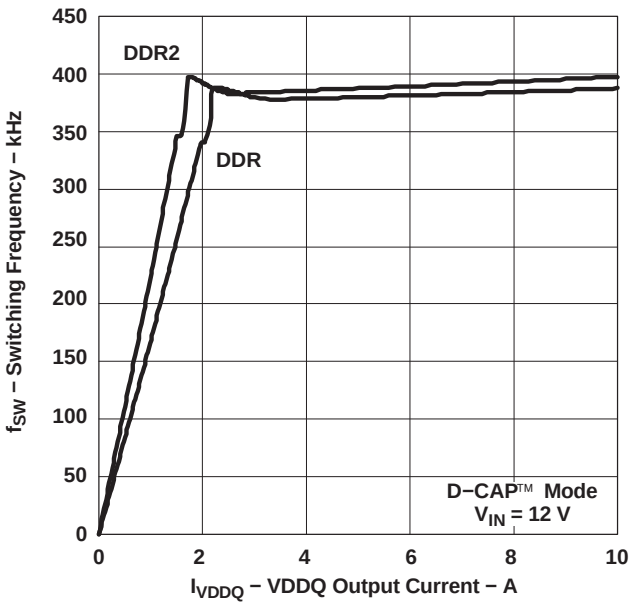


Figure 17.

VDDQ OUTPUT VOLTAGE vs OUTPUT CURRENT (DDR)

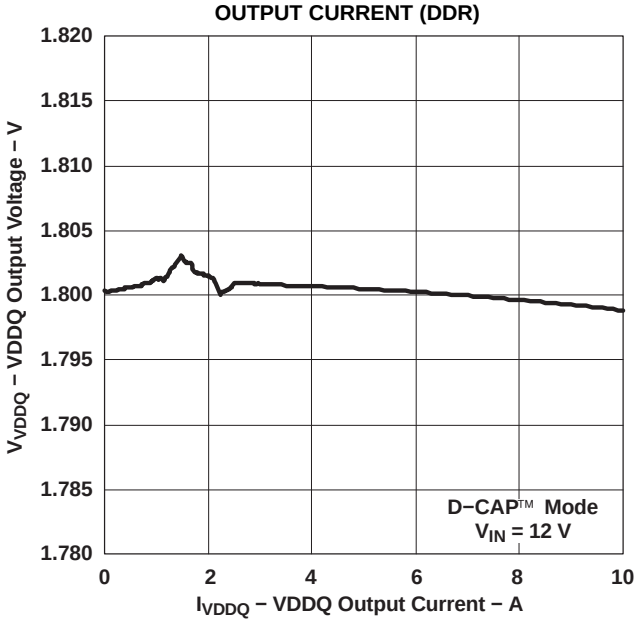


Figure 18.

VDDQ OUTPUT VOLTAGE vs INPUT VOLTAGE (DDR2)

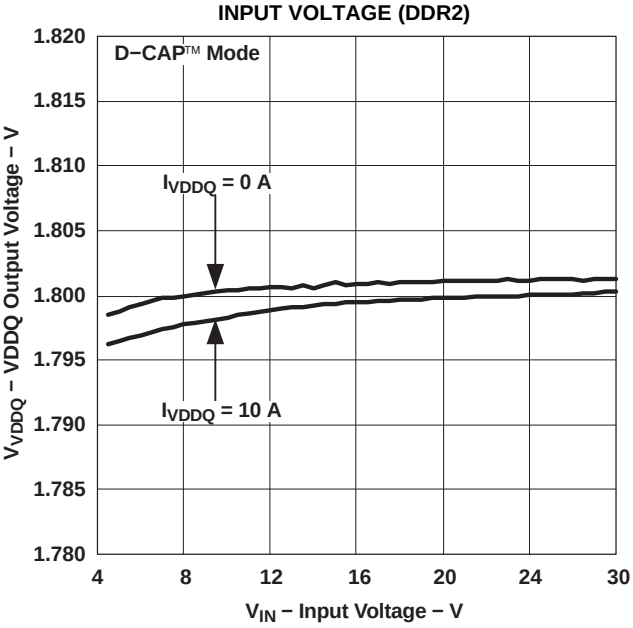


Figure 19.

TYPICAL CHARACTERISTICS (continued)

VTT OUTPUT VOLTAGE vs OUTPUT CURRENT (DDR)

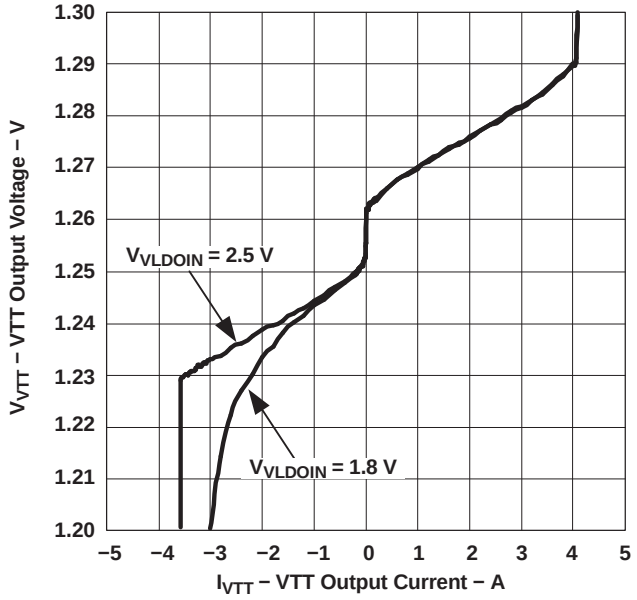


Figure 20.

VTT OUTPUT VOLTAGE vs OUTPUT CURRENT (DDR2)

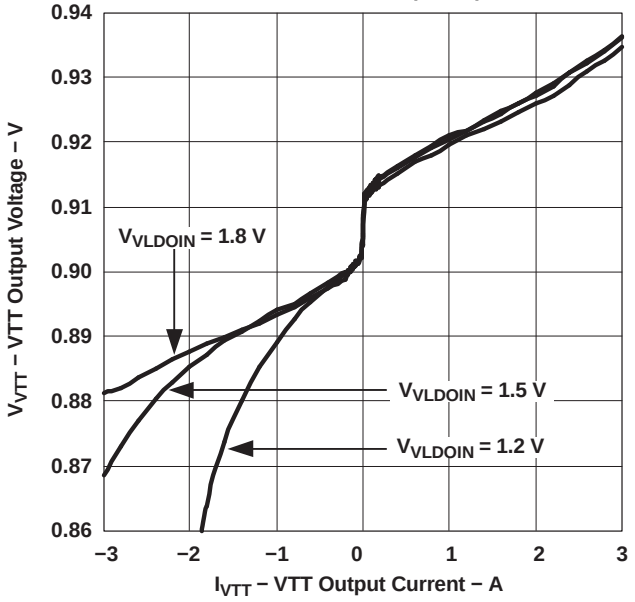


Figure 21.

VTTREF OUTPUT VOLTAGE vs OUTPUT CURRENT (DDR)

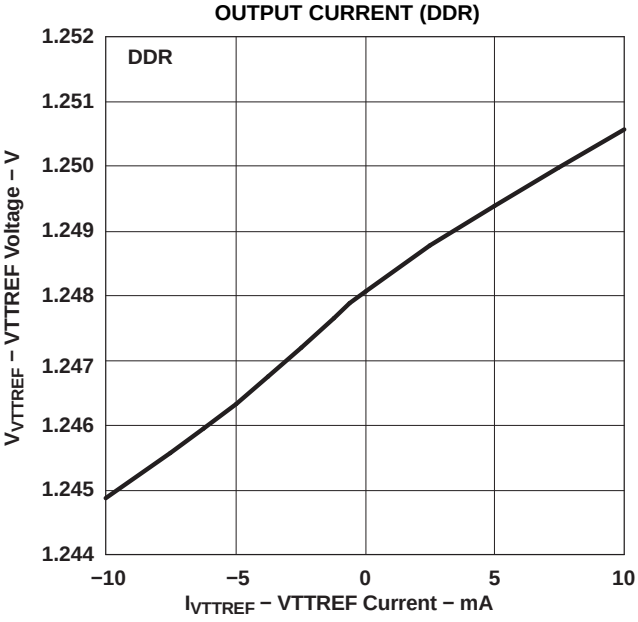


Figure 22.

VTTREF OUTPUT VOLTAGE vs OUTPUT CURRENT (DDR2)

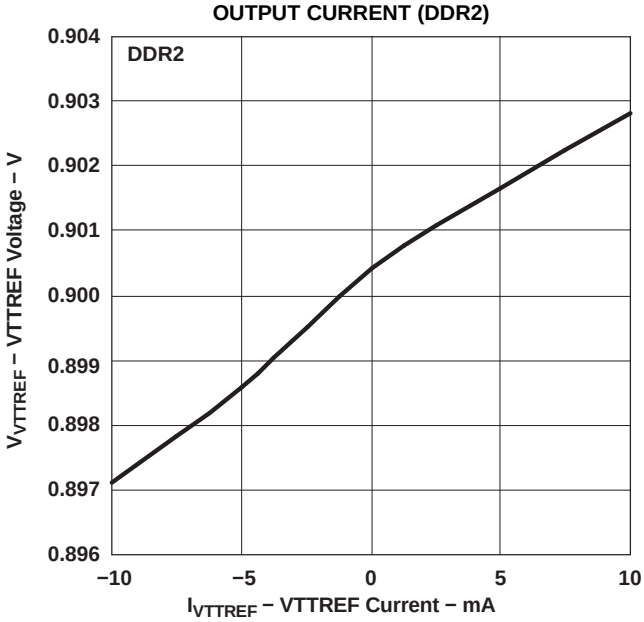


Figure 23.

TYPICAL CHARACTERISTICS (continued)

VTTREF OUTPUT VOLTAGE vs OUTPUT CURRENT (DDR3)

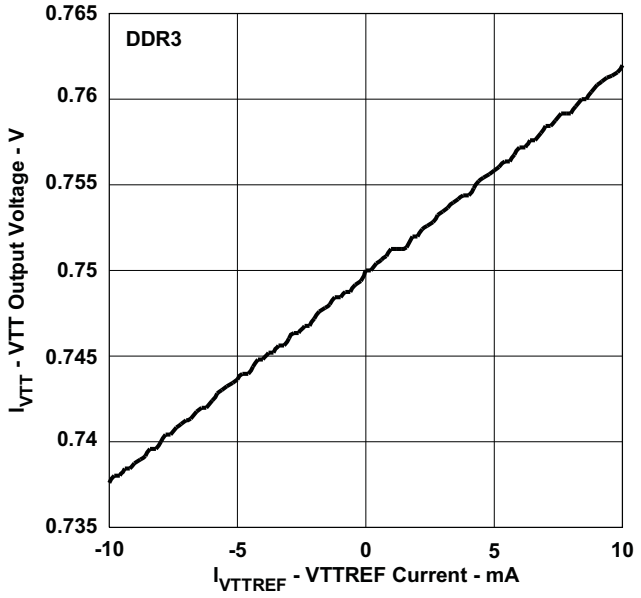


Figure 24.

VTT OUTPUT VOLTAGE vs OUTPUT CURRENT (DDR3)

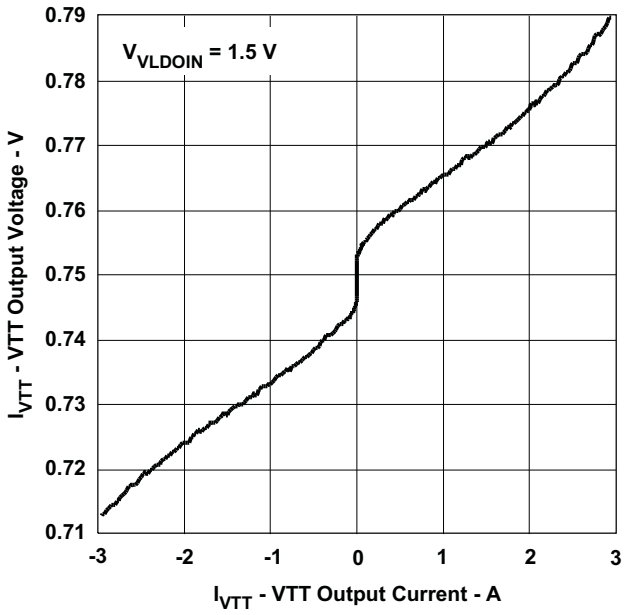


Figure 25.

VDDQ EFFICIENCY (DDR) vs VDDQ CURRENT

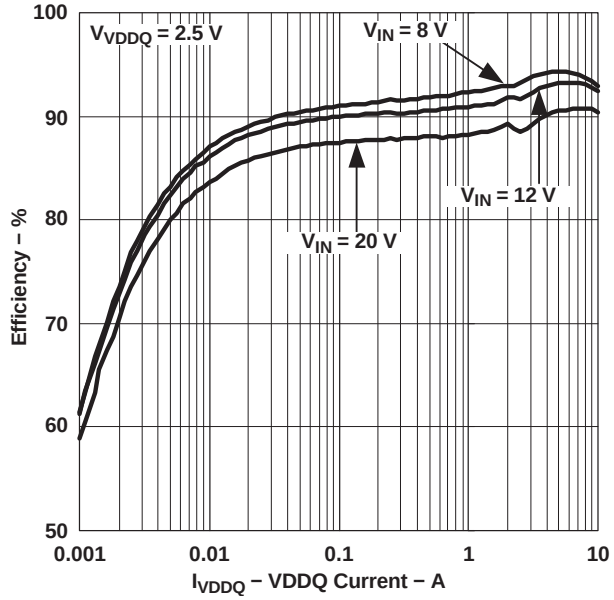


Figure 26.

VDDQ EFFICIENCY (DDR2) vs VDDQ CURRENT

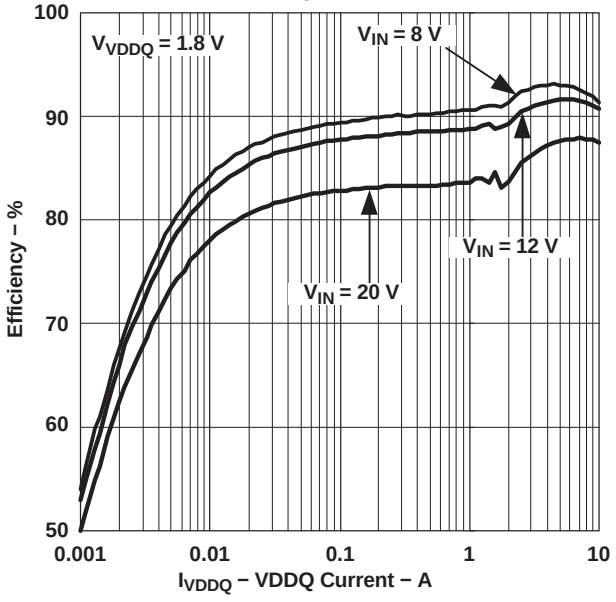
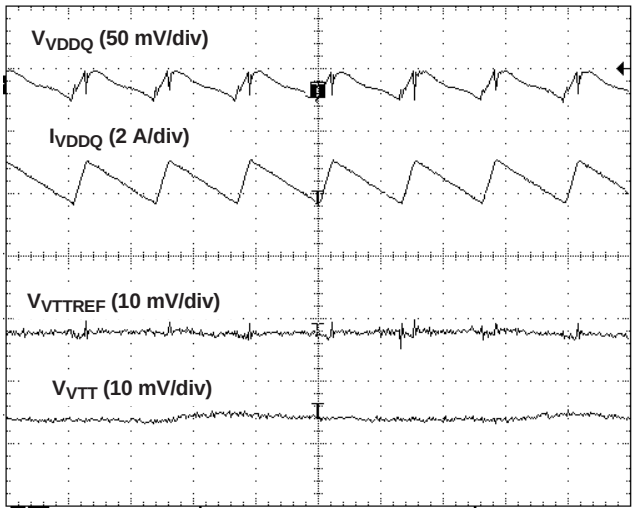


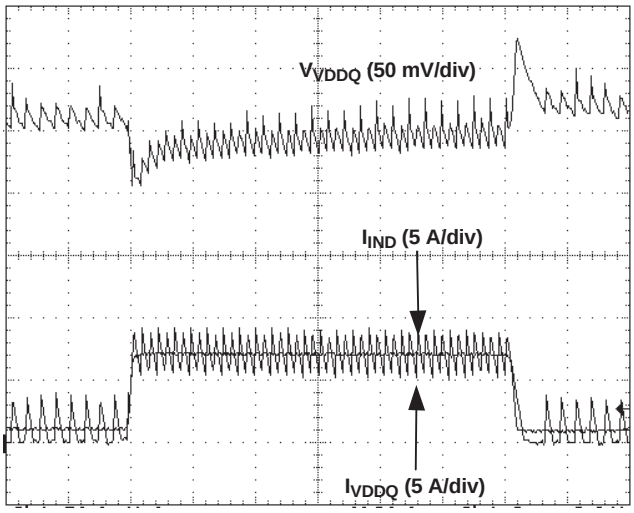
Figure 27.

TYPICAL CHARACTERISTICS (continued)



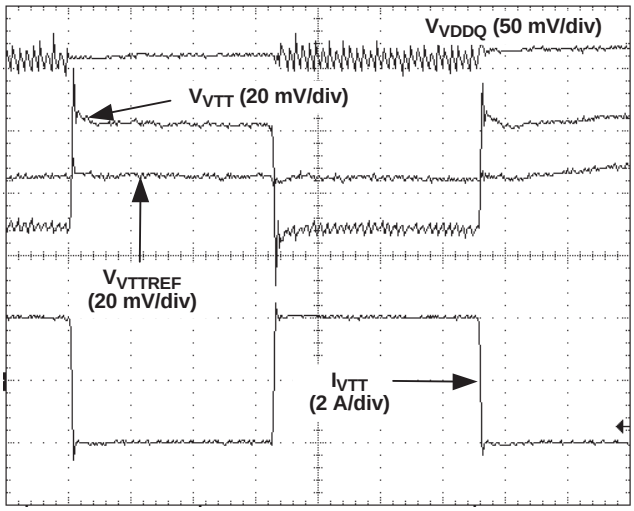
t – Time – 2 μs/div

Figure 28. Ripple Waveforms - Heavy Load Condition



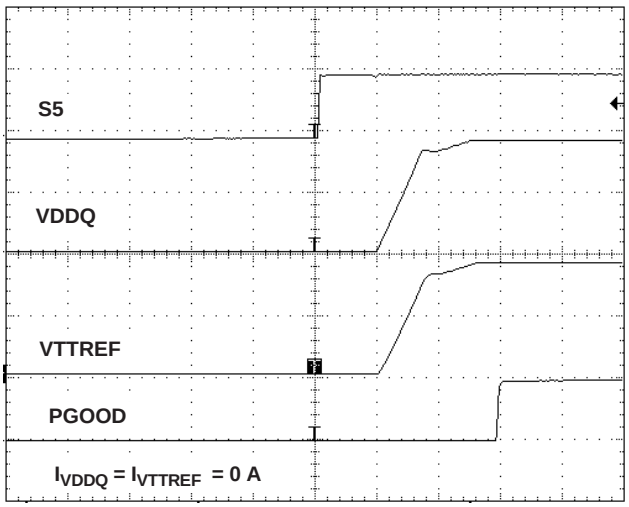
t – Time – 20 μs/div

Figure 29. VDDQ Load Transient Response



t – Time – 20 μs/div

Figure 30. VTT Load Transient Response



t – Time – 100 μs/div

Figure 31. VDDQ, VTT, and VTTREF Start-Up Waveforms

TYPICAL CHARACTERISTICS (continued)

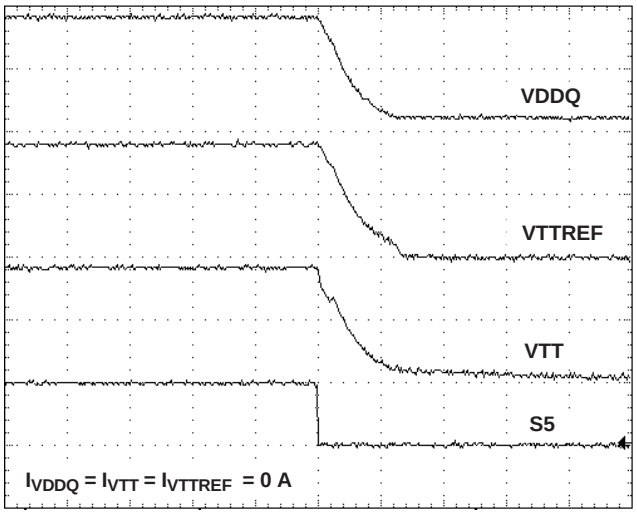


Figure 32. Soft-Start Waveforms Tracking Discharge

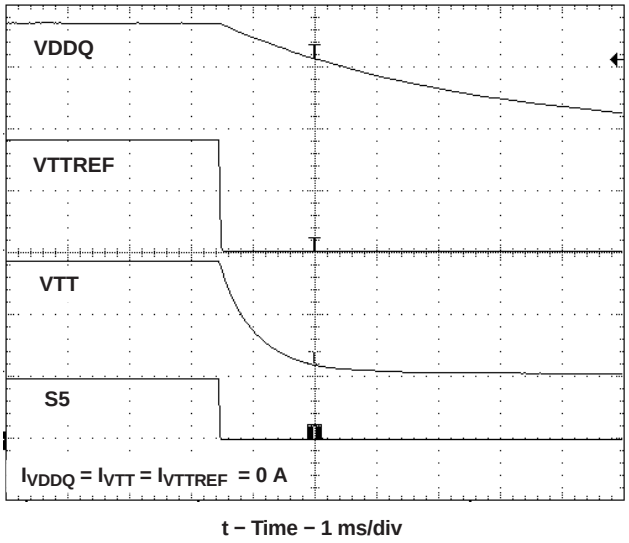


Figure 33. Soft-Stop Waveforms Non-Tracking Discharge

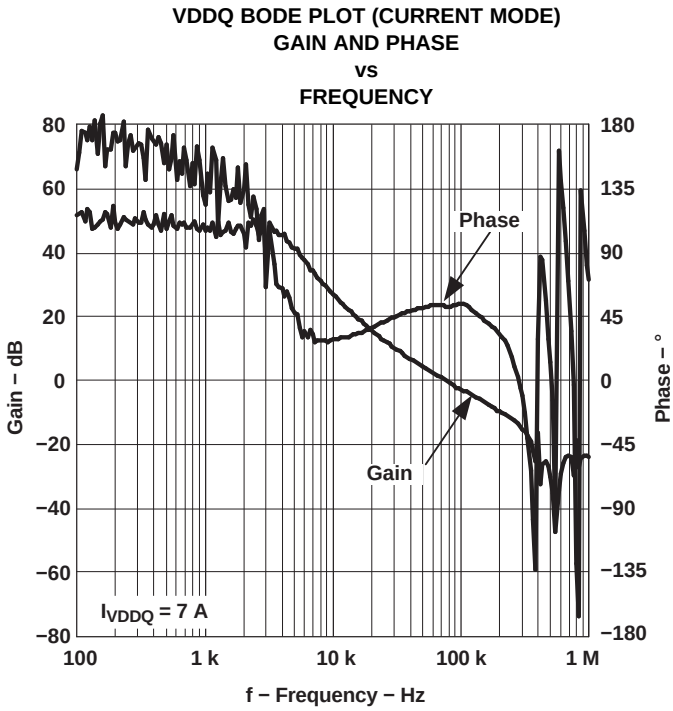


Figure 34.

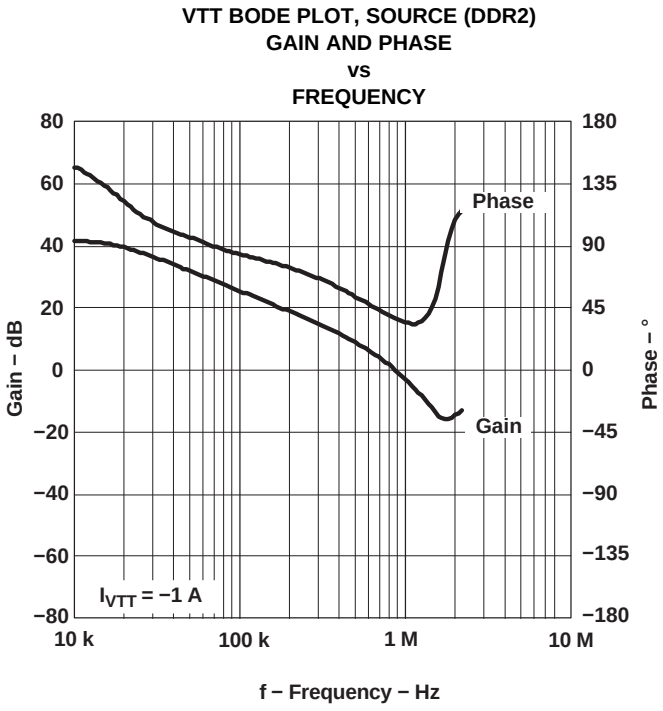


Figure 35.

TYPICAL CHARACTERISTICS (continued)

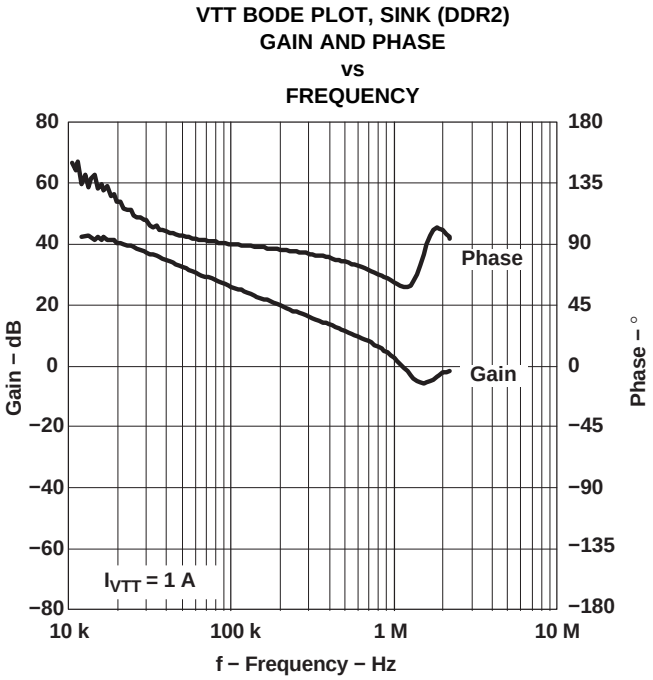


Figure 36.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51116MPWPEP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	51116M	Samples
TPS51116MPWPREP	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	51116M	Samples
V62/12602-01XE	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	51116M	Samples
V62/12602-01XE-T	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	51116M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS51116-EP :

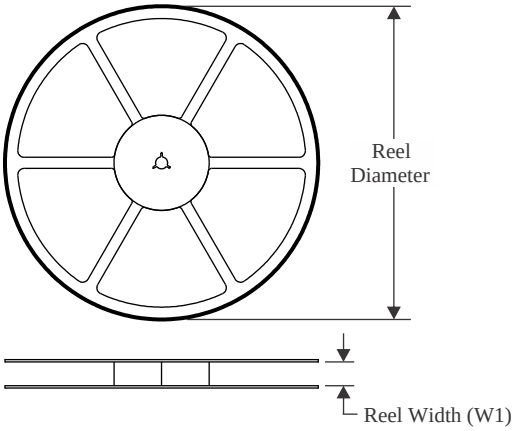
- Catalog: TPS51116

NOTE: Qualified Version Definitions:

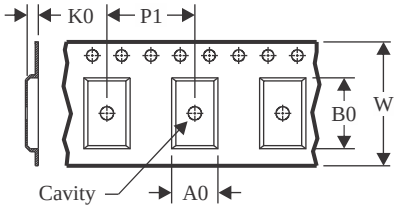
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

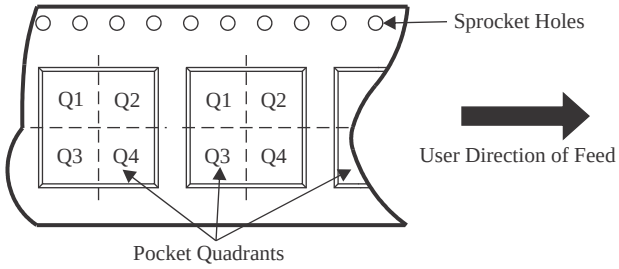


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

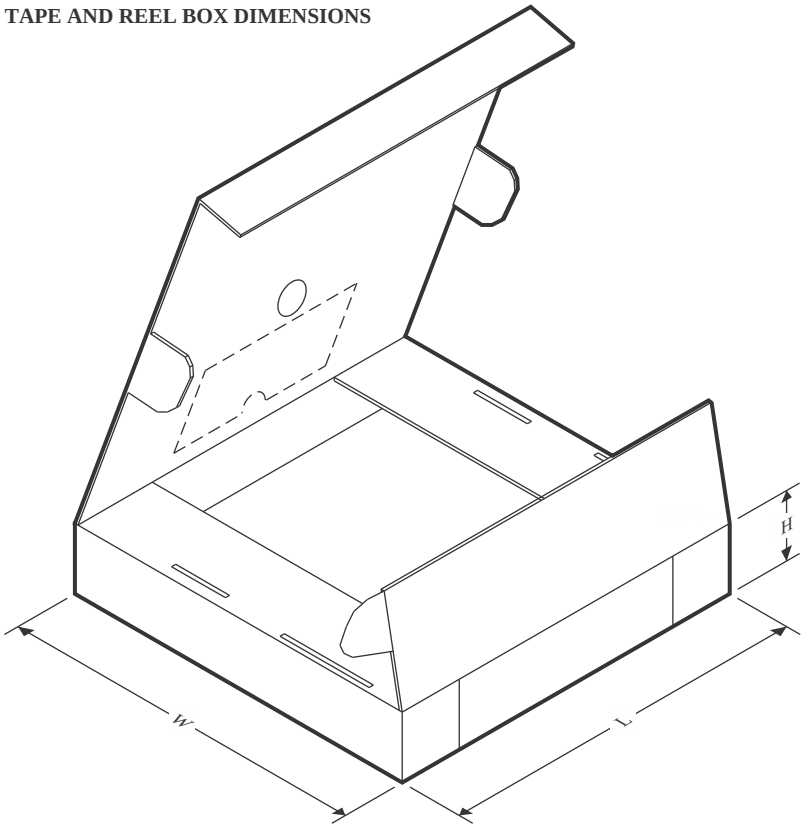
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51116MPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

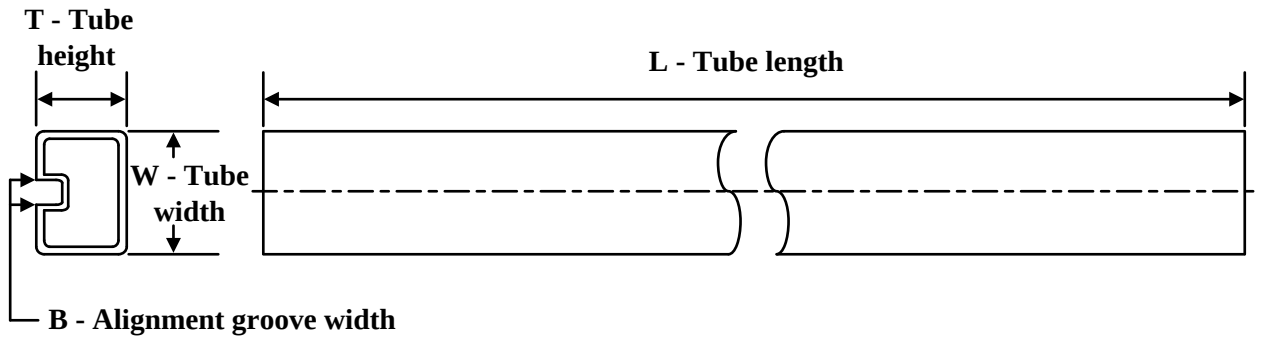
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51116MPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0

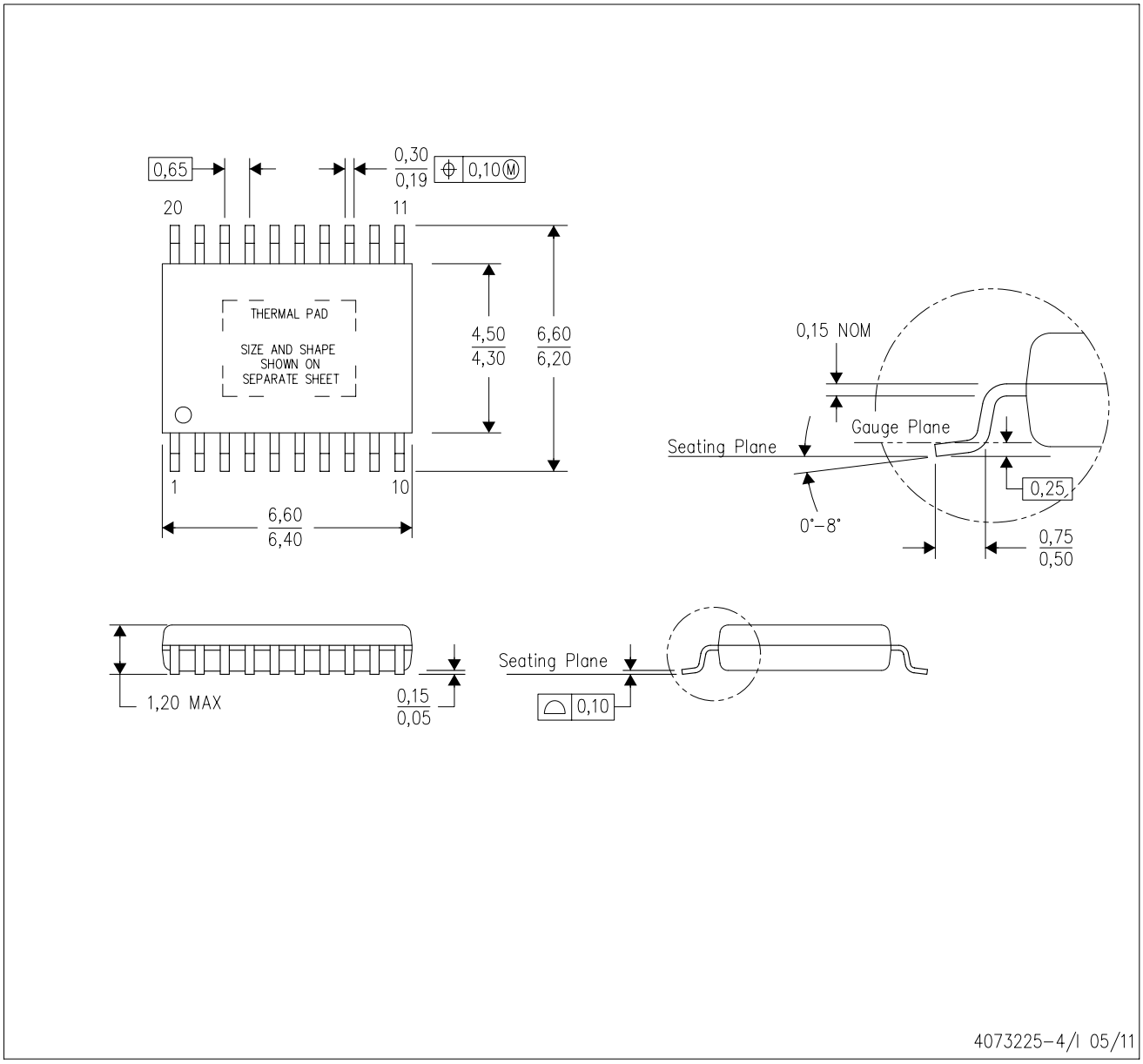
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS51116MPWPEP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
V62/12602-01XE-T	PWP	HTSSOP	20	70	530	10.2	3600	3.5

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

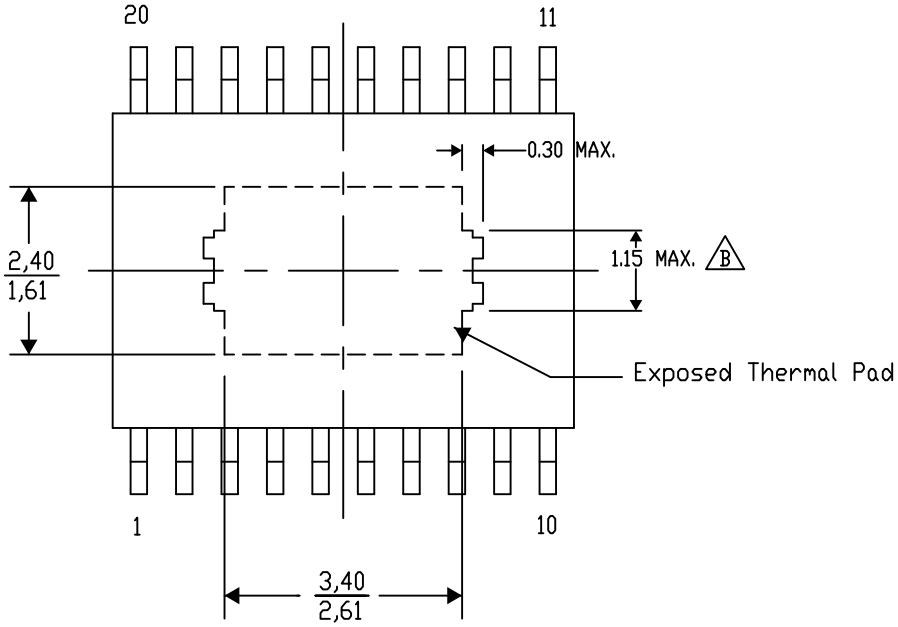
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

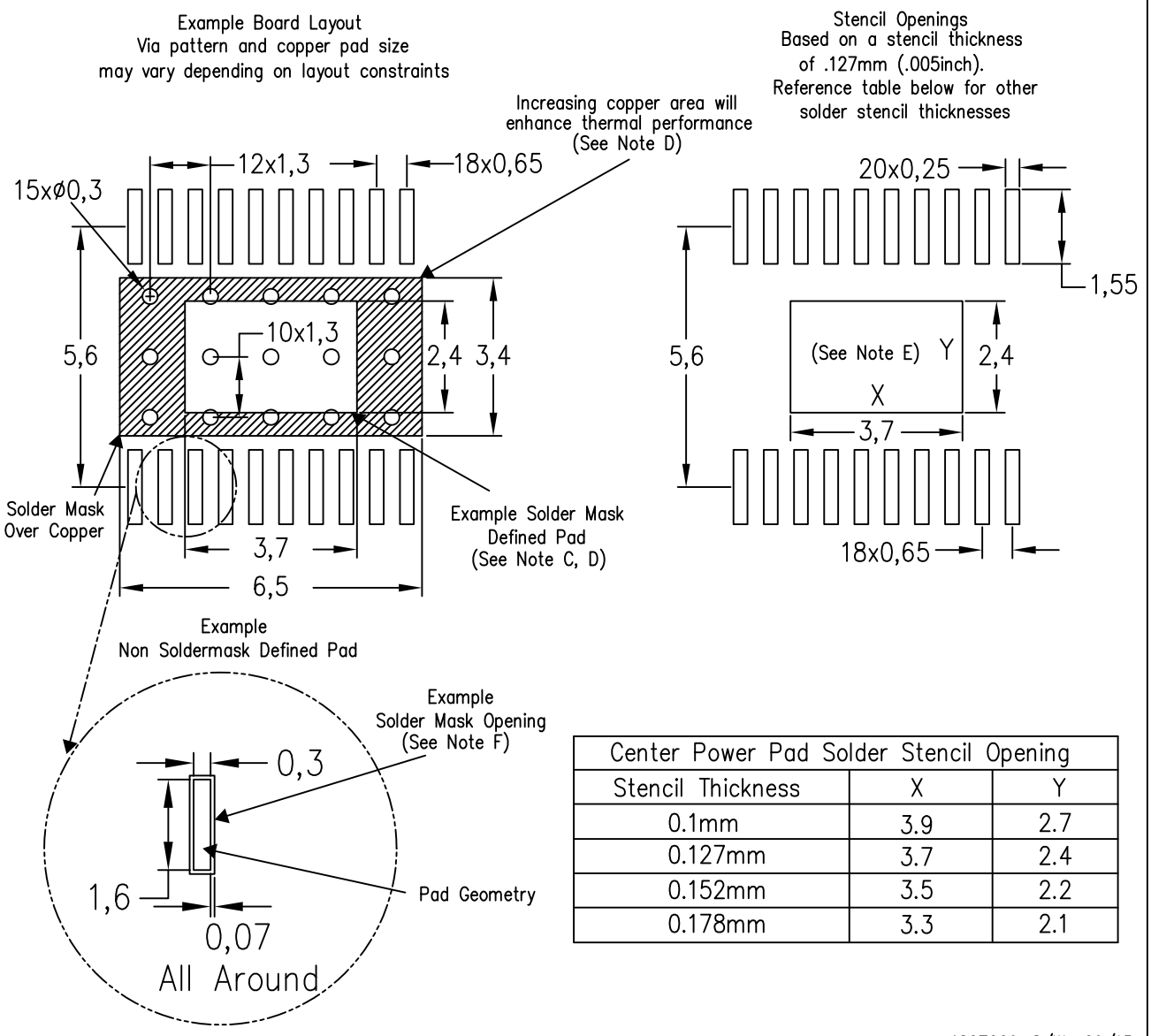
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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