TPS65036x-Q1 Automotive Camera, Radar and MCU PMIC

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with following results:
  - Device operates from 4V to 35V input supply
  - Device temperature grade 1: -40°C to +125°C
- Functional Safety -Compliant targeted
  - Developed for functional safety applications
  - Documentation to aid ISO26262 and IEC61508 system design available upon product release
  - Systematic capability and hardware integrity up to ASIL-B and SIL-2 targeted
  - Under/overvoltage monitors with Built-In Self-Test
  - Watchdog (trigger or Q&A), Error Signal Monitor
  - Temperature warning and thermal shutdown
- Wide-VIN step-down converter BUCK1
  - V_{IN} range from 4 V to 35 V
  - V_{OUT} range from 3 V to 5.5 V
  - Output current up to 2000-mA
  - 2.2-MHz switching frequency
- Two Low-VIN step-down converters BUCK2, BUCK3:
  - V_{IN} range from 3.0 V to 5.5 V
  - V_{OUT} range from 0.6 V to 3.4 V
  - Output current up to 2700-mA peak
  - 2.2-MHz or 4.4-MHz switching frequency
- One low dropout (LDO) regulator:
  - V_{IN} range from 3.0 V to 5.5 V
  - V_{OUT} range from 1.8 V to 3.4 V
  - Up to 300-mA output current
  - Low noise and high PSRR
- 3.5-mm × 3.5-mm 24-pin VQFN with wettable flanks

2 Applications

- Automotive Camera Modules
  - Surround View Camera modules
  - Rear View Camera modules
  - DMS (Driver Monitoring Systems)
  - Power Over Coax (POC) camera modules
  - E-mirror camera modules
- Automotive Radar Modules
  - Ultra-Short Range Radar
  - Kick-to-Open
  - Park Assist & Automated Parking
  - Driver Monitor Systems
  - Vehicle Occupancy Detection, Child Presence Detection (CPD)
  - Vehicle Intruder Detection
  - Seatbelt Monitoring
- Safety MCU power
  - OBC, DC/DC, Zonal controller
  - Inverter and Motor control (Traction inverter)
  - Heating & cooling (Automotive HVAC compressor module)

3 Description

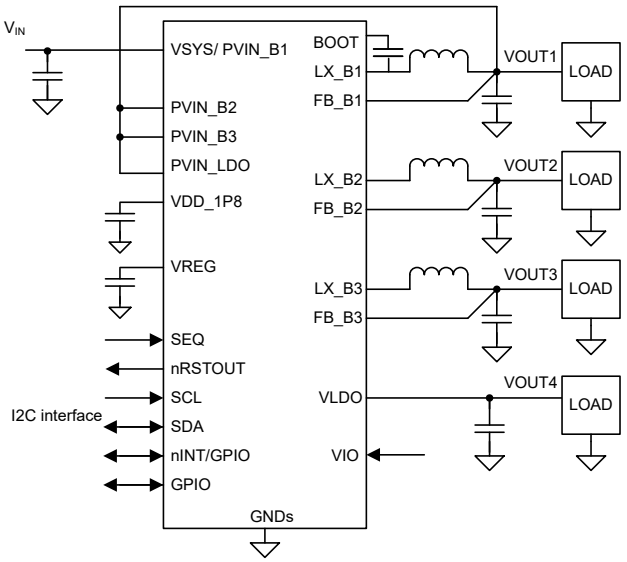
The TPS65036x-Q1 device is a highly integrated power management IC for automotive camera and radar modules and MCU power. This device combines three step-down converters and one low-dropout (LDO) regulator. The BUCK1 step-down converter has an input voltage range up to 35 V. All converters can operate in a forced fixed-frequency PWM mode or an AutoPFM mode and support optional Spread-Spectrum Modulation (SSM) for EMI reduction. The LDO can supply 300 mA and operate with an input voltage range from 3 V to 5.5 V. The TPS65036x-Q1 support Low Power Mode with control from pin or I2C.

The TPS65036x-Q1 is available in a 24-pin VQFN package (3.5 mm × 3.5 mm).

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TPS65036x-Q1	VQFN (24)	3.5 mm × 3.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



TPS65036x-Q1 Application Circuit

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4 Pin Configuration and Functions

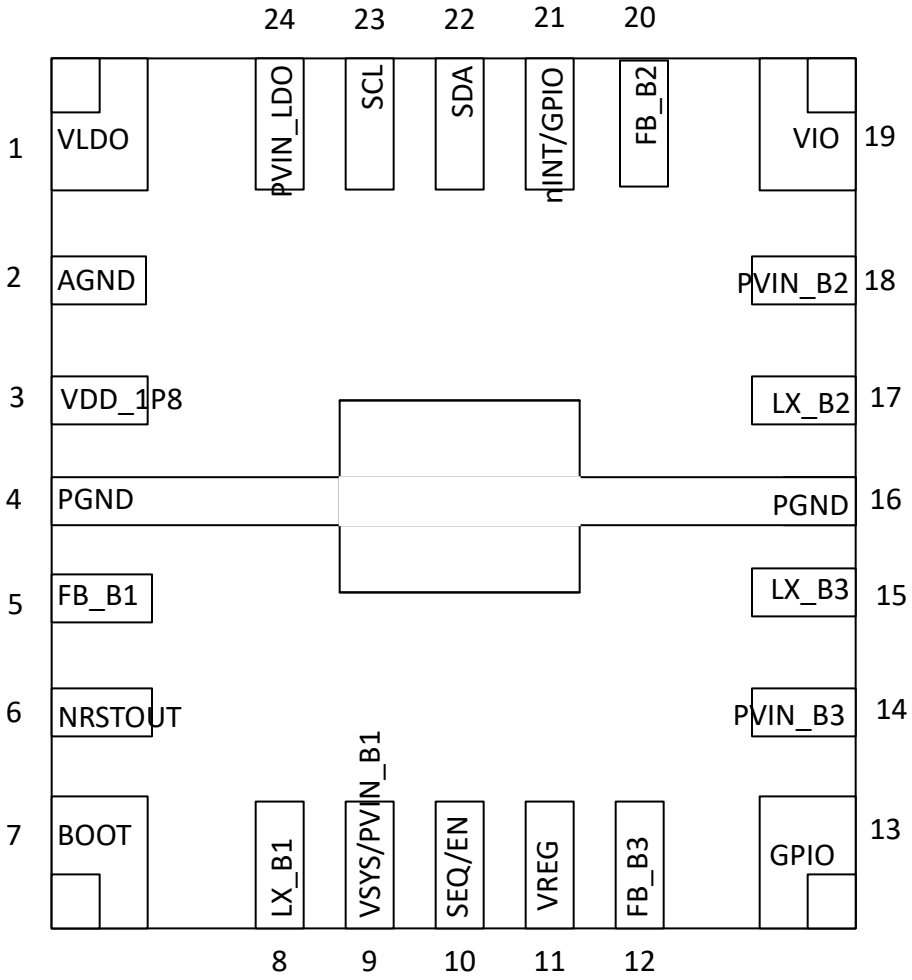

Figure 4-1. TPS65036x-Q1 24-Pin QFN (Top View)

Table 4-1. Pin Functions

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
1	VLDO	O	Analog	LDO Output Voltage. When LDO is not used, this pin can be used for monitoring an external rail. When LDO and corresponding monitoring are both deactivated in NVM pin can be left floating.	Floating
2	AGND	—	Ground	Analog Ground	Not applicable
3	VDD_1P8	PWR	Analog	Internal Reference Voltage - For Internal Use Only	Not applicable
4	PGND	—	Ground	Power Ground.	Not applicable
5	FB_B1	I	Analog	BUCK1 (Wide VinStep-Down Converter) Feedback. When BUCK1 is deactivated in NVM pin can be left floating.	Floating
6	NRSTOUT	O	Digital	Reset Output	Floating
7	BOOT	I	PWR	BOOTCAP pin for BUCK1 (Wide Vin Step-Down Converter)	Floating
8	LX_B1	—	Analog	BUCK1 (Wide Vin Step-Down Converter) Switch Node. When BUCK1 is deactivated in NVM pin can be left floating.	Floating
9	VSYS/ PVIN_B1	I	Power	Device Input Power and Input Voltage for BUCK1 (Wide Vin Step-Down Converter)	Input supply
10	SEQ	I	Digital	Enable and Sequence Control Input	Floating

ADVANCE INFORMATION

Table 4-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
11	VREG	O	Power	Gate Drive LDO Output for BUCK1 (Wide Vin Step Down Converter)	Not applicable
12	FB_B3	I	Analog	BUCK3 (Low Voltage Step-Down Converter) Feedback. When BUCK3 is not used, this pin can be used for monitoring an external rail. When BUCK3 and corresponding monitoring are both deactivated in NVM pin can be left floating.	Floating
13	GPIO	I	Digital	General Purpose Input to Sequencer.	Floating
		I	Digital	Alternative programmable function: Trigger Mode Watchdog Input	
		O	Digital	Alternative programmable function: General Purpose Output	
		I	Digital	Alternative programmable function: MCU Error Signal Monitoring Input (nERR)	
		I	Analog	Alternative programmable function: Watchdog Disable Input.	
14	PVIN_B3	I	Power	BUCK3 (Low Voltage Step-Down Converter) Input Voltage. PVIN_B2 and PVIN_B3 must be tied together and voltage applied at the same time or after the voltage on VSYS/PVIN_B1 is applied.	Input supply
15	LX_B3	O	Power	BUCK3 (Low Voltage Step-Down Converter) Switch Node.	Floating
16	PGND	—	Ground	Power Ground.	Not applicable
17	LX_B2	O	Power	BUCK2 (Low Voltage Step-Down Converter) Switch Node	Floating
18	PVIN_B2	I	Power	BUCK2 (Low Voltage Step-Down Converter) Input Voltage. PVIN_B2 and PVIN_B3 must be tied together and voltage applied at the same time or after the voltage on VSYS/PVIN_B1 is applied.	Input supply
19	VIO	I	Power	IO Supply Voltage pin.	Not applicable
20	FB_B2	I	Analog	BUCK2 (Low Voltage Step-Down Converter) Feedback. When BUCK2 is not used, this pin can be used for monitoring an external rail. When BUCK2 and corresponding monitoring are both deactivated in NVM pin can be left floating.	Floating
21	nINT/GPIO	O	Digital	Interrupt output	Floating
		I	Digital	Alternative programmable function: Trigger Mode Watchdog Input	
		I	Digital	Alternative programmable function: Control Input for Entering and Exiting Low Power Mode	
22	SDA	I/O	Ground	I2C interface bidirectional serial data (external pull up).	Pull high
23	SCL	I	Power	I2C interface serial clock (external pull up).	Pull high
24	PVIN_LDO	I	Power	LDO Input Voltage. Apply the voltage on PVINLDO at the same time or after the voltage on VSYS is applied.	Input supply

ADVANCE INFORMATION

5 Device and Documentation Support

5.1 Device Support

5.1.1 Third-Party Products Disclaimer

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2024	*	Advance Information

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

7.1 Package Option Addendum

Packaging Information

Orderable Device (Preview)	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
PTPS65036200RAYRQ1	PRE_PROD	VQFN-HR	RAY	24	3000	RoHS & Green	NIPDAU	Level2-260C	-40°C to 125°C	PO036XXQ1

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

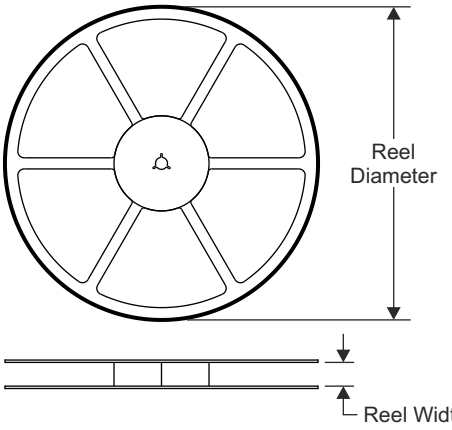
(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

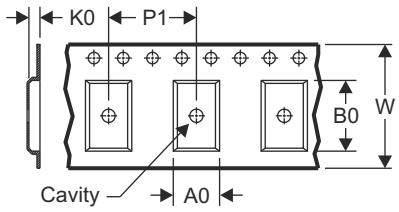
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

7.2 Tape and Reel Information

REEL DIMENSIONS

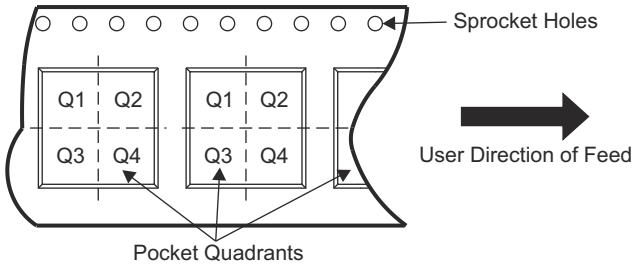


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

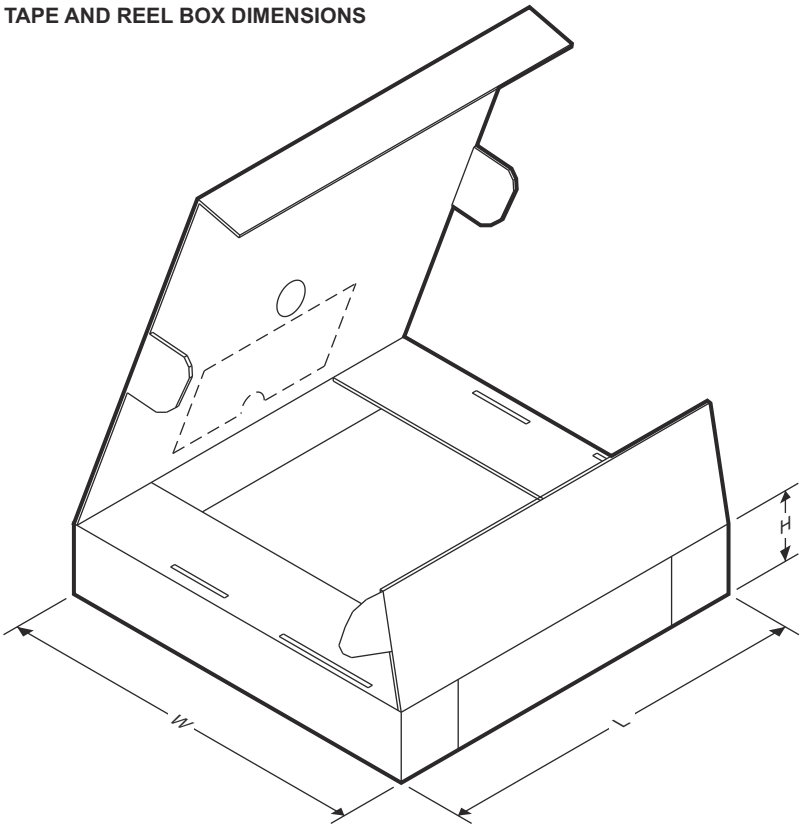


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPS65036200RAYRQ1	VQFN	RAY	24	3000	330.0	12.4	3.75	3.75	1.15	8.0	12	Q2

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPS65036200RAYRQ1	VQFN	RAY	24	3000	367.0	367.0	35.0
PTPS65036200RAYRQ1	VQFN	RAY	24	3000	360.0	360.0	36.0

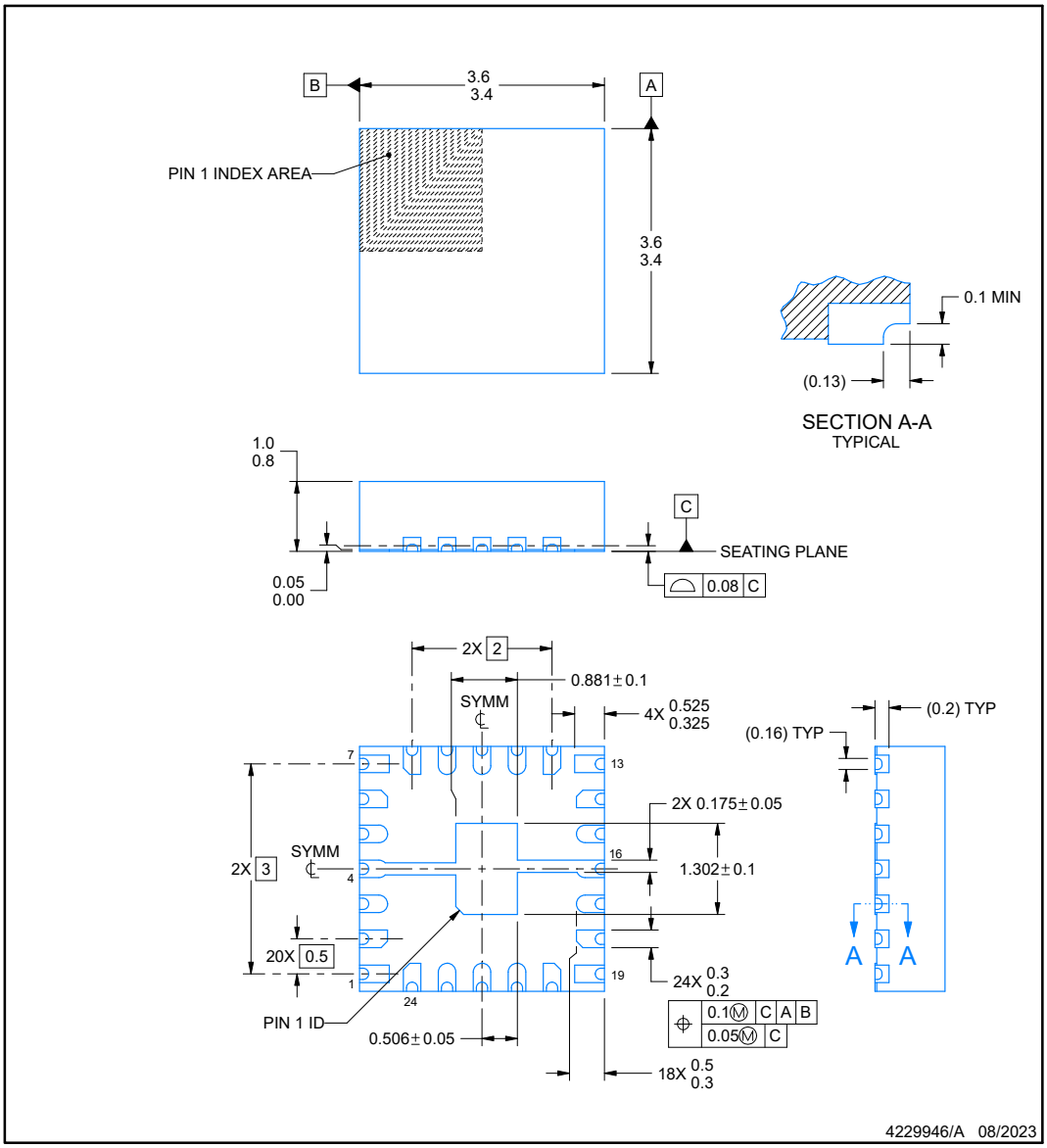
ADVANCE INFORMATION

PACKAGE OUTLINE

RAY0024B

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

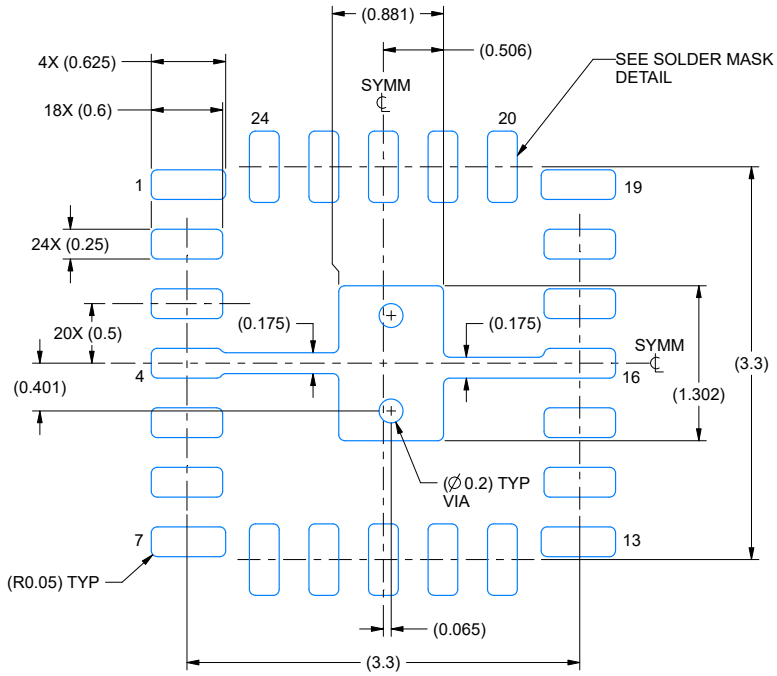
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

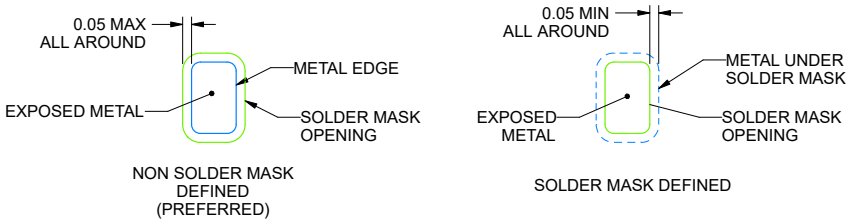
EXAMPLE BOARD LAYOUT

RAY0024B — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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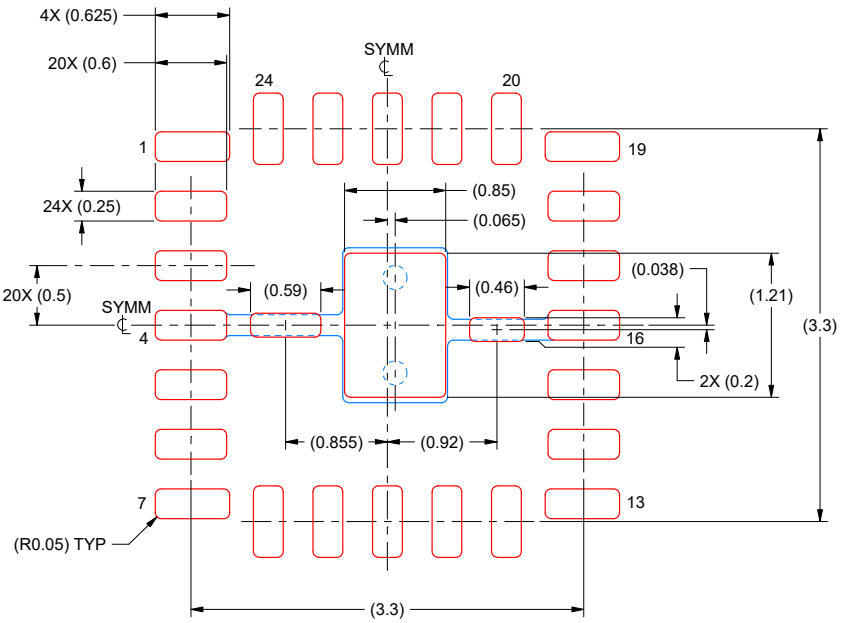
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RAY0024B — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 4 & 16: 90%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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