8-PIN HIGH-EFFICIENCY, OFFLINE LED LIGHTING CONTROLLER

Check for Samples: TPS92010

FEATURES

- **LED Lighting Current Driver Controller with Energy Saving Features**
- **Quasi-Resonant Mode Operation for Reduced EMI and Low Switching Losses (Low Voltage Switching)**
- **Low Standby Current for Deep Dimming Efficiency Power Consumption**
- **Low Startup Current: 25 µA Maximum**
- **Programmable Line and Load Overvoltage Protection**
  - **Provides Open LED Protection**
- **Internal Overtemperature Protection**
- **Current Limit Protection**
  - **Cycle-by-Cycle Power Limit**
  - **Primary-Side Overcurrent Hiccup Restart Mode**
- **1-A Sink TrueDrive™, –0.75-A Source Gate Drive Output**
- **Programmable Soft-Start**

APPLICATIONS

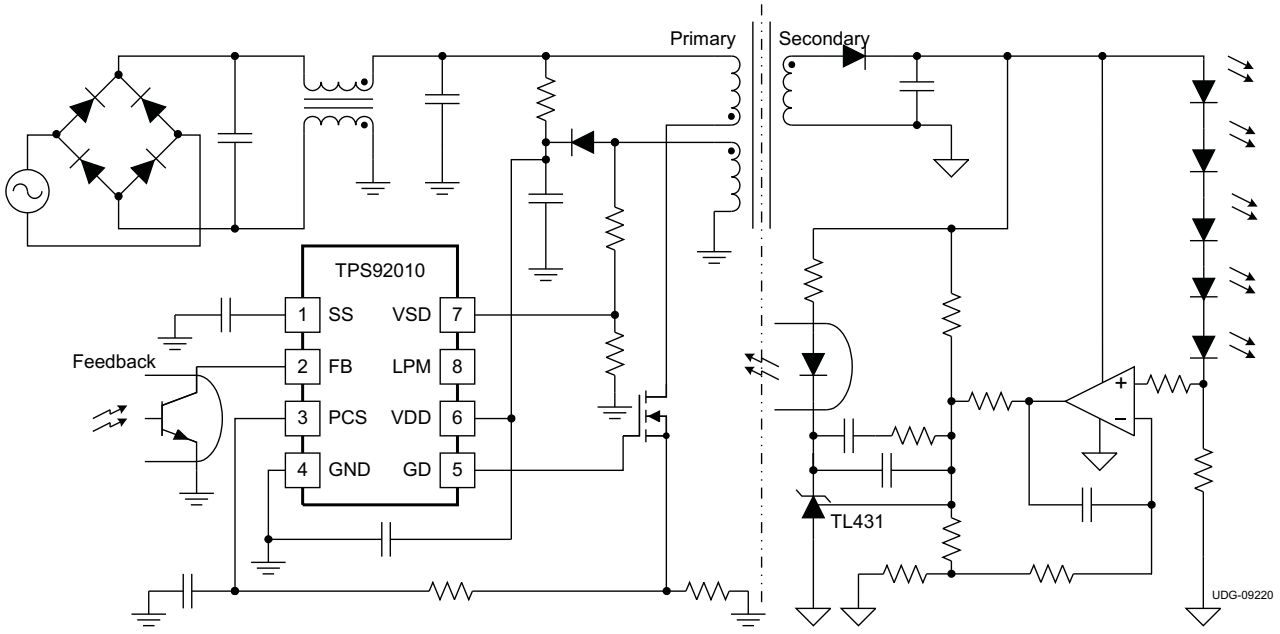
- **Residential LED Lighting Drivers for A19 E12/E26/27, GU10, MR16, PAR30/38 Integral Lamps**
- **Drivers for Wall Sconces, Pathway Lighting and Overhead Lighting**
- **Drivers for Wall Washing, Architectural and Display Lighting**

DESCRIPTION

The TPS92010 is a PWM controller with advanced energy features to provide high efficiency driving for LED lighting applications.

The TPS92010 incorporates frequency fold back and low power mode operation to reduce the operation frequency at light load and no load operations.

The TPS92010 is offered in the 8-pin SOIC (D) package. Operating junction temperature range is –40°C to 105°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TrueDrive is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			TPS92010	UNIT
VDD	Supply voltage range	I_{DD} < 20 mA	27	V
I_{DD}	Supply current		20	mA
$I_{GD(sink)}$	Output sink current (peak)		1.2	A
$I_{GD(source)}$	Output source current (peak)		–0.8	
	Analog inputs	FB, PCS, SS	–0.3 to 6.0	V
V_{VSD}			–1.0 to 6.0	
$I_{VSD(source)}$			–1.0	mA
V_{LPM}		VDD = 0 V to 30 V	30	V
	Power dissipation	SOIC-8 package, T_A = 25°C	650	mW
T_J	Operating junction temperature range		–55 to 150	°C
T_{stg}	Storage temperature		–65 to 150	
T_{LEAD}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
VDD	Input voltage		21	V
I_{GD}	Output sink current	0		A
T_J	Operating junction temperature	–40	105	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model		2000	V
CDM		1500	

ELECTRICAL CHARACTERISTICS

VDD = 15 V, 0.1-µF capacitor from VDD to GND, 3.3-nF capacitor from SS to GND charged over 3.5 V, 500-Ω resistor from VSD to -0.1 V, FB = 4.8 V, LPM = not connected, 1-nF capacitor from GD to GND, PCS = GND, T_A = –40°C to 105°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL						
$I_{STARTUP}$	Startup current	VDD = V_{UVLO} –0.3 V		12	25	µA
I_{LPM}	Standby current	V_{FB} = 0 V		350	550	µA
I_{DD}	Operating current	Not switching		2.5	3.5	mA
		130 kHz, QR mode		5.0	7.0	mA
	VDD clamp	FB = GND, I_{DD} = 10 mA	21	26	27	V
UNDERVOLTAGE LOCKOUT						
$VDD_{(uvlo)}$	Startup threshold		10.3	13.0	15.3	V
	Stop threshold		6.3	8	9.3	V
$\Delta VDD_{(uvlo)}$	Hysteresis		4.0	5.0	6.0	V
PWM (Ramp)(1)						
D_{MIN}	Minimum duty cycle	V_{SS} = GND, V_{FB} = 2 V			0%	
D_{MAX}	Maximum duty cycle	QR mode, f_S = max, (open loop)		99%		
OSCILLATOR (OSC)						
$f_{QR(max)}$	Maximum QR and DCM frequency		117	130	143	kHz
$f_{QR(min)}$	Minimum QR and FFM frequency	V_{FB} = 1.3 V	32	40	48	kHz
f_{SS}	Soft start frequency	V_{SS} = 2.0 V	32	40	48	kHz
dT_S/dFB	VCO gain	T_S for 1.6 V < V_{FB} < 1.8 V	–38	–30	–22	µs/V
FEEDBACK (FB)						
R_{FB}	Feedback pullup resistor		12	20	28	kΩ
V_{FB}	FB, no load	QR mode	3.30	4.87	6.00	V
	Low power mode ON threshold	V_{FB} threshold	0.3	0.5	0.7	V
	Low power mode OFF threshold	V_{FB} threshold	1.2	1.4	1.6	V
	Low power mode hysteresis	V_{FB} threshold		0.9		V
	Burst hysteresis	V_{FB} during low power mode	0.13	0.25	0.42	V
LOW POWER MODE						
$R_{DS(on)}$	LPM on resistance	V_{LPM} = 1 V	1.0	2.4	3.8	kΩ
$I_{LPM(leakage)}$	LPM leakage/off current	V_{FB} = 0.44 V, V_{STATUS} = 15 V	–0.1		2.0	µA
PEAK CURRENT SENSE (PCS)(1)						
$A_{PCS(FB)}$	Gain, FB = ΔV_{FB} / ΔV_{PCS}	QR mode		2.5		V/V
	Shutdown threshold	V_{FB} = 2.4 V, V_{SS} = 0 V	1.13	1.25	1.38	V
	PCS to output delay time (power limit)	PCS = 1.0 V_{PULSE}		175	300	ns
	PCS to output delay time (over current fault)	PCS = 1.45 V_{PULSE}		100	150	ns
	PCS discharge impedance	PCS = 0.1 V, V_{SS} = 0 V	25	115	250	Ω
$V_{PCS(os)}$	PCS offset	SS mode, V_{SS} ≤ 2.0 V, via FB	0.35	0.40	0.45	V

(1) R_{PCST} and C_{PCST} are not connected in the circuit for maximum and minimum duty cycle tests, current sense tests and power limit tests.

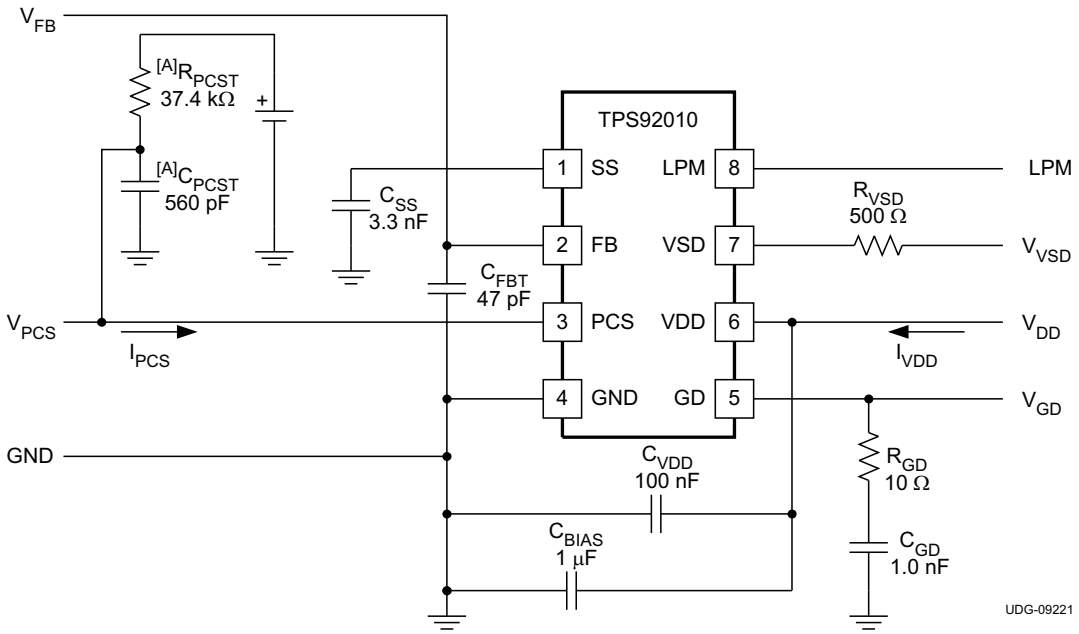
ELECTRICAL CHARACTERISTICS (continued)

VDD = 15 V, 0.1-µF capacitor from VDD to GND, 3.3-nF capacitor from SS to GND charged over 3.5 V, 500-Ω resistor from VSD to -0.1 V, FB = 4.8 V, LPM = not connected, 1-nF capacitor from GD to GND, PCS = GND, T_A = –40°C to 105°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER LIMIT (PL)(2)						
$I_{PL(Pcs)}$	PCS current	I_{VSD} = -300 µA	–165	–150	–135	µA
	PCS working range	QR mode, peak PCS voltage	0.70	0.81	0.92	V
V_{PL}	PL threshold	Peak CS voltage + PCS offset	1.05	1.20	1.37	
SOFT START (SS)						
$I_{SS(chg)}$	Softstart charge current	V_{SS} = GND	–8.3	–6.0	–4.5	µA
$I_{SS(dis)}$	Softstart discharge current	V_{SS} = 0.5 V	2.0	5.0	10	mA
V_{SS}	Switching ON threshold	Output switching start	0.8	1.0	1.2	V
VALLEY SWITCHING DETECT (VSD)						
$I_{VSD(line)}$	Valley switching detect	I_{VSD} threshold, GD = HI	–512	–450	–370	µA
$V_{VSD(on)}$	VSD voltage at OUT = HIGH	V_{FB} = 4.8 V, V_{SS} = 5.0 V, $I_{VSD(on)}$, = –300 µA	–125		–25	mV
$V_{VSD(load)}$	Load overvoltage protection	V_{VSD} threshold, GD = LO	3.37	3.75	4.13	V
THERMAL PROTECTION (TSP)(3)						
	Thermal shutdown (TSP) temperature			140		°C
	Thermal shutdown hysteresis			15		
GATE DRIVE						
t_{RISE}	Rise time	10% to 90% of 13 V typical out clamp		50	75	ns
t_{FALL}	Fall time			10	20	

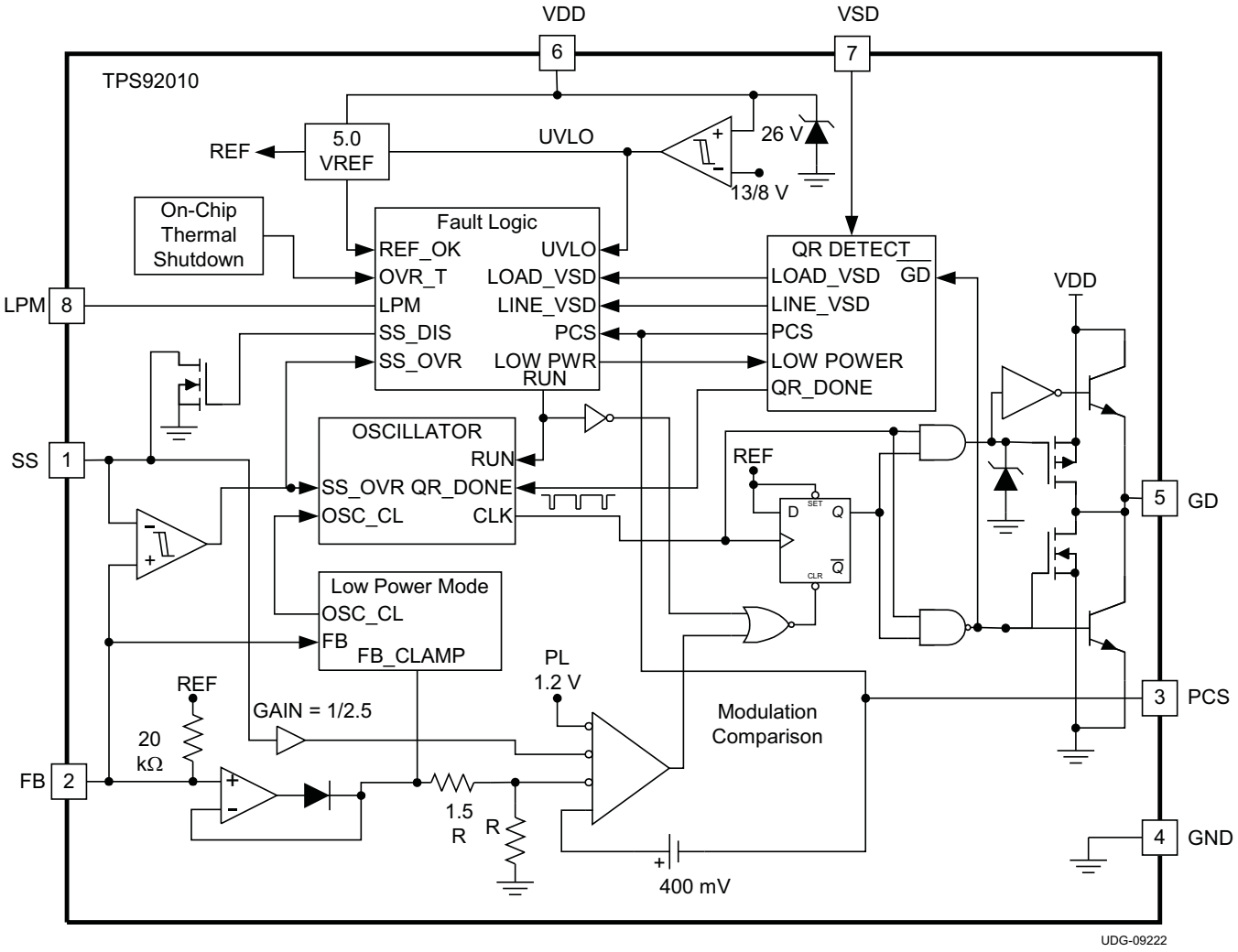
(2) R_{PCST} and C_{PCST} are not connected in the circuit for maximum and minimum duty cycle tests, current sense tests and power limit tests.
(3) Specified by design. Not production tested.

OPEN LOOP TEST CIRCUIT



A. R_{PCST} and C_{PCST} are not connected for maximum and minimum duty cycle tests, current sense tests and power limit tests.

BLOCK DIAGRAM



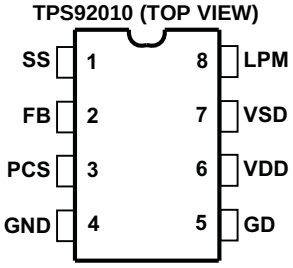
ORDERING INFORMATION

T_A	PACKAGES	PART NUMBER
–40°C to 105°C	SOIC (D)(1)	TPS92010D

(1) SOIC (D) package is available taped and reeled by adding “R” to the above part numbers. Reeled quantities for TPS92010DR is 2,500 devices per reel.

DEVICE INFORMATION

TPS92010 (TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
FB	2	I	Feedback input or control input from the output sensing network to the PWM comparator used to control the peak current in the power MOSFET. An internal 20-kΩ resistor is between this pin and the internal 5-V regulated voltage. The voltage of this pin controls the mode of operation in one of the three modes: quasi resonant (QR), frequency foldback mode (FFM) and low power mode (LPM).
GND	4	–	Ground for internal circuitry. Connect a ceramic 0.1-µF bypass capacitor between VDD and GND, with the capacitor as close to these two pins as possible.
GD	5	O	1-A sink (TrueDrive™) and 0.75-A source gate drive output. This output drives the power MOSFET and switches between GND and the lower of VDD or the 13-V internal output clamp.
LPM	8	O	The low power mode pin is an ACTIVE HIGH open drain signal that indicates the device has entered low power mode. LPM pin is high during UVLO, (VDD < startup threshold), and softstart, (SS < FB).
PCS	3	I	Peak current sense input, also programs power limit and is used to control modulation and activate overcurrent protection. The PCS voltage input originates across a current sense resistor and ground. Power limit is programmed with an effective series resistance between this pin and the current sense resistor.
SS	1	I	Soft-start programming pin. Program the soft-start rate with a capacitor to ground; the rate is determined by the capacitance and the internal soft-start charge current. Placement of the soft-start capacitor is critical and should be placed as close as possible to the SS pin and GND, keeping trace length to a minimum. All faults discharge the SS pin to GND through an internal MOSFET with an $R_{DS(on)}$ of approximately 100 Ω. The internal modulator comparator reacts to the lowest of the SS voltage, the internal FB voltage and the peak current limit.
VDD	6	I	Provides power to the device. Use a ceramic 0.1-µF by-pass capacitor for high-frequency filtering of the VDD pin, as described in the GND pin description. Operating energy is usually delivered from auxiliary winding. To prevent hiccup operation during start-up, a larger energy storage cap is also needed between VDD and GND.
VSD	7	I	The valley switching detect (VSD) pin senses line, load and resonant conditions using the primary bias winding.

APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

The TPS92010 is a multi-mode LED Lighting controller, as illustrated in Figure 1 and Figure 2. The mode of operation depends upon input and dimming conditions. Under all modes of operation, the TPS92010 terminates the GD = HI signal based on the switch current. Thus, the TPS92010 always operates in current mode control so that the power MOSFET current is always limited.

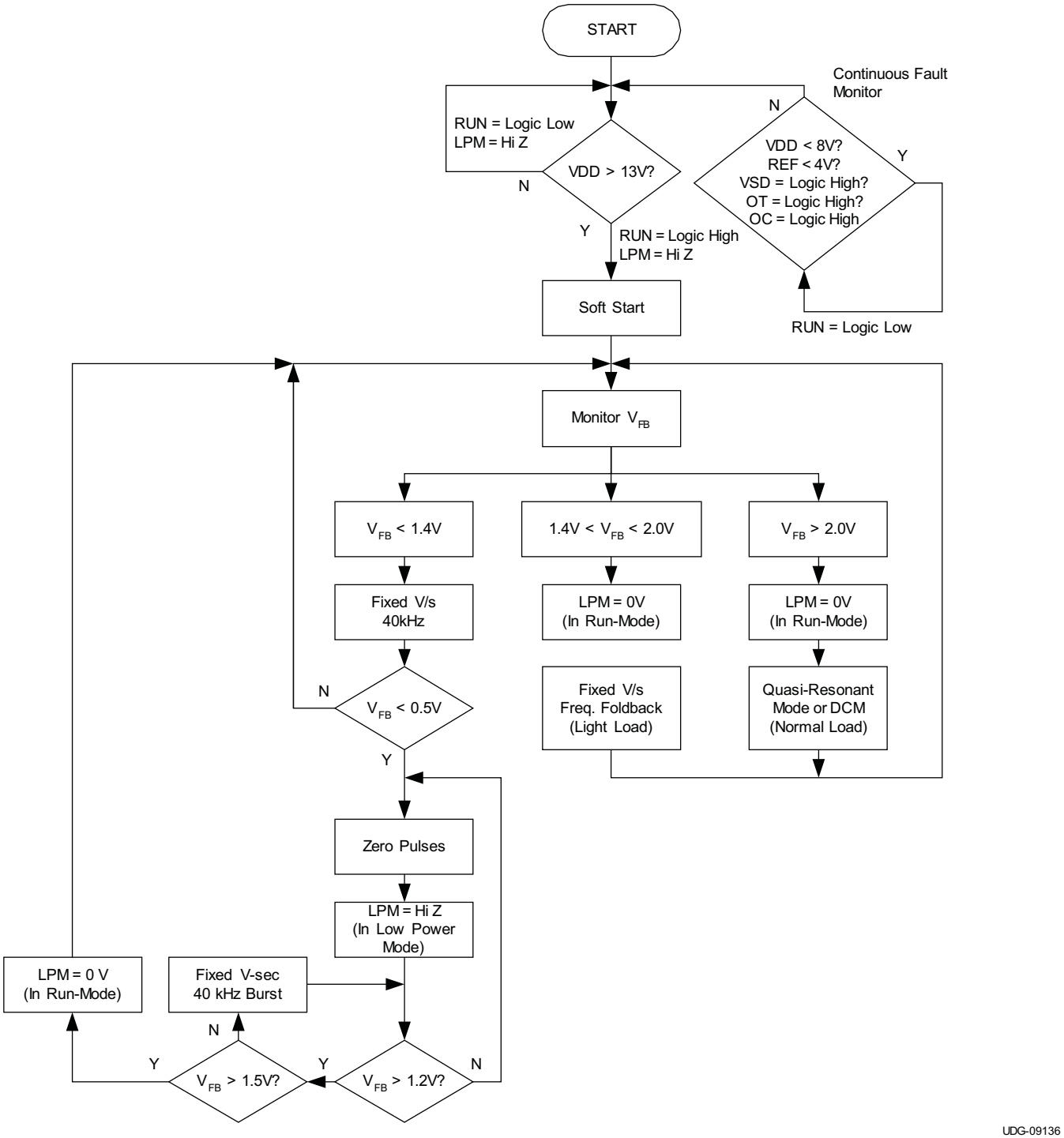


Figure 1. Control Flow Chart

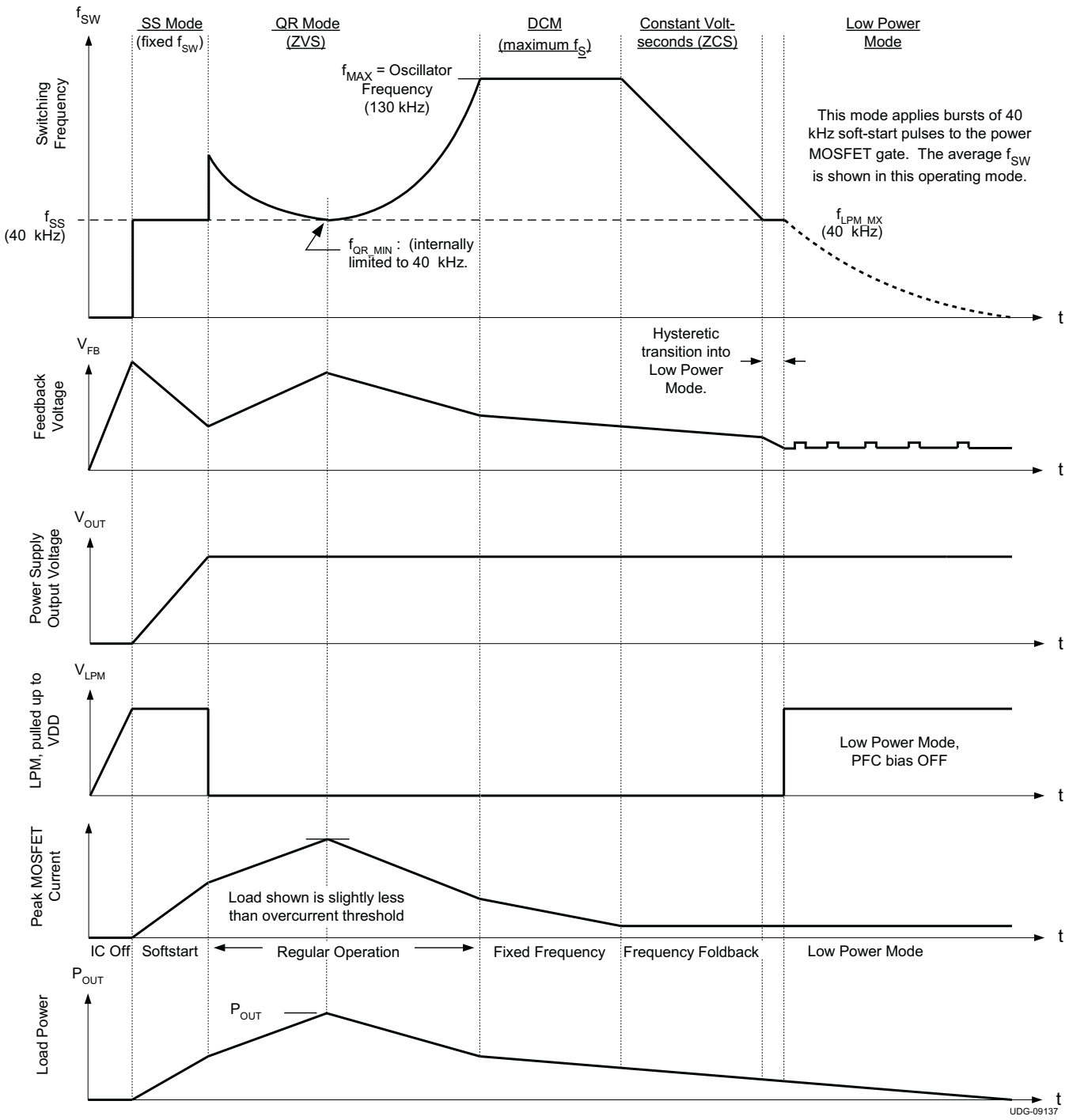


Figure 2. Operation Mode Switching Frequencies

Under normal operating conditions, the FB pin commands the operating mode of the TPS92010 at the voltage thresholds shown in Figure 3. Soft-start and fault responses are exceptions. During soft-start mode the TPS92010 controls the converter at a fixed constant switching frequency of 40 kHz. The soft-start mode is latched-OFF when V_{FB} becomes less than V_{SS} for the first time after $UVLO_{ON}$. The soft-start state cannot be recovered until after passing $UVLO_{OFF}$, and then, $UVLO_{ON}$.

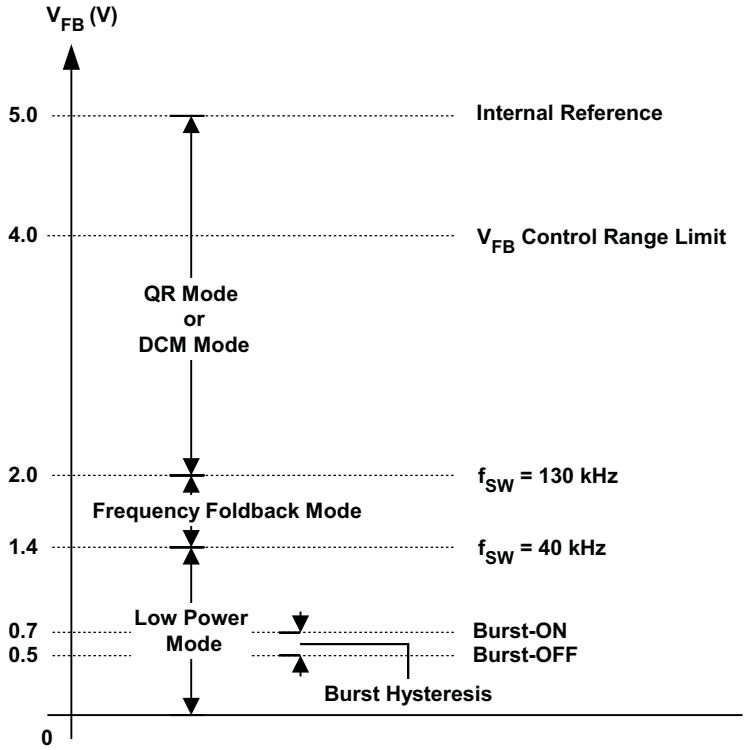


Figure 3. Mode Control with FB Pin Voltage

At normal rated operating loads (from 100% to approximately 30% full rated power) the TPS92010 controls the converter in quasi-resonant mode (QRM) or discontinuous conduction mode (DCM), where DCM operation is at the clamped maximum switching frequency (130 kHz). For loads that are between approximately 30% and 10% full rated power, the converter operates in frequency foldback mode (FFM), where the peak switch current is constant and the output is regulated by modulating the switching frequency for a given and fixed V_{IN}. Effectively, operation in FFM results in the application of constant volt-seconds to the flyback transformer each switching cycle. Voltage regulation in FFM is achieved by varying the switching frequency in the range from 130 kHz to 40 kHz. For extremely light loads (below approximately 10% full rated power), the converter is controlled using bursts of 40-kHz pulses. Keep in mind that the aforementioned boundaries of steady-state operation are approximate because they are subject to converter design parameters.

Refer to the typical applications block diagram for the electrical connections to implement the features.

Details of the functional boxes in the Block Diagram are shown in Figure 4, Figure 5, Figure 6 and Figure 7 showing how the TPS92010 executes the command of the FB voltage to have the responses that are shown in Figure 3, Figure 1 and Figure 2. The details of the functional boxes also show the various fault detections and responses that are included in the TPS92010. During all modes of operation, this controller operates in current mode control. This allows the TPS92010 to monitor the FB voltage to determine and respond to the varying load levels.

Quasi-resonant mode and DCM occurs for feedback voltages V_{FB} between 2.0 V and 4.0 V, respectively. In turn, the PCS voltage is commanded to be between 0.4 V and 0.8 V. A cycle-by-cycle power limit imposes a fixed 0.8-V limit on the PCS voltage. An overcurrent shutdown threshold in the fault logic gives added protection against high-current, slew-rate shorted winding faults, shown in Figure 7. The power limit feature in the QR DETECT circuit of Figure 6 adds an offset to the PCS signal that is proportional to the line voltage. The power limit feature is programmed with R_{PL}, as shown in the typical application diagram.

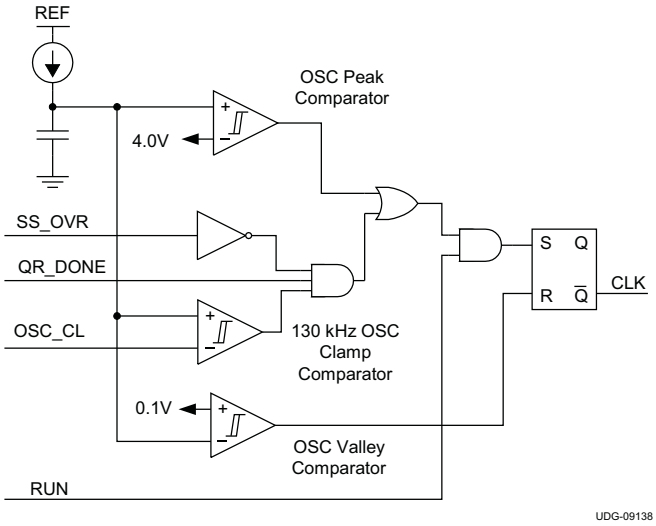


Figure 4. Oscillator Details

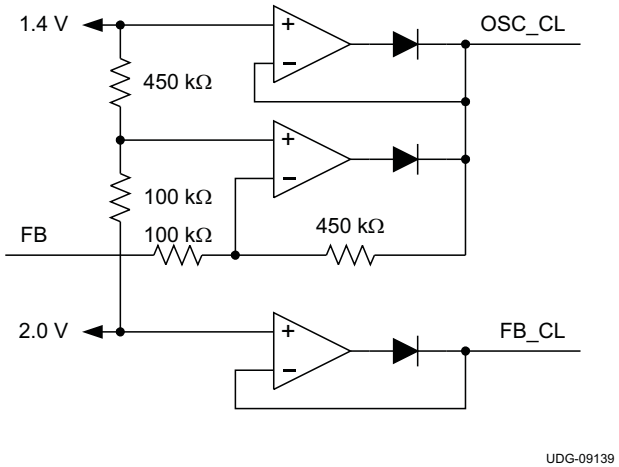


Figure 5. Mode Clamp Details

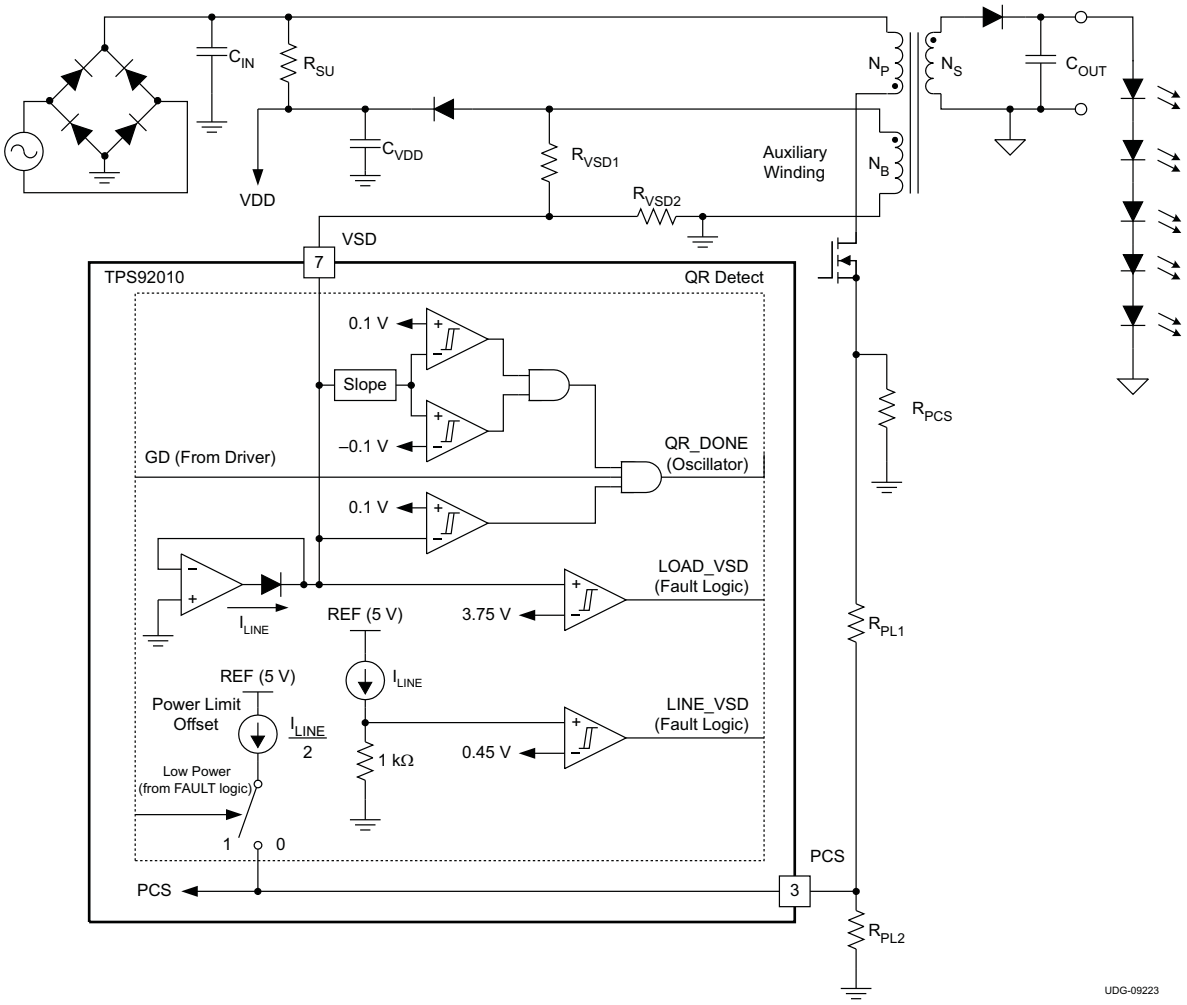


Figure 6. QR Detect Details

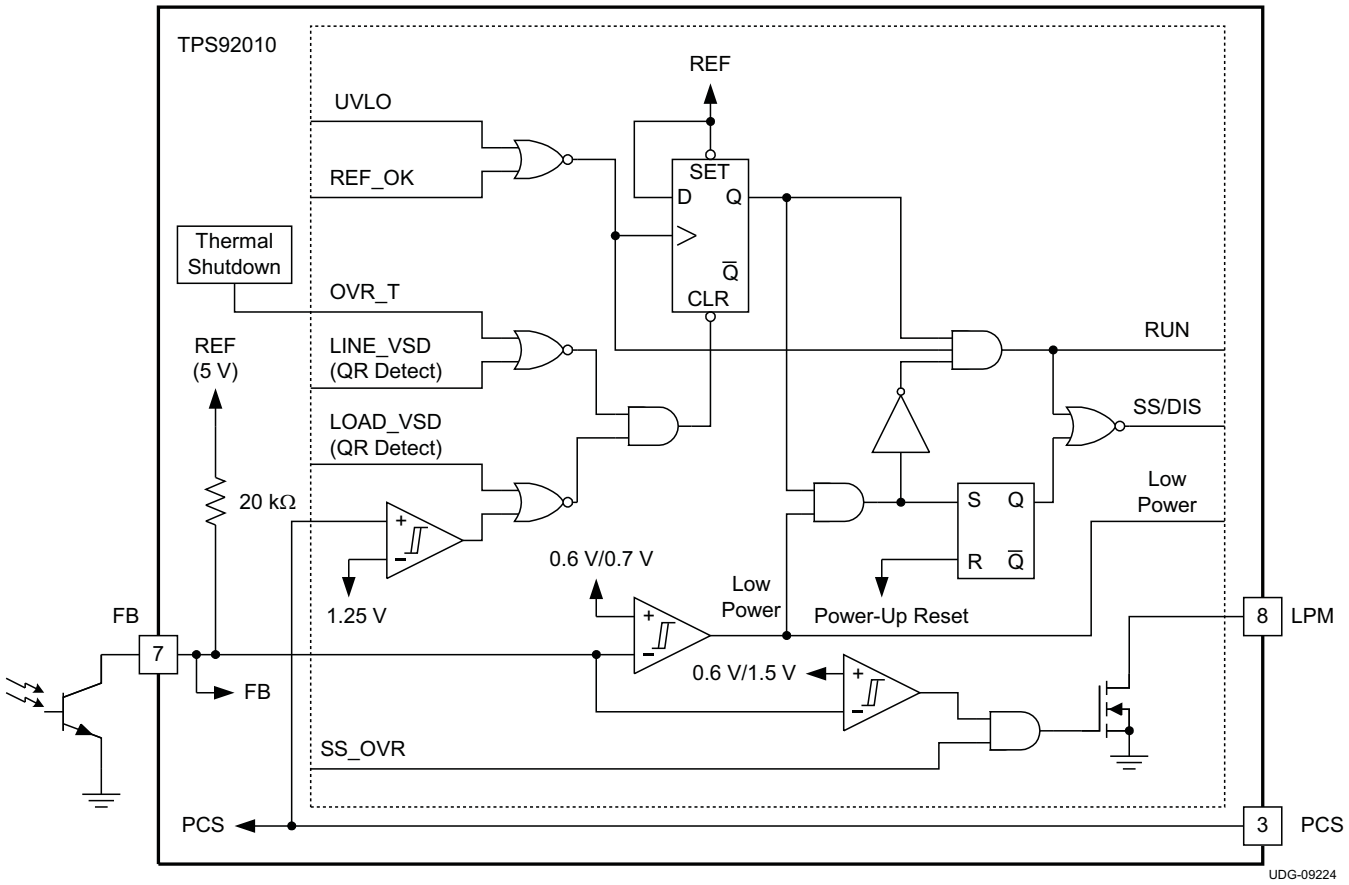


Figure 7. Fault Logic Details

Quasi-Resonant / DCM Control

Quasi-resonant (QR) and DCM operation occur for feedback voltages V_{FB} between 2.0 V and 4.0 V. In turn, the peak PCS voltage is commanded to be between 0.4 V and 0.8 V. During this control mode, the rising edge of GD always occurs at the valley of the resonant ring after demagnetization. Resonant valley switching is an integral part of QR operation. Resonant valley switching is also imposed if the system operates at the maximum switching frequency clamp. In other words, the frequency varies in DCM operation in order to have the switching event occur on the first resonant valley that occurs after a 7.7-µs (130-kHz) interval. Notice that the PCS pin has an internal dependent current source, ½ I_{LINE}. This current source is part of the cycle-by-cycle power limit function that is discussed in the Protection Features section.

Frequency Foldback Mode Control

Frequency foldback mode uses elements of the FAULT LOGIC, shown in Figure 7 and the mode clamp circuit, shown in Figure 5. At the minimum operating frequency, the internal oscillator sawtooth waveform has a peak of 4.0 V and a valley of 0.1 V. When the FB voltage is between 2.0 V and 1.4 V, the FB_CL signal in Figure 5 commands the oscillator in a voltage controlled oscillator (VCO) mode by clamping the peak oscillator voltage. The additional clamps in the OSCILLATOR restrict VCO operation between 40 kHz and 130 kHz. The FB_CL voltage is reflected to the modulator comparator effectively clamping the reflected PCS command to 0.4 V.

Low Power Mode Control

Low power mode uses elements of the FAULT LOGIC, shown in Figure 7 and the mode clamps circuit, shown in Figure 5. The OSC_CL signal clamps the Low Power-mode operating frequency at 40 kHz. Thus, when the FB voltage is between 1.4 V and 0.5 V, the controller is commanding an excess of energy to be transferred to the load which in turn, drives the error higher and FB lower. When FB reaches 0.5 V, GD pulses are terminated and do not resume until FB reaches 0.7 V. In this mode, the converter operates in hysteretic control with the GD pulse terminated at a fixed PCS voltage level of 0.4 V. The power limit offset is turned OFF during Low Power mode and it returns to ON when FB is above 1.4 V, as depicted in Figure 7. H mode reduces the average switching frequency in order to minimize switching losses and increase the efficiency at light load conditions.

Fault Logic

Advanced logic control coordinates the fault detections to provide proper power supply recovery. This provides the conditioning for the thermal protection. Line overvoltage protection and load overvoltage protection are implemented in this block. It prevents operation when the internal reference is below 4.5 V. If a fault is detected in the thermal shutdown, line overvoltage protection, load overvoltage protection, or REF, the TPS92010 undergoes a shutdown/retry cycle.

Refer to the fault logic diagram in Figure 7 and the QR detect diagram in Figure 6 to program line overvoltage protection and load overvoltage protection. To program the load overvoltage protection, select the R_{VSD1} – R_{VSD2} divider ratio to be 3.75 V at the desired output shut-down voltage. To program line overvoltage protection, select the impedance of the R_{VSD1} – R_{VSD2} combination to draw 450 µA when the V_{VSD} is 0.45 V during the ON-time of the power MOSFET at the highest allowable input voltage.

Oscillator

The oscillator, shown in Figure 4, is internally set and trimmed so it is clamped by the circuit in Figure 4 to a nominal 130-kHz maximum operating frequency. It also has a minimum frequency clamp of 40 kHz. If the FB voltage tries to drive operation to less than 40 kHz, the converter operates in low power mode.

Low Power

The LPM pin is an open drain output, as shown in Figure 7. The LPM output goes into the OFF-state when FB falls below 0.5 V and it returns to the ON-state (low impedance to GND) when FB rises above 1.4 V.

OPERATING MODE PROGRAMMING

Boundaries of the operating modes are programmed by the flyback transformer and the four components R_{PL}, R_{PCS}, R_{VSD1} and R_{VSD2}; shown in Figure 1.

The transformer characteristics that predominantly affect the modes are the magnetizing inductance of the primary and the magnitude of the output voltage, reflected to the primary. To a lesser degree (yet significant), the boundaries are affected by the MOSFET output capacitance and transformer leakage inductance. The design procedure here is to select a magnetizing inductance and a reflected output voltage that operates at the DCM/CCM boundary at maximum load and maximum line. The actual inductance should be noticeably smaller to account for the ring between the magnetizing inductance and the total stray capacitance measured at the drain of the power MOSFET. This programs the QR/DCM boundary of operation. All other mode boundaries are preset with the thresholds in the oscillator and green-mode blocks.

PROTECTION FEATURES

The TPS92010 has many protection features. Refer to Figures 1, 4, 8, 9 and 10 for detailed block descriptions that show how the features are integrated into the normal control functions.

Overtemperature

Overtemperature lockout typically occurs when the substrate temperature reaches 140ºC. Retry is allowed if the substrate temperature reduces by the hysteresis value. Upon an overtemperature fault, C_{SS} on softstart is discharged and LPM is forced to a high impedance.

Cycle-by-Cycle Power Limit

The cycle terminates when the PCS voltage plus the power limit offset exceeds 1.2 V.

In order to have power limited over the full line voltage range of the QR Flyback converter, the PCS pin voltage must have a component that is proportional to the primary current plus a component that is proportional to the line voltage due to predictable switching frequency variations due to line voltage. At power limit, the PCS pin voltage plus the internal PCS offset is compared against a constant 1.2-V reference in the PWM comparator. Thus during cycle-by-cycle power limit, the peak PCS voltage is typically 0.8 V.

The current that is sourced from the VSD pin (I_{LINE}) is reflected to a dependent current source of ½ I_{LINE}, that is connected to the PCS pin. The power limit function can be programmed by a resistor, R_{PL}, that is between the PCS pin and the current sense resistor. The current, I_{LINE}, is proportional to line voltage by the transformer turns ratio N_B/N_P and resistor R_{VSD1}. Current I_{LINE} is programmed to set the line over voltage protection. Resistor R_{PL} results in the addition of a voltage to the current sense signal that is proportional to the line voltage. The proper amount of additional voltage has the effect of limiting the power on a cycle-by-cycle basis. Note that R_{PCS}, R_{PL}, R_{VSD1} and R_{VSD2} must be adjusted as a set due to the functional interactions.

Current Limit

When the primary current exceeds maximum current level which is indicated by a voltage of 1.25 V at the PCS pin, the device initiates a shutdown. Retry occurs after a $UVLO_{OFF}/UVLO_{ON}$ cycle.

Overvoltage Protection Function

Input line overvoltage and LED open string protection is programmed with the transformer turn ratios, R_{VSD1} and R_{VSD2}. The VSD pin has a 0-V voltage source that can only source current; VSD cannot sink current.

Open String LED protection occurs when the VSD pin is clamped at 0 V. When the bias winding is negative, during GD = HI or portions of the resonant ring, the 0-V voltage source clamps VSD to 0 V and the current that is sourced from the VSD pin is mirrored to the Line_VSD comparator and the QR detection circuit. The Line_VSD comparator initiates a shutdown-retry sequence if VSD sources any more than 450 µA.

Open String LED protection occurs when the VSD pin voltage is positive. When the bias winding is positive, during demagnetization or portions of the resonant ring, the VSD pin voltage is positive. If the VSD voltage is greater than 3.75 V, the device initiates a shutdown. Retry occurs after a $UVLO_{OFF}/UVLO_{ON}$ cycle.

Undervoltage Lockout

Protection is provided to guard against operation during unfavorable bias conditions. Undervoltage lockout (UVLO) always monitors VDD to prevent operation below the UVLO threshold.

TYPICAL CHARACTERISTICS

CLAMP VOLTAGE vs JUNCTION TEMPERATURE

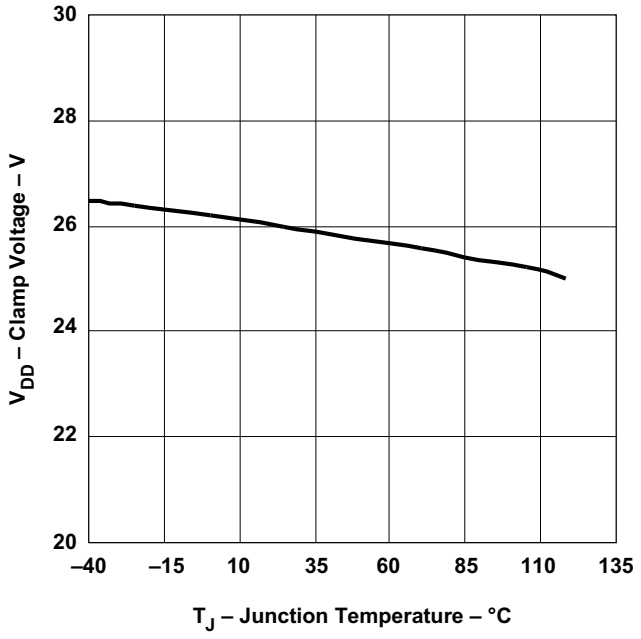


Figure 8.

SWITCHING FREQUENCY vs JUNCTION TEMPERATURE

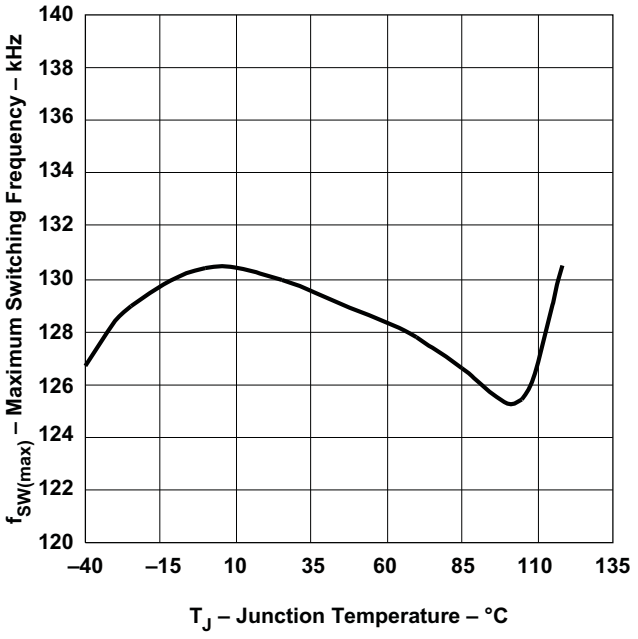


Figure 9.

PL THRESHOLD vs TEMPERATURE

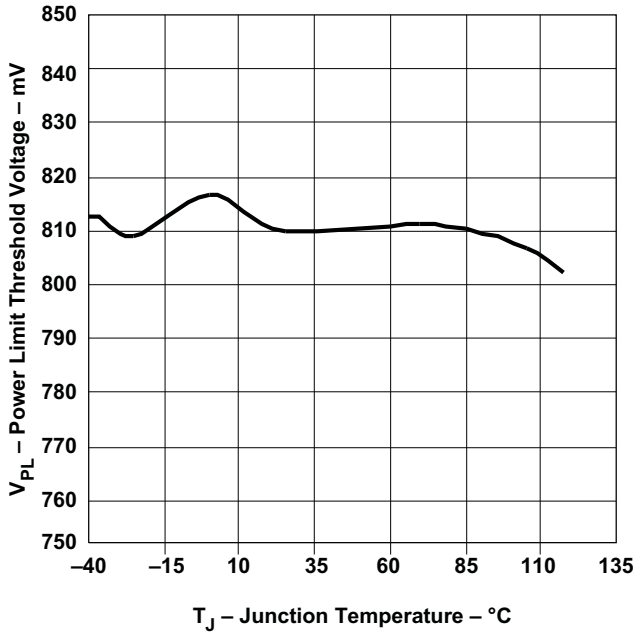


Figure 10.

OVERVOLTAGE PROTECTION THRESHOLD vs TEMPERATURE

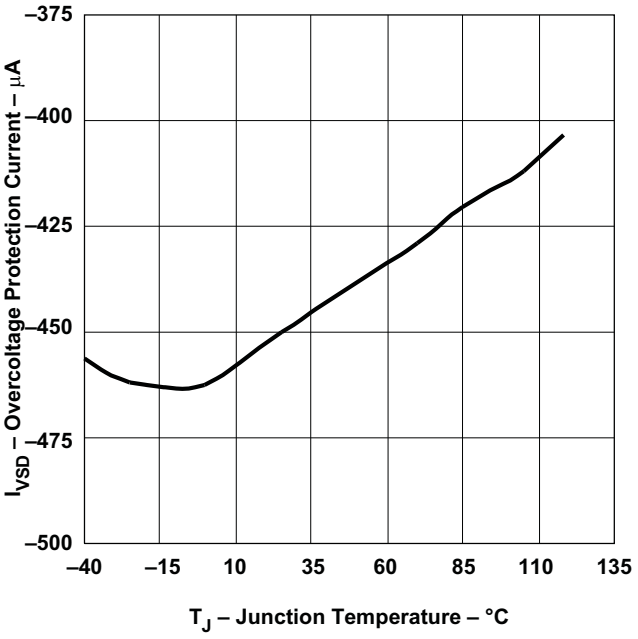


Figure 11.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92010D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	92010D	Samples
TPS92010DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	92010D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

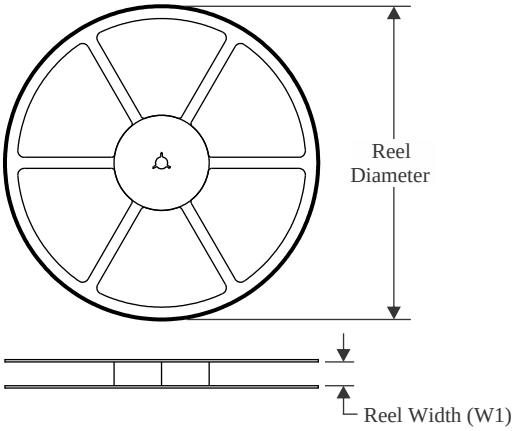
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

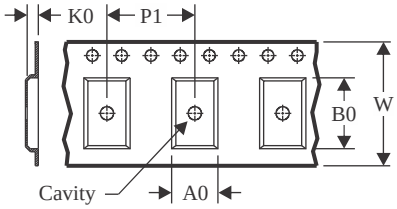
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

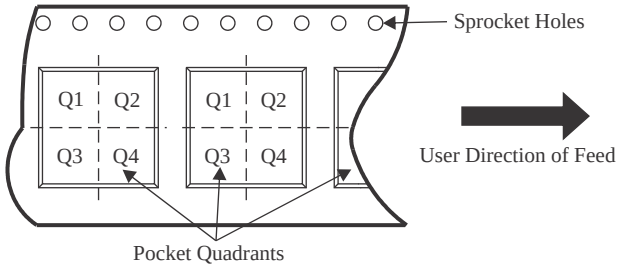


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

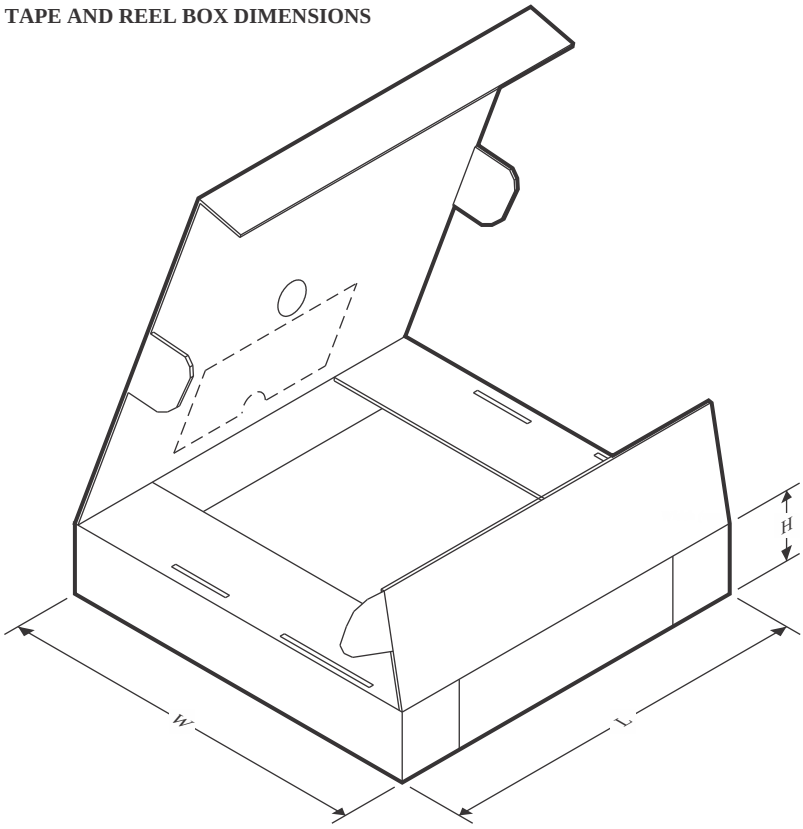
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92010DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

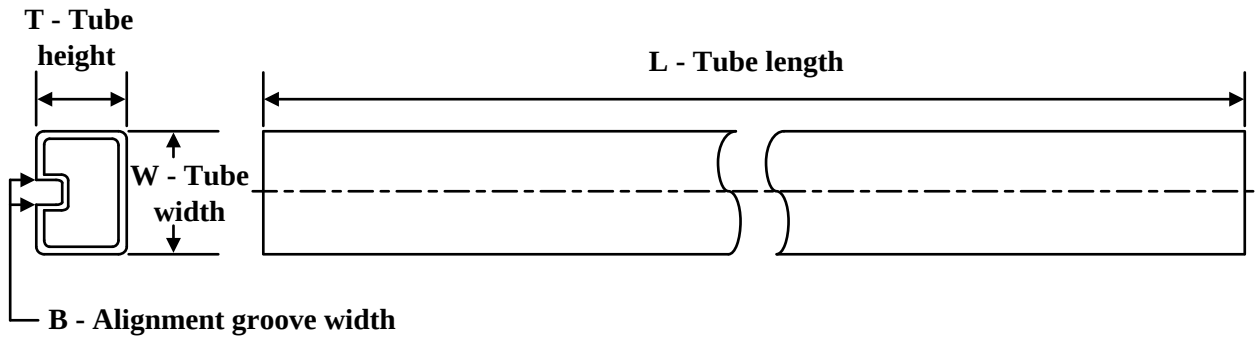
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

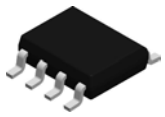
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92010DR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS92010D	D	SOIC	8	75	507	8	3940	4.32

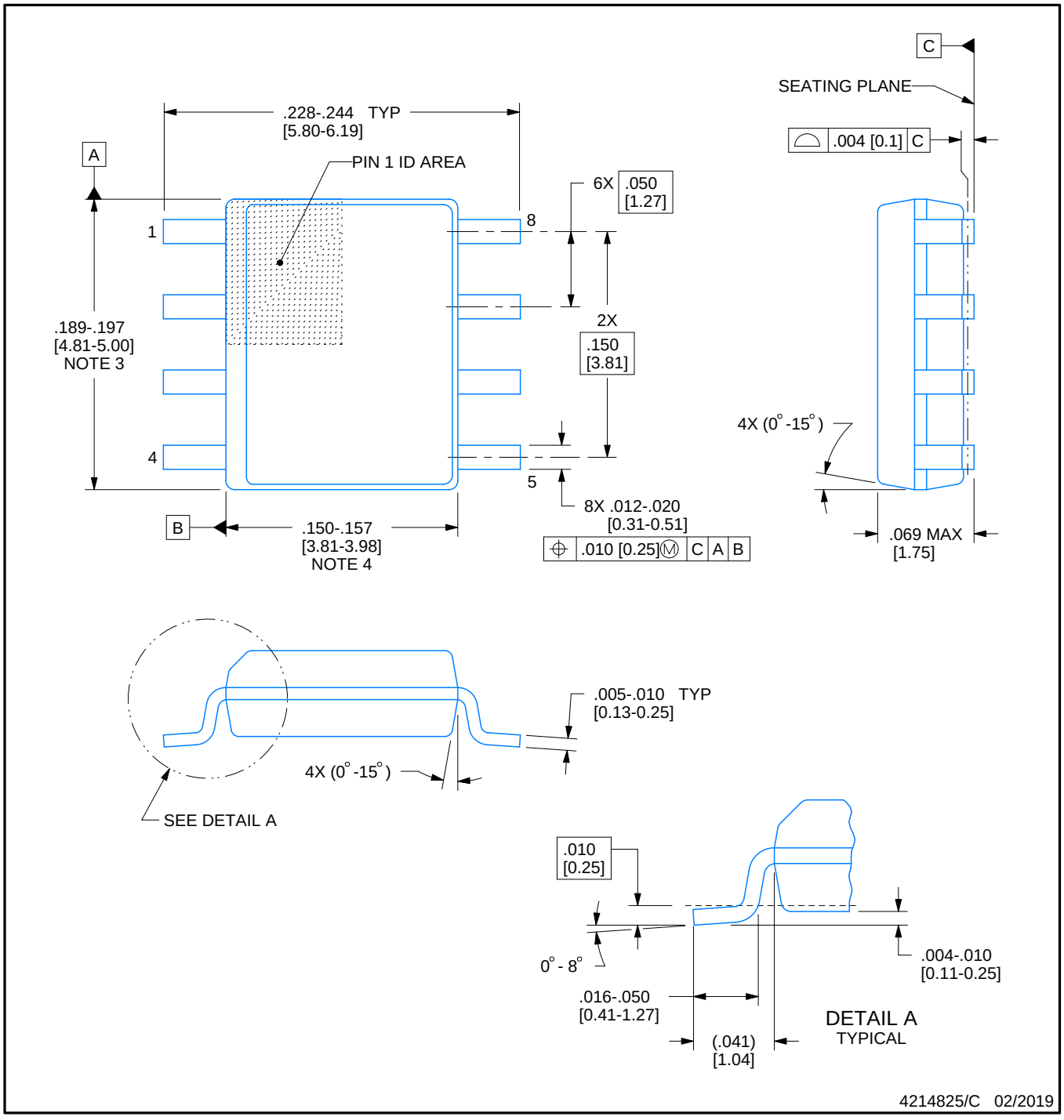


PACKAGE OUTLINE

D0008A

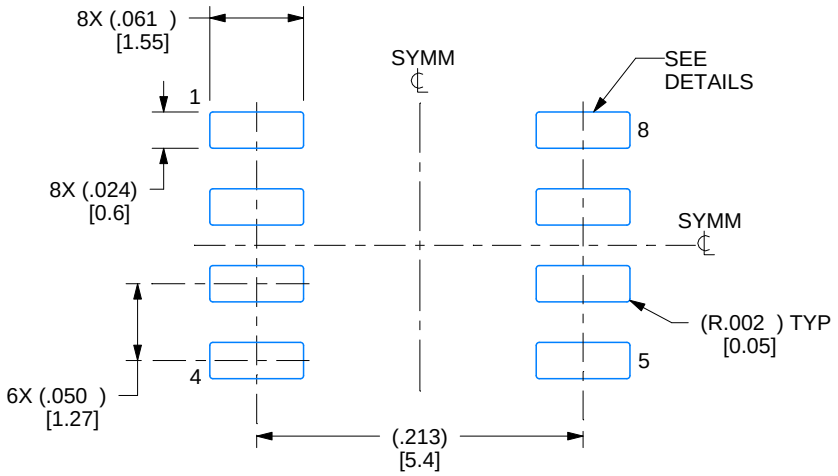
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

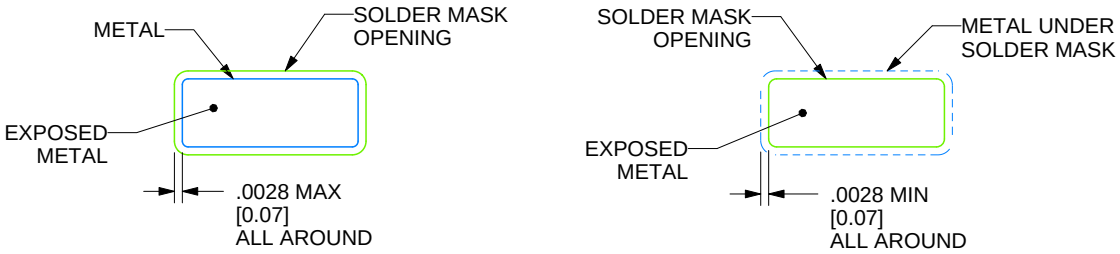


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

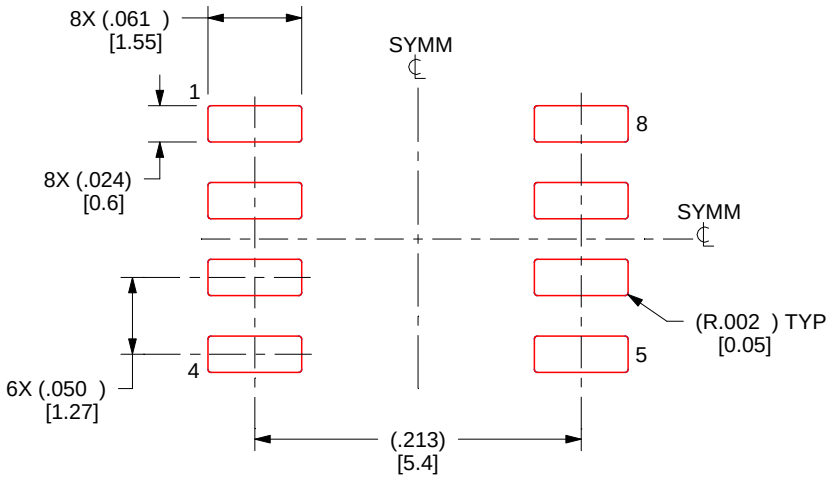
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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