TPSM82851x 2.7-V to 6-V Input, 0.5-A/1-A/2-A Step-Down Power Module With Integrated Inductor

1 Features

- 2.7-V to 6-V input voltage range
- 0.6-V to 5.5-V output voltage range
- Family of 0.5-A, 1-A and 2-A devices
- 20-µA typical quiescent current
- ±1% feedback voltage accuracy (PWM operation)
- 2.25-MHz switching frequency (PWM operation)
- 1.8-MHz to 4-MHz external synchronization
- Selectable forced PWM or PFM/PWM operation
- Adjustable soft start-up to 10 ms or tracking
- Precise ENABLE input allows
  - User-defined undervoltage lockout
  - Exact sequencing
- 100% duty cycle mode
- Active output discharge
- Power-good output with window comparator
- –40°C to 125°C operating temperature range
- 2.7-mm × 3.0-mm QFN package with 0.5-mm pitch

2 Applications

- Factory automation and control
- Signal measurement, source generation, instrumentation
- Patient monitoring and diagnostics
- Wireless infrastructure
- Ruggedized Communication: sensors, imaging, and radar

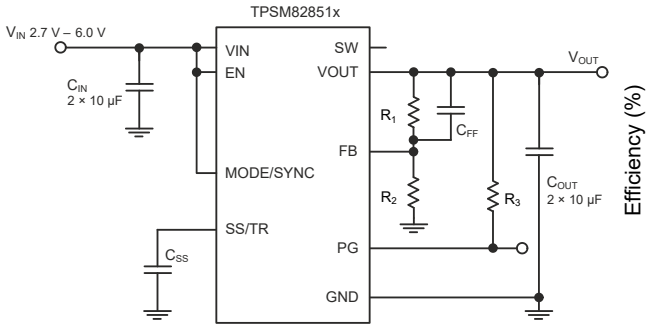
3 Description

TPSM82851x is a family of pin-to-pin compatible, 0.5-A, 1-A, and 2-A high-efficiency and easy to use synchronous step-down DC/DC power modules with integrated inductors. The devices are based on a fixed-frequency peak current-mode control topology and they can be used in telecommunication, test and measurement, and medical applications with high power density and ease of use requirements. Low resistance switches allow up to 2-A continuous output current at high ambient temperatures. The switching frequency is internally fixed at 2.25 MHz and can also be synchronized to an external clock in the range from 1.8 MHz to 4 MHz. In PFM/PWM mode, the TPSM82851x automatically enters power save mode at light loads to maintain high efficiency across the whole load range. The TPSM82851x provides a 1% feedback voltage accuracy in PWM mode which helps design a power supply with high output voltage accuracy. The SS/TR pin sets the start-up time or tracks the output voltage to an external source. This feature allows external sequencing of different supply rails and limits the inrush current during start-up.

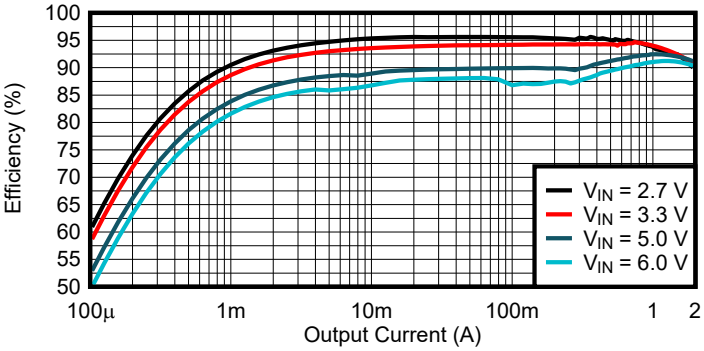
Device Information

PART NUMBER(2)	OUTPUT CURRENT	PACKAGE(1)	BODY SIZE (NOM)
TPSM828510	0.5 A	RDY (QFN, 9)	2.7 mm × 3.0 mm × 2.0 mm
TPSM828511	1 A		
TPSM828512	2 A		

(1) For more information, see Section 12.
(2) See the *Device Comparison Table*.



Simplified Schematic



Efficiency vs Output Current; V_{OUT} = 2.5 V

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4 Device Comparison Table

DEVICE NUMBER	OUTPUT CURRENT	OUTPUT VOLTAGE	TYPICAL INPUT CAPACITOR	TYPICAL OUTPUT CAPACITOR
TPSM828510RDY	0.5 A	Adjustable	2 × 4.7 µF	2 × 10 µF
TPSM828511RDY	1 A			
TPSM828512RDY	2 A			

5 Pin Configuration and Functions

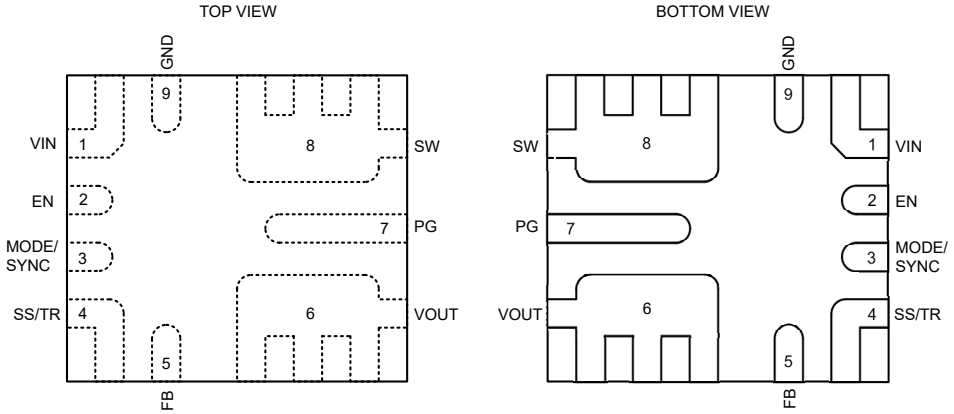


Figure 5-1. 9-Pin RDY QFN Package

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VIN	1	PWR	Power supply input. Connect the input capacitor as close as possible between the VIN and GND pins.
GND	9	PWR	Ground pin
SW	8	O	This pin is the switch pin of the converter. This pin is connected to the internal power MOSFET and the inductor. Avoid connecting this pin to larger traces as this can increase EMI. This pin can stay unconnected or be soldered to a small pad for thermal improvement.
PG	7	O	Open-drain power-good output with window comparator. This pin is pulled to GND while VOUT is outside the power-good threshold. This pin can be left open or tied to GND if not used. A pullup resistor can be connected to any voltage not larger than VIN.
VOUT	6	PWR	Output voltage pin. This pin is internally connected to the integrated inductor.
FB	5	I	Voltage feedback input. Connect the output voltage resistor divider to this pin.
SS/TR	4	I	Soft-start, tracking pin. A capacitor connected from this pin to GND defines the output voltage rise time. The pin can also be used as an input for tracking and sequencing - see *Voltage Tracking*.
MODE/SYNC	3	I	The device runs in PFM/PWM mode when this pin is pulled low. When the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. The MODE/SYNC pin can also be used to synchronize the device to an external frequency. See *Synchronizing to an External Clock*.
EN	2	I	This pin is the enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.

(1) I = input, O = output, N/A = not applicable

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN	–0.3	6.5	V
	SW (DC)	–0.3	V_{IN} + 0.3	V
	SW (AC, less than 10ns)(3)	–3	10	V
	SS/TR, PG	–0.3	V_{IN} + 0.3	V
	EN, MODE/SYNC, FB	–0.3	6.5	V
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal
(3) While switching

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.7		6	V
V_{OUT}	Output voltage range	0.6		5.5	V
C_{OUT}	Effective output capacitance(1)	8	10	200	µF
C_{IN}	Effective input capacitance(1)	5	10		µF
I_{SINK_PG}	Sink current at PG pin	0		2	mA
T_J	Junction temperature	–40		125	°C

(1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer´s DC bias curves for the effective capacitance vs DC voltage applied.

6.4 Thermal Information

THERMAL METRIC(1)		TPSM82851x RDY (JEDEC)(2) 9 PINS	TPSM82851x RDY (EVM) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.7	46.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.5	n/a	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.5	n/a	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18.3	20.8	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[1]		TPSM82851x RDY (JEDEC)[2] 9 PINS	TPSM82851x RDY (EVM) 9 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) JEDEC standard PCB with 4 layers, no thermal vias

6.5 Electrical Characteristics

Over operating junction remperature range (T_J = -40°C to +125°C) and V_{IN} = 2.7 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = V_{IN}, no load, device not switching, MODE = GND, V_{OUT} = 0.6 V		20	32	µA
I_{SD}	Shutdown current	EN = GND, typical value at TJ = 25°C, maximum value at TJ = 125°C		1.5	18	µA
V_{UVLO}	Undervoltage lock out threshold	V_{IN} rising	2.45	2.6	2.7	V
		V_{IN} falling	2.1	2.5	2.6	V
T_{JSD}	Thermal shutdown threshold	T_J rising		170		°C
	Thermal shutdown hysteresis	T_J falling		15		°C
CONTROL and INTERFACE						
$V_{EN,IH}$	Input threshold voltage at EN, rising edge		1.05	1.1	1.15	V
$V_{EN,IL}$	Input threshold voltage at EN, falling edge		0.96	1.0	1.05	V
V_{IH}	High-level input-threshold voltage at MODE/SYNC		1.1			V
$I_{EN,LKG}$	Input leakage current into EN	V_{IH} = V_{IN} or V_{IL} = GND			125	nA
V_{IL}	Low-level input-threshold voltage at MODE/SYNC				0.3	V
I_{LKG}	Input leakage current into MODE/SYNC				100	nA
t_{Delay}	Enable delay time	Time from EN high to device starts switching; V_{IN} applied already	85	150	470	µs
t_{Ramp}	Output voltage ramp time, C_{SS} = 4.7 nF	Time from device starts switching to power good; device not in current limit	0.8	1.3	1.8	ms
t_{Ramp}	Output voltage ramp time, SS/TR pin open	Time from device starts switching to power good; device not in current limit	90	150	210	µs
$I_{SS/TR}$	SS/TR source current		2	2.5	2.8	uA
	Tracking gain	V_{FB} / $V_{SS/TR}$		1		
	Tracking offset	V_{FB} when $V_{SS/TR}$ = 0 V		±1		mV
f_{SYNC}	Frequency range on MODE/SYNC pin for synchronization		1.8		4	MHz
	Duty cycle of synchronization signal at MODE/SYNC		20		80	%
	Time to lock to external frequency			50		µs
V_{TH_PG}	UVP power good threshold voltage; DC level	rising (%V_{FB})	92	95	98	%
V_{TH_PG}	UVP power good threshold voltage; DC level	falling (%V_{FB})	87	90	93	%

6.5 Electrical Characteristics (continued)

Over operating junction remperature range (T_J = -40°C to +125°C) and V_{IN} = 2.7 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TH_PG}	OVP power good threshold voltage; DC level	rising (%V_{FB})	107	110	113	%
	OVP power good threshold voltage; DC level	falling (%V_{FB})	104	107	111	%
$V_{PG,OL}$	Low-level output voltage at PG	I_{SINK_PG} = 2 mA		0.07	0.3	V
$I_{PG,LKG}$	Input leakage current into PG	V_{PG} = 5 V			100	nA
t_{PG}	PG deglitch time	for a high level to low level transition on the power good output		40		µs
OUTPUT						
V_{FB}	Feedback voltage, adjustable version			0.6		V
$I_{FB,LKG}$	Input leakage current into FB, adjustable version	V_{FB} = 0.6 V		1	70	nA
V_{FB}	Feedback voltage accuracy	PWM, $V_{IN} \geq V_{OUT}$ + 1 V	–1		1	%
V_{FB}	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT}$ + 1 V, $V_{OUT} \geq$ 1.0 V, $C_{o,eff} \geq$ 10 µF	–1		2	%
V_{FB}	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT}$ + 1 V, V_{OUT} < 1.0 V, $C_{o,eff} \geq$ 15 µF	–1		3	%
V_{FB}	Feedback voltage accuracy with voltage tracking	$V_{IN} \geq V_{OUT}$ + 1 V, $V_{SS/TR}$ = 0.3 V	–4		4	%
	Load regulation	PWM		0.05		%/A
	Line regulation	PWM, I_{OUT} = 1 A, $V_{IN} \geq V_{OUT}$ + 1 V		0.02		%/V
R_{DIS}	Output discharge resistance				100	Ω
f_{SW}	PWM Switching frequency		2.025	2.25	2.475	MHz
$t_{on,min}$	Minimum on-time of high-side FET	V_{IN} = 3.3 V, T_J = -40°C to 125°C		35	52	ns
$t_{on,min}$	Minimum on-time of low-side FET			10		ns
R_{DP}	Dropout resistance	$V_{IN} \geq$ 5 V		85	120	mΩ
I_{LIMH}	High-side FET switch current limit	DC value, for TPSM828512; V_{IN} = 3 V to 6 V	2.85	3.4	3.9	A
I_{LIMH}	High-side FET switch current limit	DC value, for TPSM828511; V_{IN} = 3 V to 6 V	2.1	2.6	3.0	A
I_{LIMH}	High-side FET switch current limit	DC value, for TPSM828510; V_{IN} = 3 V to 6 V	1.6	2.1	2.5	A
I_{LIMNEG}	Low-side FET negative current limit	DC value		–1.8		A

6.6 Typical Characteristics

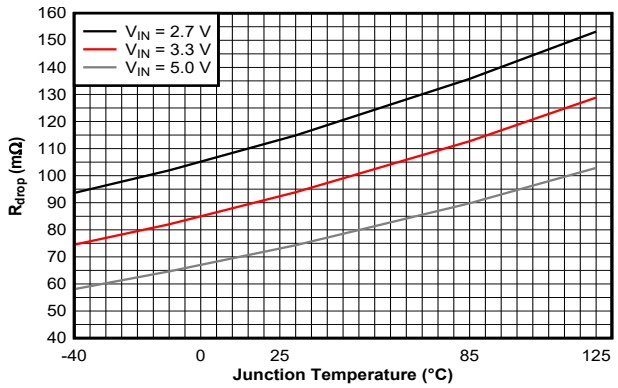


Figure 6-1. Dropout Resistance

7 Parameter Measurement Information

7.1 Schematic

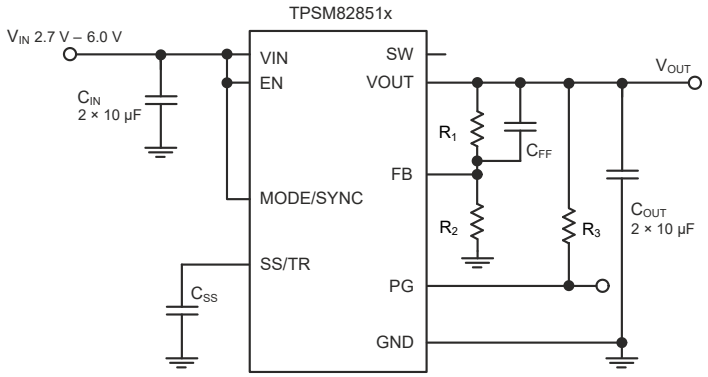


Figure 7-1. Measurement Setup for TPSM82851x

Table 7-1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER (1)
IC	TPSM828510 / TPSM828511 / TPSM828512	Texas Instruments
C_{IN}	2 × 10 µF / 6.3 V / GRM188D70J106MA73	Murata
C_{OUT}	2 × 10 µF / 6.3 V / GRM188D70J106MA73	Murata
C_{SS}	4.7 nF (equal to 1-ms start-up ramp); GCM188R72A472KA37	Any
C_{FF}	10 pF	Any
R_1	Depending on VOUT	Any
R_2	Depending on VOUT	Any
R_3	100 kΩ	Any

(1) See the *Third-party Products Disclaimer*.

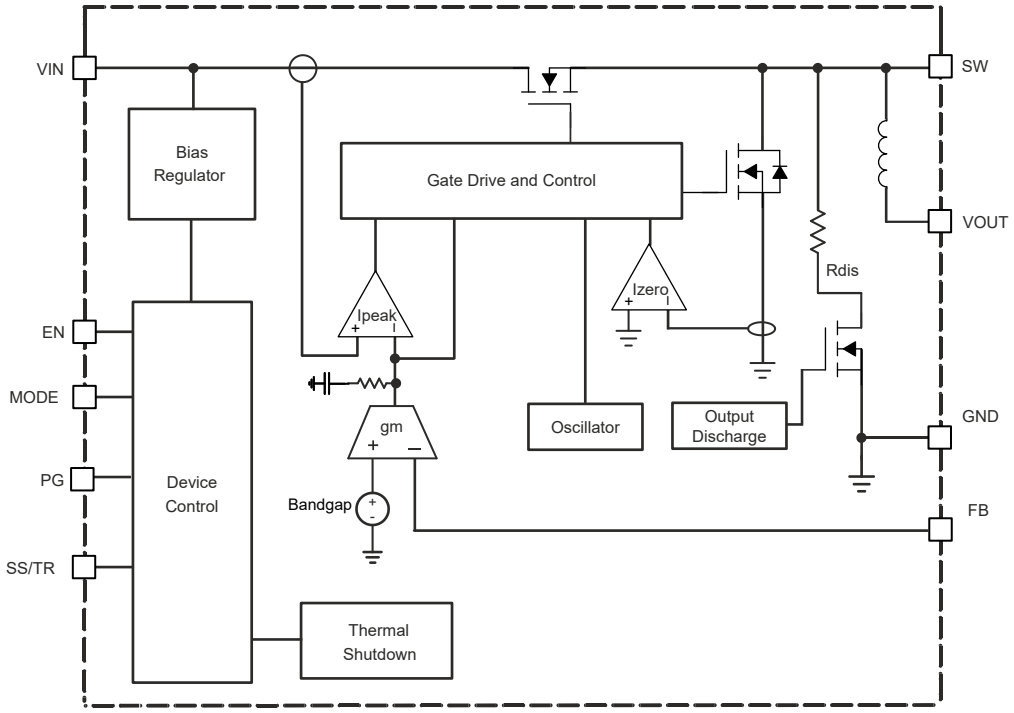
8 Detailed Description

8.1 Overview

The TPSM82851x synchronous, switch mode, DC/DC converter power modules are based on a fixed-frequency peak current-mode control topology. The control loop is internally compensated. To optimize the bandwidth of the control loop to the wide range of output capacitance that can be used with the TPSM82851x. The regulation network achieves fast and stable operation with small external components and low-ESR ceramic output capacitors.

The devices support fixed-frequency forced PWM operation with the MODE/SYNC pin tied to a logic high level. When the MODE/SYNC pin is set to a logic low level, the device operates in power save mode (PFM) at low-output currents and automatically transitions to fixed-frequency PWM mode at higher output currents. In PFM mode, the switching frequency decreases linearly based on the load to sustain high efficiency down to very low output currents. The device can be synchronized to an external clock signal in a range from 1.8 MHz to 4 MHz applied to the MODE/SYNC pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Precise Enable (EN)

The voltage applied at the enable pin of the TPSM82851x is compared to a fixed threshold of 1.1 V for a rising voltage. This comparison allows you to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The Precise Enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of the Enable pin.

The enable input threshold for a falling edge is typically 100 mV lower than the rising edge threshold. The TPSM82851x starts operation when the rising threshold is exceeded. For proper operation, terminate and do not leave the enable (EN) pin floating. Pulling the enable pin low forces the device into shutdown, with a shutdown current of typically 1 µA. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off. See the *Achieving a Clean Start-up by Using a DC/DC Converter with a Precise Enable-pin Threshold analog design journal* for more details.

8.3.2 MODE/SYNC

When MODE/SYNC is set low, the device operates in PWM or PFM mode, depending on the output current. The MODE/SYNC pin forces PWM mode when set high. The pin also allows you to apply an external clock in a frequency range from 1.8 MHz to 4 MHz for external synchronization. When an external clock is applied, the device operates in PWM mode. As with the switching frequency selection, the specification for the minimum on-time has to be observed when applying the external clock signal. The synchronization to the external clock is done on the falling edge of the applied clock to the rising edge of the internal SW pin. The MODE/SYNC pin can be changed during operation.

8.3.3 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the MOSFETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage goes below the falling threshold.

8.3.4 Power-Good Output (PG)

Power good is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. Power good is driven by a window comparator. PG is held low when the device is

- disabled,
- in undervoltage lockout,
- in thermal shutdown,
- or in soft start.

When the output voltage is in regulation hence, within the window defined in the electrical characteristics, the PG output is high impedance. V_{IN} must remain present for the PG pin to stay low. If the power-good output is not used, TI recommends to tie to GND or leave open. The PG indicator features a de-glitch, as specified in the electrical characteristics, for the transition from "high impedance" to "low" of the output.

Table 8-1. Power-Good Pin Logic

EN	DEVICE STATUS	PG LOGIC STATUS
X	V_{IN} < 2 V	Undefined
Low	V_{IN} ≥ 2 V	Low
High	2 V ≤ V_{IN} < V_{UVLO} OR in thermal shutdown OR V_{OUT} not in regulation OR device in soft start	Low
High	V_{OUT} in regulation	High impedance

8.3.5 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 170°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes low. When T_J decreases below the hysteresis amount of typically 15°C, the converter resumes normal operation, beginning with soft start. During PFM, the thermal shutdown is not active.

8.4 Device Functional Modes

8.4.1 Pulse Width Modulation (PWM) Operation

The TPSM82851x has two operating modes: Forced PWM mode and PFM/PWM mode.

With the MODE/SYNC pin set to high, the TPSM82851x operates with pulse width modulation in continuous conduction mode (CCM). The switching frequency is 2.25 MHz or defined by an external clock signal applied to the MODE/SYNC pin. With an external clock applied to MODE/SYNC, the TPSM82851x follow the frequency applied to the pin. In general, the frequency range in forced PWM mode is 1.8 MHz to 4 MHz. However, the frequency must be in a range the TPSM82851x can operate at, taking the minimum on-time into account.

8.4.2 Power Save Mode Operation (PFM/PWM)

When the MODE/SYNC pin is low, power save mode is allowed. The device operates in PWM mode as long as the peak inductor current is above the PFM threshold of about 0.8 A. When the peak inductor current drops below the PFM threshold, the device starts to skip switching pulses. In power save mode, the switching frequency decreases with the load current maintaining high efficiency.

8.4.3 100% Duty-Cycle Operation

The duty cycle of a buck converter operated in PWM mode is given as D = VOUT / VIN. The duty cycle increases as the input voltage comes close to the output voltage and the off-time gets smaller. When the minimum off-time of typically 10 ns is reached, the TPSM82851x skips switching cycles while approaching 100% mode. In 100% mode, the device keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the target. This feature is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT(min)} \times R_{DP} \quad (1)$$

where

- R_{DP} is the resistance from V_{IN} to V_{OUT}, which includes the high-side MOSFET on-resistance and DC resistance of the inductor.
- $V_{OUT\ (min)}$ is the minimum output voltage the load can accept.

8.4.4 Current Limit and Short-Circuit Protection

The TPSM82851x is protected against overload and short-circuit events. If the inductor current exceeds the current limit I_{LIMH}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. The high-side MOSFET turns on again only if the current in the low-side MOSFET has decreased below the low-side current limit. Due to internal propagation delays, the actual current can exceed the static current limit. The dynamic current limit is given as:

$$I_{peak} = I_{LIMH} + \frac{V_L}{L} \times t_{PD} \quad (2)$$

where

- I_{LIMH} is the static current limit, as specified in the electrical characteristics
- L is the effective inductance of the internal inductor (typical 0.47 µH)
- V_L is the voltage across the inductor ($V_{IN} – V_{OUT}$)
- t_{PD} is the internal propagation delay of typically 50 ns

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak} = I_{LIMH} + \frac{V_{IN} - V_{OUT}}{L} \times 50ns \quad (3)$$

8.4.5 Output Discharge

The purpose of the discharge function is to make sure a defined down-ramp of the output voltage when the device is disabled and keep the output voltage close to 0 V when the device is off. The output discharge feature is only active after the TPSM82851x has been enabled at least once since the supply voltage was applied. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active is typically 2 V. Output discharge is not activated during a current limit event.

8.4.6 Soft Start / Tracking (SS/TR)

The internal soft-start circuitry controls the output voltage slope during start-up. This control avoids excessive inrush current and makes sure a controlled output voltage rise time. This control also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high to start operation, the device starts switching after a delay of about 200 µs, then the internal reference and hence V_{OUT} rises with a slope controlled by an external capacitor connected to the SS/TR pin.

The SS/TR pin must not be connected to the SS/TR pin of other devices. TI recommends to keep C_{SS} at less than or equal to 47 nF. Larger capacitance can not fully discharge to zero during start-up. In this case the device starts the output voltage ramp at a value above zero Volt, leading to a short time period of increased device inrush current.

Leaving the SS/TR pin not connected provides the fastest start-up ramp with 160 µs typically. A capacitor connected from SS/TR to GND is charged with 2.5 µA by an internal current source during soft start. After the voltage on SS/TR exceeds 0.6 V the internal reference voltage of 0.6 V takes over control. The capacitance required to set a certain ramp-time (t_{ramp}) therefore is:

$$C_{SS}[nF] = \frac{2.5\mu A \times t_{ramp}[ms]}{0.6V} \quad (4)$$

If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin to GND to make sure a proper low level. Returning from those states causes a new start-up sequence.

A voltage of less than the internal reference voltage applied at SS/TR can be used as an external voltage reference. The following examples are potential applications for this feature:

- Track an external reference controller voltage. The output voltage follows this voltage in both directions up and down in forced PWM mode. In PFM mode, the output voltage decreases based on the load current in combination with the output capacitor value.
- Track another rail by connecting a voltage divider to the other rail and feed the junction point to SS/TR of this device as shown in Figure 9-28 and in Figure 9-29.
- Voltage sequencing and synchronization of multiple supply rails. Connect for example the open drain PG outputs of other converters to SS/TR of this converter to hold off output voltage generation until the other rails are ready and stable.
- Modulate the output voltage. The voltage level on the SS/TR pin can be changed dynamically during operation at any time after the device started switching. This can be used for example to implement dynamic core voltage scaling for MCUs/CPUs/SoCs.

Note: Apply external voltages above 0.6 V at SS/TR. This voltage is then ignored by the device and the internal reference voltage is used instead. The internal current source can pull the SS/TR pin with a pullup current of typical 2.5 µA above the 0.6-V level up to a level of approximately 1.5 V below VIN. This must be considered for the maximum voltage capability of the soft-start (SS) capacitor and for weak external voltage sources.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPSM82851x are synchronous, step-down, converter power modules. The required power inductor is integrated in a shielded version inside the TPSM82851x. The TPSM828510, TPSM828511, and TPSM828512 are pin-to-pin and BOM-to-BOM compatible, differing only in their rated output current.

9.2 Typical Application

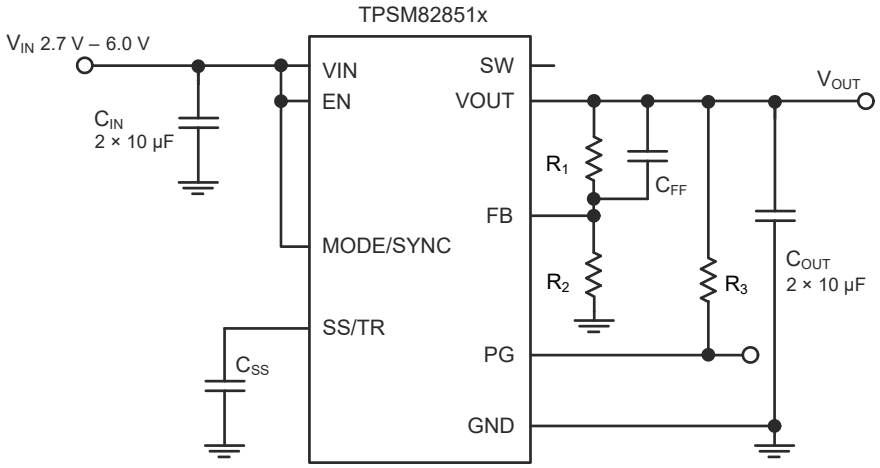


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

9.2.2 Detailed Design Procedure

9.2.2.1 Programming the Output Voltage

The output voltage of the TPSM82851x is adjustable. Choose resistors R1 and R2 to set the output voltage within a range of 0.6 V to 5.5 V according to Equation 5. To keep the feedback (FB) net robust from noise, set R2 equal to or lower than 100 kΩ to have at least 6 µA of current in the voltage divider. Lower values of FB resistors achieve better noise immunity, and lower light load efficiency, as explained in the *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter analog design journal*.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) \quad (5)$$

With V_{FB} = 0.6 V:

Table 9-1. Setting the Output Voltage

NOMINAL OUTPUT VOLTAGE V_{OUT}	R_1	R_2	C_{FF}	EXACT OUTPUT VOLTAGE
0.8 V	16.9 kΩ	51 kΩ	10 pF	0.7988 V
1.0 V	20 kΩ	30 kΩ	10 pF	1.0 V

Table 9-1. Setting the Output Voltage (continued)

NOMINAL OUTPUT VOLTAGE V_{OUT}	R_1	R_2	C_{FF}	EXACT OUTPUT VOLTAGE
1.1 V	39.2 kΩ	47 kΩ	10 pF	1.101 V
1.2 V	68 kΩ	68 kΩ	10 pF	1.2 V
1.5 V	76.8 kΩ	51 kΩ	10 pF	1.5 V
1.8 V	80.6 kΩ	40.2 kΩ	10 pF	1.803 V
2.5 V	47.5 kΩ	15 kΩ	10 pF	2.5 V
3.3 V	88.7 kΩ	19.6 kΩ	10 pF	3.315 V

9.2.2.2 Feedforward Capacitor

TI recommends a feedforward capacitor (C_{FF}) in parallel with R_1 to improve the transient response. Regardless of the FB resistor values, the C_{FF} value must always be 10 pF.

9.2.2.3 Input Capacitor

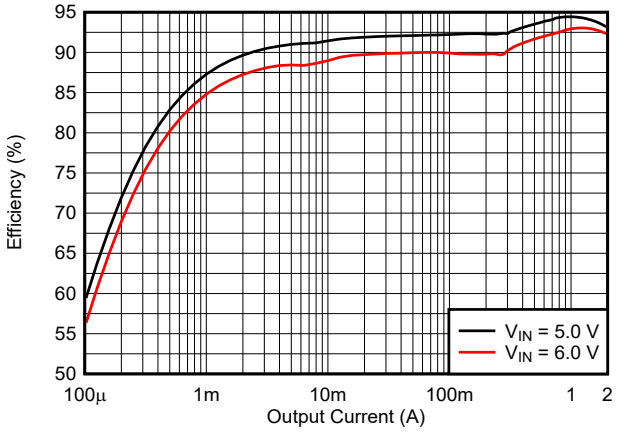
For most applications, 10-µF nominal is sufficient and recommended. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. TI recommends a low-ESR multilayer ceramic capacitor (MLCC) for best filtering and must be placed between VIN and GND as close as possible to those pins.

9.2.2.4 Output Capacitor

The architecture of the TPSM82851x allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and TI recommends them. To keep low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends to use X7R or X5R dielectric. Using a higher value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode.

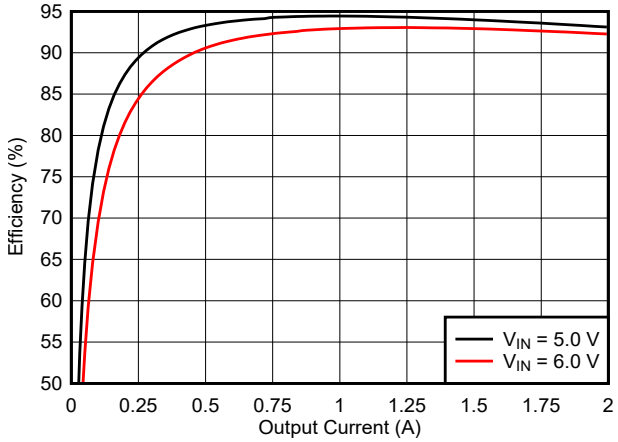
9.2.2.5 Application Curves

T_A = 25°C, V_{IN} = 5 V, V_{OUT} = 1.8 V, 1.8 MHz, PWM mode, BOM = Table 7-1 unless otherwise noted.



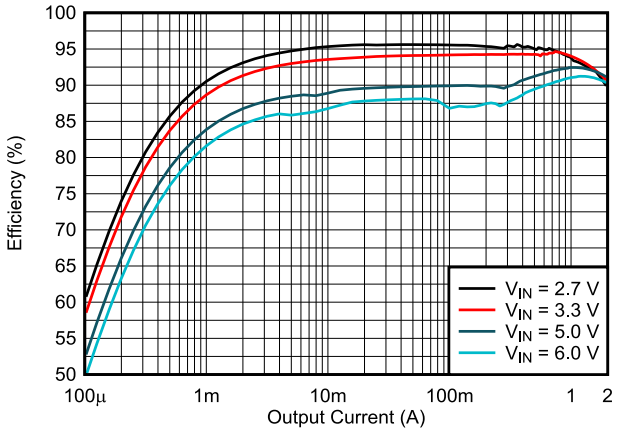
V_{OUT} = 3.3 V PFM T_A = 25°C

Figure 9-2. Efficiency versus Output Current



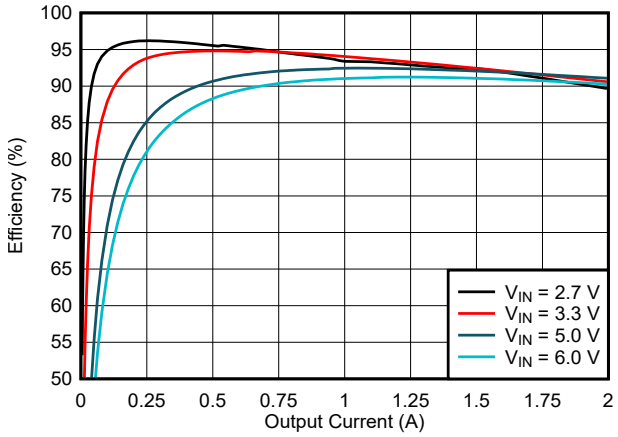
V_{OUT} = 3.3 V PWM T_A = 25°C

Figure 9-3. Efficiency versus Output Current



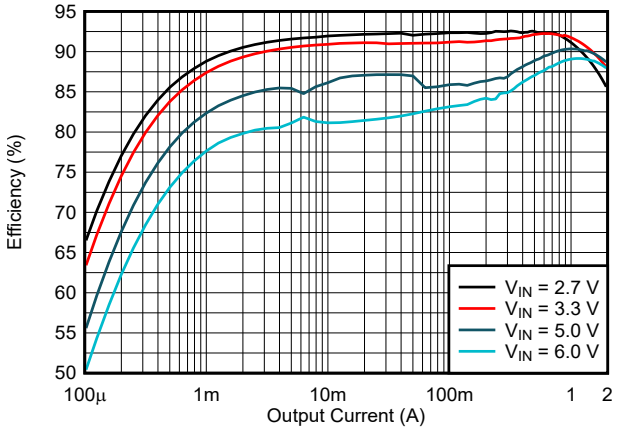
V_{OUT} = 2.5 V PFM T_A = 25°C

Figure 9-4. Efficiency versus Output Current



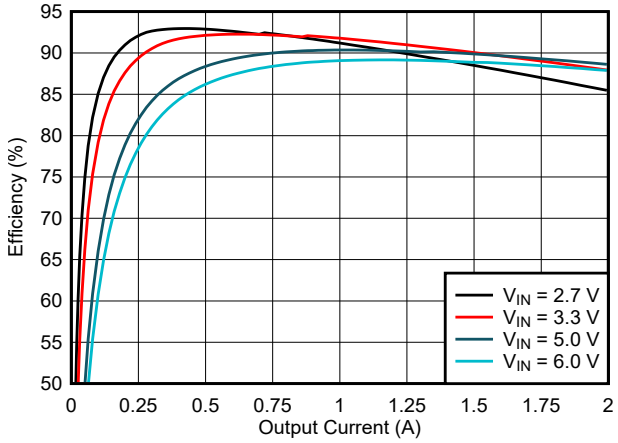
V_{OUT} = 2.5 V PWM T_A = 25°C

Figure 9-5. Efficiency versus Output Current



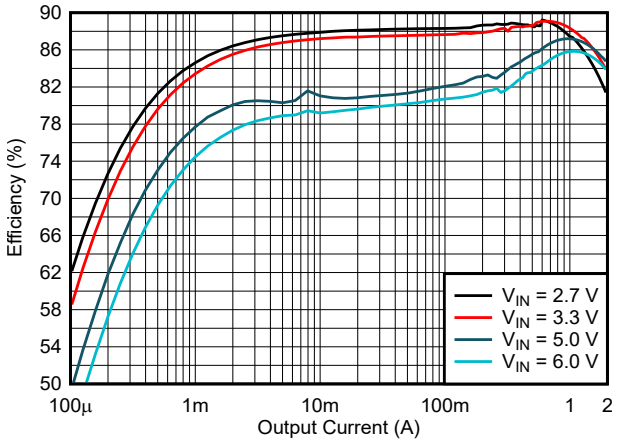
V_{OUT} = 1.8 V PFM T_A = 25°C

Figure 9-6. Efficiency versus Output Current



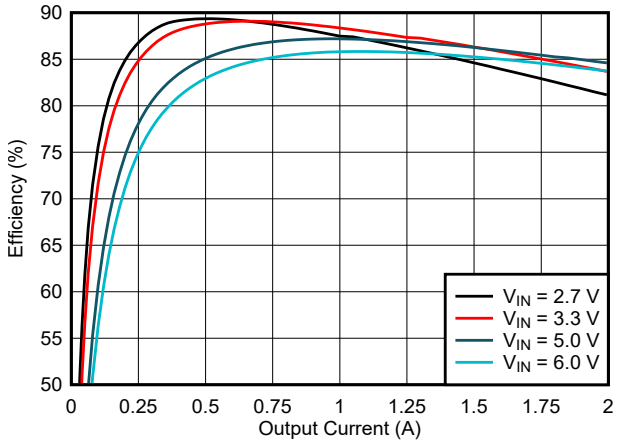
V_{OUT} = 1.8 V PWM T_A = 25°C

Figure 9-7. Efficiency versus Output Current



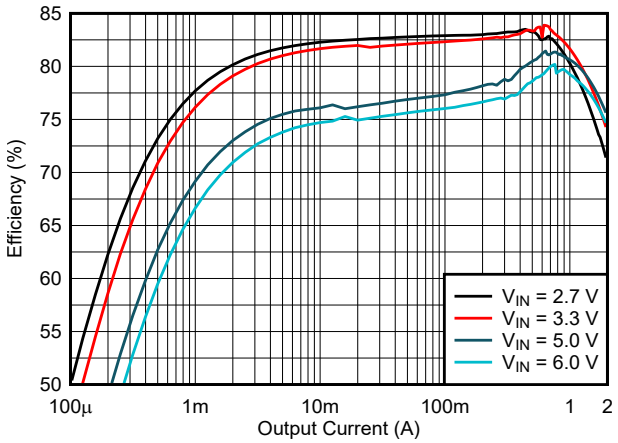
V_{OUT} = 1.2 V PFM T_A = 25°C

Figure 9-8. Efficiency versus Output Current



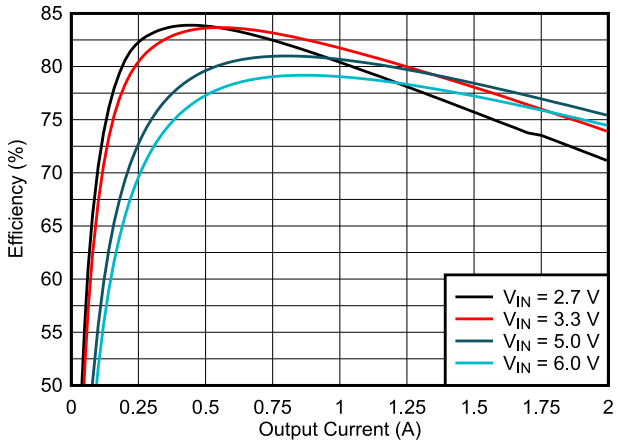
V_{OUT} = 1.2 V PWM T_A = 25°C

Figure 9-9. Efficiency versus Output Current



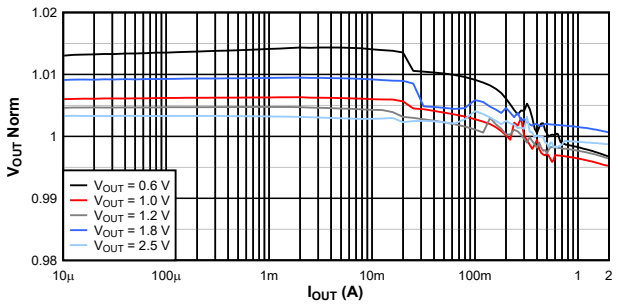
V_{OUT} = 0.6 V T_A = 25°C

Figure 9-10. Efficiency versus Output Current



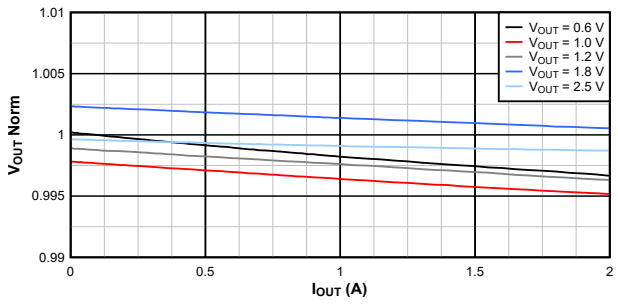
V_{OUT} = 0.6 V T_A = 25°C

Figure 9-11. Efficiency versus Output Current



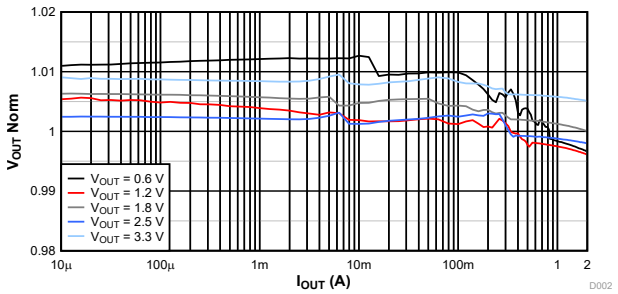
PFM Mode T_A = 25°C

Figure 9-12. Load Regulation V_{IN} = 3.3 V



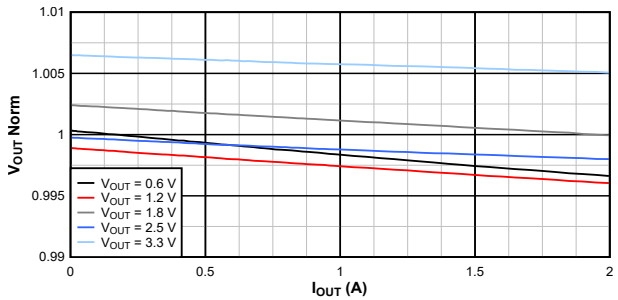
PWM Mode T_A = 25°C

Figure 9-13. Load Regulation V_{IN} = 3.3 V



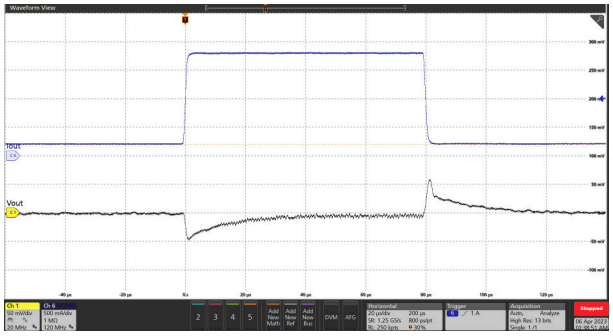
PFM Mode T_A = 25°C

Figure 9-14. Load Regulation V_{IN} = 5 V



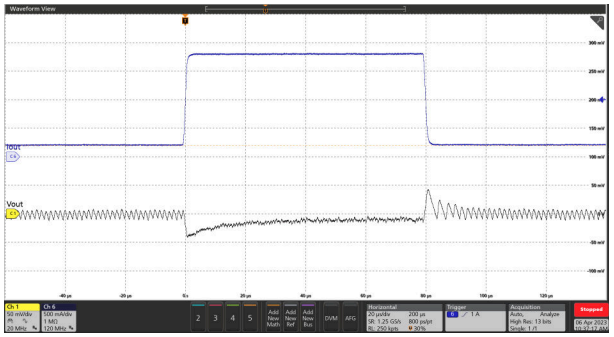
PWM Mode T_A = 25°C

Figure 9-15. Load Regulation V_{IN} = 5 V



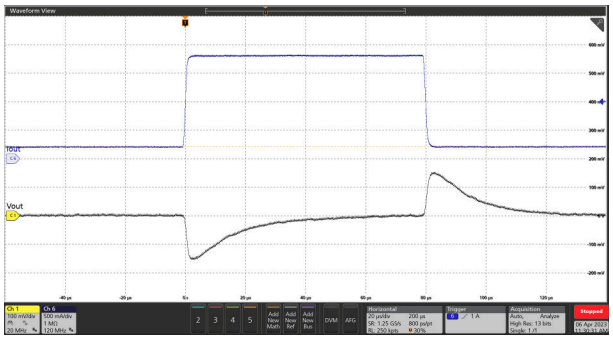
V_{OUT} = 0.6 V PWM T_A = 25°C
V_{IN} = 3.3 V I_{OUT} = 0.2 A to 1.8 A

Figure 9-16. Load Transient Response



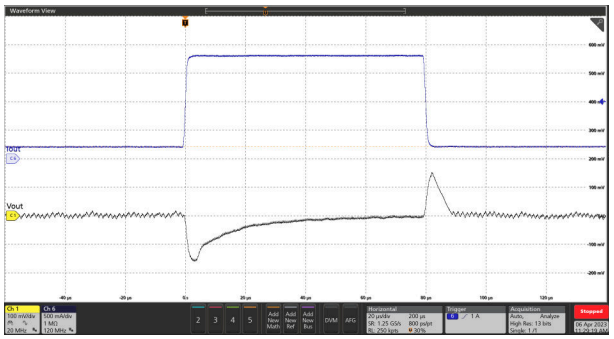
V_{OUT} = 0.6 V PFM T_A = 25°C
V_{IN} = 3.3 V I_{OUT} = 0.2 A to 1.8 A

Figure 9-17. Load Transient Response



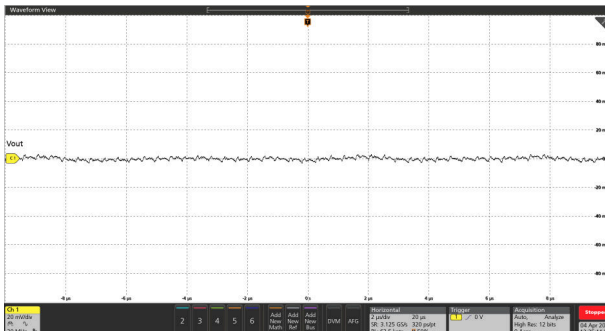
V_{OUT} = 3.3 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A

Figure 9-18. Load Transient Response



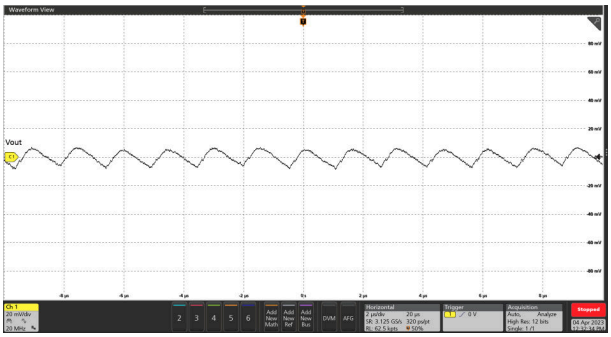
V_{OUT} = 3.3 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A

Figure 9-19. Load Transient Response



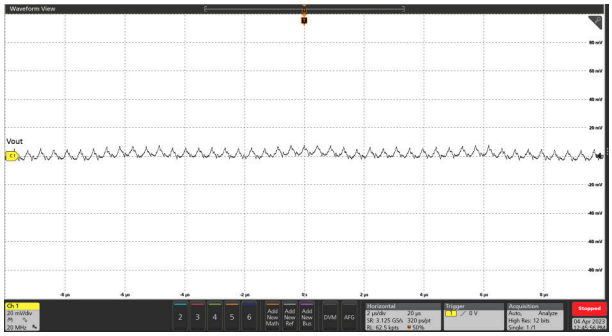
V_{OUT} = 0.6 V | PWM | T_A = 25 °C
I_{OUT} = 0.2 A | V_{IN} = 3.3 V | BW = 20 MHz

Figure 9-20. Output and Input Voltage Ripple



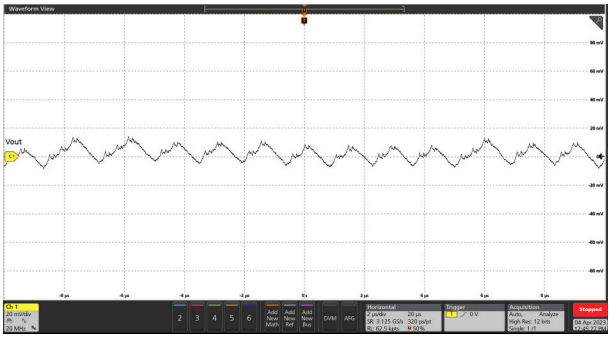
V_{OUT} = 0.6 V | PFM | T_A = 25°C
I_{OUT} = 0.2 A | V_{IN} = 3.3 V | BW = 20 MHz

Figure 9-21. Output and Input Voltage Ripple



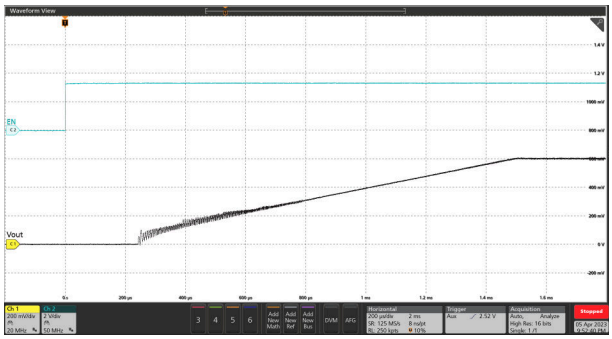
V_{OUT} = 3.3 V | PWM | T_A = 25 °C
I_{OUT} = 0.2 A | V_{IN} = 5.0 V | BW = 20 MHz

Figure 9-22. Output and Input Voltage Ripple



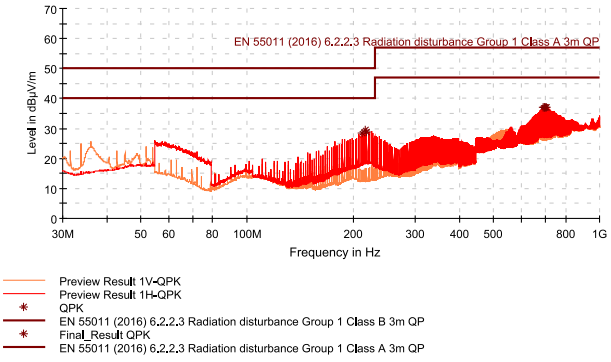
V_{OUT} = 3.3 V | PFM | T_A = 25°C
I_{OUT} = 0.2 A | V_{IN} = 5.0 V | BW = 20 MHz

Figure 9-23. Output and Input Voltage Ripple



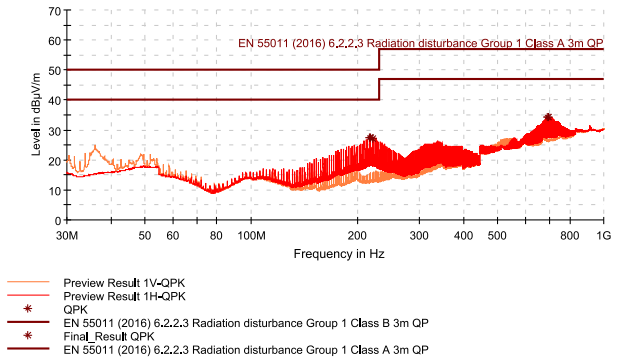
V_{OUT} = 0.6 V | PWM/PFM | T_A = 25°C
I_{OUT} = 2 A | V_{IN} = 3.3 V | C_{SS} = 4.7 nF

Figure 9-24. Start-Up Timing



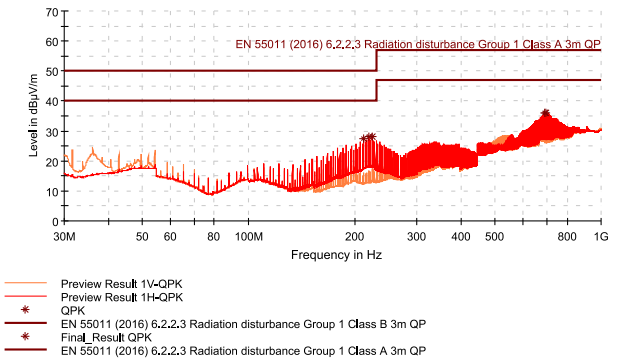
V_{OUT} = 1.2 V | PWM | T_A = 25°C
I_{OUT} = 2 A | V_{IN} = 6 V | measured on TPSM828512EVM

Figure 9-25. Radiated Emissions



V_{OUT} = 1.8 V
I_{OUT} = 2 A
PWM
V_{IN} = 6 V
T_A = 25°C
measured on
TPSM828512EVM

Figure 9-26. Radiated Emissions



V_{OUT} = 3.3 V
I_{OUT} = 2 A
PWM
V_{IN} = 6 V
T_A = 25°C
measured on
TPSM828512EVM

Figure 9-27. Radiated Emissions

9.3 System Examples

9.3.1 Voltage Tracking

The SS/TR pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in Figure 9-28. From 0 V to 0.6 V, the internal reference voltage to the internal error amplifier follows the SS/TR pin voltage. When the SS/TR pin voltage is above 0.6 V, the voltage tracking is disabled and the FB pin voltage is regulated at 0.6 V. The device achieves ratiometric or coincidental (simultaneous) output tracking, as shown in Figure 9-29.

Set the R2 value properly to achieve accurate voltage tracking by taking the 2.5-µA charging current into account. 1 kΩ or smaller is a sufficient value for R2. For decreasing SS/TR pin voltage, the device does not sink current from the output when the device is in PFM mode. The resulting decrease of the output voltage can be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is VIN+0.3 V.

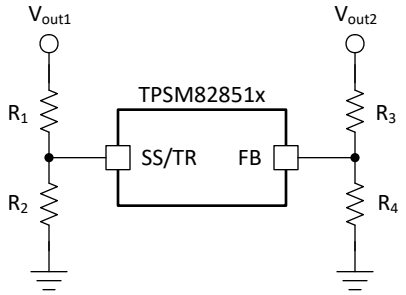


Figure 9-28. Schematic for Output Voltage Tracking

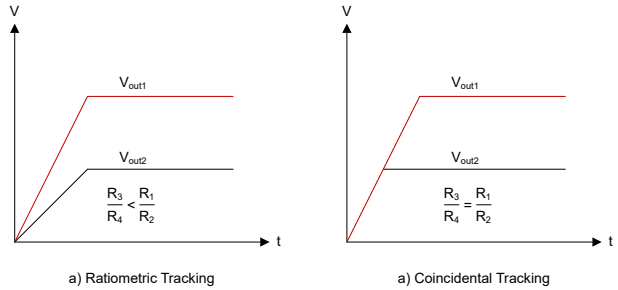


Figure 9-29. Output Voltage Tracking

9.3.2 Synchronizing to an External Clock

The TPSM82851x can be synchronized by applying a clock on the MODE/SYNC pin. There is no need for any additional circuitry. See Figure 9-30. The clock can be applied, changed, and removed during operation. TI recommends the value of the R_{CF} resistor to be chosen such that the internally defined frequency and the externally-applied frequency are close to each other to have a fast settling time to the external clock. Synchronizing to a clock is not possible, if the COMP/FSET pin is connected to Vin or GND. Figure 9-31 and Figure 9-32 show the external clock being applied and removed. When an external clock is applied, the device operates in PWM mode.

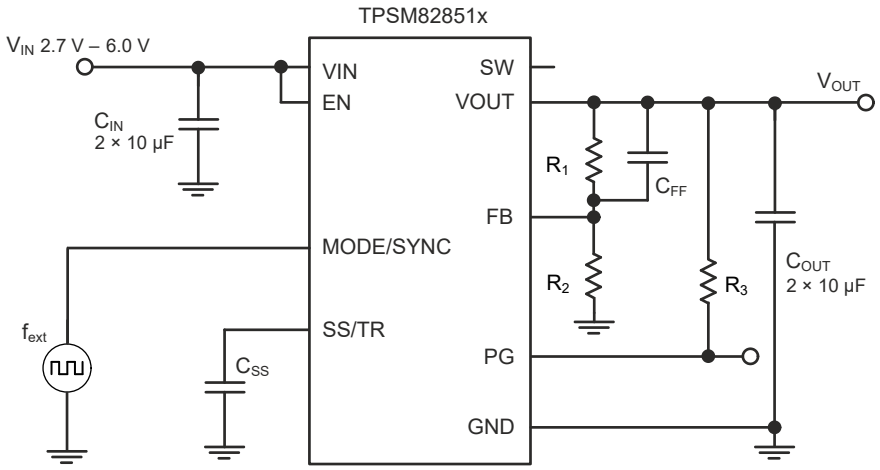
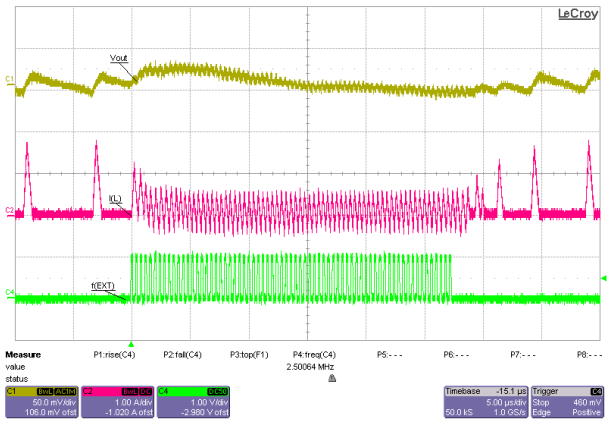
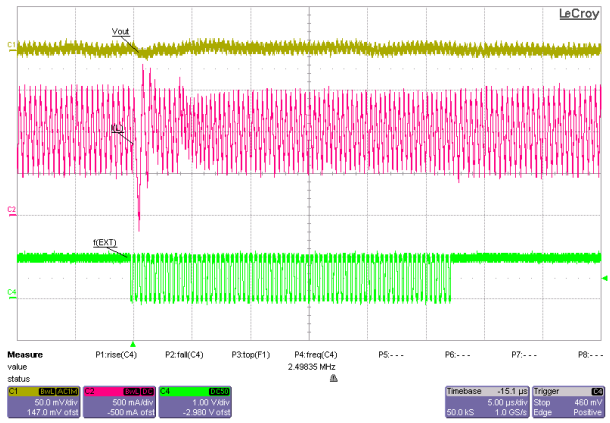


Figure 9-30. Frequency Synchronization



V_{IN} = 5 V R_{CF} = 8.06 kΩ I_{OUT} = 0.1 A
V_{OUT} = 1.8 V f_{EXT} = 2.5 MHz

Figure 9-31. Applying and Removing the Synchronization Signal (PFM)



V_{IN} = 5 V R_{CF} = 8.06 kΩ I_{OUT} = 1 A
V_{OUT} = 1.8 V f_{EXT} = 2.5 MHz

Figure 9-32. Applying and Removing the Synchronization Signal (FPWM)

9.4 Power Supply Recommendations

The TPSM82851x device family has no special requirements for the input power supply. Rate the output current of the input power supply according to the supply voltage, output voltage, and output current of the TPSM82851x.

9.5 Layout

9.5.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPSM82851x demands careful attention to make sure of best performance. A poor layout can lead to issues like bad line and load regulation, instability, increased EMI radiation, and noise sensitivity. Refer to the *Five Steps to a Great PCB Layout for a Step-Down Converter analog design journal* for a detailed discussion of general best practices. Specific recommendations for the device are listed below.

- Place the input capacitor as close as possible to the VIN and GND pins of the device. This placement is the most critical component placement. Route the input capacitor directly to the VIN and GND pins avoiding vias.
- Place the output capacitor ground close to the VOUT and GND pins and route directly avoiding vias.
- Place the FB resistors, R1 and R2, and the feedforward capacitor C_{FF} close to the FB pin and place C_{SS} close to the SS/TR pin to minimize noise pickup.
- The recommended layout is implemented on the EVM and shown in *TPSM82851xEVM Evaluation Module EVM user's guide* and in *Layout Example*.
- See the recommended land pattern for the TPSM82851x at the end of this data sheet. For best manufacturing results, create the pads as solder mask defined (SMD), when some pins (such as VIN, VOUT, and GND) are connected to large copper planes. Using SMD pads keeps each pad the same size and avoids solder pulling the device during reflow.

9.5.2 Layout Example

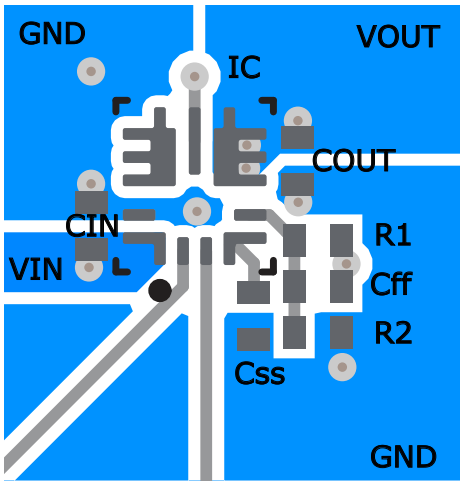


Figure 9-33. Example Layout

9.5.2.1 Thermal Consideration

The TPSM82851x module temperature must be kept less than the maximum rating of 125°C. The following are three basic approaches for enhancing thermal performance:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the approximate module temperature of the TPSM82851x, apply the typical efficiency stated in this data sheet to the desired application condition to compute the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by the power dissipation thermal resistance. For more details on how to use the thermal parameters in real applications, see the application notes: *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics*.

The thermal values in *Thermal Information* used the recommended land pattern, shown at the end of this data sheet, including the 18 vias as shown. The TPSM82851x was simulated on a PCB defined by JEDEC 51-7. The 9 vias on the GND pins were connected to copper on other PCB layers, while the remaining 9 vias were not connected to other layers.

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPSM82810EVM-089 Evaluation Module* EVM user's guide
- Texas Instruments, *TPSM82851xEVM Evaluation Module* EVM user's guide
- Texas Instruments, *Five Steps to a Great PCB Layout for a Step-Down Converter analog design journal*
- Texas Instruments, *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter* analog design journal
- Texas Instruments, *Achieving a Clean Start-up by Using a DC/DC Converter with a Precise Enable-pin Threshold* analog design journal
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2023	*	Initial release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM828510RDYR	ACTIVE	QFN-FCMOD	RDY	9	3000	RoHS & Green	Call TI	Call TI	-40 to 125	88510	Samples
TPSM828511RDYR	ACTIVE	QFN-FCMOD	RDY	9	3000	RoHS & Green	Call TI	Call TI	-40 to 125	88511	Samples
TPSM828512RDYR	ACTIVE	QFN-FCMOD	RDY	9	3000	RoHS & Green	Call TI	Call TI	-40 to 125	88512	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

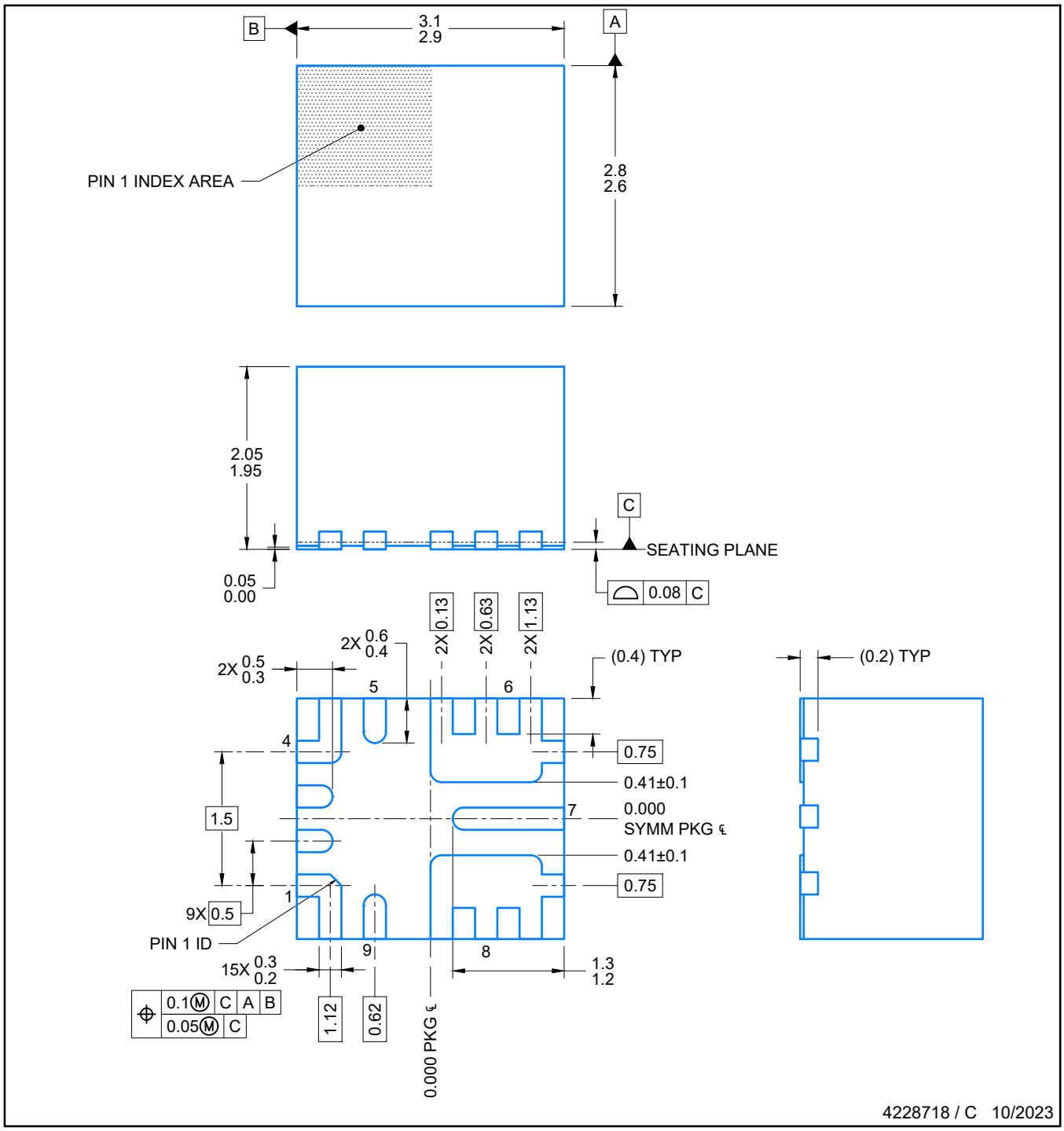
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

RDY0009A

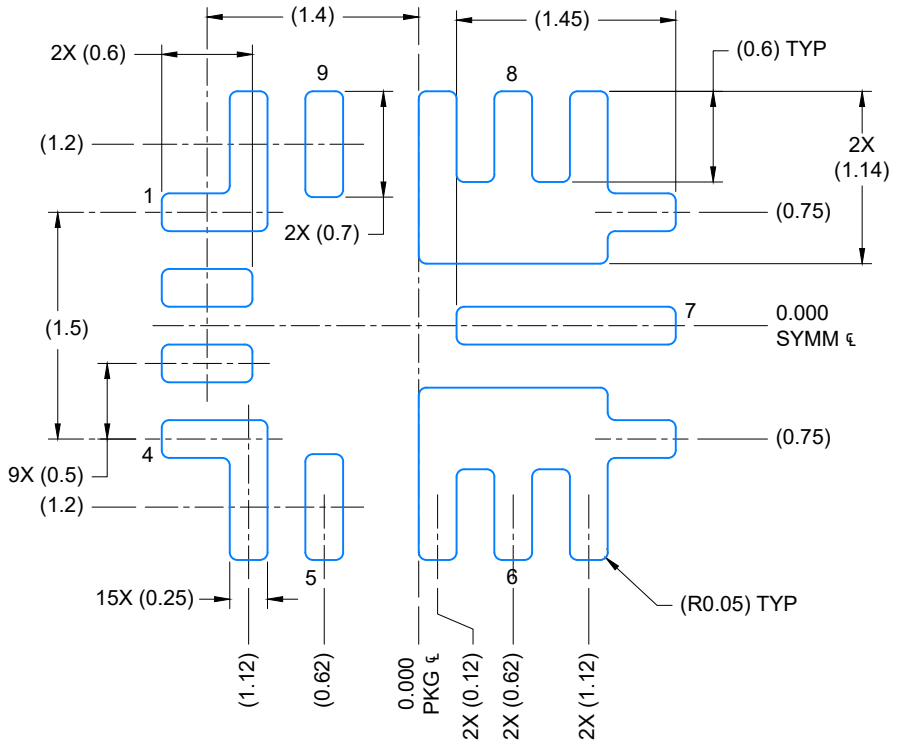
QFN - FCMOD - 2.05 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

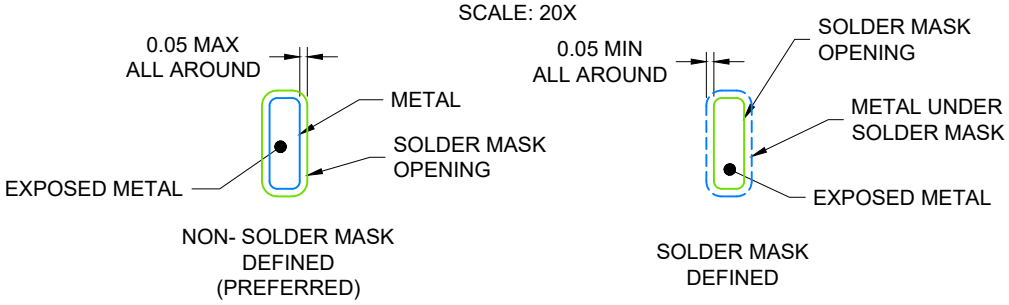
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X



SOLDER MASK DETAILS

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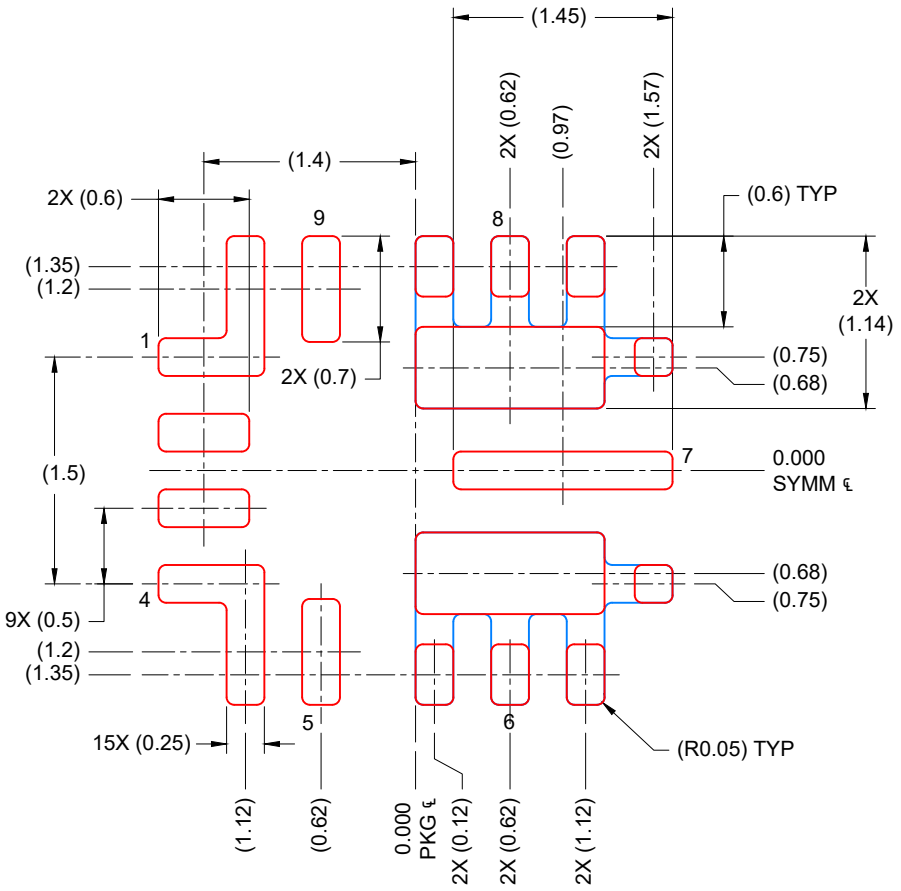
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 6 & 8 = 84%
SCALE: 20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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