TUSB2E11 USB 2.0-eUSB2 Repeater

1 Features

- USB 2.0 and eUSB2 (rev 1.2) compliant
- Low-speed, full-speed, high-speed signaling
- Best-in-class high-speed total jitter of 20ps
- Register access protocol receptor capable
- Host and device mode (dual-role device) support
- Auto detection for I^2C or strap-pin options
  - Three strap-pins for USB 2.0 high-speed channel compensation settings
  - I^2C device interface for more configurations
- Device variants
  - eUSB2 1.0V or 1.2V signaling interface
  - eUSB2 trace loss compensation levels for different product form-factors
  - 1.2V or 1.8V I^2C interface
- Optional battery charging and detection support
  - BC 1.2 CDP or DCP divider mode advertising
  - Data-aware USB Type-C™ compatible BC 1.2 SDP, CDP, and DCP divider mode detection
  - Dual-role auto switching between charger advertising or detection
- CTA-936 USB Carkit UART support
- Supports auto-resume ECR as well as L2 interrupt resume mode
- Optional GPIOs: interrupt GPIO2, debug, I^2C ↔ GPIO0/1
- I^2C accessible debug capabilities for manufacturing tests

2 Applications

- Notebooks and desktops
- Cell phones
- Tablets
- Wearables
- Portable electronics

3 Description

The TUSB2E11 is a USB compliant eUSB2 to USB 2.0 repeater supporting both device and host modes.

The device supports USB low-speed (LS), full-speed (FS) signals, and high-speed (HS) signals.

The device has multiple patented designs to provide robust interoperability, optimum performance, and power.

For systems without an I^2C interface, the device offers eight individual settings with three strap-pins for USB 2.0 channel Equivalent Series Resistance (ESR) up to 20Ω. Device variants are available for different levels of eUSB2 trace length compensation up to 10 inches.

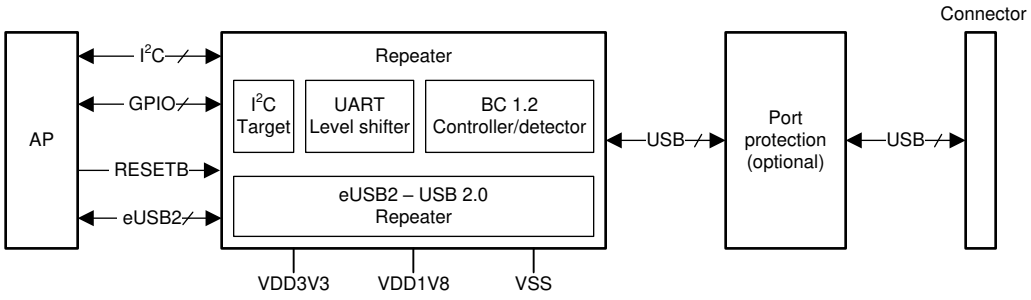
The I^2C interface permits additional flexibility for fine tuning of device RX equalization and TX amplitude, slew rate and pre-emphasis to pass electrical compliance tests and compensate for channel loss.

Various debug options are available through the three GPIO pins that can be configured to monitor various USB bus states or interrupt as well as CTA-936 UART mode that can provide SoC debug capabilities. GPIO0 and GPIO1 can be used as general purpose I^2C to GPIOs bridge.

Package Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE(3)
TUSB2E11	YCG (DSBGA, 15)	1.75mm × 1.05mm

(1) See the *Device Comparison* table.
(2) For more information, see Section 14.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Device Version Comparison....2
4.1 Device Variants....3
5 Pin Configuration and Functions....4
6 Specifications....9
6.1 Absolute Maximum Ratings....9
6.2 ESD Ratings....9
6.3 Recommended Operating Conditions....9
6.4 Thermal Information....10
6.5 Electrical Characteristics....10
6.6 Switching Characteristics....17
6.7 Timing Requirements....19
6.8 Typical Characteristics....21
7 Parameter Measurement Information....22
8 Detailed Description....23
8.1 Overview....23
8.2 Functional Block Diagram....23
8.3 Feature Description....24
8.4 Device Functional Modes....24
8.5 Manufacturing Test Modes....30
8.6 I²C Target Interface....32
9 Register Access Protocol (RAP)....34
10 Register Map....35
10.1 TUSB2E11 Registers....35
11 Application and Implementation....48
11.1 Application Information....48
11.2 Typical Application....48
11.3 Power Supply Recommendations....51
11.4 Layout....52
12 Device and Documentation Support....54
12.1 Device Support....54
12.2 Documentation Support....54
12.3 Receiving Notification of Documentation Updates....54
12.4 Support Resources....54
12.5 Trademarks....54
12.6 Electrostatic Discharge Caution....54
12.7 Glossary....54
13 Revision History....54
14 Mechanical, Packaging, and Orderable Information....55

4 Device Version Comparison

Table 4-1. Device Register Comparison Table

	Register Address	B0 default	B1 default
Table 10-5	0x70h	0x73h	0x7Ch
Table 10-6	0x71h	0x38h	0x3Ch
Table 10-7	0x72h	0x90h	0x92h
Table 10-8	0x73h	0x04h	0x83h
Table 10-9	0x77h	0x00h	0x00h
Table 10-10	0x78h	0x0Bh	0x0Bh
Table 10-11	0x79h	0x40h	0x60h
Table 10-12	0x50h	0x02h	0x02h
Table 10-13	0xB0h	0x02h	0x03h
Table 10-14	0xB2h	0x00h	0x00h
Table 10-15	0xB3h	0x00h	0x00h
Table 10-16	0xB4h	0x00h	0x00h
Table 10-18	0xB6h	0xC0h	0xC0h
Table 10-22	0x60h	0x00h	0x00h
Table 10-23	0xF5h	0x32h	0x32h

Table 4-2. Device Feature Comparison Table

Features	B0	B1
Low Power Mode (RESETB = low)	not supported	supported (9 µW)
Auto-resume ECR	not supported	supported (enabled by default) [see register 0x78h]
L2 State Interrupt Resume	supported	supported

4.1 Device Variants

The following table describes the key differences between TUSB2E11x device variants.

Table 4-3. Device Variant Information

Orderable Device	Package Type	Package Drawing	Pins	Version	I/O Voltage(1)	Device Marking
TUSB2E111YCGR	WCSP	YCG	15	B1	1.8V	T2E111A
TUSB2E112YCGR	WCSP	YCG	15	B1	1.2V	T2E112

(1) **I/O Voltage:** I2C Bus voltage and GPIO voltage

For more information and availability of device variants such as eUSB2 1.0 signaling interface, 1.2V I^2C interface, and 1.2V GPIO interface please contact support.

5 Pin Configuration and Functions

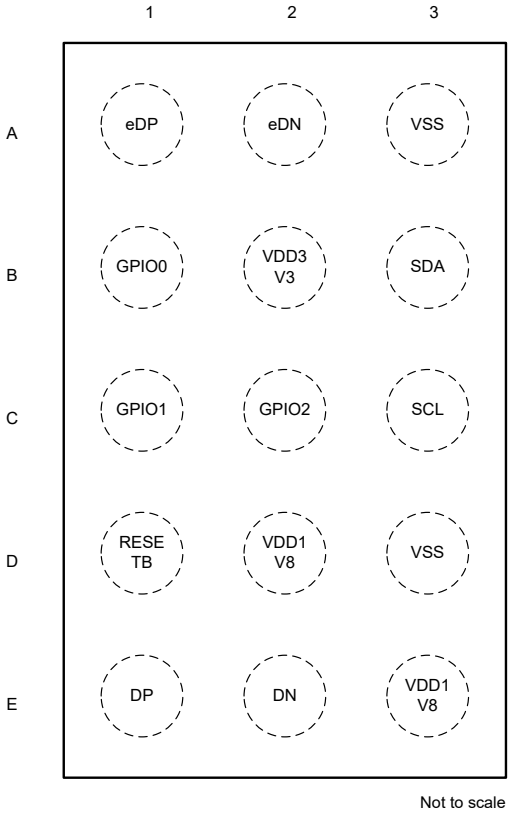


Figure 5-1. TUSB2E11 YCG Package, 15-Pin DSBGA (Top View)

Table 5-1. Pin Functions

PIN		TYPE[2]	REST STATE	ASSOCIATED ESD SUPPLY	DESCRIPTION				
NAME	NO.								
VDD3V3	B2	PWR	N/A	N/A	3.3V Supply Voltage				
VDD1V8	D2, E3	PWR	N/A	N/A	1.8V Supply Voltage				
VSS	A3, D3	GND	N/A	N/A	GND				
RESETB	D1	I	N/A	VDD1V8	• Active Low Reset • Upon deassertion of RESETB, the repeater is enabled and be in eUSB2 default mode awaiting configuration from eDSPr or eUSPr. • If RESETB is not actively controlled, a pullup resistor 100kΩ to VDD1V8 is required.				
SCL	C3	I	Internal pulldown 1MΩ typical (disabled after reset)[1]	VDD1V8	I^2C Clock	Device Mode Matrix	**SCL**	**SDA**	**Mode**
							Low	See Table 5-4 for more details	Non-I^2C USB Repeater
SDA	B3	I/O	Hi-Z[1]	VDD1V8	Bidirectional I^2C data Open drain I/O		High	Low	Non-I^2C UART mode Repeater
							High	High	I^2C Enabled

Table 5-1. Pin Functions (continued)

PIN		TYPE[2]	REST STATE	ASSOCIATED ESD SUPPLY	DESCRIPTION
NAME	NO.				
GPIO2	C2	I/O	Internal pulldown 1MΩ typical (disabled after reset)	VDD1V8	• In I^2C mode GPIO2 is an open-drain active low level interrupt output. Connect GPIO2 to input of APU and a pullup resistor to use interrupt features • In non I^2C mode GPIO2 defaults to USB configuration input at power up reset. • When a pullup resistor is used to set high input, ensure VIH is met accounting for internal pulldown as small as 500kΩ • GPIO2 is an open-drain output after reset and can be left floating when not used.
GPIO0	B1	I/O	Internal pulldown 1MΩ typical (disabled after reset)[1]	VDD1V8	Defaults to an input mode at power up reset. RESETB assertion and deassertion or soft reset reverts GPIO0 to input mode • In I^2C mode GPIO0 defaults to control Carkit UART mode: active low to enable Carkit UART mode. Default Carkit UART direction is DP → eDP (RX) and eDN → DN (TX). GPIO0 must be pulled up to be in USB repeater mode. • In non I^2C mode GPIO0 defaults to USB configuration input at power up reset. • When a pullup resistor is used to set high input, ensure VIH is met accounting for internal pulldown as small as 500kΩ
GPIO1	C1	I/O	Internal pulldown 1MΩ typical (disabled after reset)[1]	VDD1V8	Defaults to an input mode at power up reset. RESETB assertion and deassertion or soft reset reverts GPIO1 to input mode • In I^2C mode GPIO1 defaults to debug input • In non I^2C mode GPIO1 defaults to USB Configuration input at power up reset. • When a pullup resistor is used to set high input, ensure VIH is met accounting for internal pulldown as small as 500kΩ
eDN	A2	I/O	Hi-Z	VDD1V8	eUSB2 port D-
eDP	A1	I/O	Hi-Z	VDD1V8	eUSB2 port D+
DN	E2	I/O	Hi-Z	VDD3V3	USB port D-
DP	E1	I/O	Hi-Z	VDD3V3	USB port D+

(1) When configured as an input but not actively driven, use 1MΩ external pulldown to strap low.
(2) I = input, I/O = input or output, PWR= power, GND = ground

Table 5-2. Pin Configuration for Device Mode

Device Mode	SCL (C3)	SDA (B3)	GPIO0 (B1)	GPIO1 (C1)	GPIO2 (C2)
I^2C Mode	Pull-up Input sampled at reset	Pull-up Input sampled at reset	Default to Input • Low = UART Mode • High = USB repeater mode Function can be reconfigured through register	Default to Input Function can be reconfigured through register	Default to Open drain output (can be left floating when not used) Function can be reconfigured through register
Non I^2C UART mode	Pull-up Input sampled at reset	Pull-down Input sampled at reset	Default to Input • Low = UART transfer enabled • High = UART transfer disabled	High-Z (can be left floating)	High-Z (can be left floating)
Non I^2C USB repeater mode	Pull-down Input sampled at reset See Table 5-4	See Table 5-4	Default input sampled at reset. See Table 5-3		

Table 5-3. Pin Configuration for USB PHY Tuning without I²C

GPIO2	GPIO1	GPIO0	Equivalent series resistance (ESR) between repeater and USB connector	U_EQ_P1 setting	U_HS_TX_AMPLITUDE_P1 setting	U_HS_TX_PRE_EMPHASIS_P1 setting	U_SQUELCH_THRESHOLD_P1 setting	U_DISCONNECT_THRESHOLD_P1 setting	HS Term
			Ω	dB	mV	dB	mV	mV	Ω
Float	Float	Float	2.5	0.06 (3'b000)	840 (4'b0101)	0.5 (3'b000)	104 (3'b100)	625 (4'b0101)	45
Float	Float	Pull-Up	5	0.06 (3'b000)	880 (4'b0111)	0.9 (3'b001)	98 (3'b101)	645 (4'b0110)	45
Float	Pull-Up	Float	7.5	0.58 (3'b001)	900 (4'b1000)	0.9 (3'b001)	98 (3'b101)	645 (4'b0110)	45
Float	Pull-Up	Pull-Up	10	1.09 (3'b010)	920 (4'b1001)	0.9 (3'b001)	98 (3'b101)	685 (4'b1000)	45
Pull-Up	Float	Float	12.5	1.56 (3'b011)	940 (4'b1010)	1.2 (3'b010)	91 (3'b110)	685 (4'b1000)	45
Pull-Up	Float	Pull-Up	15	2.26 (3'b100)	980 (4'b1100)	1.2 (3'b010)	91 (3'b110)	685 (4'b1000)	45
Pull-Up	Pull-Up	Float	17.5	2.67 (3'b101)	1000 (4'b1101)	1.7 (3'b011)	91 (3'b110)	685 (4'b1000)	45
Pull-Up	Pull-Up	Pull-Up	20	2.67 (3'b101)	1020 (4'b1110)	1.7 (3'b011)	85 (3'b111)	705 (4'b1001)	42.75

Table 5-4. Pin Configuration for Battery Charging in non I²C Mode

Device Mode			Repeater State			Charger Detection Status	VBUS Control Output
	SCL (C3)	SDA (B3)	Unconfigured	Host Repeater	Peripheral Repeater	{GPIO2, GPIO1}	GPIO0
Non I²C USB repeater mode	Pull-down resistor to ground 0 to 160Ω	Input • Low = BC 1.2 disabled • High = BC 1.2 enabled	When BC 1.2 is enabled, charger detection	N/A	N/A	• 2'b00: No charger detected • 2'b01: CDP or DCP charger detected • 2'b10: DCP (1.5A) or Divider Mode (2.1A) charger detected • 2'b11: Divider Mode (2.4A) charger detected	N/A
Non I²C USB repeater mode	Pull-down resistor to ground 1.5kΩ to 2kΩ	Input VBUS_Valid input: use a voltage divider to reduce VBUS voltage to appropriate VIH for 1.8V or 1.2V I/O mode.	When VBUS_valid is high enable charger detection	N/A	Charger detection is enabled		
Non I²C USB repeater mode	Pull-down resistor to ground 3.4kΩ to 3.96kΩ	Input • Low = BC 1.2 disabled • High = BC 1.2 enabled	When BC 1.2 is enabled, advertise charging BC 1.2 DCP	Advertise CDP	N/A	N/A	Active High Push-Pull output for VBUS switch Control • High = VBUS ON • Low = VBUS OFF
Non I²C USB repeater mode	Pull-down resistor to ground 7.5kΩ to 11kΩ	Input • Low = BC 1.2 disabled • High = BC 1.2 enabled	When BC 1.2 is enabled, advertise charging (auto cycle between BC 1.2 DCP and Divider mode)	Advertise CDP	N/A	N/A	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	V_{DD3V3}	–0.3	4.32	V
Analog Supply voltage range	V_{DD1V8}	–0.3	2.1	V
Voltage range	DP, DN, (with OVP enabled), 1000 total number of short events and cumulative duration of 1000 hrs.	–0.3	6	V
Voltage range	eDP, eDN	–0.3	1.6	V
Voltage range	RESETB, GPIO0, GPIO1, GPIO2, SCL, SDA	–0.3	2.1	V
Junction temperature	$T_{J(max)}$		125	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD3V3}	Supply voltage (VDD3V3)	3.0	3.3	3.6	V
V_{DD1V8}	Analog Supply voltage (VDD1V8)	1.62	1.8	1.98	V
$V_{\_I2C\_Pullup}$	I2C and GPIO open drain Bus Voltage (1.2 V Variant)	1.08	1.2	1.32	V
$V_{\_I2C\_Pullup}$	I2C and GPIO open drain Bus Voltage (1.8 V Variant)	1.62	1.8	1.98	V
USB Voltage	DP, DN	0		3.6	V
eUSB2 voltage	eDP, eDN	0		1.32	V
Digital voltage	GPIO0, GPIO1, GPIO2, SCL, SDA (1.8 V Variant)	0		1.98	V
Digital voltage	GPIO0, GPIO1, GPIO2, SCL, SDA (1.2 V Variant)	0		1.32	V
RESETB	RESETB (1.2 V or 1.8 V Variant)	0		1.98	V
T_A	Operating free-air temperature	−20		85	°C
T_J	Junction temperature	−20		105	°C
T_{CASE}	Case temperature	−20		105	°C
T_{PCB}	PCB temperature (1 mm away from the device)	−20		92	°C

6.4 Thermal Information

THERMAL METRIC[1]		TUSB2E11 YCG (DSBGA) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	22.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
P_{WC_1V8}	Absolute worst case peak power consumption (VDD1V8 only) for power supply budgeting	I2C interface active, GPIOs in output mode, repeater in HS mode with USB transmitting, maximum RX EQ, max TX VOD and PE settings, maximum transition density. T_A = −20°C to 85°C.			280	mW
P_{WC_3V3}	Absolute worst case peak power consumption (VDD3V3 only) for power supply budgeting	I2C interface active, GPIOs in output mode, repeater in HS mode with USB transmitting, maximum RX EQ, max TX VOD and PE settings, maximum transition density. T_A = –20°C to 85°C.			30	mW
P_{WCFS_3V3}	Absolute worst case peak power consumption (VDD3V3 only) for power supply budgeting	I2C interface active, GPIOs in output mode, repeater in FS mode with USB Asynchronous traffic. T_A = –20°C to 85°C.			75	mW
P_{HS_IOC}	USB Audio ISOC High-speed	Maximum TX Vod/Maximum TX PE for both USB and eUSB2. Averaged over 8 ms and only 1 uFrame with data packet. Toff threshold = 1/32. Host Peripheral Mode.		35		mW
P_{PD}	Powered down	Device powered, RESETB=Low, T_A=25°C, (DP/DN Voltage ≤ VDD3V3).			9	µW
$P_{Disabled}$	Disabled	Device powered, I2C/GPIO interfaces functional but idle, repeater is disabled and put into the lowest power state and non-functional. T_A=25°C, (DP/DN Voltage ≤ VDD3V3).		43	95	µW
P_{Detach}	USB unconnected	I2C/GPIO interfaces idle, repeater is connected to a eUSB2 PHY and waiting for a USB attach event. T_A = 25°C, (DP/DN Voltage ≤ VDD3V3)		43	85	µW
$P_{Suspend}$	L2 Suspend (host mode)	I2C/GPIO interfaces idle, USB link is in L2, repeater is monitoring for a resume/ remote wake event. T_A = 25°C, (DP/DN Voltage ≤ VDD3V3). In peripheral mode additional current is present due the DP pull up.		45	85	µW

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{Sleep}	L1 Sleep	I2C/GPIO interfaces idle, repeater is supporting a USB connection, USB link is in L1 (host exists L1 every 1 ms) and repeater is monitoring for a L1 exit event. T_A = 25°C, (DP/DN Voltage ≤ VDD3V3)		2.3	5	mW
P_{LS_Active}	Low Speed Active	I2C/GPIO interfaces idle, repeater in LS mode, maximum transition density. T_A = 85°C.		7.2	24	mW
P_{FS1_Active}	Full Speed Active (ASYNC Traffic)	I2C/GPIO interfaces idle, repeater in FS mode, maximum transition density. T_A = 85°C.		45	80	mW
P_{FS2_Active}	Full Speed Active (ISO Traffic)	I2C/GPIO interfaces idle, repeater in FS mode, maximum transition density. T_A = 85°C.		9	24	mW
$P_{HS\_Idle\_Host}$	High Speed Idle (Host mode)	L0.Idle. TA = 85°C. (Typical at 25°C).		26	70	mW
$P_{HS\_Idle\_Peripheral}$	High Speed Idle (Peripheral mode)	L0.Idle. TA = 85°C. (Typical at 25°C).		108	200	mW
DIGITAL INPUTS						
V_{IH}	High level input voltage	GPIO0, GPIO1, GPIO2 (1.2 V Variant)	0.702			V
V_{IH}	High level input voltage	GPIO0, GPIO1, GPIO2 (1.8 V Variant)	1.053			V
V_{IL}	Low-level input voltage	GPIO0, GPIO1, GPIO2 (1.2 V Variant)			0.462	V
V_{IL}	Low-level input voltage	GPIO0, GPIO1, GPIO2 (1.8 V Variant)			0.693	V
V_{IL}	Low-level input voltage	RESETB			0.35	V
V_{IH}	High level input voltage	RESETB	0.75			V
I_{IH}	High level input current	V_{IH} = 1.98 V, VDD3V3=3.0 V or 0 V, VDD1V8=1.62 V or 0 V RESETB, GPIO0, GPIO1			0.5	µA
I_{IL}	Low level input current	V_{IL} = 0 V, VDD3V3=3.0 V or 0 V, VDD1V8=1.62 V or 0 V RESETB, GPIO0, GPIO1			0.5	µA
DIGITAL OUTPUTS						
V_{OH}	High level output voltage	GPIO0, GPIO1, GPIO2, push-pull I/O mode (I_{OH} = 20 µA and maximum 3 pF C_{load}) (1.2 V Variant)	0.81			V
V_{OH}	High level output voltage	GPIO0, GPIO1, GPIO2, push-pull I/O mode (I_{OH} = 20 µA and maximum 3 pF C_{load})(1.8 V Variant)	1.21			V
V_{OL}	Low level output voltage	GPIO0, GPIO1, GPIO2, push-pull I/O mode (I_{OL} = 1 mA) (1.2 V Variant)			0.25	V
V_{OL}	Low level output voltage	GPIO0, GPIO1, GPIO2, push-pull I/O mode (I_{OL} = 1 mA) (1.8 V Variant)			0.35	V
I_{OL_PP}	Low level output current in push-pull mode	GPIO0, GPIO1, GPIO2 (1.2 V Variant), VOL=0.4 V	2.5	4	5.6	mA
I_{OL_PP}	Low level output current in push-pull mode	GPIO0, GPIO1, GPIO2 (1.8 V Variant), VOL=0.4 V	4	6	8	mA
I_{OH_PP}	High level output current in push-pull mode	GPIO0, GPIO1, GPIO2, push-pull I/O mode, VOH=0.9 V (1.2 V Variant)	22			µA
I_{OH_PP}	High level output current in push-pull mode	GPIO0, GPIO1, GPIO2, push-pull I/O mode, VOH=0.9 V (1.8 V Variant)	50			µA
I2C (SDA, SCL)						
V_{IL}	Low level input voltage, 1.2 V variant	SDA, SCL, $V_{\_I2C\_Pullup}$ = 1.08 V			0.387	V

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low level input voltage, 1.8 V variant	SDA, SCL, $V_{\_I2C\_Pullup}$ = 1.96 V			0.588	V
V_{IH}	High level input voltage, 1.2 V variant	SDA, SCL, $V_{\_I2C\_Pullup}$ = 1.08 V	0.833			V
V_{IH}	High level input voltage, 1.8 V variant	SDA, SCL, $V_{\_I2C\_Pullup}$ = 1.96 V	1.372			V
V_{HYS}	Input hysteresis, 1.2 V variant	$V_{\_I2C\_Pullup}$ = 1.08 V	0.020			V
V_{HYS}	Input hysteresis, 1.8 V variant	$V_{\_I2C\_Pullup}$ = 1.96 V	0.098			V
I_{IH}	High level input leakage current	V_{IH} = 1.98 V			0.5	µA
I_{IL}	Low level input leakage current	V_{IL} = 0 V			0.5	µA
V_{OL}	Low level output voltage (1 kΩ pull up), 1.2 V variant	I_{OL} = 2.5 mA, V_I2C_Pullup = 1.08 V			0.2	V
V_{OL}	Low level output voltage (1 kΩ pull up), 1.8V variant	I_{OL} = 2.5 mA, V_I2C_Pullup = 1.96 V			0.3	V
I_{OL}	Open drain drive strength, 1.2 V Variant	VOL = 0.4 V	1.6	2.4	3.0	mA
I_{OL}	Open drain drive strength, 1.8 V Variant	VOL = 0.4 V	8	10	12.6	mA
UART I/O						
V_{OLI}	Internal output low	Internal UART output (eDP/eDN) 1.2 V signaling			0.1	V
V_{OHI}	Internal output high	Internal UART output (eDP/eDN) 1.2 V signaling	0.918		1.32	V
V_{ILI}	Internal input low	Internal UART input (eDP/eDN) 1.2 V signaling	–0.1		0.399	V
V_{IHI}	Internal input high	Internal UART input (eDP/eDN) 1.2 V signaling	0.819		1.386	V
V_{OLE}	External output low	External UART output (DP/DN) 3.3 V signaling	0		0.3	V
V_{OHE}	External output high	External UART output (DP/DN) 3.3 V signaling	2.8		3.6	V
V_{ILE}	External input low	External UART input (DP/DN) 3.3 V signaling			0.8	V
V_{IHE}	External input high	External UART input (DP/DN) 3.3 V signaling	2			V
USB (DP, DN)						
Z_{inp_Dx}	Impedance to GND, no pull up or pull down	Vin=3.6 V, V_{DD3V3}=3.0 V, *Input Characteristics* (1)	390			kΩ
C_{IO_Dx}	Capacitance to GND	Measured with VNA at 240 MHz, Driver Hi-Z			10	pF
R_{PUI}	Bus pull-up resistor on upstream facing port (idle)	*High-speed Device Speed Identification* (1)	0.92	1.1	1.475	kΩ
R_{PUR}	Bus pull-up resistor on upstream facing port (receiving)	*High-speed Device Speed Identification* (1)	1.525	2.2	2.99	kΩ
R_{PD}	Bus pull-down resistor on downstream facing port	*High-speed Device Speed Identification* (1)	14.35	19	24.6	kΩ
V_{HSTERM}	Termination voltage in high speed	The output voltage in the high-speed idle state, *High-speed Input Characteristics* (1)	–10		10	mV
USB TERMINATION						
Z_{HSTERM_P}	Driver Output Resistance (which also serves as high speed termination)	(VOH= 0 to 600 mV) *Full-speed (12 Mb/s) Driver Characteristics* (1), Default, U_HS_TERM_Px setting 01	40.6	45	49.4	Ω
Z_{HSTERM_N}	Driver Output Resistance (which also serves as high speed termination)	(VOH= 0 to 600 mV) *Full-speed (12 Mb/s) Driver Characteristics* (1), Default, U_HS_TERM_Px setting 01	40.6	45	49.4	Ω

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB INPUT LEVELS LS/FS						
V_{IH}	High (driven)	*Receiver Characteristics* (1) (measured at the connector)	2			V
V_{IHZ}	High (floating)	*Receiver Characteristics* (1) (HOST downstream port pull-down resistor enabled and external device pull up 1.5 kΩ ± 5% to 3.0-3.6 V)	2.7		3.6	V
V_{IL}	Low	*Receiver Characteristics* (1)			0.8	V
V_{DI}	Differential Input Sensitivity (hysteresis is off)	|(D+)-(D-)|; Differential Input Sensitivity Range for Low-/full-speed (1); (measured at connector) V_{CM}=0.8 V to 2.0 V			0.2	V
USB OUTPUT LEVELS LS/FS						
V_{OL}	Low	*USB Driver Characteristics* (1), (measured at connector with RL of 1.425 kΩ to 3.6 V.)	0		0.3	V
V_{OH}	High (Driven)	*USB Driver Characteristics* (1), (measured at the connector with RL of 14.25 kΩ to GND.)	2.8		3.6	V
Z_{FSTERM}	Driver Series Output Resistance	*USB Driver Characteristics* (1), measured it during VOL or VOH	28		44	Ω
V_{CRS2}	Output Signal Crossover Voltage	Measured as in *Data Signal Rise and Fall Time* (1), excluding the first transition from the Idle state. With external 1.5 kΩ pull up on DP to 3.0 V	1.3		2	V
V_{CRS}	Output Signal Crossover Voltage	Measured as in *Data Signal Rise and Fall Time* (1), excluding the first transition from the Idle state	1.3		2	V
USB INPUT LEVELS HS						
V_{HSSQ}	High-speed squelch/no-squelch detection threshold	*Full-/High-speed Signaling Level* (1), specification refers to peak differential signal amplitude), measured at 240 MHz with increasing amplitude, U_SQUELCH_THRESHOLD_Px setting 011, V_{CM}= -50 mV to 500 mV	111	128	161	mV
V_{HSSQ}	High-speed squelch/no-squelch detection threshold	*Full-/High-speed Signaling Levels* (1), (specification refers to peak differential signal amplitude), measured at 240 MHz with increasing amplitude, U_SQUELCH_THRESHOLD_Px setting 100, V_{CM}= -50 mV to 500 mV	104	125	150	mV
V_{HSDSC}	High-speed disconnect detection threshold	*Full-/High-speed Signaling Levels* (1), (specification refers to differential signal amplitude). (HW Default), U_DISCONNECT_THRESHOLD_Px setting 0000, V_{CM}=200 mV to 600 mV	525	575	625	mV
V_{HSDSC}	High-speed disconnect detection threshold	*Full-/High-speed Signaling Levels* (1) (specification refers to differential signal amplitude). (+25.6%), U_DISCONNECT_THRESHOLD_Px setting 1000, V_{CM}=280 mV to 680 mV	685	757	846	mV
$EQ_{\_UHS}$	USB high-speed data receiver equalization, (measured indirectly through jitter)	240 MHz, U_EQ_Px setting 000	−0.37	0.06	0.57	dB
$EQ_{\_UHS}$	USB High-speed data receiver equalization, (measured indirectly through jitter)	240 MHz, U_EQ_Px setting 010	0.62	1.09	1.57	dB

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB OUTPUT LEVELS HS						
V_{HSOH}	High-speed data signaling high	*Full-/High-speed Signaling Levels* (1), measured single-ended peak voltage per USB 2.0 test measurement spec, U_HS_TX_AMPLITUDE_Px setting 0011, PE disabled, Test load is an ideal 45 Ω to GND on DP and DN	360	400	440	mV
V_{HSOH}	High-speed data signaling high	*Full-/High-speed Signaling Levels* (1), measured single ended peak voltage per USB 2.0 test measurement spec, U_HS_TX_AMPLITUDE_Px setting 1100, PE disabled, Test load is an ideal 45 Ω to GND on DP and DN	441	490	539	mV
V_{HSOD}	High-speed data signaling swing	Measured p-p, 0%, U_HS_TX_AMPLITUDE_Px setting 0011, PE disabled, Test load is an ideal 45 Ω to GND on DP and DN.	720	800	880	mV
V_{HSOD}	High-speed data signaling swing	Measured p-p, 22.5%, U_HS_TX_AMPLITUDE_Px setting 1100, PE disabled,Test load is an ideal 45 Ω to GND on DP and DN.	882	980	1078	mV
V_{HSOL}	High-speed data signaling low, driver is off termination is on (measured single ended)	*Full-/High-speed Signaling Levels* (1), PE disabled, test load is an ideal 45 Ω to GND on DP and DN.	–10		10	mV
V_{CHIRPJ}	Host or hub chirp J level (differential voltage)	*Full-/High-speed Signaling Levels* (1), (PE is disabled. swing setting has no impact but slew rate control has impact), Test load is an ideal 1.5 kΩ pull up on DP.	700	900	1100	mV
V_{CHIRPK}	Device chirp K level (differential voltage)	*Full-/High-speed Signaling Levels* (1), (PE is disabled. swing setting has no impact but slew rate control has impact), Test load is an ideal 45 Ω to GND on DP and DN.	-900	-760	-500	mV
V_{CHIRPK}	Host or hub Chirp K level (differential voltage)	*Full-/High-speed Signaling Levels* (1), (PE is disabled. swing setting has no impact but slew rate control has impact), Test load is an ideal 1.5 kΩ pull up on DP.	-900	-700	-500	mV
$U2\_TX_{PE}$	High-speed TX pre-emphasis	U_HS_TX_PRE_EMPHASIS_Px setting 000, test load is an ideal 45 Ω to GND on DP and DN.	0.25	0.5	0.75	dB
$U2\_TX_{PE}$	High-speed TX pre-emphasis	U_HS_TX_PRE_EMPHASIS_Px setting 100, test load is an ideal 45 Ω to GND on DP and DN.	1.7	2.1	2.5	dB
$U2\_TX_{PE\_UI}$	High-speed TX pre-emphasis width	U_HS_TX_PE_WIDTH_Px setting 11 (measured with PE=2.5 dB setting of 101), Test load is an ideal 45 Ω to GND on DP and DN.	0.54	0.65	0.77	UI
eUSB2 TERMINATION						
R_{SRC_HS}	High-speed transmit source termination impedance	*High-Speed Tx Electrical Specification* (2)	33	40	47	Ω
ΔR_{SRC_HS}	High-speed source impedance mismatch	*High-Speed Tx Electrical Specification* (2)			4	Ω
R_{RCV_DIF}	High-speed differential receiver termination (repeater)	*High-Speed Rx Electrical Specification* (2)	74	80	86	Ω

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PD}	Pull-down resistors on eDP/eDN	*Pull-down* [2], active during LS, FS and HS	6	8	10	kΩ
R_{SRC_LSFS}	Transmit output impedance	*Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%* [2], TX output impedance	28	44	59	Ω
C_{IO_eDx}	Differential Capacitance	Measured with VNA at 240 MHz, Driver Hi-Z (VCM = 120 mV to 450 mV), measured differentially.		3.9	5.2	pF
eUSB2 FS/LS INPUT LEVELS						
V_{IL}	Single-ended input low	*Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%* [2]	–0.1		0.399	V
V_{IL}	Single-ended input low	*Low-Speed /Full-Speed DC Specifications for 1.0 V ± 10%* [2]	−0.1		0.332	V
V_{IH}	Single-ended input high	*Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%* [2]	0.819		1.386	V
V_{IH}	Single-ended input high	*Low-Speed /Full-Speed DC Specifications for 1.0 V ± 10%* [2]	0.682		1.1	V
V_{HYS}	Receive single-ended hysteresis voltage	*Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%* [2]	43.2			mV
V_{HYS}	Receive single-ended hysteresis voltage	*Low-Speed /Full-Speed DC Specifications for 1.0 V ± 10%* [2]	38			mV
eUSB2 FS/LS OUTPUT LEVELS						
V_{OL}	Single-ended output low	*Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%* [2]			0.1	V
V_{OL}	Single-ended output low	*Low-Speed /Full-Speed DC Specifications for 1.0 V ± 10%* [2]			0.1	V
V_{OH}	Single-ended output high	*Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%* [2]	0.918		1.32	V
V_{OH}	Single-ended output high	*Low-Speed /Full-Speed DC Specifications for 1.0 V ± 10%* [2]	0.765		1.1	V
eUSB2 HS INPUT LEVELS						
V_{RX_CM}	Receive DC common mode range (low)	*High-Speed Rx Electrical Specification* [2] (normative), low DC common mode RX must tolerate			120	mV
V_{RX_CM}	Receive DC common mode range (high)	*High-Speed Rx Electrical Specification* [2] (normative), high DC common mode RX must tolerate	280			mV
$V_{CM\_RX\_AC}$	Receiver AC common mode (50 MHz–480 MHz)	*High-Speed Rx Electrical Specification* [2] (informative), across the DC common-mode range of 120 mV to 280 mV. (RX capability tested with intentional TX rise/fall time mismatch and prop delay mismatch)	-60		60	mV
C_{RX_CM}	Receive center-tapped capacitance	*High-Speed Rx Electrical Specification* [2] (informative)	15		50	pF
V_{EHSSQ}	Squelch/No-squelch detect threshold	*High-Speed Rx Electrical Specification* [2], (measured as differential peak voltage at 240 MHz with increasing amplitude) E_SQUELCH_THRESHOLD_Px setting 100, V_{CM} = 120 mV to 450 mV	60	81	97	mV

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{EHSSQ}	Squelch/No-squelch detect threshold	*High-Speed Rx Electrical Specification* [2], (measured as differential peak voltage at 240 MHz with increasing amplitude) E_SQUELCH_THRESHOLD_Px setting 110, V_{CM} = 120 mV to 450 mV	47	67	83	mV
EQ_{EHS}	eUSB2 high-speed data receiver equalization, (measured indirectly through jitter)	240 MHz E_EQ_P1x setting 0000	−0.2	0.34	0.73	dB
eUSB2 HS OUTPUT LEVELS						
V_{EHSOD}	Transmit differential (terminated)	Measured p2p, R_L = 80 Ω, E_HS_TX_AMPLITUDE_ Px setting 011, ideal 80 Ω Rx differential termination load	378	420	462	mV
E_TXPE	High-speed TX Pre-emphasis	E_HS_TX_PRE_EMPHASIS_Px setting 000	−0.2	0	0.2	dB
$E\_TX_{PE\_UI}$	High-speed TX Pre-emphasis width	E_HS_TX_PE_WIDTH_Px setting 00	0.29	0.40	0.59	UI
$V_{E\_TX\_CM}$	Transmit DC common mode	*High-Speed Tx Electrical Specification* [2]	170		230	mV

(1) USB 2.0 Promoter Group 2000, USB 2.0 Specification USB 2.0 Promoter Group
(2) USB Implementers Forum (2018). Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification, Rev. 1.2 USB Implementers Forum

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB (DP, DN), HS Driver Switching Characteristics						
T_{HSR}	Rise time (10% – 90%)	*Data Signal Rise and Fall, Eye Patterns* [1], U_HS_TX_SLEW_RATE_Px setting 11, ideal 45 Ω to GND loads on DP and DN, pre-emphasis disabled.	530	625	740	ps
T_{HSF}	Fall time (10% – 90%)	*Data Signal Rise and Fall, Eye Patterns*, U_HS_TX_SLEW_RATE_Px setting 11, ideal 45 Ω to GND loads on DP and DN, pre-emphasis disabled.	530	625	740	ps
USB (DP, DN), FS Driver Switching Characteristics						
T_{FR}	Rise time (10% – 90%)	*Data Signal Rise and Fall Time and Full-speed Load* [1]	4		20	ns
T_{FF}	Fall time (10% – 90%)	*Data Signal Rise and Fall Time and Full-speed Load* [1]	4		20	ns
T_{FRFM}	(T_{FR}/T_{FM})	*Data Signal Rise and Fall, Eye Patterns* [1], excluding the first transition from the Idle state	90		111.1	%
USB (DP, DN), LS Driver Switching Characteristics						
T_{LR}	Rise time (10% – 90%)	*Data Signal Rise and Fall Time and Full-speed Load* [1]	75		300	ns
T_{LF}	Fall time (10% – 90%)	*Data Signal Rise and Fall Time and Full-speed Load* [1]	75		300	ns
eUSB2 (eDP, eDN), HS Driver Switching Characteristics						
T_{EHSRF}	Rise/fall time (20% – 80%)	*Full-Speed/Low-Speed Electrical Specification* [2], ideal 80 Ω Rx differential termination E_HS_TX_SLEW_RATE_Px setting = 01	355	440	525	ps
T_{EHSRF_MM}	Transmit rise/fall mismatch	*Full-Speed/Low-Speed Electrical Specification* [2], rise/fall mismatch = absolute delta of (rise – fall time) / (average of rise and fall time).			25	%
eUSB2 (eDP, eDN), LS/FS Driver Switching Characteristics						
T_{ERF}	Rise/fall time (10% – 90%)	*Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%* [2]	2		6	ns
T_{ERF_MM}	Transmit rise/fall mismatch	*Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%* [2]			25	%
I2C (SDA)						
T_r	Rise time (STD)	Bus Speed = 100 kHz, C_L= 200 pF, R_{PU} = 4 kΩ, I_{OL} ≅ 1 mA	600			ns
T_r	Rise time (FM)	Bus Speed = 400 kHz, C_L= 200 pF, R_{PU} = 2.2 kΩ, I_{OL} ≅ 2 mA	180			ns
T_r	Rise time (FM+)	Bus Speed = 1 MHz, C_L= 10 pF, R_{PU} = 1 kΩ, I_{OL} ≅ 4 mA	72			ns
T_r	Rise time (STD)	Bus Speed = 100 kHz, C_L= 200 pF, R_{PU} = 4 kΩ, I_{OL} ≅ 2 mA			1000	ns
T_r	Rise time (FM)	Bus Speed = 400 kHz, C_L= 200 pF, R_{PU} = 1 kΩ, I_{OL} ≅ 8 mA			300	ns
T_r	Rise time (FM+)	Bus Speed = 1 MHz, C_L= 50 pF, R_{PU} = 1 kΩ, I_{OL} ≅ 4 mA			120	ns
T_f	Fall time (STD)	Bus Speed = 100 kHz, C_L= 200 pF, R_{PU} = 2.2 kΩ, I_{OL} ≅ 4 mA			106.5	ns

6.6 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_f	Fall time (FM)	Bus Speed = 400 kHz, C_L= 200 pF, R_{PU} = 1 kΩ, I_{OL} ≅ 8 mA			106.5	ns
T_f	Fall time (FM+)	Bus Speed = 1 MHz, C_L= 90 pF, R_{PU} = 1 kΩ, I_{OL} ≅ 8 mA			81.5	ns
T_f	Fall time (STD)	Bus Speed = 100 kHz, C_L= 10 pF, R_{PU} = 4 kΩ, , I_{OL} ≅ 2 mA	6.5			ns
T_f	Fall time (FM)	Bus Speed = 400 kHz, C_L= 10 pF, R_{PU} = 2.2 kΩ, I_{OL} ≅ 4 mA	6.5			ns
T_f	Fall time (FM+)	Bus Speed = 1 MHz, C_L= 10 pF, R_{PU} = 1 kΩ, I_{OL} ≅ 8 mA	6.5			ns

(1) USB 2.0 Promoter Group 2000, USB 2.0 Specification USB 2.0 Promoter Group
(2) USB Implementers Forum (2018). Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification, Rev. 1.2 USB Implementers Forum

6.7 Timing Requirements

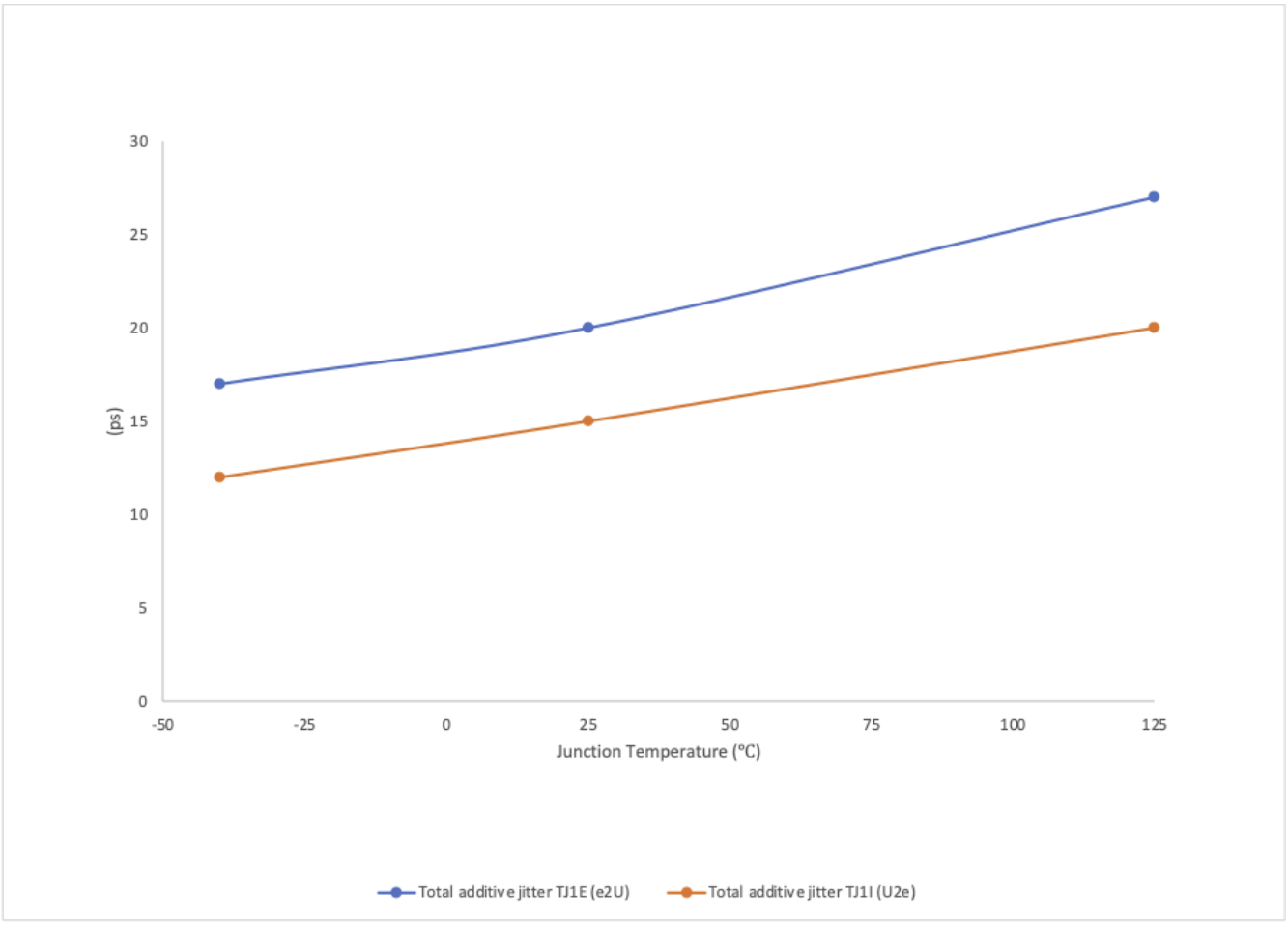
		MIN	NOM	MAX	UNIT
I/O TIMING					
$t_{\_GPIO\_PW}$	Minimum GPIO pulse width for interrupt event	8			µs
RESET TIMING					
$t_{\_VDD1V8\_RAMP}$	Ramp time for VDD1V8 to reach minimum 1.62 V			2	ms
$t_{\_VDD3V3\_RAMP}$	Ramp time for VDD3V3 to reach minimum 3.0 V			2	ms
$t_{\_aRESETB}$	Duration for RESETB to be asserted low to complete reset while powered	10			us
$t_{\_RH\_READY}$	Time for the device to be ready to accept RAP and I^2C requests and eUSB2 interface to be ready after RESETB is de-asserted or (VDD1V8 and VDD3V3) reach the minimum recommended voltages, whichever is later.			3	ms
$t_{\_RS\_READY}$	Time for the device to be ready to accept RAP and I2C requests and eUSB2 interface to be ready after a soft reset through I^2C.			350	µs
REPEATER TIMING					
T_{J1E}	Total additive jitter for eUSB2 to USB 2.0 (output jitter − input jitter) of the repeater.		20	42	ps
T_{J1I}	Total additive jitter for USB 2.0 to eUSB2 (output jitter − input jitter) of the repeater.		17	42	ps
$T_{e\_to\_U\_DJ1}$	eUSB2 to USB 2.0 repeater FS jitter to next transition (Per *Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%* [1] condition for supply and GND delta).	−6.0		+6.0	ns
$T_{U\_to\_e\_DJ1}$	USB 2.0 to eUSB2 repeater FS jitter to next transition (Per *Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%* [1] condition for supply and GND delta).	−3.0		+3.0	ns
T_{DJ2_e2U}	repeater FS paired transition jitter in eUSB2 to USB 2.0 direction (relaxed relative to THDJ2 defined by USB 2.0 ± 1 ns). eUSB2 in 1.2 V signaling mode.	−1.5		+1.5	ns
T_{DJ2_U2e}	repeater FS paired transition jitter in USB 2.0 to eUSB2 direction (relaxed relative to THDJ2 defined by USB 2.0 ± 1 ns). eUSB2 in 1.2 V signaling mode.	−1.5		+1.5	ns
MODE TIMING					
T_{MODE_SWITCH}	Time needed to change mode from UART bypass mode to and from USB mode			1	µs
T_{UART_START}	Time needed to start transmitting UART data, post toggling GPIO0 to '0' when in UART strap mode (SCL=1, SDA=0 at power-up)			2	ms
I2C (FM+)					
t_{SU_STA}	Start setup time, SCL (T_r=72 ns – 120 ns), SDA (T_f=6.5 ns – 81.5 ns), 1 MHz FM+	260			ns
t_{SU_STO}	Stop setup time, SCL (T_r=72 ns –120 ns), SDA (T_f=6.5 ns – 81.5 ns), 1 MHz FM+	260			ns
t_{HD_STA}	Start hold time, SCL (T_r=72 ns – 120 ns), SDA (T_f=6.5 ns – 81.5 ns), 1 MHz FM+	260			ns
t_{SU_DAT}	Data input or false start/stop, setup time, SCL (T_r=72 ns – 120 ns), SDA (T_f=6.5 ns – 81.5 ns), 1 MHz FM+	50			ns
t_{HD_DAT}	Data input or False start/stop, hold time, SCL (T_r=72 ns – 120 ns), SDA (T_f=6.5 ns – 81.5 ns), 1 MHz FM+	0			ns
t_{VD_DAT}, t_{VD_ACK}	SDA output delay, SCL (T_r=72 ns – 120 ns), SDA (T_f=6.5 ns – 81.5 ns), 1 MHz FM+	20		450	ns
$t_{HD\_DAT\_SL}$	Data hold time when device is transmitting	6.67			ns
t_{SP}	Glitch width suppressed	50		91	ns
t_{BUF}	Bus free time between a STOP and START condition (Master minimum spec that device must tolerate)	0.5			µs

6.7 Timing Requirements (continued)

		MIN	NOM	MAX	UNIT
t_{LOW}	Low period for SCL clock (minimum spec that device must tolerate)	0.5			µs
t_{HIGH}	High period for SCL clock (minimum spec that device must tolerate)	0.26			µs
I2C (FM)					
t_{SU_STO}	Stop setup time, SCL (T_r=180 ns – 300 ns), SDA (T_f=6.5 ns – 106.5 ns), 400 kHz FM	600			ns
t_{HD_STA}	Start hold time, SCL (Tr=180 ns – 300 ns), SDA (Tf=6.5 ns – 106.5 ns), 400 kHz FM	600			ns
t_{SU_STA}	Start setup time, SCL (T_r=180 ns – 300 ns), SDA (T_f=6.5 ns – 106.5 ns), 400 kHz FM	600			ns
t_{SU_DAT}	Data input or false start/stop, setup time, SCL (T_r=180 ns – 300 ns), SDA (T_f=6.5 ns – 106.5 ns), 400 kHz FM	100			ns
t_{HD_DAT}	Data input or false start/stop, hold time, SCL (T_r=180 ns – 300 ns), SDA (T_f=6.5 ns – 106.5 ns), 400 kHz FM	0			ns
t_{VD_DAT}, t_{VD_ACK}	SDA output delay, SCL (T_r=180 ns – 300 ns), SDA (T_f=6.5 ns – 106.5 ns), 400 kHz FM	20		900	ns
$t_{HD\_DAT\_SL}$	Data hold time when device is transmitting	13.5			ns
t_{SP}	Glitch width suppressed	50		91	ns
t_{BUF}	Bus free time between a STOP and START condition (minimum spec that device must tolerate)	1.3			µs
t_{LOW}	Low period for SCL clock (minimum spec that device must tolerate)	1.3			µs
t_{HIGH}	High period for SCL clock (Master minimum spec that device must tolerate)	0.6			µs
I2C (STD)					
t_{SU_STO}	Stop setup time, SCL (T_r=600 ns – 1000 ns), SDA (T_f=6.5 ns – 106.5 ns), 100 kHz STD	4			µs
t_{HD_STA}	Start hold time, SCL (Tr=600 ns – 1000 ns), SDA (Tf=6.5 ns – 106.5 ns), 100 kHz STD	4			µs
t_{SU_STA}	Start setup time, SCL (T_r=600 ns – 1000 ns), SDA (T_f=6.5 ns – 106.5 ns), 100 kHz STD	4.7			µs
t_{SU_DAT}	Data input or false start/stop, setup time, SCL (T_r=600 ns – 1000 ns), SDA (T_f=6.5 ns – 106.5 ns), 100 kHz STD	250			ns
t_{HD_DAT}	Data input or false start/stop, hold time, SCL (T_r=600 ns – 1000 ns), SDA (T_f=6.5 ns – 106.5 ns), 100 kHz STD	5			µs
t_{VD_DAT}, t_{VD_ACK}	SDA output delay, SCL (T_r=600 ns – 1000 ns), SDA (T_f=6.5 ns – 106.5 ns), 100 kHz STD			3.45	µs
$t_{HD\_DAT\_SL}$	Data hold time when device is transmitting	13.5			ns
t_{SP}	Glitch width suppressed	50		91	ns
t_{BUF}	Bus free time between a STOP and START condition (minimum spec that device must tolerate)	4.7			µs
t_{LOW}	Low period for SCL clock (minimum spec that device must tolerate)	4.7			µs
t_{HIGH}	High period for SCL clock (minimum spec that device must tolerate)	4.0			µs

(1) USB Implementers Forum (2018). Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification, Rev. 1.2 USB Implementers Forum

6.8 Typical Characteristics



TJ1E is for egress direction from eUSB2 to USB and TJ1I is for ingress direction from USB to eUSB2

Figure 6-1. Total Additive Jitter (Typical)

7 Parameter Measurement Information

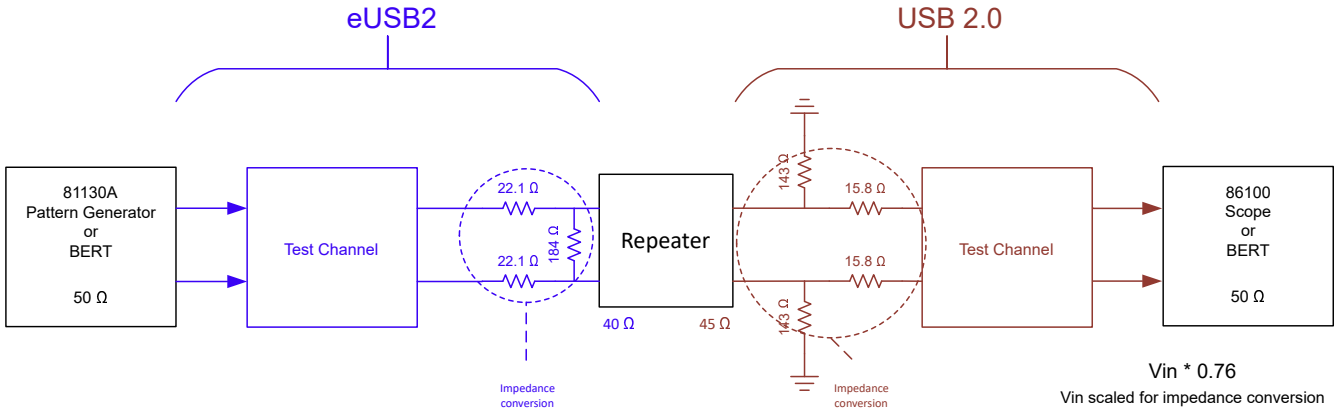


Figure 7-1. USB 2.0 TX Output (Egress) Jitter, Eye Mask Test Setup

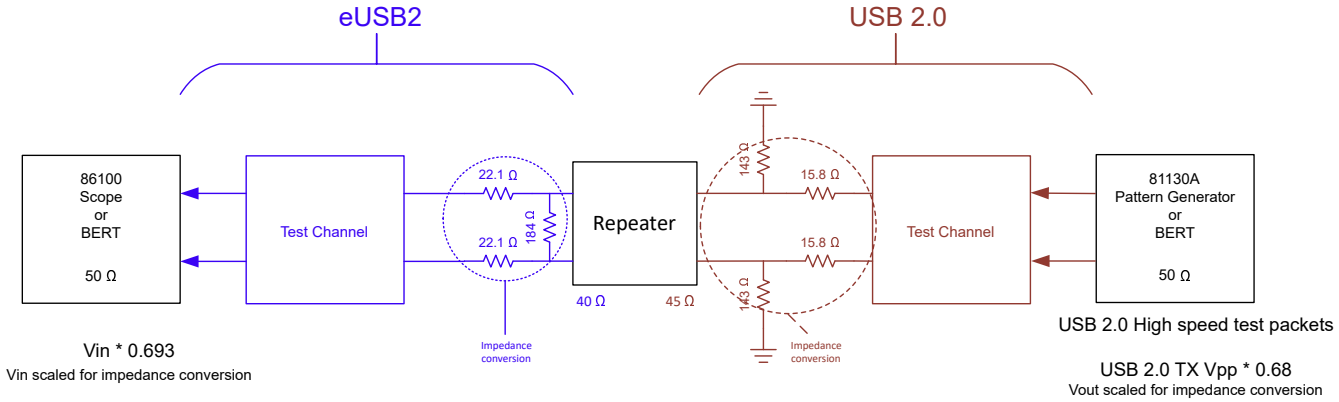


Figure 7-2. eUSB2 TX Output (Ingress) Jitter, Eye Mask Test Setup

8 Detailed Description

8.1 Overview

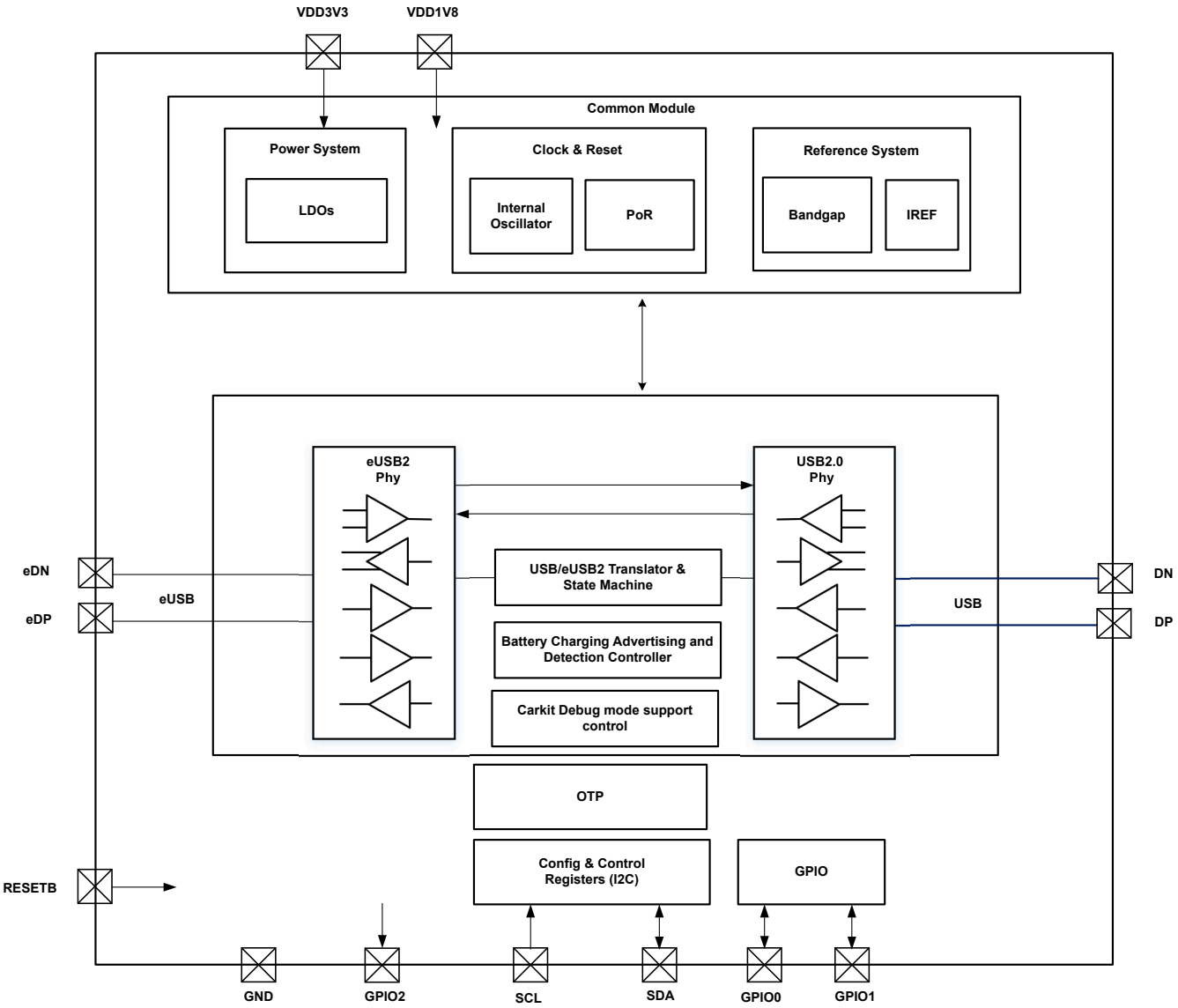
The TUSB2E11 is an eUSB2 to USB 2.0 repeater that resides between the SoC with an eUSB2 port and an external connector that supports USB 2.0. The device can be configured by the register access protocol (RAP) or through the I^{2}C. The repeater is configurable as either a host or device repeater (DRD repeater).

I^{2}C port supports up to 1MHz (fast mode plus) for internal register access. A subset of internal registers can be accessed through the register access protocol. Simultaneous register access using RAP and through the I^{2}C is supported with RAP having priority over I^{2}C.

To power up in I^{2}C mode, make sure both SDA and SCL have pullup resistors to appropriate I^{2}C bus voltage.

GPIO2 output pin can be configured to provide an active low open-drain or selectable active low or active high push-pull level sensitive interrupt output to the SoC.

8.2 Functional Block Diagram



8.3 Feature Description

The TUSB2E11 is an USB compliant eUSB2 to USB 2.0 repeater supporting both device and host modes. Both USB and eUSB2 offer fully tunable TX and RX through I^2C. Additionally, USB TX and RX can be tuned when I^2C is not used.

8.4 Device Functional Modes

8.4.1 Repeater Mode

Upon deassertion of RESETB or software reset and after t_{RH_READY} or t_{RS_READY}, the TUSB2E11 enables and enters the default state. In the default state, the TUSB2E11 is ready to accept eUSB2 packets, RAP, and I^2C requests. The repeater will either be in host repeater mode or peripheral repeater mode depending on the receipt of either host mode enable or peripheral mode enable.

When the TUSB2E11 is repeating high-speed packets, either from eUSB2 to USB 2.0 or from USB 2.0 to eUSB2, up to 4UI (may include partial UI) of HS SOP can be truncated. This is the same as a standard USB 2.0 HUB operating in high speed mode which can truncate up to 4UI.

When the TUSB2E11 is repeating high-speed packets from eUSB2 to USB 2.0, up to 1.6UI of random dribble bits (may include partial UI) can be introduced after HS EOP. This is the less than a standard USB 2.0 HUB operating in high speed mode which can have up to 4UI of random dribble bits.

When the TUSB2E11 is repeating high-speed packets from USB 2.0 to eUSB2, up to 5UI of random dribble bits (may include partial UI) can be introduced after HS EOP. This is more than a standard USB 2.0 HUB operating in high speed mode which can have up to 4UI of random dribble bits. eDSPr/eUSPr receiving eUSB2 high-speed packets should ignore 5UI of dribble bits after detecting no stuffed bit insertion indicating HS EOP.

Table 8-1. Number of Hubs Supported with Host and Peripheral Repeater

Number of eUSB2 Repeaters	Number of Hubs Operating at HS	Number of Hubs Operating at FS	
1	4	2	Number of hubs operating at FS is reduced due to $T_{e\_to\_U\_DJ1}$ and T_{RJR1}. Number of hubs operating at HS is reduced due to 2 3 1 SOP truncation and EOP dribble
2	3	1	
0	5	5	non-eUSB2 system for reference

8.4.2 Power Down Mode

RESETB can be used as a power down pin when asserted low. Power down mode puts the TUSB2E11 in lowest power mode.

8.4.3 Disabled Mode

The repeater can be disabled by setting DISABLE bit through the I^2C.

8.4.4 UART Mode

In I^2C mode GPIO0 defaults to being an enable control for Carkit UART mode. GPIO0 is an active low signal to enable Carkit UART mode. GPIO0 is intended to be controlled through APU or SoC. When APU or SoC is not powered on or the firmware has not been loaded, the GPIO0 is low, enabling the UART mode to allow APU or SoC debug interface to be accessed through the USB port.

Default Carkit UART direction is DP → eDP (RX) and eDN → DN (TX).

On the rising edge of GPIO0, followed by T_{MODE_SWITCH}, the TUSB2E11 enables and enters the default state. In the default state, the TUSB2E11 is ready to accept eUSB2 port reset, configuration or RAP. The repeater mode will be configured as host or peripheral depending on the eUSB2-defined configuration received from eUSBr and acknowledged by the repeater.

UART mode enable is controlled through GPIO0 after power up. This can be changed through UART_use_bit1_P1 bit in UART-PORT1 register, so UART mode enable can be controlled through a register instead of GPIO0.

8.4.5 Auto-Resume ECR

Optional host repeater auto-resume is supported by the TUSB2E11 in L1/L2 by driving Resume K at D+/D- until SOResume is received from eDSPr. In addition, the TUSB2E11 eUSPh holds the Remote Wake line state until SORresume is received from eDSPr.

This auto-resume feature provides host controller extra time to exit low power state and issue SOResume while the TUSB2E11 UDSP drives resume within 1 ms (TURSM) hub resume timing requirement. To take advantage of this low power feature, host controller shall implement low power mechanism to detect wake on eDSPr lines while host controller is in low power state.

This auto-resume is not needed if host controller is capable of initiating SOResume within 1 ms of detecting Remote Wake on eDSPr.

This auto-resume is enabled by default but can be disabled via bit 6 of register 0x78. This auto-resume ECR mode is disabled when L2 interrupt mode is enabled. When L2 interrupt mode is enabled, resume K at D+/D- is still driven when Remote wake is detected on UDSP but eUSPh is held at SE0 instead of in Remote Wake state. See the *L2 State Interrupt Modes* section for more details.

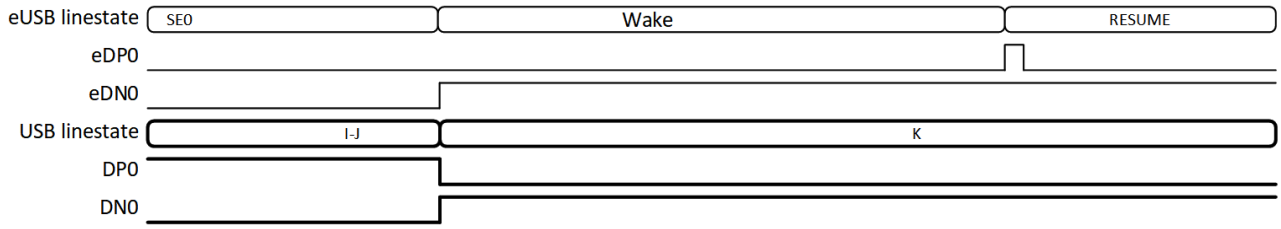


Figure 8-1. Timing Diagram for Auto-Resume for HS/FS

8.4.6 L2 State Interrupt Modes

To prevent signaling on eUSB2 while the eDSP is powered off, make sure both L2 remote wake interrupt and disconnect event interrupt modes are enabled. The special remote wake sequence when L2 remote wake interrupt mode is enabled.

- System enables interrupt USB_REMOTE_WAKE_P1.
- Repeater is in host mode and has received a CM.L2.
- Repeater detects wake on USB 2.0
- Repeater asserts interrupt.
- Repeater reflects *resume* on USB 2.0, but does not signal wake on eUSB2.
- Repeater waits for eDSPr to signal start of resume with no intervening configuration, connect, or reset sequence.
- Repeater and eDSP follow normal eUSB2 protocol to signal resume starting and ending in L0.

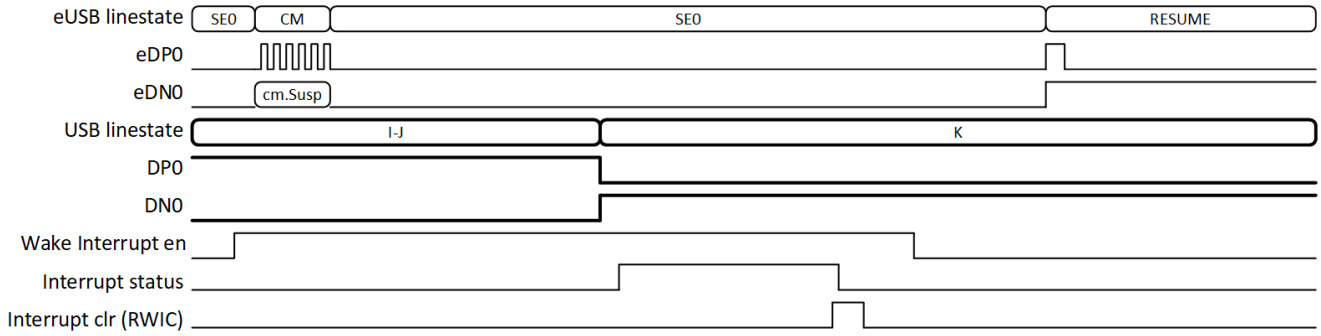


Figure 8-2. Timing Diagram for Wake Interrupt for HS/FS

The special wake on disconnect sequence when disconnect event interrupt mode is enabled

- System enables interrupt USB_DISCONNECT_P1.
- Repeater is in host mode and has received a CM.L2.
- Repeater detects SE0 for disconnect on USB 2.0.
- Repeater asserts interrupt.
- Interrupt must be cleared prior to eDSPr reinitializing the TUSB2E11 as a host.
- Repeater does not signal or report USB 2.0 SE0 on eUSB2.
- Repeater waits for eDSPr to power up, which starts with port reset announcement.
- Repeater and eDSP follow normal eUSB2 protocol, ending in unconnected state of host mode.

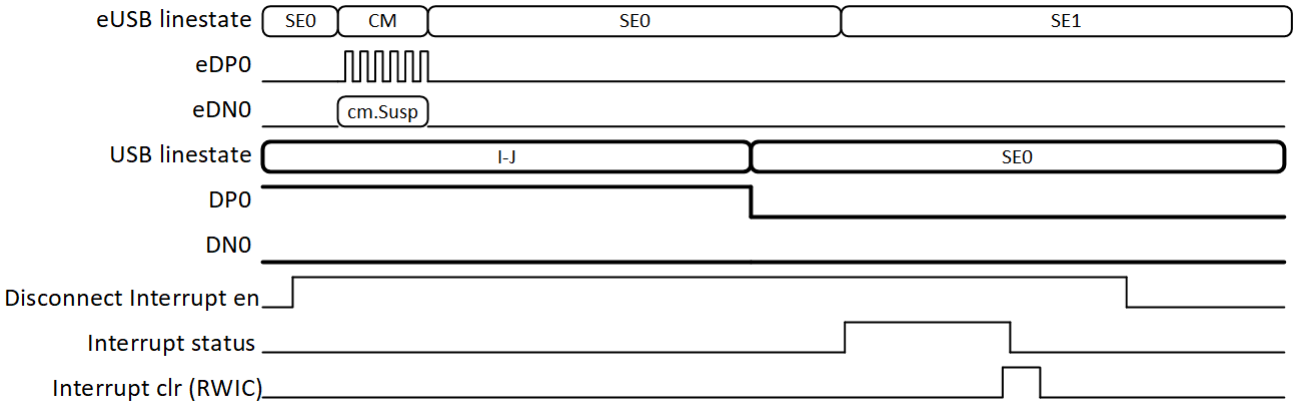


Figure 8-3. Timing Diagram for Disconnect Interrupt for HS/FS

8.4.7 Attach Detect Interrupt Mode

When attach event detect is enabled, the TUSB2E11 issues an interrupt event instead of signaling attach on eUSB2.

- System enables interrupt USB_DETECT_ATTACH_P1. Interrupt has to be enabled prior to any connect event.
- Repeater is in host mode.
- Repeater detects attach on USB 2.0.
- Repeater debounces attach for 60µs and asserts interrupt instead of signaling attach on eUSB2.
- Interrupt must be disabled prior to eDSPr reinitializing as a host to process attach through normal mechanism.

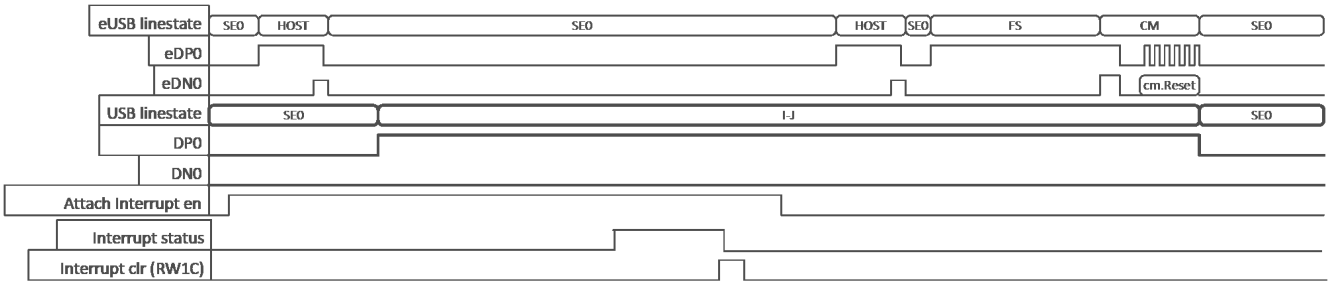


Figure 8-4. Timing Diagram for Attach Detect Interrupt for HS/FS

8.4.8 GPIO Mode

GPIO0

The GPIO0 pin is in input mode at power up, and is sampled during reset.

The GPIO0 defaults to active low UART mode (bypass mode) enable control after power up. This can be changed through the UART_use_bit1_P1 bit in UART-PORT1 register, so GPIO0 can be repurposed. Refer to UART Mode.

The GPIO0 pin can be configured to be input or output mode through the I^2C register write. Output event is selected through the I^2C register. Refer to *GPIO0_CONFIG register* for more information.

The GPIO0 input status change can be reported through the GPIO2 as an interrupt if enabled through the I^2C. Status change trigger can be programmed to be edge trigger or level trigger through the I^2C.

The GPIO0 pin in output mode defaults to open-drain output but can be configured to be push-pull output. GPIO0 pin can drive up to 3pF loads when in push-pull mode.

The GPIO0 pin reverts back to input upon RESETB assert, deassert, or soft reset.

In non I^2C mode, the GPIO0 is used for USB PHY tuning.

GPIO1

The GPIO1 pin is in input mode at power up, and is sampled during reset.

The GPIO1 is configured as an enable control for battery charger detection in repeater default state if DEFAULT_STATE_BC_P1 is set to 0x01 through the BC_CONTROL register.

The GPIO1 pin can be configured to be input or output mode through the I^2C register write. Output event is selected through the I^2C register. Refer to GPIO1_CONFIG register.

The GPIO1 input status change can be reported through the GPIO2 as an interrupt if enabled through the I^2C. Status change trigger can be programmed to be edge trigger or level trigger through the I^2C.

The GPIO1 pin in output mode defaults to open-drain output but can be configured to be push-pull output. GPIO1 pin can drive up to 3pF loads when in push-pull mode.

The GPIO1 pin reverts back to input upon RESETB assert, deassert, or soft reset.

In non I^2C mode, the GPIO1 is used for USB PHY tuning.

GPIO2

The GPIO2 pin defaults to open drain interrupt (INT) active low output at power up but can be programmed through the I^2C to be a push-pull output. In push-pull mode, the device can be programmed to be either active high or active low. The interrupt output is a level-sensitive interrupt. Trigger events can be selected through the I^2C.

Connect GPIO2 to APU to use interrupt functions and a pullup resistor (open drain mode).

The GPIO2 interrupt output can be configured through the INT_ENABLE and INT_STATUS registers.

The GPIO2 can be configured as battery charger detect indicator instead of the interrupt output through the BC_CONTROL register.

In non I^2C mode, the GPIO2 is used for USB PHY tuning.

8.4.9 USB 2.0 High-Speed HOST Disconnect Detection

The USB 2.0 specification does not specify high-speed output differential swing V_{OD} during disconnect without external load. Only chirp level and the HS host disconnect threshold are specified. Specification implicitly assumes high-speed output differential swing V_{OD} doubles during disconnect. However, the high-speed output differential swing during disconnect depends on the USB 2.0 TX output swing and pre-emphasis setting, as the common-mode voltage increase saturates the output swing level. If the output swing level is saturated, the VOD may not double.

The HS host disconnect threshold shall be adjusted to provide the most margin to avoid false disconnect as well as failure to detect a disconnect. See Table 8-2.

Table 8-2. Recommended USB 2.0 High-speed HOST Disconnect Thresholds per USB HSTX Amplitude and Pre-Emphasis

	USB HS TX Pre-Emphasis					
USB HS TX Amplitude (Vp-p)	**0.5dB (0h)**	**0.9dB (1h)**	**1.2dB (2h)**	**1.7dB (3h)**	**2.1dB (4h)**	**2.5dB (5h)**
740mV (0h)	545mV (1h)	545mV (1h)	545mV (1h)	545mV (1h)	545mV (1h)	545mV (1h)
760mV (1h)	565mV (2h)	565mV (2h)	565mV (2h)	565mV (2h)	565mV (2h)	565mV (2h)
780mV (2h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)
800mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)
820mV (4h)	605mV (4h)	605mV (4h)	605mV (4h)	605mV (4h)	605mV (4h)	605mV (4h)
840mV (5h)	625mV (5h)	625mV (5h)	625mV (5h)	625mV (5h)	625mV (5h)	625mV (5h)
860mV (6h)	645mV (6h)	645mV (6h)	645mV (6h)	645mV (6h)	625mV (5h)	625mV (5h)
880mV (7h)	645mV (6h)	645mV (6h)	645mV (6h)	645mV (6h)	645mV (6h)	645mV (6h)
900mV (8h)	665mV (7h)	665mV (7h)	665mV (7h)	665mV (7h)	665mV (7h)	645mV (6h)
920mV (9h)	685mV (8h)	685mV (8h)	685mV (8h)	665mV (7h)	665mV (7h)	665mV (7h)
940mV (Ah)	685mV (8h)	685mV (8h)	685mV (8h)	685mV (8h)	665mV (7h)	665mV (7h)
960mV (Bh)	705mV (9h)	705mV (9h)	705mV (9h)	685mV (8h)	685mV (8h)	665mV (7h)
980mV (Ch)	725mV (Ah)	705mV (9h)	705mV (9h)	705mV (9h)	685mV (8h)	685mV (8h)
1000mV (Dh)	725mV (Ah)	725mV (Ah)	705mV (9h)	705mV (9h)	685mV (8h)	685mV (8h)
1020mV (Eh)	725mV (Ah)	725mV (Ah)	725mV (Ah)	705mV (9h)	705mV (9h)	685mV (8h)
1040mV (Fh)	745mV (Bh)	725mV (Ah)	725mV (Ah)	705mV (9h)	705mV (9h)	685mV (8h)

8.4.10 Frame Based Low Power Mode

The USB2.0 standard defines high-speed microframes that occur every 125µs. Using a patented design, the TUSB2E11 monitors idle conditions within every high-speed microframe. The TUSB2E11 will enter a low power state if the bus is idle for greater than FRAME_LP_OFF_THRESHOLD and will remain in the low power state until the start of the next µSOF. This feature is enabled by default and can be disabled by clearing HOST_FRAME_LP_EN or DEVICE_FRAME_LP_EN bits.

Table 8-3 shows an example of the typical high-speed idle power the TUSB2E11 consumes based on the value of the FRAME_LP_OFF_THRESHOLD and whether or not the frame base low power is enabled. These results assume the TUSB2E11 is in host repeater mode.

Table 8-3. Typical High-Speed Idle Power for Frame Base LP Mode

HOST_FRAME_LP_EN	FRAME_LP_OFF_THRESHOLD	1.8V current (mA)	3.3V current (mA)
0 (Disabled)	N/A	56	2.8
1 (Enabled)	0x0 (1/32)	11	2.0
1 (Enabled)	0x1 (1/16)	12	2.0
1 (Enabled)	0x2 (1/8)	15	2.1
1 (Enabled)	0x3 (1/4)	22	2.2

Note

Frame based low power mode is enabled by default. If using TUSB2E11 in pin-strap mode, this feature can not be disabled. Contact support if a device variant with frame based low power mode disabled in pin-strap mode is needed.

8.4.11 Battery Charging

The TUSB2E11 supports standard USB battery charging specification 1.2 (BC1.2) and the divider mode and 1.2V DCP proprietary charging protocols as listed in Table 8-4. The BC1.2 functionality includes charger advertisement and charger detection when enabled in non-I2C mode using strap (refer to Table 5-4) or I2C mode through register configuration.

When the TUSB2E11 is configured as a host repeater, the TUSB2E11 supports charger advertisement whereas when the TUSB2E11 is configured as peripheral repeater it supports charger detection. When configured as peripheral repeater, the TUSB2E11 detects charger type if Battery Charging detection in peripheral mode is enabled. The TUSB2E11 can detect ACP3, ACP2, ACP1, DCP 1.2V biased short mode, USB standard DCP short mode and CDP types of charger. When configured as a host repeater, the TUSB2E11 acts as charger advertiser if CDP is enabled. The TUSB2E11 can advertise ACP3, DCP 1.2V, DCP or CDP modes. When in an unconfigured state, the behavior of battery charging state machine is controlled by strap settings in non-I2C mode or by register settings in I2C mode. When the TUSB2E11 is in an unconfigured state charger advertisement mode, GPIO0 directs system to power-cycle VBUS to enable a portable device to exit dedicated charging port mode and switch to host or peripheral state where data transfer is possible.

Table 8-4. Battery Charging Supported Protocols

Charging Protocol	Standard or Proprietary	Charging Current (A)	Data Transfer Allowed	Charger Detection or Advertise
SDP (Standard Downstream Port)	Standard BC1.2	0.5 or 0.9	Yes	Detection
CDP (Charging Downstream Port)	Standard BC1.2	1.5	Yes	Detection and Advertise
DCP (Dedicated Charging Port)	Standard BC1.2	1.5	No	Detection and Advertise
1.2V DCP	Proprietary	2	No	Detection and Advertise
ACP0 or Divider Mode 0	Proprietary	0.5	No	Detection
ACP1 or Divider Mode 1	Proprietary	1	No	Detection
ACP2 or Divider Mode 2	Proprietary	2.1	No	Detection
ACP3 or Divider Mode 3	Proprietary	2.4	No	Detection and Advertise

In I2C mode, the behavior of the battery charging state machine in the TUSB2E11 is controlled by the DEFAULT_STATE_BC_P1, BC_DETECTION_EN_P1, and CDP_2_EN_P1 register fields. In the unconfigured state, the battery charging state machine also depends on EN_BC input from GPIO1 in I2C mode.

Table 8-5. Battery Charging Behavior in I2C Mode

GPIO1 (BC_EN)	DEFAULT_STATE_BC_P1 bit	TUSB2E11 Behavior in each state		
		Unconfigured	Host Repeater	Peripheral repeater
Low	X	No action	As per CDP_2_EN_P1.	Act as charger detector including divider mode detector once SOC directs repeater to connect when BC_DETECTION_EN_P1 set.
High	0x0	No Action		
High	0x1	Act as a charger detector including divider mode.		
High	0x2	Advertise standard DCP if 1P2V_MODE_DIS = 1, else advertise 1.2V DCP.		
High	0x3	If 1P2V_MODE_DIS = 0, then advertise ACP3 → 1.2V DCP → DCP until no connect in auto cycling mode. If 1P2V_MODE_DIS = 1 then advertise ACP3 → DCP until no connect in auto cycling mode.		

8.5 Manufacturing Test Modes

The following test procedures show how to use I^2C to enter test modes to perform continuity test of DP/DM during manufacturing or debug. During this mode the TUSB2E11 does not operate as a repeater.

8.5.1 USB DP Test Procedure

I2C Commands to use DP pullup to test DP/DM continuity:

Enable GPIOs and DP Pull-up:

h00, hA0 <-set gpio0 to push-pull output mode

h40, hA0 <-set gpio1 to push-pull output mode

hD5, h28

hD6, h04

hD7, h10 <-DP pullup is now on

hCE, h18

hDC, h15 <-muxes DP / DM status onto GPIO lines

Status Readback Check:

h00 = hA0 <-DM status on bit 4 (normal, DM low)

h40 = hB0 <-DP status on bit 4 (normal, DP high)

h00 = hB0 <-DM status on bit 4 (DP + DM shorted together)

h40 = hA0 <-DP status on bit 4 (DP shorted to ground)

Exit Test Mode:

hB2, h80 <-soft reset (end test)

8.5.2 USB DM Test Procedure

I2C Commands to use DM pullup to test DP/DM continuity:

Enable GPIOs and DM Pull-up:

h00, hA0 <-set gpio0 to push-pull output mode

h40, hA0 <-set gpio1 to push-pull output mode

hD5, h28

hD6, h04

hD7, h08 <-DM pullup is now on

hCE, h18

hDC, h15 <-mux DP / DM status onto GPIO lines

Status Readback Check:

h00 = hB0 <-DM status on bit 4 (normal, DM high)

h40 = hA0 <-DP status on bit 4 (normal, DP low)

h40 = hB0 <-DP status on bit 4 (DP + DM shorted together)

h00 = hA0 <-DM status on bit 4 (DM shorted to ground)

Exit Test Mode:

hB2, h80 <-soft reset (end test)

8.6 I²C Target Interface

I²C target interface enables access to internal registers by the system application processor. The primary function of the interface is to enable configuring various PHY parameters, controlling the GPIO pins, and enabling USB-BC functions. The TUSB2E11 repeater functions operate upon power up without requiring I²C configuration.

The TUSB2E11 has I²C 7-bit target address of 0x3E. 8-bit address of Write: 0x7C and Read: 0x7D.

I²C default target address can be changed at the factory through one time programming.

I²C drive strength can be changed through the I²C.

Table 8-6. Recommended I²C Drive Strength for I²C Bus Speed, Bus Pull Up and Bus Capacitance

I²C FM+ (1MHz Max)	I²C drive strength (I_{OL}) selection			
	I2C bus pullup R_{PU}			
C(bus)pF	1kΩ	2.2kΩ	4kΩ	7kΩ
10-50	≅8mA	≅4mA	N/A	N/A
10-90	≅8mA	N/A	N/A	N/A
10-150	N/A	N/A	N/A	N/A
10-200	N/A	N/A	N/A	N/A

I²C FM (400kHz Max)	I²C drive strength (I_{OL}) selection			
	I²C bus pullup R_{PU}			
C(bus)pF	1kΩ	2.2kΩ	4kΩ	7kΩ
10-50	≅8mA	≅4mA	≅2mA	N/A
10-90	≅8mA	≅4mA	N/A	N/A
10-150	≅8mA	≅8mA	N/A	N/A
10-200	≅8mA	N/A	N/A	N/A

I²C STD (100kHz Max)	I²C drive strength (I_{OL}) selection			
	I²C bus pullup R_{PU}			
C(bus)pF	1kΩ	2.2kΩ	4kΩ	7kΩ
10-50	≅8mA	≅4mA	≅2mA	≅1mA
10-90	≅8mA	≅4mA	≅2mA	≅1mA
10-150	≅8mA	≅4mA	≅2mA	≅2mA
10-200	≅8mA	≅4mA	≅2mA	≅2mA

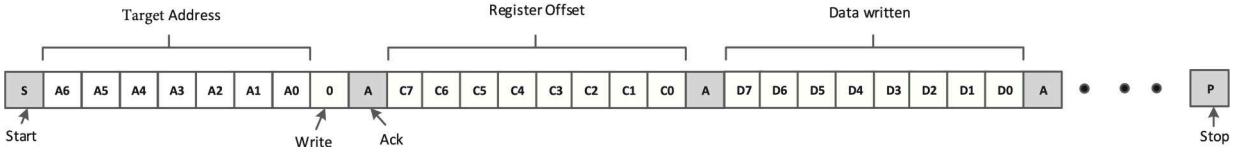


Figure 8-5. I²C Write with Data

Use the following procedure to write data to the TUSB2E11 I²C registers (refer to Figure 8-5):

1. The host initiates a write operation by generating a start condition (S), followed by the TUSB2E11 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB2E11 acknowledges the address cycle.
3. The host presents the register offset within the TUSB2E11 to be written, consisting of one byte of data, MSB-first.
4. The TUSB2E11 acknowledges the sub-address cycle.
5. The host presents the first byte of data to be written to the I²C register.

6. The TUSB2E11 acknowledges the byte transfer.
7. The host may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB2E11.
8. The host terminates the write operation by generating a stop condition (P).

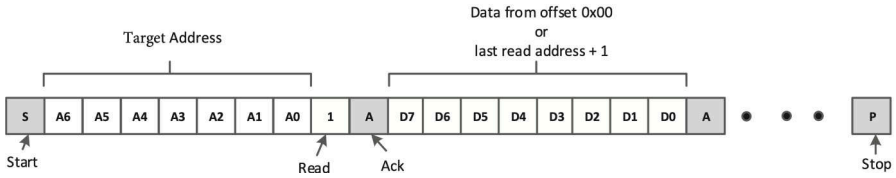


Figure 8-6. I²C Read Without Repeated Start

Use the following procedure to write data to the TUSB2E11 I²C registers without a repeated Start (refer Figure 8-6).

1. The host initiates a read operation by generating a start condition (S), followed by the TUSB2E11 7-bit address and a zero-value “W/R” bit to indicate a read cycle.
2. The TUSB2E11 acknowledges the 7-bit address cycle.
3. Following the acknowledge the host continues sending clock.
4. The TUSB2E11 transmit the contents of the memory registers MSB-first starting at register 00h or last read register offset+1. If a write to the I²C register occurred prior to the read, then the TUSB2E11 shall start at the register offset specified in the write.
5. The TUSB2E11 waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the host after each byte transfer; the I²C host acknowledges reception of each data byte transfer.
6. If an ACK is received, the TUSB2E11 transmits the next byte of data as long as host provides the clock. If a NAK is received, the TUSB2E11 stops providing data and waits for a stop condition (P).
7. The host terminates the write operation by generating a stop condition (P).

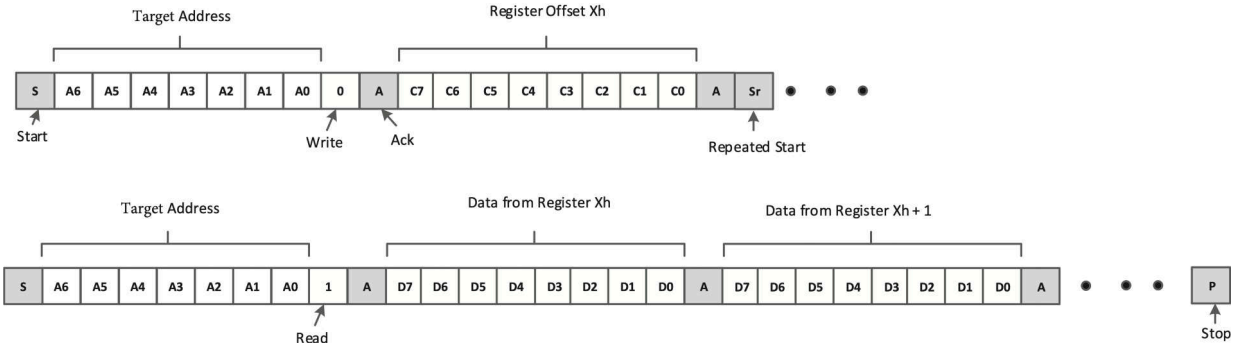


Figure 8-7. I²C Read with Repeated Start

Use the following procedure to write data to the TUSB2E11 I²C registers with a repeated Start (refer Figure 8-7).

1. The host initiates a read operation by generating a start condition (S), followed by the TUSB2E11 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB2E11 acknowledges the 7-bit address cycle.
3. The host presents the register offset within the TUSB2E11 to be written, consisting of one byte of data, MSB-first.
4. The TUSB2E11 acknowledges the register offset cycle.
5. The host presents a repeated start condition (Sr).
6. The host initiates a read operation by generating a start condition (S), followed by the TUSB2E11 7-bit address and a one-value “W/R” bit to indicate a read cycle.
7. The TUSB2E11 acknowledges the 7-bit address cycle.
8. The TUSB2E11 transmit the contents of the memory registers MSB-first starting at the register offset.

9. The TUSB2E11 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the host after each byte transfer; the I2C host acknowledges reception of each data byte transfer.
10. If an ACK is received, the TUSB2E11 transmits the next byte of data as long as host provides the clock. If a NAK is received, the TUSB2E11 stops providing data and waits for a stop condition (P).
11. The host terminates the read operation by generating a stop condition (P).

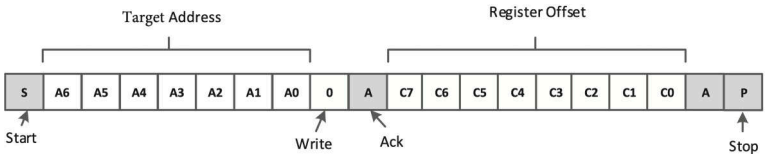


Figure 8-8. I2C Write Without Data

Use the following procedure to set a starting sub-address for I2C reads (refer to Figure 8-8).

1. The host initiates a write operation by generating a start condition (S), followed by the TUSB2E11 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB2E11 acknowledges the address cycle.
3. The host presents the register offset within the TUSB2E11 to be written, consisting of one byte of data, MSB-first.
4. The TUSB2E11 acknowledges the register offset cycle.
5. The host terminates the write operation by generating a stop condition (P).

Note

After initial power-up, if no register offset is included for the read procedure (refer to Figure 8-6), then reads start at register offset 00h and continue byte by byte through the registers until the I2C host terminates the read operation. During a read operation, the TUSB2E11 auto-increments the I2C internal register address of the last byte transferred independent of whether or not an ACK was received from the I2C host.

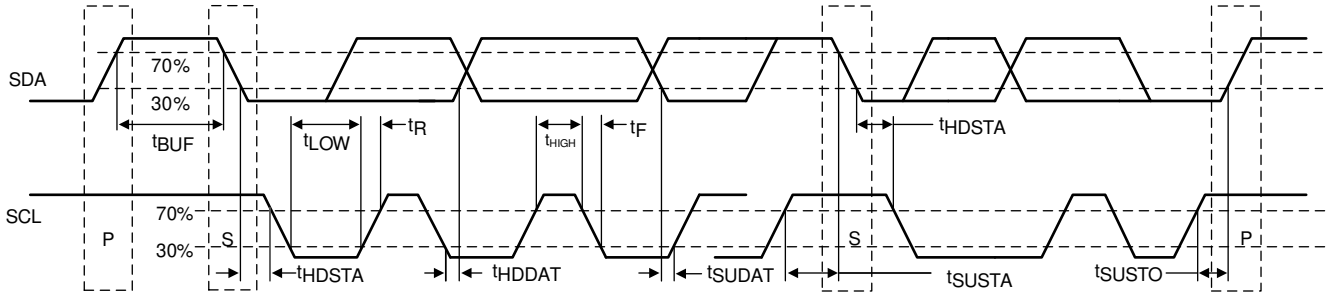


Figure 8-9. I2C Timing Diagram

9 Register Access Protocol (RAP)

The repeater in the TUSB2E11 supports the register access protocol (RAP) over eUSB2 to allow access to the related registers.

RAP accessible registers are indicated with corresponding RAP addresses in the register map. Default value of a subset of the registers are factory programmable and are indicated in register map.

10 Register Map

10.1 TUSB2E11 Registers

Table 10-1 lists the TUSB2E11 registers. All register offset addresses not listed in Table 10-1 should be considered as reserved locations and the register contents should not be modified.

Table 10-1. TUSB2E11 Registers

Offset	Acronym	Register Name	Section
70h	U_TX_ADJUST_PORT1	RAP Register for Port 1 (Write = 30h, Read = 0h), Default through OTP	Go
71h	U_HS_TX_PRE_EMPHASIS_P1	RAP Register for Port 1 (Write = 31h, Read = 1h), Default through OTP	Go
72h	U_RX_ADJUST_PORT1	RAP Register for Port 1 (Write = 32h, Read = 2h), Default through OTP	Go
73h	U_DISCONNECT_SQUELCH_PORT1	RAP Register for Port 1 (Write = 33h, Read = 3h), Default through OTP	Go
77h	E_HS_TX_PRE_EMPHASIS_P1	RAP Register for Port 1 (Write = 37h, Read = 7h), Default through OTP	Go
78h	E_TX_ADJUST_PORT1	RAP Register for Port 1 (Write = 38h, Read = 8h), Default through OTP	Go
79h	E_RX_ADJUST_PORT1	RAP Register for Port 1 (Write = 39h, Read = 9h), Default through OTP	Go
0h	GPIO0_CONFIG		Go
40h	GPIO1_CONFIG		Go
50h	UART_PORT1	RAP Register for Port 1 (Write = 10h, Read = 20h)	Go
B0h	REV_ID		Go
B2h	GLOBAL_CONFIG		Go
B3h	INT_ENABLE_1		Go
B4h	INT_ENABLE_2		Go
B5h	FRAME_LP_CONTROL	Controls for Frame Based LP mode	Go
B6h	BC_CONTROL		Go
B7h	BC_STATUS_1		Go
A3h	INT_STATUS_1		Go
A4h	INT_STATUS_2		Go
60h	CONFIG_PORT1		Go
F5h	TEST_MODE1		Go

Complex bit access types are encoded to fit into small table cells. Table 10-2 shows the codes that are used for access types in this section.

Table 10-2. TUSB2E11 Access Type Codes

Access Type	Code	Description
Read Type		
H	H	Set or cleared by hardware
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
WtoP	W	Write

Table 10-2. TUSB2E11 Access Type Codes (continued)

Access Type	Code	Description
Reset or Default Value		
- *n*		Value after reset or the default value

10.1.1 GPIO0_CONFIG Register (Offset = 00h) [Reset = 00h]

GPIO0_CONFIG is shown in GPIO0_CONFIG Register Field Descriptions.

Return to the Summary Table.

Table 10-3. GPIO0_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO0_OD_PP	R/W	0h	GPIO0 output type 0h = open-drain output 1h = push pull output
6	Reserved	R	0h	Reserved
5	GPIO0_DIRECTION	R/W	0h	GPIO0 direction 0h = input 1h = output
4	GPIO0_INPUT_STATUS	RH	0h	Logical value of GPIO0 pin input (0=Low, 1=High) 0h = input is low 1h = input is high
3-0	GPIO0_OUTPUT_SELECT	R/W	0h	Dh = HIGH_OUTPUT – output is forced static high Eh = LOW_OUTPUT – output is forced static low

10.1.2 GPIO1_CONFIG Register (Offset = 40h) [Reset = 00h]

GPIO1_CONFIG is shown in GPIO1_CONFIG Register Field Descriptions.

Return to the Summary Table.

Table 10-4. GPIO1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_OD_PP	R/W	0h	GPIO1 output type selection 0h = open-drain output 1h = push pull output
6	GPIO1_IN_TRIGGER_TYPE	R/W	0h	GPIO1 input trigger type selection for interrupt 0h = edge trigger input 1h = level trigger input (GPIO2 output reflects the input level state)
5	GPIO1_DIRECTION	R/W	0h	GPIO1 direction selection 0h = input 1h = output
4	GPIO1_INPUT_STATUS	RH	0h	Logical value of GPIO1 pin input status (0=Low, 1=High) 0h = input is low 1h = input is high

Table 10-4. GPIO1_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	GPIO1_OUTPUT_SELECT	R/W	0h	GPIO1 output selection 0h = Remote wakeup – host repeater is receiving remote wake but has not seen start of resume 1h = USB disconnect – host repeater is actively forwarding LS/FS disconnect. 2h = USB_HS_Unsquelched – host repeater in L0 seeing USB HS or in reset seeing Chirp 3h = PVTB – HOST repeater is actively transmitting ESE1 due to HS disconnect. 4h = DEFAULT – waiting to be configured host/peripheral 5h = HOST – in host repeater mode 6h = PERIPHERAL – in peripheral repeater mode 7h = CONNECTED – repeater is connected, connection seen acknowledged by start of reset 8h = RESET – reset in progress, reset is detected is high, L0 is low 9h = L0 – fully configured and repeating data, keep-alive and reset/ disconnect Ah = L1 – device has received CM.FS/CM.L1,has stopped repeating and is waiting for wake or resume Bh = L2 – device has received CM.L2, has stopped repeating and is waiting for wake or resume. Ch = GPIO1_HS_TEST – in host repeater in L0 mode, received CM.TEST Dh = HIGH_OUTPUT – output is forced static high Eh = LOW_OUTPUT – output is forced static low Fh = OVP – over voltage (DP/DN voltage > VOVP_TH) detected on the USB DP/DN

10.1.3 U_TX_ADJUST_PORT1 Register (Offset = 70h) [Reset = 7Ch]

U_TX_ADJUST_PORT1 is shown in Table 10-5.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

Table 10-5. U_TX_ADJUST_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	U_HS_TERM_P1	RH/W	1h	0h = 42.75Ω (typical) 1h = 45Ω (typical) (default) 2h = 47.25Ω (typical) 3h = 49.5Ω (typical)
5-4	U_HS_TX_SLEW_RATE_P1	RH/W	3h	0h = 425 ps (typical) 1h = 465 ps (typical) 2h = 510 ps (typical) 3h = 625 ps (typical) (OTP default)

Table 10-5. U_TX_ADJUST_PORT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	U_HS_TX_AMPLITUDE_P1	RH/W	Ch	0h = 800mV – 7.5%, 740mV (typical) 1h = 800mV – 5.0%, 760mV (typical) 2h = 800mV – 2.5%, 780mV (typical) 3h = 800mV (USB 2.0 specification nominal), 800mV (typical) (B0 OTP default) 4h = 800mV + 2.5%, 820mV (typical) 5h = 800mV + 5.0%, 840mV (typical) 6h = 800mV + 7.5%, 860mV (typical) 7h = 800mV + 10%, 880mV (typical) 8h = 800mV + 12.5%, 900mV (typical) 9h = 800mV + 15%, 920mV (typical) Ah = 800mV + 17.5%, 940mV (typical) Bh = 800mV + 20%, 960mV (typical) Ch = 800mV + 22.5%, 980mV (typical) (B1 OTP default) Dh = 800mV + 25%, 1000mV (typical) Eh = 800mV + 27.5%, 1020mV (typical) Fh = 800mV + 30%, 1040mV (typical)

10.1.4 U_HS_TX_PRE_EMPHASIS_P1 Register (Offset = 71h) [Reset =3Ch]

U_HS_TX_PRE_EMPHASIS_P1 is shown in Table 10-6.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

Table 10-6. U_HS_TX_PRE_EMPHASIS_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CDP_2_EN_P1	RH/W	0h	0h = CDP advertising disabled 1h = CDP advertising enabled
6	Reserved	RH/W	0h	Reserved
5-4	U_HS_TX_PE_WIDTH_P1	RH/W	3h	0h = 0.35 UI (typical) 1h = 0.45 UI (typical) 2h = 0.55 UI (typical) 3h = 0.65 UI (typical) (OTP default)
3	U_HS_TX_PE_ENABLE_P1	RH/W	1h	USB HS TX pre-emphasis enable Default through OTP PE is disabled during chirp J (VCHIRPJ) or chirp K (VCHIRPK) 0h = Disabled 1h = Enabled (OTP default)
2-0	U_HS_TX_PRE_EMPHASIS_P1	RH/W	4h	0h = 0.5dB (typical) (B0 OTP default) 1h = 0.9dB (typical) 2h = 1.2dB (typical) 3h = 1.7dB (typical) 4h = 2.1dB (typical) (B1 OTP default) 5h = 2.5dB (typical) 6h = not recommended 7h = not recommended

10.1.5 U_RX_ADJUST_PORT1 Register (Offset = 72h) [Reset = 92h]

U_RX_ADJUST_PORT1 is shown in Table 10-7.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

Table 10-7. U_RX_ADJUST_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	RH/W	9h	Reserved
3	Reserved	RH/W	0h	Reserved
2-0	U_EQ_P1	RH/W	2h	0h = 0.06dB (typical) (B0 OTP default) 1h = 0.58dB (typical) 2h = 1.09dB (typical) (B1 OTP default) 3h = 1.56dB (typical) 4h = 2.26dB (typical) 5h = 2.67dB (typical) 6h = 3.03dB (typical) 7h = 3.35dB (typical)

10.1.6 U_DISCONNECT_SQUELCH_PORT1 Register (Offset = 73h) [Reset = 83h]

U_DISCONNECT_SQUELCH_PORT1 is shown in Table 10-8.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

Table 10-8. U_DISCONNECT_SQUELCH_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	U_DISCONNECT_THRESHOLD_P1	RH/W	8h	0h = 525mV (minimum), 0% (B0 OTP default) 1h = 545mV (minimum), +4% 2h = 565mV (minimum), +8% 3h = 585mV (minimum), +11% 4h = 605mV (minimum), +15% 5h = 625mV (minimum), +19% 6h = 645mV (minimum), +23% 7h = 665mV (minimum), +27% 8h = 685mV (minimum) (B1 OTP default), +31% 9h = 705mV (minimum), +34% Ah = 725mV (minimum), +38% Bh = 745mV (minimum), +42% Ch = 765mV (minimum), +46% Dh = 785mV (minimum), +50% Eh = 805mV (minimum), +53% Fh = 825mV (minimum), +57%
3	Reserved	RH/W	0h	Reserved
2-0	U_SQUELCH_THRESHOLD_P1	RH/W	3h	0h = 130mV (minimum), +30% 1h = 124mV (minimum), +24% 2h = 117mV (minimum), +17% 3h = 111mV (minimum), +11% (B1 OTP default) 4h = 104mV (minimum), +4% (B0 OTP default) 5h = 98mV (minimum), −2% 6h = 91mV (minimum), −9% 7h = 85mV (minimum), −15%

10.1.7 E_HS_TX_PRE_EMPHASIS_P1 Register (Offset = 77h) [Reset = 0h]

E_HS_TX_PRE_EMPHASIS_P1 is shown in Table 10-9.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

Table 10-9. E_HS_TX_PRE_EMPHASIS_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	E_HS_TX_PRE_EMPHASIS_P1	RH/W	0h	0h = 0dB (typical) (default) 1h = 0.67dB (typical) 2h = 1.29dB (typical) 3h = 1.87dB (typical) 4h = 2.41dB (typical) 5h = 2.92dB (typical) 6h = 3.41dB (typical) 7h = 3.86dB (typical)
4-3	E_HS_TX_PE_WIDTH_P1	RH/W	0h	0h = 0.40 UI (typical) (default) 1h = 0.5 UI (typical) 2h = 0.55 UI (typical) 3h = 0.65 UI (typical)
2-1	Reserved	RH/W	0h	Reserved
0	BC_DETECTION_ENABLE_P1	RH/W	0h	Enables battery charger (BC) detection during peripheral repeater mode. BC detection is disabled if the corresponding register is written low. Detection enable is further gated with connect announcement by SoC. After detection attempt completes, repeater enables the pull up. 0h = detection disabled. 1h = detection enabled

10.1.8 E_TX_ADJUST_PORT1 Register (Offset = 78h) [Reset = 0Bh]

E_TX_ADJUST_PORT1 is shown in Table 10-10.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

Table 10-10. E_TX_ADJUST_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RH/W	0h	Reserved
6	Autoresume Disable	RH/W	0h	Added in B1 0h = autoresume enabled 1h = autoresume disabled
5	Reserved	RH/W	0h	Reserved
4-3	E_HS_TX_SLEW_RATE_P1	RH/W	1h	0h = 390 ps (typical) 1h = 440 ps (typical) (default) 2h = 460 ps (typical) 3h = 490 ps (typical)
2-0	E_HS_TX_AMPLITUDE_P1	RH/W	3h	0h = 360mV (typical) 1h = 380mV (typical) 2h = 400mV (typical) 3h = 420mV (typical) (default) 4h = 440mV (typical) 5h = 460mV (typical) 6h = 480mV (typical) 7h = 500mV (typical)

10.1.9 E_RX_ADJUST_PORT1 Register (Offset = 79h) [Reset = 60h]

E_RX_ADJUST_PORT1 is shown in Table 10-11.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

Table 10-11. E_RX_ADJUST_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RH/W	0h	Reserved
6-4	E_SQUELCH_THRESHOLD_P1	RH/W	6h	0h = 104mV (typical) 1h = 101mV (typical) 2h = 98mV (typical) 3h = 90mV (typical) 4h = 81mV (typical) (B0 OTP default) 5h = 73mV (typical) 6h = 67mV (typical) (B1 OTP default) 7h = 60mV (typical)
3-0	E_EQ_P1	RH/W	0h	0h = 0.34dB (typical) (default) 1h = 0.71dB (typical) 2h = 1.02dB (typical) 3h = 1.36dB (typical) 4h = 1.64dB (typical) 5h = 1.94dB (typical) 6h = 2.19dB (typical) 7h = 2.45dB (typical) 8h = 2.69dB (typical) 9h = 2.93dB (typical) Ah = 3.13dB (typical) Bh = 3.35dB (typical) Ch = 3.53dB (typical) Dh = 3.72dB (typical) Eh = 3.89dB (typical) Fh = 4.07dB (typical)

10.1.10 UART_PORT1 Register (Offset = 50h) [Reset = 02h]

UART_PORT1 is shown in Table 10-12.

Return to the Summary Table.

Table 10-12. UART_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0h	Reserved
4	uart_cross_P1	R/W	0h	Select whether plus and minus pins are crossed between USB 2.0 and eUSB2 during UART mode 0h = if UART mode is enabled, pair eD+ with D+ and eD- with D- 1h = if UART mode is enabled, pair eD+ with D- and eD- with D+
3	UART_use_bit1_P1	R/W	0h	Select whether UART enable select is set by register bit 1 or not 0h = bit 1 ignored. UART mode enabled by GPIO0 1h = bit 1 (UART_en_by_reg_not_pin_P1) enabled
2	UART_dir_not_Carkit_P1	R/W	0h	Set UART mode, direction, low for Carkit and high for opposite 0h = UART mode uses Carkit directions, D+ to eUSB2 and eD- to USB 2.0 1h = UART mode directions are opposite of Carkit, D- to eUSB2 and eD+ to USB 2.0
1	UART_en_by_reg_not_pin_P1	R/W	1h	Select whether Carkit UART mode is enabled by register or by GPIO0 pin 0h = select GPIO0 pin to enable UART mode 1h = select UART_mode_en_P1 register to enable UART mode
0	UART_mode_en_P1	R/W	0h	If GPIO0 is not selected to enable Carkit UART mode, this register enables the Carkit UART mode. 0h = disable UART mode between eUSB2 and USB 2.0 pins 1h = enable UART mode between eUSB2 and USB 2.0 pins

10.1.11 REV_ID Register (Offset = B0h) [Reset = 02h]

REV_ID is shown in Table 10-13.

Return to the Summary Table.

Table 10-13. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REV_ID	RH	02h	Device revision. 01h = A0 02h = B0 03h = B1

10.1.12 GLOBAL_CONFIG Register (Offset = B2h) [Reset = 0h]

GLOBAL_CONFIG is shown in Table 10-14.

Return to the Summary Table.

Table 10-14. GLOBAL_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SOFT_RST	HWtoP	0h	Writing a 1 to this field is equivalent to pulsing RESETB low
6	DISABLE_P1	R/W	0h	Disabled Mode Repeater 1 (I2C remains Active) (If port is not disconnected, wait until disconnect event to disable the repeater) 0h = repeater enabled 1h = repeater disabled
5	Reserved	R	0h	Reserved
4	GPIO2_OUT_TYPE	R/W	0h	GPIO2 output type 0h = open drain 1h = push-pull
3	GPIO2_POLARITY	R/W	0h	GPIO2 pin polarity in push-pull mode only (open-drain mode is always active low) 0h = active high 1h = active low
2-0	Reserved	R	0h	Reserved

10.1.13 INT_ENABLE_1 Register (Offset = B3h) [Reset = 00h]

INT_ENABLE_1 is shown in INT_ENABLE_1 Register Field Descriptions.

Return to the Summary Table.

Table 10-15. INT_ENABLE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_RISING_EDGE	R/W	0h	INT_GPIO1_RISING_EDGE enable. When GPIO1_IN_TRIGGER_TYPE = 0 (Edge), this enables interrupt on Rising Edge of GPIO1. When GPIO1_IN_TRIGGER_TYPE = 1 (Level), this enables interrupt when GPIO1 = High. 0h = not enabled 1h = enabled

Table 10-15. INT_ENABLE_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	GPIO1_FALLING_EDGE	R/W	0h	INT_GPIO1_FALLING_EDGE enable. When GPIO1_IN_TRIGGER_TYPE = 0 (Edge), this enables interrupt on Falling Edge of GPIO1. When GPIO1_IN_TRIGGER_TYPE = 1 (Level), this enables interrupt when GPIO1 = Low. 0h = not enabled 1h = enabled
5	Reserved	R	0h	Reserved
4	Reserved	R	0h	Reserved
3	USB_REMOTE_WAKE_P1	R/W	0h	INT_USB_REMOTE_WAKE_P1 enable. See *L2 State Interrupt Modes* 0h = not enabled 1h = enabled
2	USB_DISCONNECT_P1	R/W	0h	INT_USB_DISCONNECT_P1 enable. See *L2 State Interrupt Modes* 0h = not enabled 1h = enabled
1	Reserved	R	0h	Reserved
0	Reserved	R	0h	Reserved

10.1.14 INT_ENABLE_2 Register (Offset = B4h) [Reset = 00h]

INT_ENABLE_2 is shown in INT_ENABLE_2 Register Field Descriptions.

Return to the Summary Table.

Table 10-16. INT_ENABLE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_OVERRIDE_EN	R/W	0h	Override GPIO2 INT output 0h = not enabled 1h = enabled See INT_VALUE
6	INT_VALUE	R/W	0h	Value to drive on GPIO2 when INT_OVERRIDE_EN=1 GPIO2 output pin indicates the interrupt assertion. The GPIO2 output pin follows the GPIO2 pin configuration. In open-drain mode the GPIO2 output pin is active low to indicate interrupt assertion. In push-pull mode, the GPIO2 output pin follows active low/high configuration to indicate GPIO2 assertion. 0h = output: interrupt not asserted 1h = output: interrupt asserted
5	BC_CHG_DET_P1	R/W	0h	INT_BC_CHG_DET_P1 enable. 0h = not enabled 1h = enabled
4	Reserved	R	0h	Reserved
3	USB_DETECT_ATTACH_P1	R/W	0h	INT_USB_DET_ATTACH_P1 enable. Enable device attach detection while eDSP is powered down See *Attach Detect Interrupt Mode* 0h = not enabled 1h = enabled
2	Reserved	R	0h	Reserved
1	USB_OVP_P1	R/W	0h	Over Voltage Port 1 interrupt enable 0h = not enabled 1h = enabled

Table 10-16. INT_ENABLE_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	Reserved	R	0h	Reserved

10.1.15 FRAME_LP_CONTROL Register (Offset = B5h) [Reset = A2h]

BC_CONTROL is shown in Table 10-17.

Return to the Summary Table.

Table 10-17. FRAME_LP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HOST_FRAME_LP_EN	RH/W	1h	Host repeater frame-based low power enable. Default through OTP 0 = Not Enabled 1 = Enabled
6	DEVICE_FRAME_LP_EN	RH/W	0h	Peripheral repeater frame-based low power enable. Default through OTP 0 = Not Enabled 1 = Enabled
5	Reserved	R	1h	Reserved
4	Reserved	R	0h	Reserved
3-2	FRAME_LP_OFF_THRESHOLD	RH/W	0h	Idle duration as a fraction of frame length until Frame-based Low Power state entered Default through OTP 0h = 1/32 1h = 1/16 2h = 1/8 3h = 1/4
1	IDLE_LP_EN	RH/W	1h	Enable response-based low power mode Default through OTP 0h = Not enabled 1h = Enabled
0	Reserved	R	0h	Reserved

10.1.16 BC_CONTROL Register (Offset = B6h) [Reset = C0]

BC_CONTROL is shown in BC_CONTROL Register Field Descriptions.

Return to the Summary Table.

Table 10-18. BC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	i2c_ds_config	RH/W	3h	I2C open-drain output drive strength selection This is intended to be set through I2C. 0h ≅1mA (typical) 1h ≅2mA (typical) 2h ≅4mA (typical) 3h ≅8mA (typical) (default)

Table 10-18. BC_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	DEFAULT_STATE_BC_P1	RH/W	0h	Battery charger advertisement or detection selected for default state of eUSB2 repeater 0h = neither detect nor advertise charger 1h = detect charger starting when GPIO1 goes high. 2h = advertise short mode DCP. DCP is 1.2V if 1P2V_MODE is '1' else pure BC 1.2 DCP 3h = auto-cycle ACP3 to short mode DCP. Short mode passes through 1.2V DCP for 12 seconds prior to pure BC 1.2 DCP if 1P2V_MODE is '1'
3	VBUS_CONTROL_POLARITY	RH/W	0h	Select polarity of VBUS control output pin 0h = active high 1h = active low
2	1P2V_MODE_DIS	RH/W	0h	Disable advertising 1.2V mode in default state whether enabled to auto-cycle or not 0h = 1.2V mode enabled 1h = 1.2V mode disabled
1	INT_PIN_FUNCTION	RH/W	0h	Select function of GPIO2 pin in I2C mode 0h = INT (interrupt) 1h = CHG_DET (Charger Detected)
0	CHG_DET_POLARITY	RH/W	0h	Select polarity of CHG_DET I2C mode status output pin 0h = active low 1h = active high

10.1.17 BC_STATUS_1 Register (Offset = B7h) [Reset = 00h]

BC_STATUS_1 is shown in BC_STATUS_1 Register Field Descriptions.

Return to the Summary Table.

Table 10-19. BC_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RH	0h	Reserved
6-4	CHARGER_TYPE_DET_P1	RH	0h	Type of battery charger detected on Port 1 0h = SDP – 500mA 1h = divider 0 – 500mA 2h = divider 1 – 1 A 3h = CDP – 1.5 A 4h = BC 1.2 DCP – 1.5 A 5h = 1.2V pullup and short – 2 A 6h = divider 2 – 2.1 A 7h = divider 3 – 2.4 A
3	Reserved	RH	0h	Reserved
2-0	Auto_DCP_STATE_P1	RH	0h	State of auto-DCP sequence on Port 1 0h = no advertisement 5h = divider 3 (2.4 A) 6h = 1.2V pullup and short 7h = BC 1.2 DCP

10.1.18 INT_STATUS_1 Register (Offset = A3h) [Reset = 00h]

INT_STATUS_1 is shown in INT_STATUS_1 Register Field Descriptions.

Return to the Summary Table.

Table 10-20. INT_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_GPIO1_RISING_EDGE	R/W1C	0h	GPIO1 Rising Edge enable 0h = no interrupt 1h = interrupt
6	INT_GPIO1_FALLING_EDGE	R/W1C	0h	GPIO1 Falling Edge enable 0h = no interrupt 1h = interrupt
5	Reserved	R	0h	Reserved
4	Reserved	R	0h	Reserved
3	INT_USB_REMOTE_WAKE_P1	R/W1C	0h	Remote Wake Event Detect on USB Port 1 See *L2 State Interrupt Modes* 0h = no interrupt 1h = interrupt
2	INT_USB_DISCONNECT_P1	R/W1C	0h	Disconnect event has occurred on Port 1 See *L2 State Interrupt Modes* 0h = no interrupt 1h = interrupt
1-0	Reserved	R	0h	Reserved

10.1.19 INT_STATUS_2 Register (Offset = A4h) [Reset = 00h]

INT_STATUS_2 is shown in INT_STATUS_2 Register Field Descriptions.

Return to the Summary Table.

Table 10-21. INT_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	Reserved
5	INT_BC_CHG_DET_P1	R/W1C	0h	Detected battery charger on Port 1 0h = no interrupt 1h = interrupt
4	Reserved	R	0h	Reserved
3	INT_USB_DET_ATTACH_P1	R/W1C	0h	Device Attach event has occurred on Port 1 See *Attach Detect Interrupt Mode* 0h = no interrupt 1h = interrupt
2	Reserved	R	0h	Reserved
1	INT_USB_OVP_P1	R/W1C	0h	Over voltage condition has occurred (DP/DN) 0h = no interrupt 1h = interrupt
0	Reserved	R	0h	Reserved

10.1.20 CONFIG_PORT1 Register (Offset = 60h) [Reset = 00h]

CONFIG_PORT1 is shown in CONFIG_PORT1 Register Field Descriptions.

Return to the Summary Table.

Table 10-22. CONFIG_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R	0h	Reserved
4-3	HOST_DEVICE_P1	RH	0h	Port1 is configured as a Host repeater or a Device repeater 0h = not configured 1h = host repeater 2h = device repeater 3h = reserved
2-1	Reserved	R	0h	Reserved
0	CDP_2_STATUS_P1	RH	0h	Primary detection detected on port1 if CDP_2_EN_P1=1 0h = CDP primary detection detected 1h = CDP primary detection not detected

10.1.21 TEST_MODE1 Register (Offset = F5h) [Reset = 3Xh]

TEST_MODE1 is shown in TEST_MODE1 Register Field Descriptions.

Return to the Summary Table.

Table 10-23. TEST_MODE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	0h	Reserved, make sure to rewrite what was read
3	FORCE_HS_L0	R/W	0h	Force repeater into high-speed L0 state for test purposes only. 0h = normal repeater mode (setting this bit to 0 does not return the device to normal repeater mode, the device required a hard reset, soft reset or power cycled) 1h = forced high-speed L0 mode
2-0	Reserved	R/W	Xh	Variant ID. 00h = 1.2V I/O 02h = 1.8V I/O Must not change the value, rewrite the value that is read.

11 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

11.1 Application Information

The TUSB2E11 can be used in either HOST or Peripheral implementation. The mode is configured by the eUSB2 SoC.

11.2 Typical Application

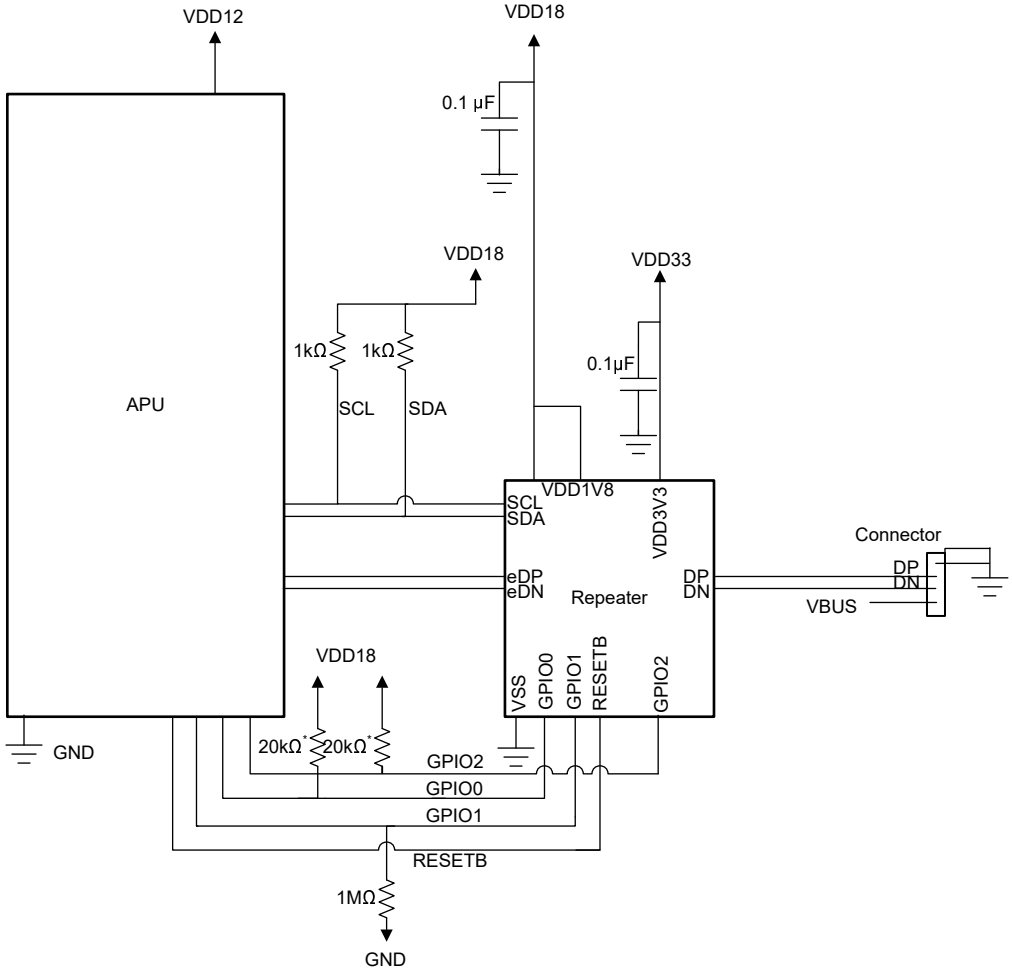


Figure 11-1. Typical System Implementation Using 1.8V I²C Variant

The 0.1µF recommendation per supply pin is based on capacitor placement of 2 mm or less trace length away. If the placement of capacitor is further away, the value of the capacitor needs to be redetermined to account for the additional trace inductance and maintain resonance around 12MHz. Additionally, make sure the system power design has adequate bulk capacitance to account for maximum transient current expected by the device when transitioning from low power mode to active mode. GPIO2 can be optionally used as interrupt output. Make sure to adjust the pullup resistor on GPIO[0:2] based on the leakage of the APU I/O so that VIH and VIL of GPIO0 are met.

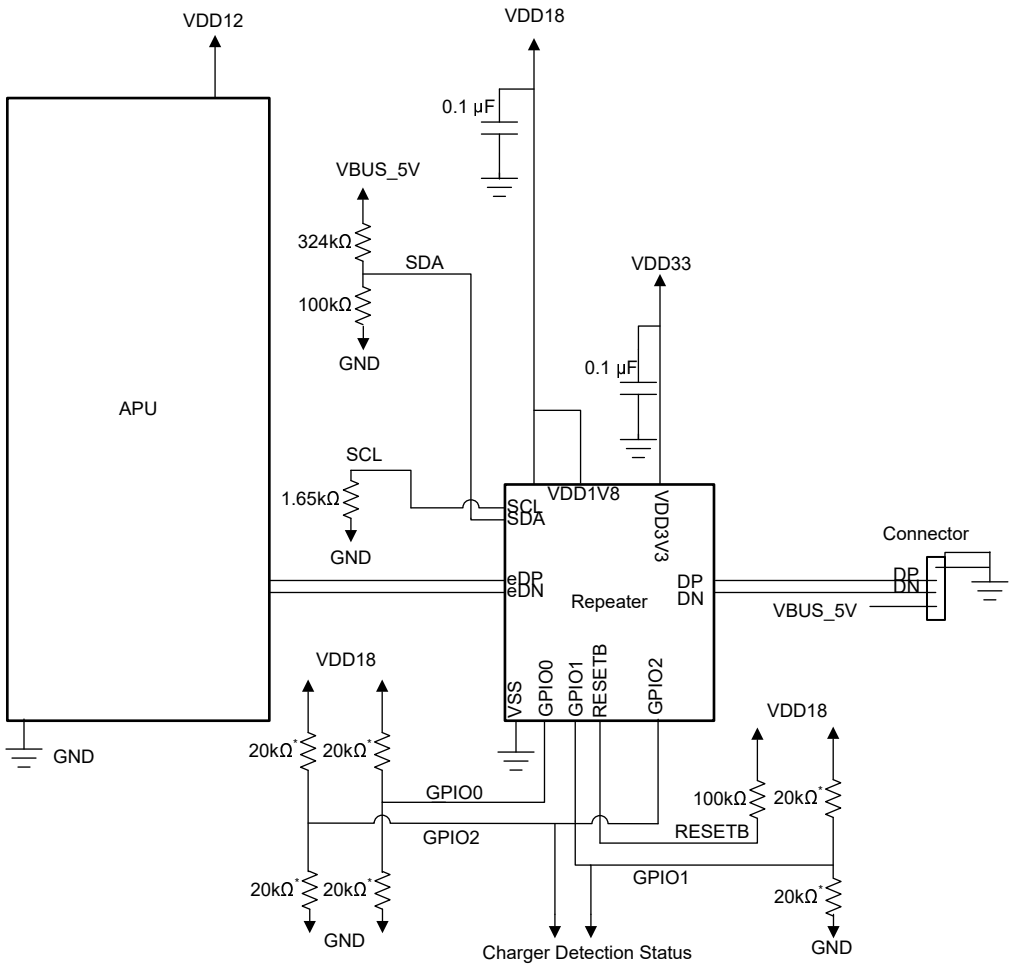


Figure 11-2. Typical System Implementation Using 1.8V Variant without I²C (Configured for Charger Detection)

The 0.1µF recommendation per supply pin is based on capacitor placement of 2 mm or less trace length away. If the placement of the capacitor is further away, then the value of the capacitor needs to be redetermined to account for the additional trace inductance and maintain resonance around 12MHz. Additionally, make sure the system power design has adequate bulk capacitance to account for maximum transient current expected by the device when transitioning from low power mode to active mode. GPIO2 can be optionally used as interrupt output. Select the pullup and pulldown resistors on GPIO[0:2] based on the USB PHY tuning needs. Use SDA for Vbus_valid detection with a voltage divider. GPIO1 and GPIO2 can be routed as needed for charger detection status. Pull-down resistor value on SCL determines the battery charging mode.

11.2.1 Design Requirements

The TUSB2E11 requires a valid reset signal as described in the *Power Supply Recommendations* section.

For design examples, use the parameters shown in Table 11-1, Table 11-2, and Table 11-3.

Table 11-1. Design Parameters for High Loss USB 2.0 System Using I²C

PARAMETER			VALUE(1)
V_{DD3V3}			3.3V ±10%
V_{DD1V8}			1.8V ±5%
I²C support required in system (Yes or No)			Yes
Parameter	**Register**	**Setting**	**Value**

Table 11-1. Design Parameters for High Loss USB 2.0 System Using I²C (continued)

PARAMETER			VALUE(1)
USB 2.0 TX Swing (peak to peak)	U_TX_ADJUST_PORT1 (Offset = 70h)	7Ch	980mVp-p
USB 2.0 TX Pre-emphasis	U_HS_TX_PRE_EMPHASIS_P1 (Offset = 71h)	3Ch	2.1dB
USB 2.0 RX Equalization	U_RX_ADJUST_PORT1 (Offset = 72h)	92h	1.09dB
USB 2.0 HS host disconnect threshold (peak differential)	U_DISCONNECT_SQUELCH_PORT1 (Offset = 73h)	83h	685mV
USB 2.0 HS squelch/RX sensitivity threshold (peak differential)	U_DISCONNECT_SQUELCH_PORT1 (Offset = 73h)	83h	111mV

Table 11-2. Design Parameters for Medium Loss USB 2.0 System Using I²C

PARAMETER			VALUE(1)
V_{DD3V3}			3.3V ±10%
V_{DD1V8}			1.8V ±5%
I²C support required in system (Yes or No)			Yes
Parameter	**Register**	**Setting**	**Value**
USB 2.0 TX Swing (peak to peak)	U_TX_ADJUST_PORT1 (Offset = 70h)	79h	920mVp-p
USB 2.0 TX Pre-emphasis	U_HS_TX_PRE_EMPHASIS_P1 (Offset = 71h)	39h	0.9dB
USB 2.0 RX Equalization	U_RX_ADJUST_PORT1 (Offset = 72h)	92h	1.09dB
USB 2.0 HS host disconnect threshold (peak differential)	U_DISCONNECT_SQUELCH_PORT1 (Offset = 73h)	83h	685mV
USB 2.0 HS squelch/RX sensitivity threshold (peak differential)	U_DISCONNECT_SQUELCH_PORT1 (Offset = 73h)	83h	111mV

(1) These parameters are starting values for a high loss system. Further tuning might be required based on specific loss profile and measurements.

Table 11-3. Design Parameters for Medium Loss USB 2.0 System without I²C and Configured for Charger Detection

PARAMETER				VALUE(1)
V_{DD3V3}				3.3V ±10%
V_{DD1V8}				1.8V ±5%
I²C support required in system (Yes or No)				No
SCL (pulldown resistor to ground)				1.65kΩ
SDA (pulldown resistor to ground)				100kΩ
SDA (pullup resistor to VBUS5V)				324kΩ
Parameter	**GPIO0**	**GPIO1**	**GPIO2**	**Value**
USB 2.0 TX Swing (peak to peak)	Float	Pull-up	Pull-up	920mVp-p
USB 2.0 TX Pre-emphasis	Float	Pull-up	Pull-up	0.9dB
USB 2.0 RX Equalization	Float	Pull-up	Pull-up	1.09dB
USB 2.0 HS host disconnect threshold (peak differential)	Float	Pull-up	Pull-up	685mV
USB 2.0 HS squelch/RX sensitivity threshold (peak differential)	Float	Pull-up	Pull-up	98mV

(1) These parameters are starting values for a medium loss system. Further tuning might be required based on specific loss profile and measurements.

11.2.2 Detailed Design Procedure

The best PHY setting is dependent upon the signal chain loss characteristics of the target platform. The recommendation is to start with lowest level of compensation for TX swing and pre-emphasis, and then increment until the optimal eye diagram margin is achieved. The same recommendation apply to the RX sensitivity or squelch threshold setting where TI recommends to adjust from low threshold until optimum RX sensitivity and squelch margins are achieved.

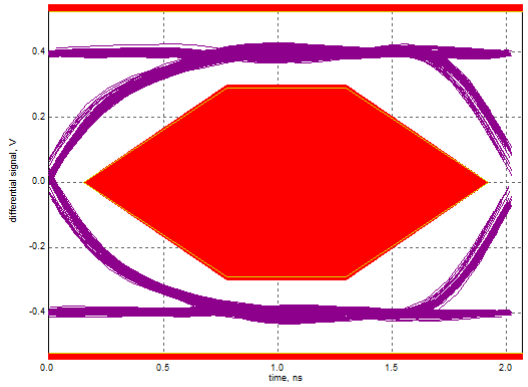
To optimize the TUSB2E11 RX equalization, monitor the corresponding TX eye diagram to achieve best RX EQ setting. In other words, to optimize eUSB2 RX equalization, monitor USB 2.0 TX eye and monitor eUSB2.0 TX eye to optimize USB RX equalization.

HS host disconnect threshold shall be adjusted to provide the most margin to avoid false disconnect as well as failure to detect a disconnect. See Table 8-2.

Note

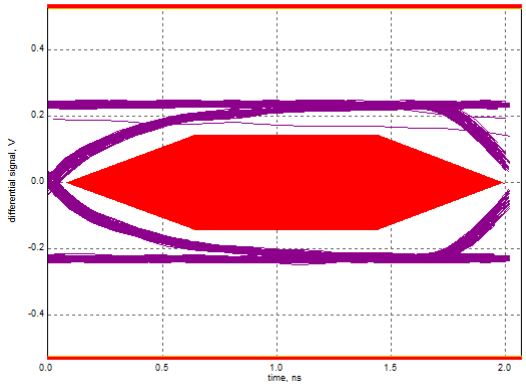
The TUSB2E11 compensates for extra attenuation in the signal path according to the configuration of the TX and RX settings. General recommendation is to use just enough pre-emphasis and equalization to achieve eye margin and not over-equalize to avoid excessive jitter. Maximum PE width and slew rates are recommended.

11.2.3 Application Curves



U_HS_TX_AMPLITUDE_P1 = 3h

Figure 11-3. USB 2.0 TX Eye Diagram with Near-End Mask



E_HS_TX_AMPLITUDE_P1 = 3h

Figure 11-4. eUSB2 TX Eye Diagram with eTP1 (Terminated) Mask

11.3 Power Supply Recommendations

11.3.1 Power Up Reset

RESETB pin is active low reset pin and can also be used as a power down pin.

The TUSB2E11 does not have power supply sequence requirements between VDD3V3 and VDD1V8.

Make sure the maximum VDD3V3 and VDD1V8 ramp time to reach minimum supply voltages is 2ms.

Digital and analog inputs may be applied when VDD3V3 and VDD1V8 are in unpowered state.

Internal power on reset circuit along with the external RESETB input pin allows for proper initialization when RESETB is deasserted high prior to the power rails being valid. If RESETB deassert high before the power supplies are stable, internal power on reset circuit holds off internal reset until the supplies are stable.

I^2C/RAP and eUSB2 interfaces are ready after t_{RH_READY} upon deassertion of RESETB or power up.

I²C/RAP and eUSB2 interfaces are ready after t_{RH_READY} upon soft reset through the I²C.

Upon deassertion of RESETB (after t_{RH_READY}) or software reset (after t_{RH_READY}), the TUSB2E11 enables and enters the default state. In the default state, the TUSB2E11 is ready to accept eUSB2 packets, RAP and I²C requests. The repeater can either be in host repeater mode or device repeater mode depending on the receipt of either host mode enable or peripheral mode enable.

11.4 Layout

11.4.1 Layout Guidelines

1. Place supply bypass capacitors as close to VDD1V8 and VDD3V3 pins as possible and avoid placing the bypass caps near the eDP/eDN and DP/DN traces.
2. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around the via to minimize the capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
3. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
4. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
5. Avoid stubs on the high-speed USB signals due to signal reflections. If a stub is unavoidable, then the stub must be less than 200 mil.
6. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.
7. Avoid crossing over anti-etch, commonly found with plane splits.
8. Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 11-5.

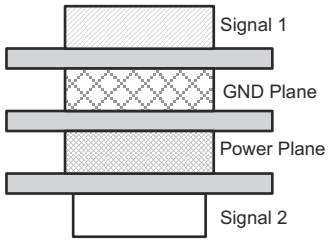


Figure 11-5. Four-Layer Board Stack-Up

11.4.2 Example Layout for Application with 1.8V I²C Variant

Figure 11-6 shows how GPIO2 can be optionally used as an open drain interrupt output with a pullup resistor to VDD18.

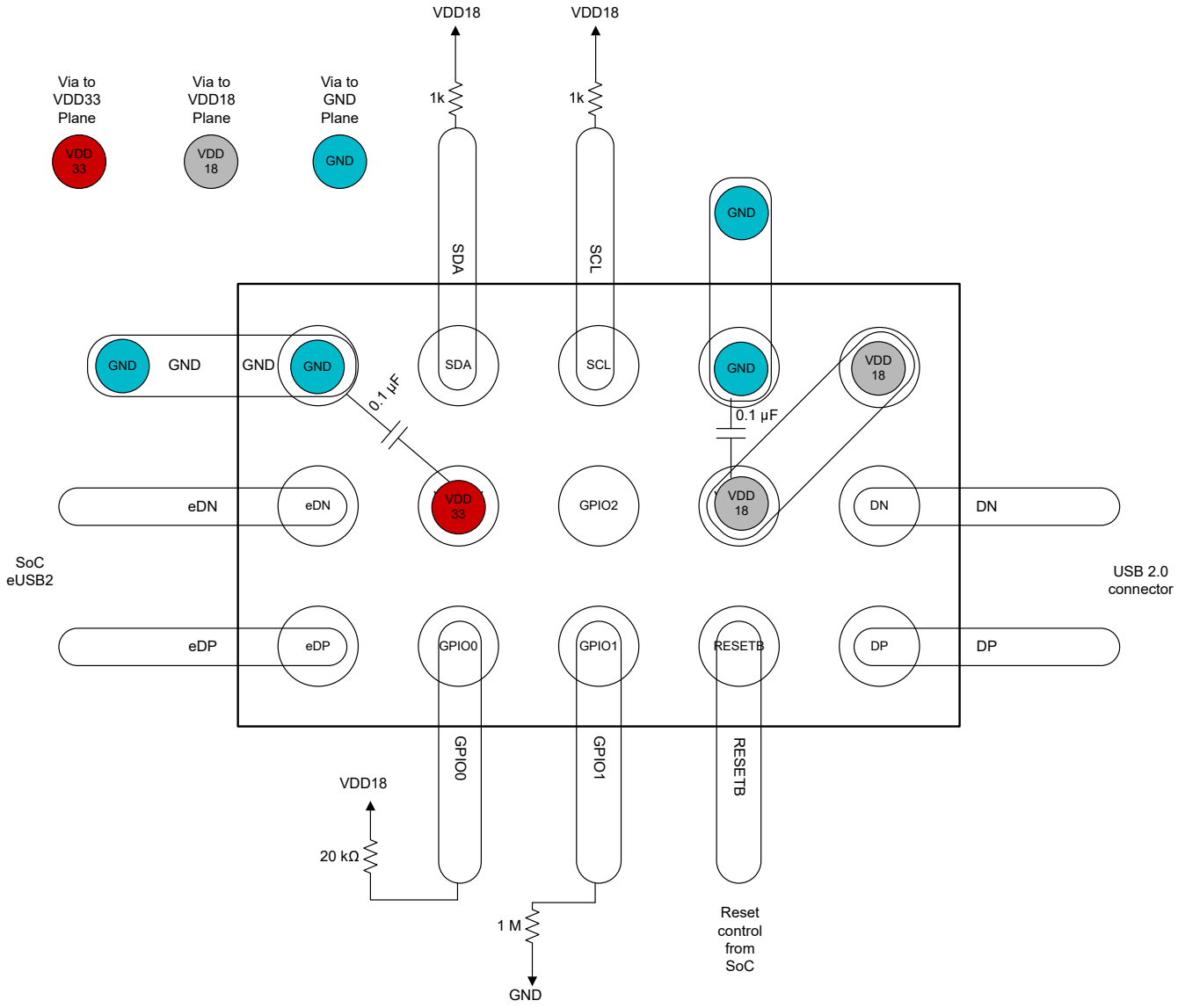


Figure 11-6. Example Layout for Application with 1.8V I²C Variant

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *High-Speed Interface Layout Guidelines* application note
- USB 2.0 Promoter Group (2000). *USB 2.0 Specification* USB 2.0 Promoter Group
- USB Implementers Forum (2018). *Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification, Rev. 1.2* USB Implementers Forum

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2024) to Revision E (November 2024)	Page
• Added RAP address for writes	35

Changes from Revision C (January 2024) to Revision D (April 2024)	Page
• Added section on Frame Based low power mode	28
• Added section on Battery Charging	29
• Added offset 0xB5 to the register map	35

Changes from Revision B (August 2023) to Revision C (January 2024)	Page
• Changed I^2C 7-bit target address from: 0x5E to: 0x3E	32

Changes from Revision A (June 2022) to Revision B (August 2023)	Page
• Updated the *Package Information* table to include package lead size	1
• Clarify ROC for RESETB	9
• Updated register F5h to indicate OPN variants	35

Changes from Revision * (November 2021) to Revision A (June 2022)	Page
• First public release of the data sheet	1

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB2E111YCGR	ACTIVE	DSBGA	YCG	15	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-20 to 85	T2E111A	Samples
TUSB2E112YCGR	ACTIVE	DSBGA	YCG	15	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-20 to 85	T2E112	Samples
TUSB2E112YCGT	ACTIVE	DSBGA	YCG	15	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-20 to 85	T2E112	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

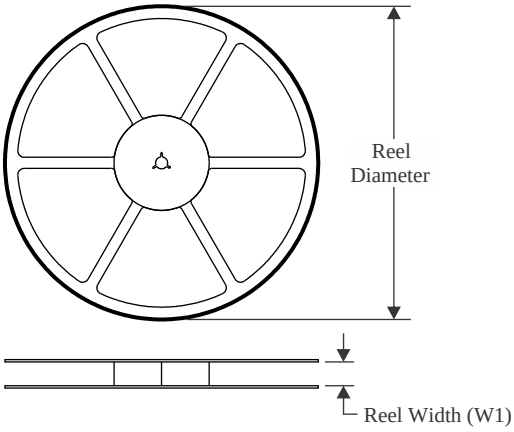
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

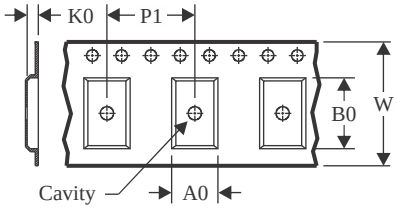
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

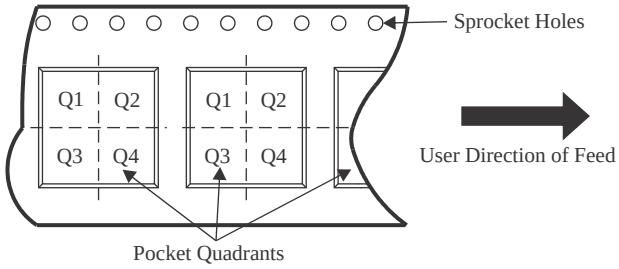


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

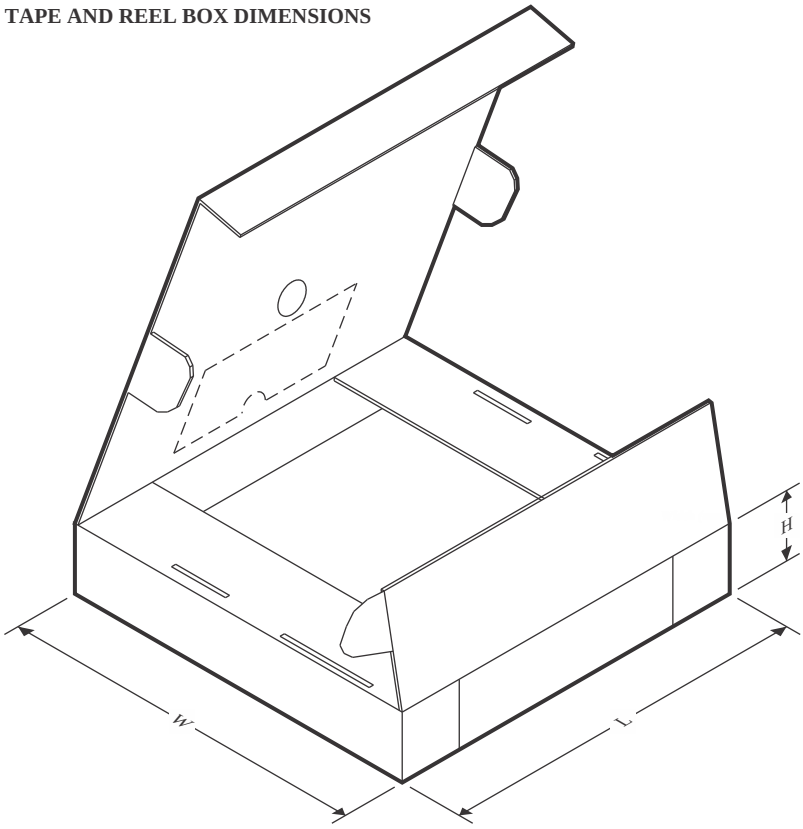
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB2E111YCGR	DSBGA	YCG	15	3000	180.0	8.4	1.42	2.16	0.65	4.0	8.0	Q1
TUSB2E112YCGR	DSBGA	YCG	15	3000	180.0	8.4	1.42	2.16	0.65	4.0	8.0	Q1
TUSB2E112YCGT	DSBGA	YCG	15	250	180.0	8.4	1.42	2.16	0.65	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

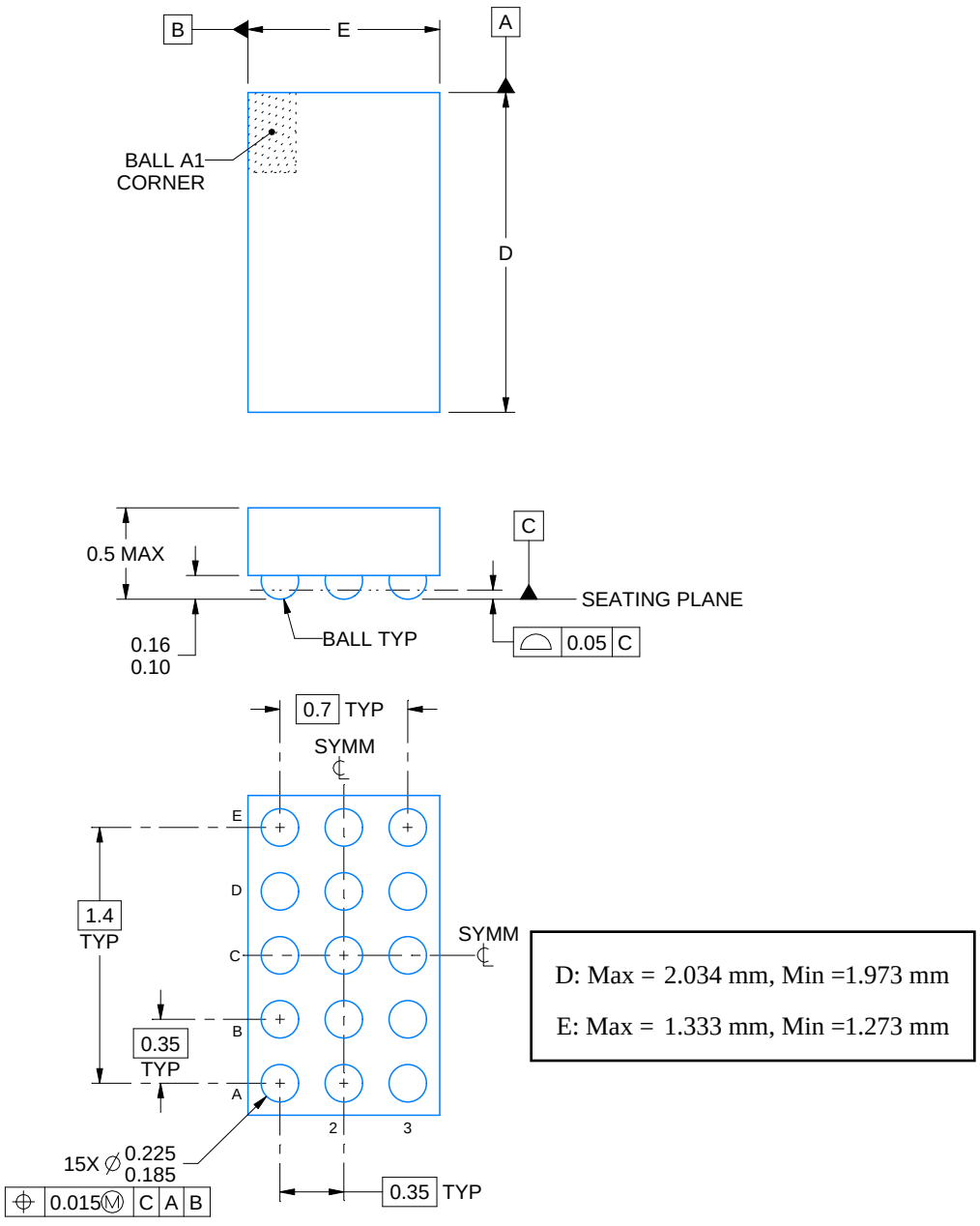
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB2E111YCGR	DSBGA	YCG	15	3000	182.0	182.0	20.0
TUSB2E112YCGR	DSBGA	YCG	15	3000	182.0	182.0	20.0
TUSB2E112YCGT	DSBGA	YCG	15	250	182.0	182.0	20.0

PACKAGE OUTLINE

YCG0015

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



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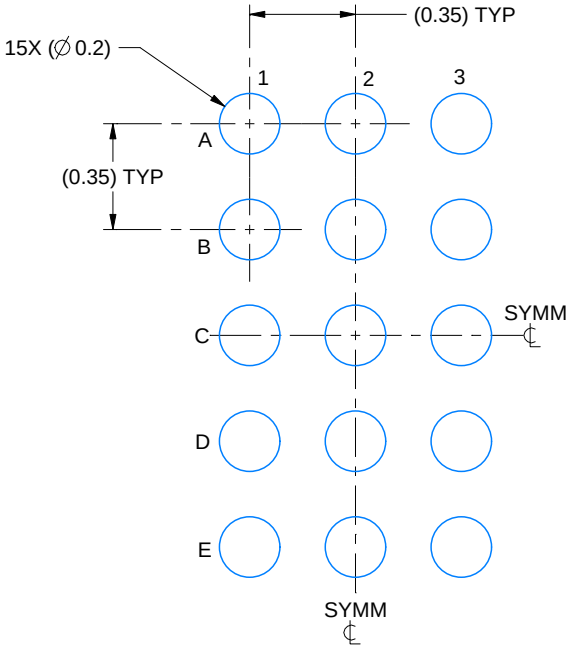
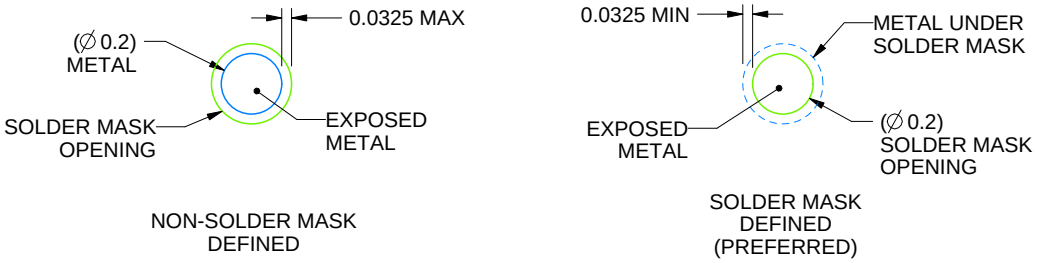
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

4224261/C 12/2021

NOTES: (continued)

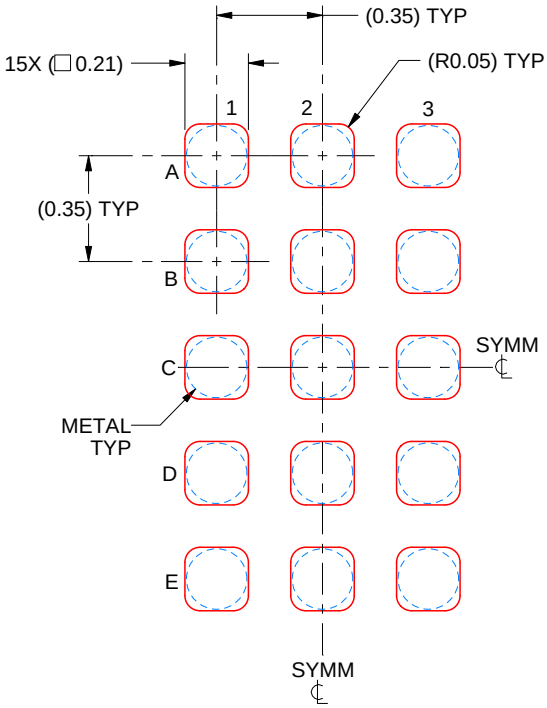
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCG0015

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

4224261/C 12/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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