Analog Engineer's Circuit

Three-Wire PT100 RTD Measurement Circuit With Low-Side Reference and Two IDAC Current Sources

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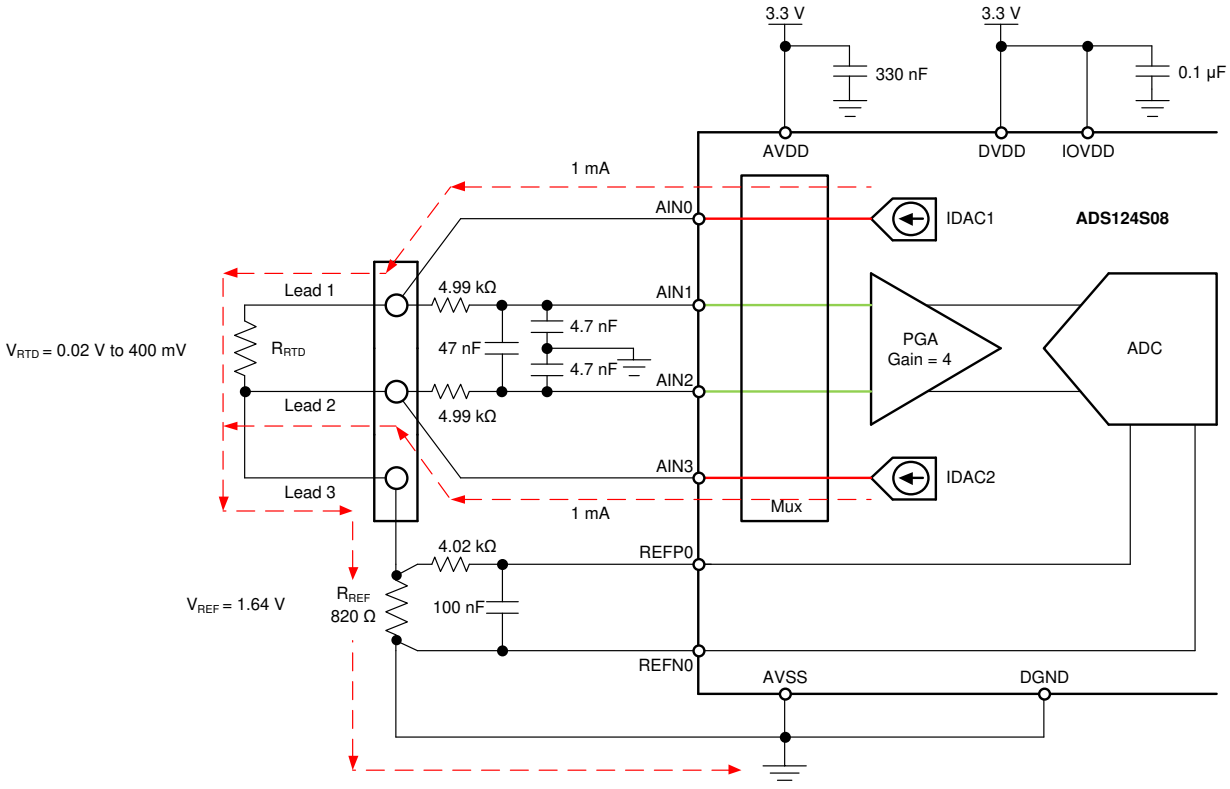
Power Supplies		
AVDD	**AVSS**	**DVDD, IOVDD**
3.3V	0V	3.3V

Design Description

This cookbook design describes a temperature measurement for a three-wire RTD using the ADS124S08. This design uses two matched IDAC excitation currents for lead-resistance cancellation. This topology creates a ratiometric measurement for a PT100 type RTD with a temperature measurement range from –200°C to 850°C. Included in this design are ADC register settings and pseudo code is provided to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab instrumentation*, and *factory automation*. For more information about making precision ADC measurements with a variety of RTD wiring configurations, see *A Basic Guide to RTD Measurements*.



Design Notes

1. Use supply decoupling capacitors for both the analog and digital supplies. AVDD must be decoupled with at least a 330-nF capacitor to AVSS. DVDD and IOVDD (when not connected to DVDD) must be decoupled with at least a 0.1-µF capacitor to DGND. See the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet for details on power supply recommendations.
2. Do not route the excitation currents through input filter resistors, using the same pin as an ADC input and as the output for an IDAC current source. Excitation currents reacting with series resistance adds error to the measurement.
3. A 1-µF capacitor is required between REFOUT and REFCOM to enable the internal reference for the IDAC current.
4. Use a precision reference resistor with high accuracy and low drift. Because the measurement is ratiometric, accuracy is dependent on the error of this reference resistor. A 0.01% resistor contributes a gain error similar to that as the ADC.
5. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
6. Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. An example design and analysis of these filters is found in *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.
7. This design shows connections to four input pins of the ADC multiplexer. Remaining analog inputs may be used for RTD, *thermocouple*, or other measurements.
8. Because of lead-resistance cancellation, the three-wire measurement offers more accuracy than comparable *two-wire RTD measurements*. For measurements with other RTD wiring configurations, see *A Basic Guide to RTD Measurements*.

Component Selection

1. Identify the range of operation for the RTD.

   As an example, a PT100 RTD has a range of approximately 20Ω to 400Ω if the temperature measurement range is from −200°C to 850°C. The reference resistor must be larger than the maximum RTD value. The reference resistance and PGA gain determines the positive full scale range of the measurement.
2. Use two matched IDAC current sources to cancel the lead-resistance error.

   Two matched IDAC current sources are used for lead-resistance cancellation. Assuming the resistances of lead 1 and lead 2 are the same, and the currents of IDAC1 and IDAC2 are the same, then the lead-resistance error may be cancelled. Cancellation can be shown through the measured voltages at AIN1 and AIN2.

   IDAC1 drives current into the RTD through lead 1. IDAC2 drives a matched current into lead 2. The voltage at AIN1 is calculated with the following equation.

   $$V_{AIN1} = I_{IDAC1} \bullet (R_{LEAD1} + R_{RTD}) + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{REF})$$

   At the same time, voltage at AIN2 is also calculated.

   $$V_{AIN2} = I_{IDAC2} \bullet R_{LEAD2} + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{REF})$$

   The measurement of the ADC is the difference between AIN1 and AIN2, which is the subtraction of the first two equations to get the following.

   $$V_{AIN1} - V_{AIN2} = [I_{IDAC1} \bullet (R_{LEAD1} + R_{RTD}) + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{REF})] - [I_{IDAC2} \bullet R_{LEAD2} + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{REF})]$$

   The R_{LEAD3} and R_{REF} terms drop out.

   $$V_{AIN1} - V_{AIN2} = I_{IDAC1} \bullet (R_{LEAD1} + R_{RTD}) - I_{IDAC2} \bullet R_{LEAD2}$$

So if R_{LEAD1} and R_{LEAD2} are equal and I_{IDAC1} and I_{IDAC2} are equal (to become I_{IDAC}), then the lead resistance errors cancel.

$$V_{AIN1} – V_{AIN2} = I_{IDAC} • R_{RTD}$$

3. Determine values for the IDAC excitation currents and reference resistor.

   The excitation current source in this design is selected to be 1mA. This maximizes the value of the RTD voltage while keeping the self-heating of the RTD low. The typical range of RTD self-heating coefficients is 2.5mW/°C for small, thin-film elements and 65mW/°C for larger, wire-wound elements. With 1-mA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4mW and keeps the measurement errors from self-heating to less than 0.01°C.

   After selecting the IDAC current magnitude, set R_{REF} = 820Ω. Using two matched 1-mA excitation currents sets the reference at 1.64V and the maximum RTD voltage is 400mV. The reference voltage acts as a level shift to place the input measurement to near mid-supply, putting the measurement in the PGA input operating range. With these values, the PGA gain can be set to 4 so that the maximum RTD voltage is near the positive full scale range without exceeding it.

   The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

   Using the maximum RTD resistance, the ADC input voltages are calculated in the following equations. The small lead resistances can be ignored for this calculation.

   $$V_{AIN1} = (I_{IDAC1} • R_{RTD}) + [(I_{IDAC1} + I_{IDAC2}) • R_{REF}] = (1mA • 400Ω) + (2mA • 820Ω) = 2.04V$$

   $$V_{AIN2} = (I_{IDAC1} + I_{IDAC2}) • R_{REF} = 2mA • 820Ω = 1.64V$$

   $$V_{INMAX} = 1mA • 400Ω = 400mV$$

4. Verify that the design is within the range of operation of the ADC.

   First, verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given that the gain is 4 and that AVDD is 3.3V and AVSS is 0V. As shown in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the absolute input voltage must satisfy the following:

   $$AVSS + 0.15V + [|V_{INMAX}| • (Gain − 1) / 2] < V_{AIN1}, V_{AIN2} < AVDD − 0.15V − [|V_{INMAX}| (Gain − 1) / 2]$$

   $$0V + 0.15V + [|V_{INMAX}| • (Gain − 1) / 2] < V_{AIN1}, V_{AIN2} < 3.3V − 0.15V − [|V_{INMAX}| (Gain − 1) / 2]$$

   $$0.75V < V_{AIN1}, V_{AIN2} < 2.55V$$

   Because the maximum and minimum input voltages seen at AIN1 and AIN2 (2.04V and 1.64V) are between 0.75V and 2.55V, the inputs are in the PGA operating range.

   Second, verify that the voltage seen at the IDAC output is within the current source compliance voltage. The IDAC1 pin is AIN0 which has the same voltage as AIN1. At the maximum voltage, V_{AIN0} is 2.04V. As shown in the Electrical Characteristics table in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the output voltage of the IDAC pin must be between AVSS and AVDD − 0.6V for an IDAC current of 1mA. In this example, with AVDD = 3.3V, the IDAC output must be:

   $$AVSS < V_{AIN0} = V_{AIN1} < AVDD − 0.6V$$

   $$0V < V_{AIN0} < 2.7V$$

With the previous result, the output compliance of the IDAC1 is satisfied. Because the IDAC2 pin is always at a lower voltage than the IDAC1 voltage, both current sources are in the compliance range.

5. Select values for the differential and common-mode input filtering for the ADC inputs and reference inputs.

   This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 × higher than the data rate of the ADC. The common-mode capacitors are selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 × higher than the differential input filtering. While series filter resistors offer some amount of input protection, keep the input resistors lower than 10kΩ, to allow for proper input sampling for the ADC.

   With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors be reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

   In this design, the data rate is chosen to be 20SPS using the low-latency filter of the ADS124S08. This filtering provides a low noise measurement with single-cycle settling and the ability to reject 50-Hz and 60-Hz line noise. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations.

   $$f_{IN\_DIFF} = 1 / [2 \cdot \pi \cdot C_{IN\_DIFF} (R_{RTD} + 2 \cdot R_{IN})]$$

   $$f_{IN\_CM} = 1 / [2 \cdot \pi \cdot C_{IN\_CM} (R_{RTD} + R_{IN} + R_{REF})]$$

   For the ADC input filtering, R_{IN} = 4.99kΩ, C_{IN_DIFF} = 47nF, and C_{IN_CM} = 4.7nF. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5.6kHz.

   The bandwidth for the reference input filtering is approximated in the following equation.

   $$f_{REF} = 1 / [2 \cdot \pi \cdot C_{REF} \cdot (R_{REF} + R_{IN\_REF})]$$

   For the reference input filtering, R_{IN_REF} = 4.02kΩ and C_{REF} = 100nF. This sets the differential filter bandwidth to 330Hz. Because REFN0 is set to ground, the common-mode filtering is removed. Matching the ADC input and reference input filtering may not be possible. However, keeping the bandwidth close may reduce noise in the measurement.

   For an in-depth analysis of component selection for input filtering, see *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.

6. If IDAC current mismatch error is significant, use two measurements to chop the error (optional).

   One of the original assumptions in the lead-resistance cancellation is that IDAC1 and IDAC2 match. If the two IDAC currents do not match, the mismatch causes an error that appears as gain error. The voltage across the RTD comes from the current of IDAC1, while the voltage across the reference resistor comes from the current of IDAC1 + IDAC2. For the ADS124S08, the typical IDAC current mismatch for a 1-mA IDAC current is 0.07%. This mismatch error leads to a gain error of 0.35% in the measurement. To remove this current mismatch error, the IDAC excitation currents may be chopped. This involves taking two measurements with the IDAC currents swapped.

   For chopping, first take a measurement with IDAC1 set to AIN0 and IDAC2 set to AIN3. Then set IDAC1 to AIN3 and IDAC2 to AIN0, swapping the current sources, and take a second measurement. In the first case, IDAC1 drives the RTD, in the second case IDAC2 drives the RTD. In both cases, the sum of IDAC1 and IDAC2 drive the reference resistor. By averaging the two chopped cases, the mismatch error is removed from the measurement. For a more detailed analysis of chopping see the IDAC Current Chopping section of the *A Basic Guide to RTD Measurements* application report.

Measurement Conversion

RTD measurements are typically ratiometric measurements. Using a ratiometric measurement, the ADC output code does not need to be converted to a voltage. This means that the output code gives a measurement only as

a ratio of the value of the reference resistor and does not require a precise value for the excitation current. The only requirement is that the current through the RTD and reference resistor are the same.

Equations for the measurement conversion are shown for a 24-bit ADC (without IDAC current chopping):

$$\text{Output Code} = 2^{23} \cdot \text{Gain} \cdot (V_{RTD} / V_{REF}) = 2^{23} \cdot \text{Gain} \cdot (I_{IDAC1} \cdot R_{RTD}) / [(I_{IDAC1} + I_{IDAC2}) \cdot R_{REF}]$$

If I_{IDAC1} is equal to I_{IDAC2} then the IDAC current terms drop out.

$$\text{Output Code} = 2^{23} \cdot \text{Gain} \cdot (I_{IDAC} \cdot R_{RTD}) / (2 \cdot I_{IDAC} \cdot R_{REF}) = 2^{22} \cdot \text{Gain} \cdot (R_{RTD} / R_{REF})$$

$$R_{RTD} = R_{REF} \cdot [\text{Output Code} / (\text{Gain} \cdot 2^{22})]$$

The ADC converts the measurement to the RTD equivalent resistance. Because of non-linearity in the RTD response, the conversion of the resistance to temperature requires an calculation from equation or lookup table. For more information about the conversion of RTD resistance to temperature, see *A Basic Guide to RTD Measurements*.

Register Settings

Configuration Register Settings for a Three-Wire PT100 RTD Measurement with Low-Side Reference and Two IDAC Current Sources Using the ADS124S08

Register Address	Register Name	Setting	Description
02h	INPMUX	12h	Select AIN_P = AIN1 and AIN_N = AIN2
03h	PGA	0Ah	PGA enabled, Gain = 4
04h	DATARATE	14h	Continuous conversion mode, low-latency filter, 20-SPS data rate
05h	REF	12h	Positive reference buffer enabled, negative reference buffer disabled, REFP0 and REFN0 reference inputs selected, internal reference always on
06h	IDACMAG	07h	IDAC magnitude set to 1mA
07h	IDACMUX	30h	IDAC1 set to AIN0, IDAC2 set to AIN3
08h	VBIAS	00h	VBIAS not used for any input
09h	SYS	10h	Normal mode of operation
07h (1)	IDACMUX	03h	IDAC1 set to AIN3, IDAC2 set to AIN0

(1) This second IDACMUX setting and conversion is used for chopping IDAC excitation current sources (optional).

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS124S0x in continuous conversion mode. The dedicated $\overline{\text{DRDY}}$ pin indicates availability of new conversion data. Pseudo code is shown without the use of the STATUS byte and CRC data verification. ADS124S08 *firmware example code* is available from the ADS124S08 product folder.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input
Set CS low;
Send 06;// RESET command to make sure the device is properly reset after power-up
Set CS high;
Set CS low;// Configure the device
Send 42// WREG starting at 02h address
05// Write to 6 registers
12// Select AINP = AIN1 and AINN = AIN2
0A// PGA enabled, Gain = 8
14// Continuous conversion mode, low-latency filter, 20-SPS data rate
12// Positive reference buffer enabled, negative reference buffer disabled,
  // REFP1 and REFN1 reference selected, internal reference always on
07// IDAC magnitude set to 1mA
30;// IDAC1 set to AIN0, IDAC2 set to AIN3
Set CS high;
Set CS low; // For verification, read back configuration registers
Send 22// RREG starting at 02h address
```

```
05// Read from 6 registers
00 00 00 00 00 00;// Send 6 NOPs for the read
Set CS high;
Set CS low;
Send 08;// Send START command to start converting in continuous conversion mode;
Set CS high;
Loop
{
Set CS low;// Configure the device for first chopped measurement
Send 47// WREG starting at 07h address
00// Write to 1 register
30;// IDAC1 set to AIN0, IDAC2 set to AIN3
Set CS high;
Wait for DRDY to transition low;
Set CS low;
Send 12// Send RDATA command
00 00 00;// Send 3 NOPs (24 SCLKs) to clock out data, Record Measurement 1
Set CS high;
Set CS low;// Configure the device for chopped current sources (optional)
Send 47// WREG starting at 07h address
00// Write to 1 register
03;// IDAC1 set to AIN3, IDAC2 set to AIN0
Set CS high;
Wait for DRDY to transition low;
Set CS low;
Send 12// Send RDATA command
00 00 00;// Send 3 NOPs (24 SCLKs) to clock out data, Record Measurement 2
Set CS high;
Average Measurement 1 and Measurement 2;
}
Set CS low;
Send 0A;//STOP command stops conversions and puts the device in standby mode;
Set CS to high;
```

RTD Circuit Comparison Table

RTD Circuit Topology	Advantages	Disadvantages
Two-wire RTD, low-side reference	Least expensive	Least accurate, no lead-resistance cancellation
Three-wire RTD, low-side reference, two IDAC current sources	Allows for lead-resistance cancellation	Sensitive to IDAC current mismatch, mismatch can be removed by swapping IDAC currents and averaging two measurements
Three-wire RTD, low-side reference, one IDAC current source	Allows for lead-resistance cancellation	Requires two measurements, first for RTD measurement, second for lead-resistance cancellation
Three-wire RTD, high-side reference, two IDAC current sources	Allows for lead-resistance cancellation, less sensitive to IDAC mismatch than using low side reference	Requires extra resistor for biasing, added voltage may not be compatible with low supply operation
Four-wire RTD, low-side reference	Most accurate, no lead-resistance error	Most expensive

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS124S08	24-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS124S08	Link to similar devices
ADS114S08 (1)	16-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS114S08	Link to similar devices

(1) The ADS114S08 is a 16-bit version of the ADS124S08 and may be used in similar applications.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, ADS124S08 Evaluation Module
- Texas Instruments, *ADS1x4S08 Evaluation Module User's Guide*

- Texas Instruments, ADS1x4S08 Firmware Example Code
- Texas Instruments, *A Basic Guide to RTD Measurements*
- Texas Instruments, *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2020) to Revision C (August 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	1

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