TEXAS INSTRUMENTS

DEM-DAI1870 EVM

User's Guide

February 2008 *AIP Consumer Audio—TI Japan*

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About This Manual

This document provides the information needed to set up and operate the DEM-DAI1870 EVM evaluation module, a test platform for the 16-bit, low-power PCM1870 stereo analog-to-digital converter (ADC). For a more detailed description of the PCM1870 product line, please refer to the product data sheet available from the Texas Instruments web site at http://www.ti.com. Support documents are listed in the section of this guide entitled ***Related Documentation from Texas Instruments***.

How to Use This Manual

Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the DEM-DAI1870 EVM.

Chapter 1 gives an overview of the PCM1870 ADC and the DEM-DAI1870 EVM. The EVM block diagram and primary features are also discussed.

Chapter 2 provides general information regarding EVM handling and unpacking, absolute operating conditions, and the default switch and jumper configuration. This chapter also discusses the EVM controller software

Chapter 3 is the hardware setup guide for the EVM, providing all of the necessary information needed to configure the EVM switches and jumpers for product evaluation.

Chapter 4 reviews the DEM-DAI1870 EVM switch and jumper configuration.

Chapter 5 discusses how to set up jumpers on the DEM-DAI1870 EVM motherboard for performance evaluation using an audio analyzer. It also presents the process for measuring dynamic characteristics and provides example characteristic data.

Chapter 6 includes the EVM electrical schematics, printed circuit board (PCB) layout, and the bill of materials.

Information About Cautions and Warnings

This document contains caution statements.

CAUTION

This is an example of a caution statement. A caution statement describes a situation that could potentially damage your software or equipment.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

The following documents provide information regarding Texas Instruments integrated circuits used in the assembly of the DEM-DAI1870 EVM. These documents are available from the TI web site. The last character of the literature number corresponds to the document revision that is current at the time of the writing of this User's Guide. Newer revisions may be available from the TI web site at http://www.ti.com/ or call the Texas Instruments Literature Response Center at (800) 477–8924 or the Product Information Center at (972) 644–5580. When ordering, identify the document(s) by both title and literature number.

Data Sheet	Literature Number
PCM1774 Product data sheet	SLAS551
PCM1870 Product data sheet	SLAS544A
DIT4096 Product data sheet	SBOS225B

If You Need Assistance

If you have questions regarding either the use of this evaluation module or the information contained in the accompanying documentation, please contact the Texas Instruments Product Information Center at (972) 644–5580 or visit the TI web site at www.ti.com.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense is required to take whatever measures may be required to correct this interference.

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Description

The DEM-DAI1870 EVM is a complete evaluation platform for the 16-bit, low-power PCM1870 ADC with microphone bias and microphone amplifier. All necessary connectors and circuitry are provided for interfacing to audio test systems and commercial audio equipment.

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1.1 Introduction—PCM1870

The PCM1870 is a low-power stereo ADC designed for portable digital audio applications. This ADC integrates a line-input amplifier, boost amplifier, microphone bias, programmable gain control, sound effects, and automatic level control (ALC).

It is available in a 4 mm × 5 mm QFN package and a 2.49 mm × 3.49 mm DSBGA package to reduce the overall device footprint. The PCM1870 accepts Right-Justified, Left-Justified, I^{2}S™, and digital signal processing (DSP) formats, providing an easy interface to audio DSPs and encoder chips. Sampling rates up to 50 kHz are supported. The user-programmable functions are accessible through a two- or three-wire serial control port.

1.1.1 Key Features

Major features of the PCM1870 include:

- Analog Front End:
  - Stereo single-ended input with multiplexer (mux)
  - Mono differential input
  - Stereo programmable gain amplifier (PGA)
  - Microphone amplifier (+12dB, +20dB) and bias
- Analog Performance Dynamic Range: 90 dB
- Power-Supply Voltage:
  - 1.71 V to 3.6 V for digital I/O section
  - 1.71 V to 3.6 V for digital core section
  - 2.4 V to 3.6 V for analog section
- Low Power Dissipation:
  - 13 mW in record, 1.8/2.4 V, 48 kHz, stereo
  - 5.3 mW in record, 1.8/2.4 V, 8 kHz, mono
  - 3.3 μW in all power down
- Sampling Frequency: 5 kHz to 50 kHz
- Auto Level Control for Recording
- Operation From a Single Clock Input without PLL
- System Clock:
  - Common-audio clock (256 f_S/384 f_S), 12 MHz/24 MHz, 13 MHz/26 MHz, 13.5 MHz/27 MHz, 19.2 MHz/38.4 MHz, 19.68 MHz/39.36 MHz
- Two- (I^{2}C™) or Three- (SPI™) Wire Serial Control
- Programmable Function by Register Control:
  - Digital soft mute
  - Power up/down control for each module
  - +30-dB to –12-dB gain for analog inputs
  - 0-dB/12-dB/20-dB boost for microphone input
  - Parameter settings for ALC
  - Three-band tone control and 3D sound
  - High-pass filter and two-stage notch filter
- Pop-Noise Reduction Circuit
- Register-compatible with PCM3793A/94A and PCM1774
- Operating Temperature Range: –40°C to +85°C
- Packages: 4 mm × 5 mm QFN and 2.49 mm × 3.49 mm DSBGA

1.2 Pin Assignments and Terminal Functions

Figure 1-1 shows the pin assignments for the PCM1870. Table 1-1 lists the terminal functions (for the QFN-24 package option).

PCM1870RHF Package
(Top View)

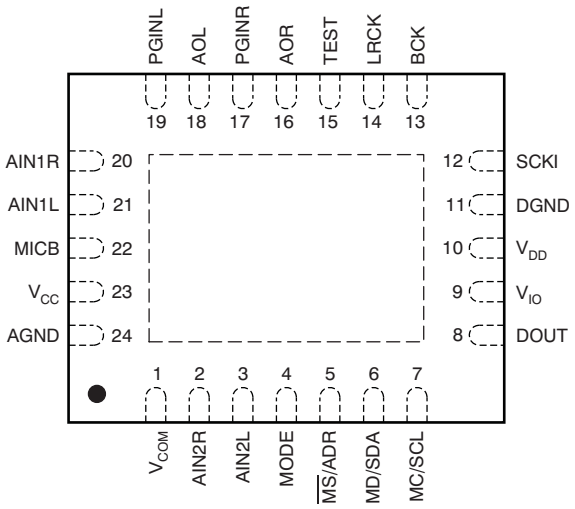

Figure 1-1. PCM1870 Pin Assignments

Table 1-1. PCM1870 Terminal Functions

Name	QFN-24 Terminal	I/O	Description
V_{COM}	1	–	Common voltage for analog
AIN2R	2	I	Analog input 2 for R-channel
AIN2L	3	I	Analog input 2 for L-channel
MODE	4	I	Two-wire or three-wire interface selection (LOW: SPI, HIGH: I^2C)
$\overline{MS}$/ADR	5	I	Mode control select for three-wire/two-wire interface
MD/SDA	6	I/O	Mode control data for three-wire/two-wire interface
MC/SCL	7	I	Mode control clock for three-wire/two-wire interface
DOUT	8	O	Serial audio data output
V_{IO}	9	–	Power supply for digital I/O
V_{DD}	10	–	Power supply for digital core
DGND	11	–	Ground for digital
SCKI	12	I	System clock
BCK	13	I/O	Serial bit clock
LRCK	14	I/O	Left and right channel clock
TEST	15	I	Test pin. Should be connected to ground.
AOR	16	O	Microphone amp output for R-channel
PGINR	17	I	Analog input to gain amp for R-channel
AOL	18	O	Microphone amp output for L-channel
PGINL	19	I	Analog input to gain amp for L-channel
AIN1R	20	I	Analog input 1 for R-channel
AIN1L	21	I	Analog input 1 for L-channel
MICB	22	O	Microphone bias source output
V_{CC}	23	–	Power supply for analog
AGND	24	–	Ground for analog

1.3 DEM-DAI1870 EVM Description

The DEM-DAI1870 evaluation module permits user control of the entire PCM1870 system. The EVM allows users to record in analog through a line input, and digitally with a stereo/mono microphone input through an optical cable or by RCA jacks, as shown in Figure 1-2.

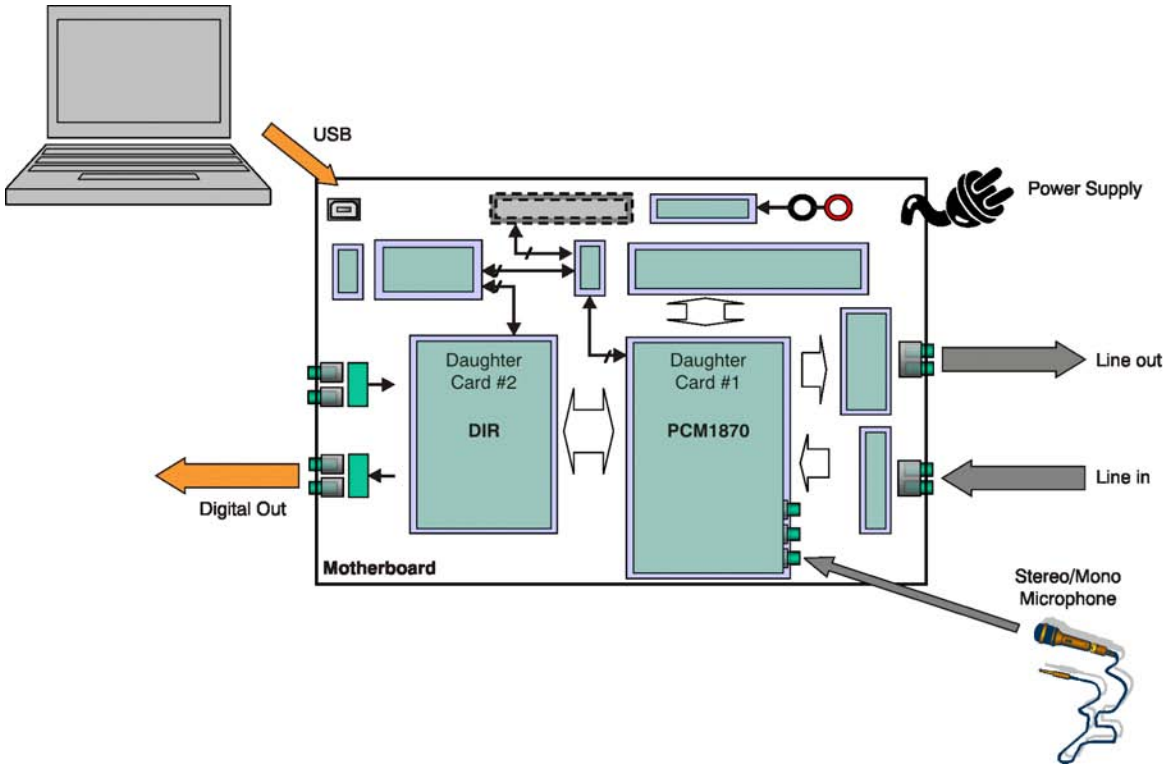

Figure 1-2. DEM-DAI1870 EVM System Diagram

Getting Started

This chapter provides information regarding handling and unpacking the DEM-DAI1870 EVM, as well as the EVM absolute operating conditions and a description of the factory default switch and jumper configurations.

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2.1 Electrostatic Discharge Warning

Many of the components on the DEM-DAI1870 EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

CAUTION

Failure to observe ESD handling procedures may result in damage to EVM components.

2.2 Unpacking the EVM

Upon opening the DEM-DAI1870 EVM package, please check to make sure that the following items are included:

- One DEM-DAI/LPC-USB (Motherboard)
- One DEM-PCM1870RHF/1774RGP-A (Daughter Card #1)
- One DEM-TRCV/LPC (Daughter Card #2)

If any of these items are missing, please contact the Texas Instruments Product Information Center nearest you to inquire about a replacement.

2.3 Default Configuration

Figure 2-1 and Figure 2-2 illustrate the default EVM configuration and the default external equipment connection configuration, respectively.

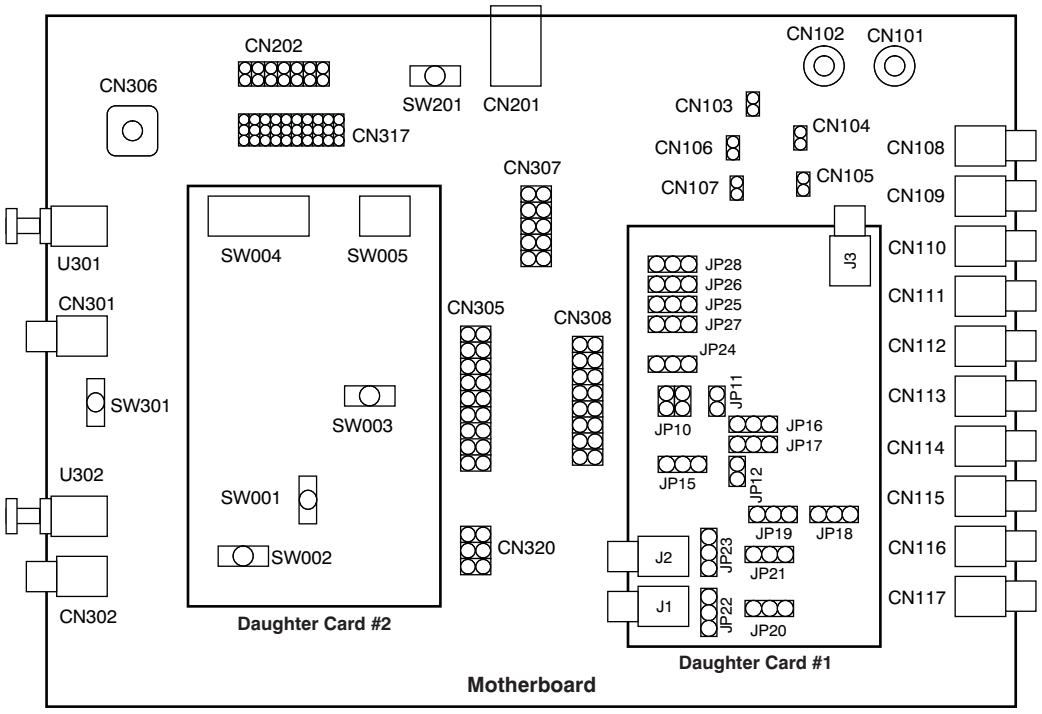

Figure 2-1. EVM Configuration

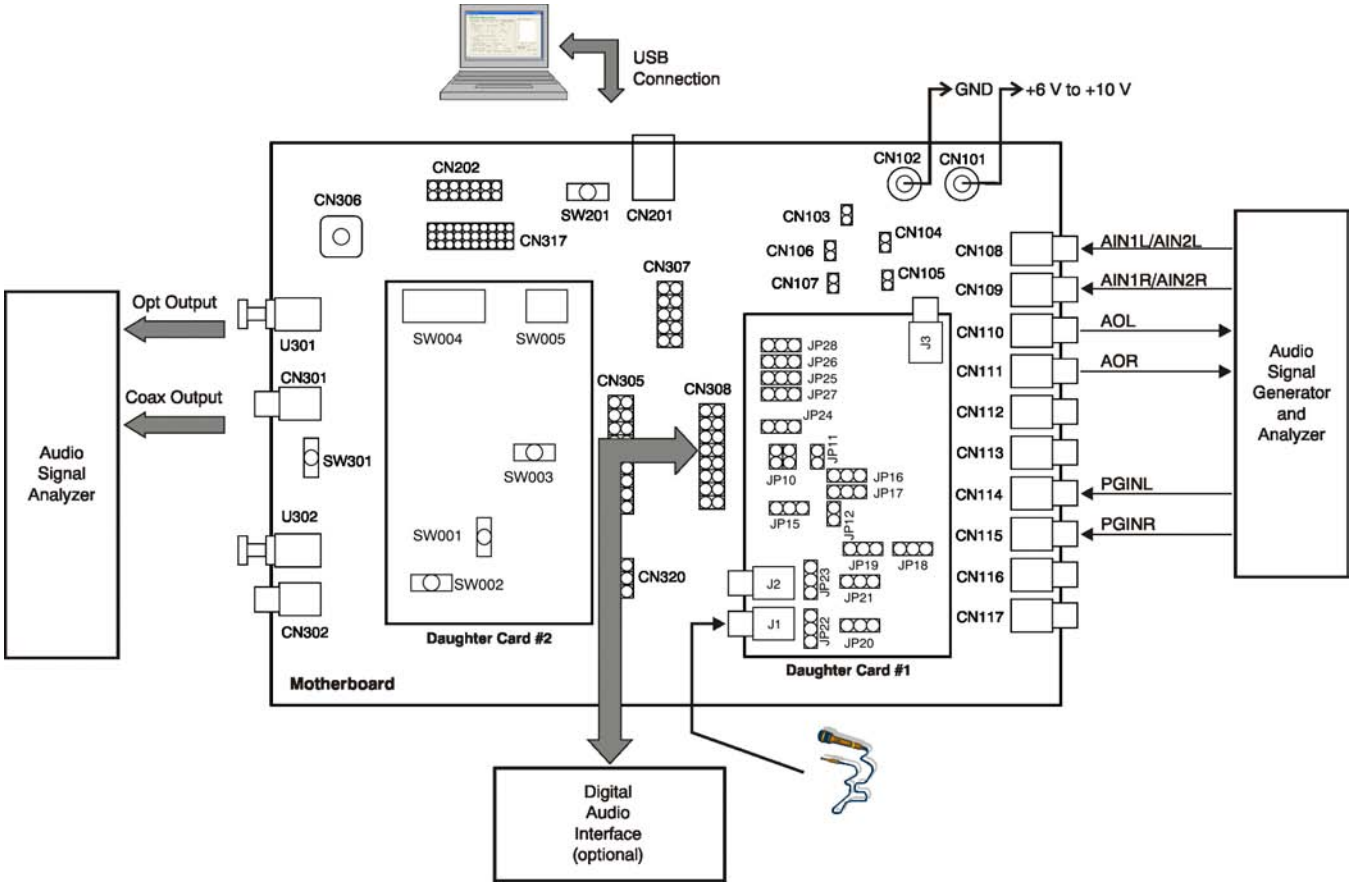

Figure 2-2. EVM and External Equipment Connections

The factory default configuration for the DEM-DAI1870 EVM is listed below.

Motherboard:

- CN101, CN102: Connect dc power supply positive lead (+) to CN101 and negative lead (–) to CN102
- SW301: Set *Opt* or *Coax* output for the proper cable connection

Daughter Card #1 (DEM-PCM1870RHF/1774RGP-A):

- JP1-9, JP13, JP14, and JP29: these jumper pins are not used
- For other jumper settings, please refer to the chapter, Switches and Connectors.

Daughter Card #2 (DEM-TRVC/LPC):

- SW001: Set *Opt* or *Coax* for S/PDIF input to DIR:LC89052T
- SW002: Set to silkscreen *SW002 RESET* side (releasing reset)
- SW003: Set *X'tal* to use onboard crystal oscillator

There is no need to change the setting of the shorting plugs for basic operation. Jumper settings strongly depend on the audio interface.

Set-Up Guide

This chapter discusses how to set up the DEM-DAI1870 EVM and describes the EVM software.

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3.1 Basic Operating Set-Up

Follow these steps to set up the DEM-DAI1870 EVM for operation.

Step 1. When using the kit for the first time, install the TUSB3410 VCP (Virtual COM Port) driver to the host PC. To install the driver, refer to the *Virtual COM Port Driver Installation Instructions.pdf* located in the DEM-DAI1870 folder of the software CD or available for download through the TI web site.

Step 2. Connect the audio signal sources and/or receiver, using one of these connections:

- S/PDIF cable (optical or coaxial)
- Analog input/output (RCA)

Step 3. Connect microphone, audio amplifier, or measurement equipment, if necessary.

Step 4. Confirm that jumpers CN103–CN107 are shorted.

Step 5. Connect the USB cable between the host PC and the motherboard (CN201).

Step 6. Apply +6 V to +10 V to the motherboard (CN101, CN102 for power supply).

Step 7. Execute *EVM1870A.exe*.

When the installation is complete, the EVM software is ready to use.

3.2 Software Control and Operation

This section of the user's guide reviews the operation and configuration of the EVM controller software.

3.2.1 User Interface Panel

After finishing the installation process (as explained in Section 3.1), the user interface panel shown in Figure 3-1 appears.

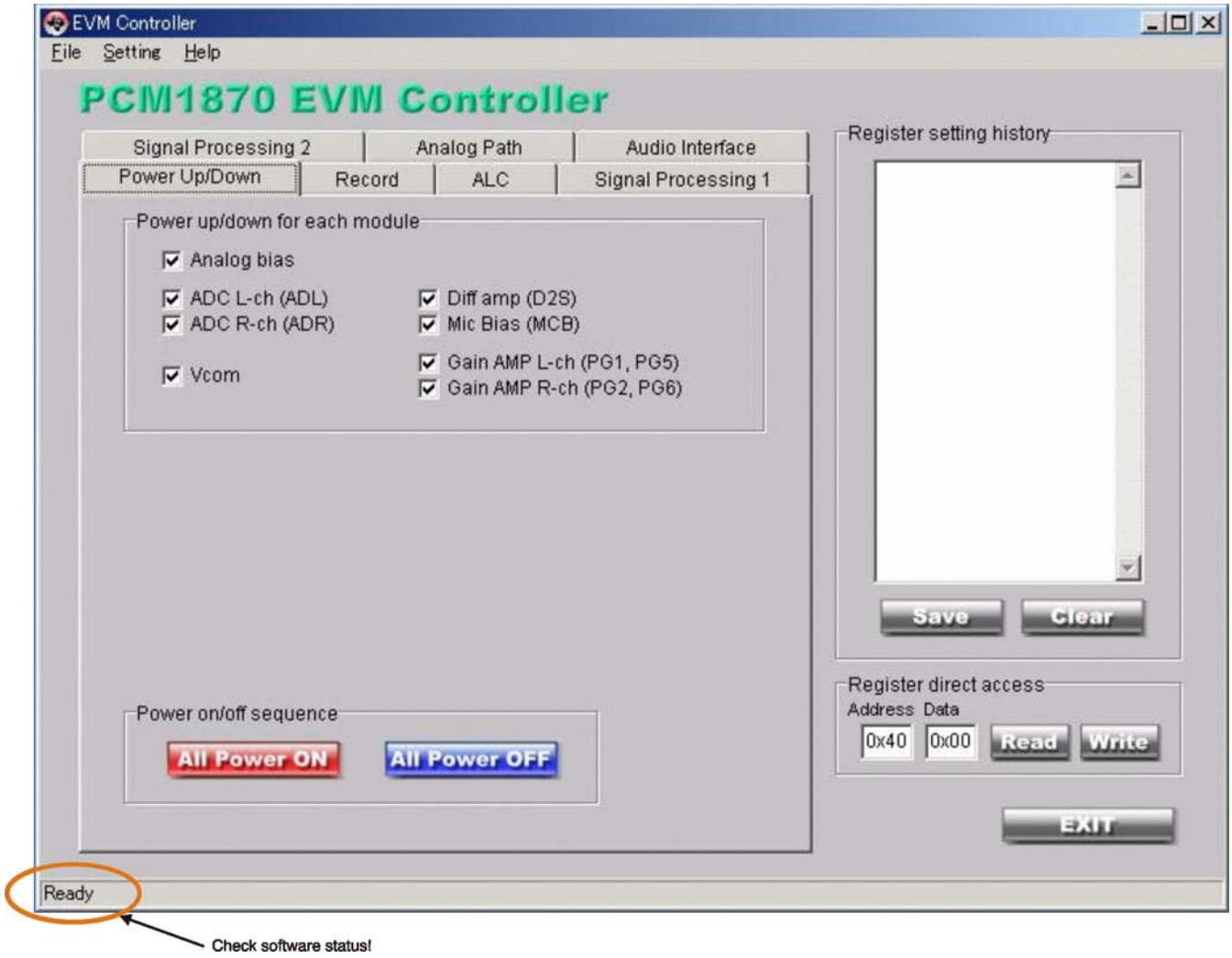


Figure 3-1. User Interface Window

Check to see that a ***Ready*** notation appears in the lower left-hand corner after successful I^2C communication is established. Otherwise, you will see an error box showing a communication error (as shown in Figure 3-2).

Figure 3-2. Communication Error Message

If you receive this error message, confirm the set-up procedures and restart the software. Shut it down and then execute *EVM1870A.exe* a second time.

There are four primary sections of the user interface panel (see Figure 3-1):

- Module controller, for functions such as record, signal processing, audio format, and so forth;
- Power on/off sequence controller
- Register setting history controller
- Register direct access controller

3.2.2 Power On/Off Sequence

By default, each module is set without any of the checkboxes toggled in the Power Up/Down menu. All modules are set to a power-down condition.

Click *All Power On* (the red box, as shown in Figure 3-3) to easily start EVM operation, instead of powering up the module manually.

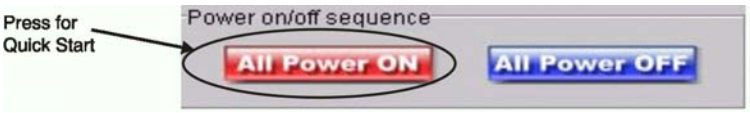


Figure 3-3. Power On/Off Sequence Function Buttons

Note: If pressing the Power On/Off sequence button has no effect, check to see that the two files *power_on.csv* and *power_off.csv* are located in the same folder on the PC as the EVM software (EVM1870A.exe).

3.2.3 Module Function Controls

The PCM1870 EVM controller software contains seven tabs:

- Power Up/Down: to power up and power down each module
- Record: executes gain control for ADC input
- ALC: tunes the Automatic Level Control function
- Signal Processing 1: adjusts the tone control and notch filter coefficient
- Signal Processing 2: adjusts the zero-crossing control and high-pass filtering
- Analog Path: selects analog input
- Audio Interface: selects the audio interface for the ADC

This section discusses each of these tab operations and controls.

3.2.3.1 Power Up/Down

This menu (shown in Figure 3-4) allows users to manually power up or power down each module. Click the appropriate checkboxes to power up or power down a specific module. Table 3-1 shows the register mapping for each module setting.

Abbreviations such as *ADL/ADR*, *D2S*, and *PG1, PG2* stand for corresponding modules that are described in the block diagram of the PCM1870 (see Figure 3-6).

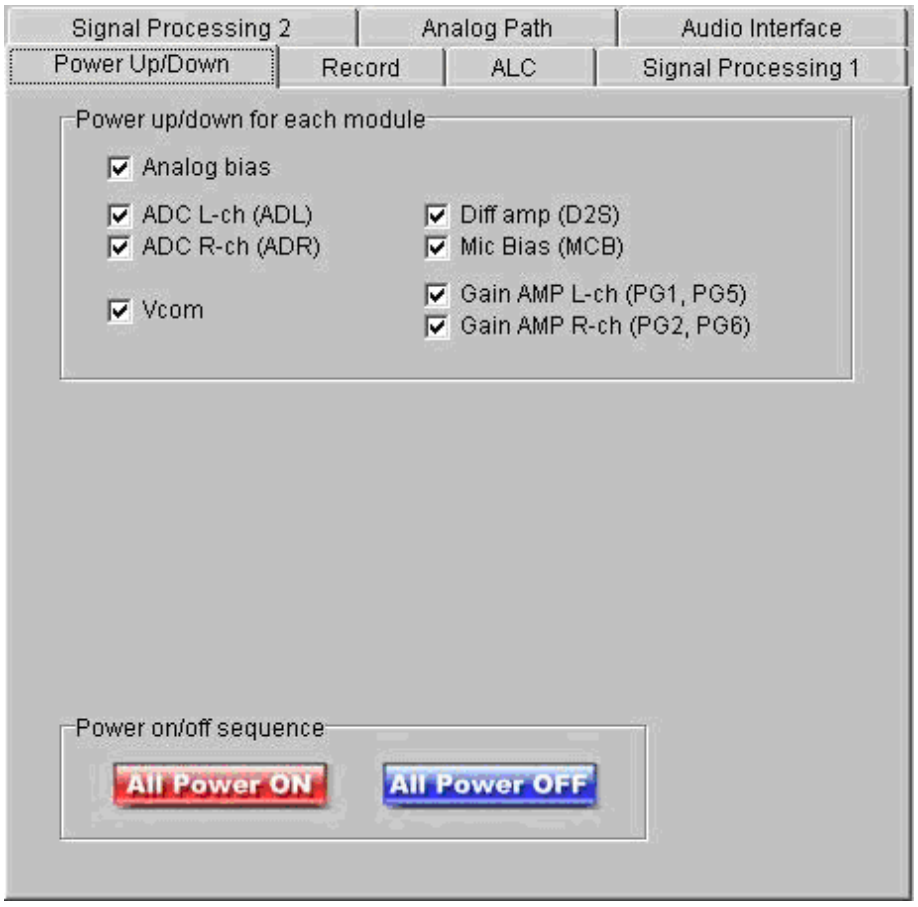


Figure 3-4. Internal Module Power Up/Down Function Menu Tab

Table 3-1. Register Mapping for Power Up/Down Module

Check Box	Internal Module	Register
Analog Bias	Analog bias	Reg#73 bit7 [PBIS]
V_{COM}	Analog common voltage	Reg#74 bit0 [PCOM]
ADC L-ch (ADL)	ADC and decimation filter L-channel	Reg#82 bit0 [PADL]
ADC R-ch (ADR)	ADC and decimation filter R-channel	Reg#82 bit1 [PADR]
Gain AMP L-ch (PG1, PG5)	Gain amp L-channel (PG1 and PG5)	Reg#82 bit4 [PAIL]
Gain AMP R-ch (PG2, PG6)	Gain amp R-channel (PG2 and PG6)	Reg#82 bit5 [PAIR]
Diff amp (D2S)	D2S for AIN1	Reg#82 bit3 [PADS]
Mic Bias (MCB)	Microphone bias amp	Reg#82 bit2 [PMCB]

3.2.3.2 Record

Figure 3-5 shows the Record function tab options.

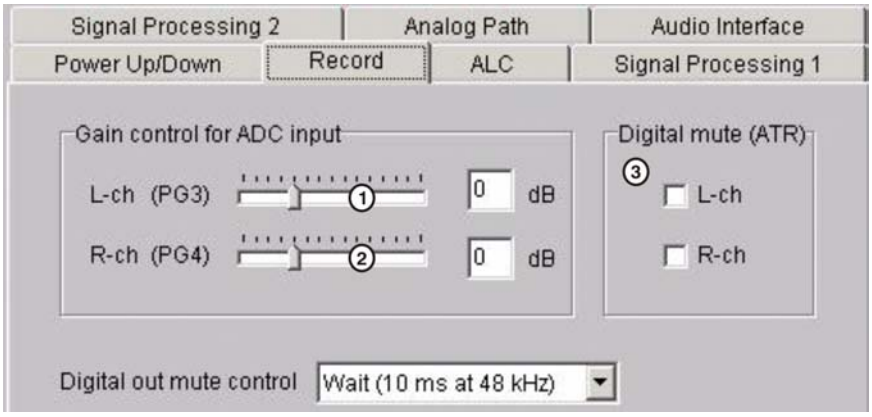


Figure 3-5. Record Function Menu Tab

Figure 3-6 shows the EVM modules that correspond to the record function.

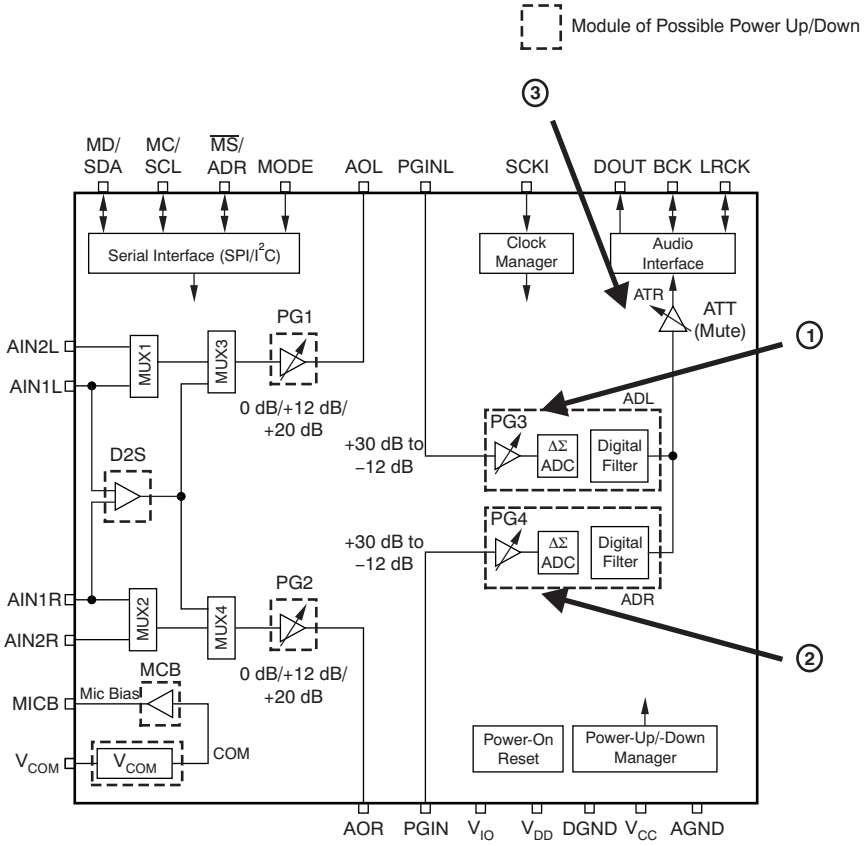


Figure 3-6. EVM Modules Corresponding to Record Function

Gain Control for ADC Input Options

Move the L-ch (PG3) and R-ch (PG4) sliders to adjust the gain of the incoming analog signal inputs to the ADC.

- The L-ch slider manipulates the programmable gain amp (PG3) placed in front of the ADC.
- The R-ch slider controls the programmable gain amp (PG4) placed in front of the ADC.

Digital Mute (ATR) Options

Click the respective *Digital mute (ATR)* checkboxes if a mute function is needed for the ADC digital output.

- The mute checkbox enables a digital soft mute on the ADC for each channel.
- Mute waiting control enables a mute control.

Digital Out Mute Control Options

Select the *Digital out mute control* drop-down menu to enable the mute time control.

- Apply *wait* or *no wait* for the ADC mute.

3.2.3.3 ALC (Automatic Level Control)

Figure 3-7 shows the Automatic Level Control (ALC) function menu tab.

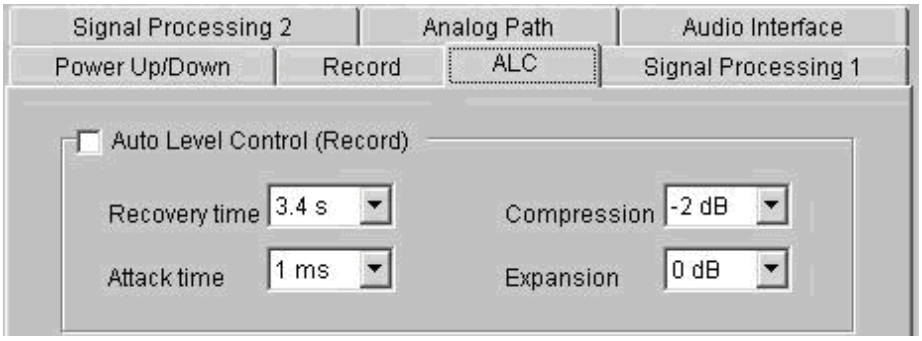


Figure 3-7. ALC Function Menu Tab

Auto Level Control (Record) Options

Select *Recovery time* and *Attack time* using the respective drop-down menu and corresponding gain control for each option to use the automatic level control function.

ALC compression and expansion characteristics are shown in Figure 3-8.

Compression is defined as avoiding degradation of sound quality by saturation when there are strong or excessively large sound data input.

Expansion means to boost weak or low input data in order to adjust the moderate amplitude level for recording.

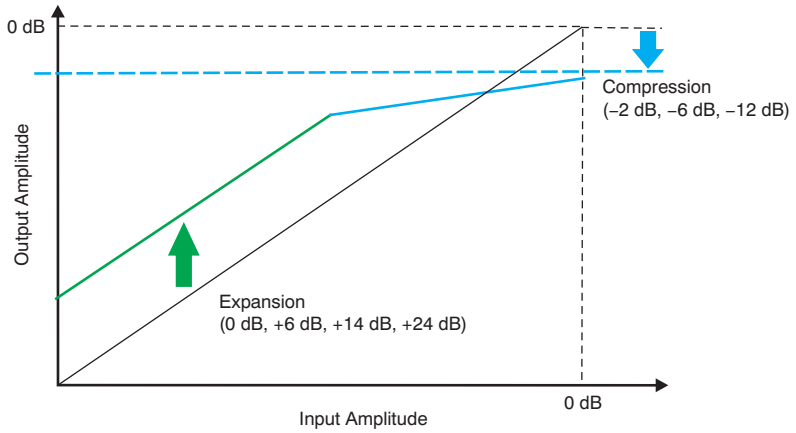


Figure 3-8. ALC Compression and Expansion Characteristics

3.2.3.4 Signal Processing 1

Figure 3-9 illustrates the Signal Processing 1 function menu tab.

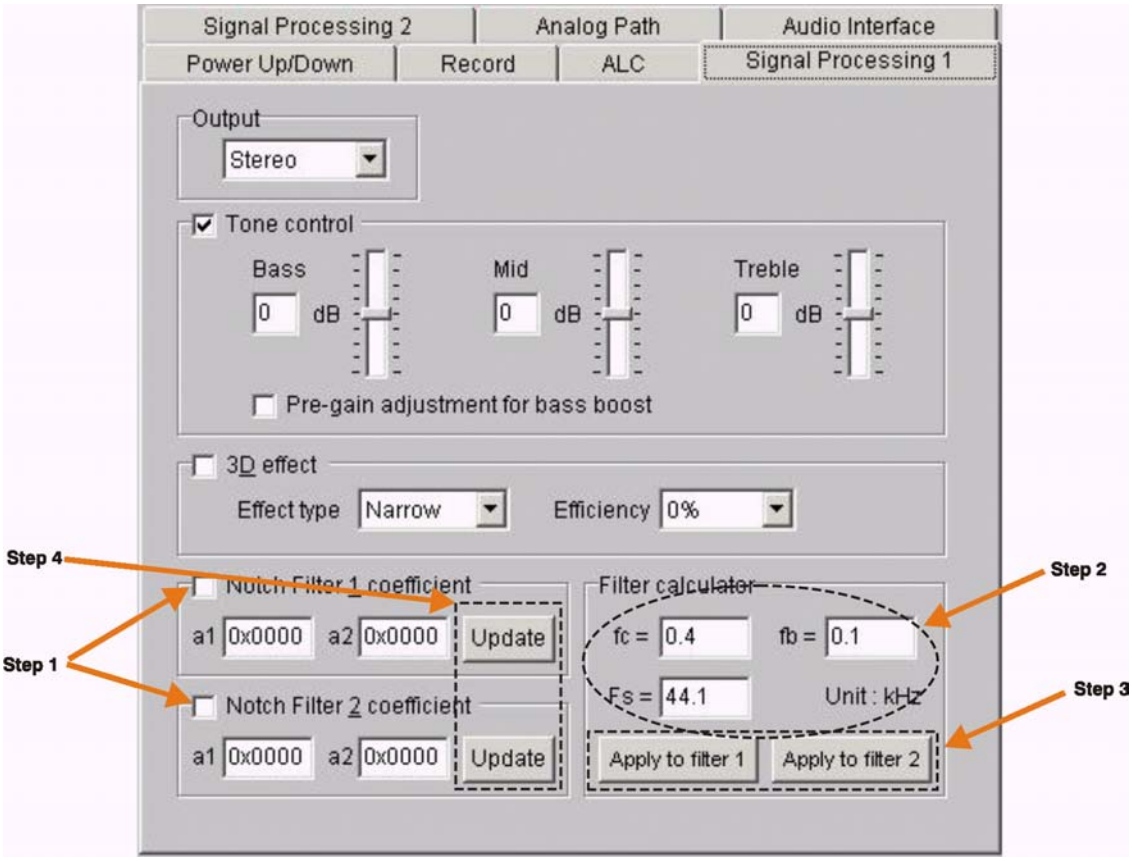


Figure 3-9. Signal Processing 1 Function Menu Tab

Output Options

Select the *Source* drop-down menu to choose between a stereo or mono configuration.

- The output configuration can be selected by choosing stereo or mono.

Tone Control Options

Move the Bass, Mid, and Treble sliders to adjust the tone control gain. The tones are controlled by the respective tone sliders. A three-band tone control characteristic plot is shown in Figure 3-10.

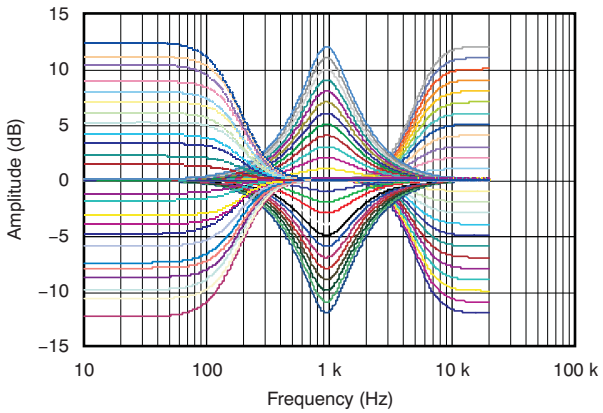


Figure 3-10. Three-Band Tone Control (Bass, Mid, Treble)

3D Effect Options

By implementing a 3D effect in this option box, the PCM1870 provides 3D sound to the headphone and speaker outputs with low power consumption during ADC operation. Check the *3D effect*, then select an *Effect* type and an *Efficiency* drop-down menu to obtain the desired 3D enhancement.

Effect type means the selection of a band-pass filter (BPF); the BPF filters the sound, and enables a high percentage of heavy 3D enhancements to be applied to the signal.

Effect type and efficiency are controlled through the use of checkboxes.

Notch Filter 1 Coefficient, Notch Filter 2 Coefficient Options

In some applications, incoming noise such as motor control noise, CCD noise and other mechanical noise may not be negligible. The PCM1870 provides a very useful function to reduce such interference with the notch filter function.

When the checkbox of Notch Filter 1 Coefficient or Notch Filter 2 Coefficient is checked, coefficient a_1 and a_2 of the notch filter can be programmed at each edit box. (Note that not all users need to calculate these coefficients for a given application.)

Load the values of f_c, f_b and f_S into the Filter Calculator group box.

Click *Apply to Filter 1* or *Apply to Filter 2*. The calculated coefficient will then appear in the a_1 and a_2 edit box.

Finally, click the *Update* button for each Notch filter coefficient. To complete the notch filter operation, the *Update* button must be clicked.

Note that Update step is required each time new or different parameters are loaded to the dialog box.

Follow these steps to update the notch filter coefficient:

Step 1. Click the checkbox of Notch Filter 1 Coefficient or Notch Filter 2 Coefficient.

Step 2. Input the parameter values f_c, f_b and f_S.

Step 3. Click *Apply to Filter 1* or *Apply to Filter 2*.

Step 4. Update for each notch filter coefficient.

Each coefficient is calculated using the following equations.

$a_1 = –(1 + a_2)\cos(\omega_o)$

$a_2 = [1 – \tan(\omega_b/2)] / [1 + \tan(\omega_b/2)]$

where:

- f_S = sampling frequency
- f_c = center frequency
- f_b = bandwidth
- $\omega_o = 2\pi f_c/f_S$ represents the angular center frequency
- $\omega_b = 2\pi f_b/f_S$ is the parameter to adjust bandwidth

Here are several example coefficient calculations using Equation 3-1 and Equation 3-2. These measurements are also shown in Figure 3-12.

Given: f_S = 16 kHz, f_c = 0.5 kHz, f_b = 0.2 kHz

a_2 = 0.924390492 (converted decimal to hex: 3B29h)

a_1 = –1.887413868 (converted decimal to hex: 8735h)

a_2: F[215:208] = 3Bh, F[207:200] = 29h

a_1: F[115:108] = 87h, F[107:100] = 35h

Figure 3-11 illustrates the notch filter characteristic. All users can select any frequencies that can be used by the application system based on the notch filter coefficient theory discussed here.

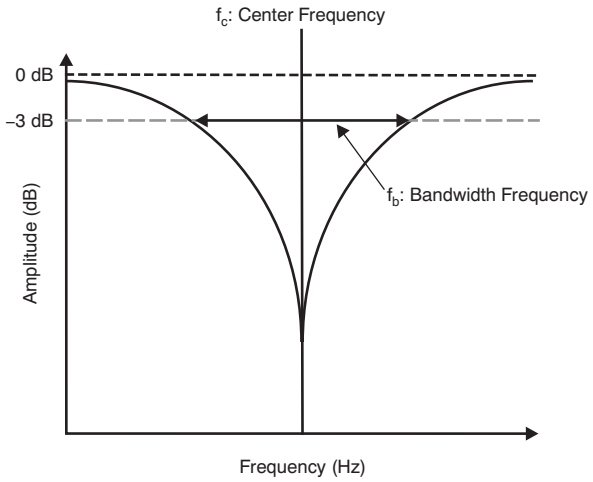


Figure 3-11. Notch Filter Characteristic Model

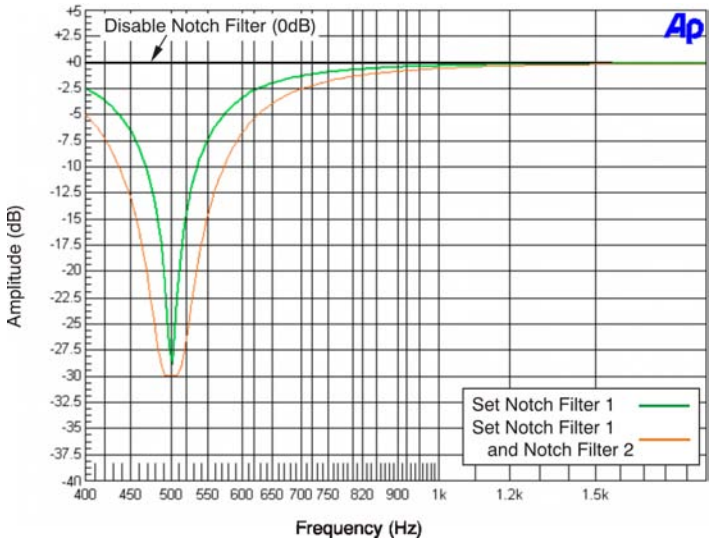


Figure 3-12. Example of Measured Notch Filter Characteristic

3.2.3.5 Signal Processing 2

The Signal Processing 2 Function menu tab is shown in Figure 3-13.

Figure 3-13. Signal Processing 2 Function Menu Tab

Zero Cross Control Options

Select the *Zero cross control* to enable the zero crossing function. When zero crossing is enabled, digital attenuation and the analog volume level change at the zero crossing point to avoid an audible zipper noise.

High-Pass Filter Options

Choose the *High Pass Filter* menu to determine the cutoff frequency (f_c) of the incoming analog signal inputs to the ADC.

The cutoff frequency of the ADC high-pass filter is provided as a sampling frequency of 48 kHz in this drop down menu, so that the cutoff will be scaled down to the corresponding value when sampling frequencies other than 48kHz (such as 16 kHz or 22.05 kHz) are used.

The ADC high-pass filter cutoff frequency can be set from this option.

3.2.3.6 Analog Path

Figure 3-14 shows the Analog Path Function menu.

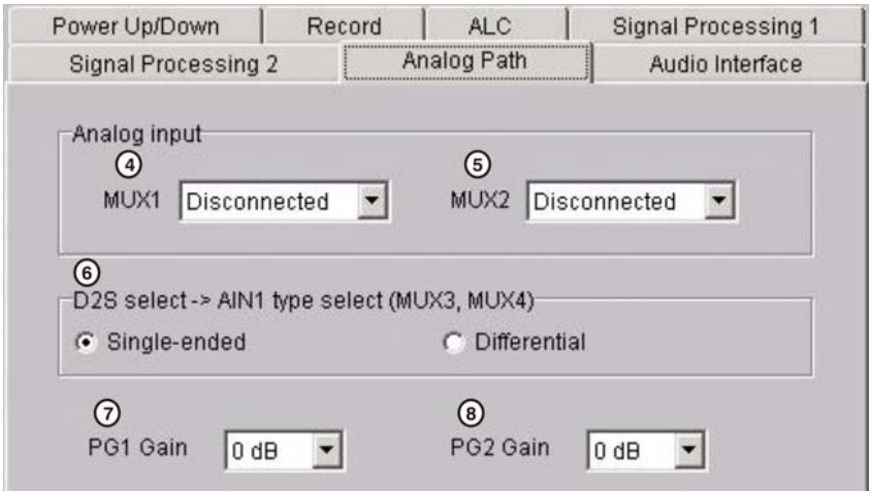


Figure 3-14. Analog Path Function Menu Tab

Figure 3-15 illustrates the modules that correspond to the analog path function.

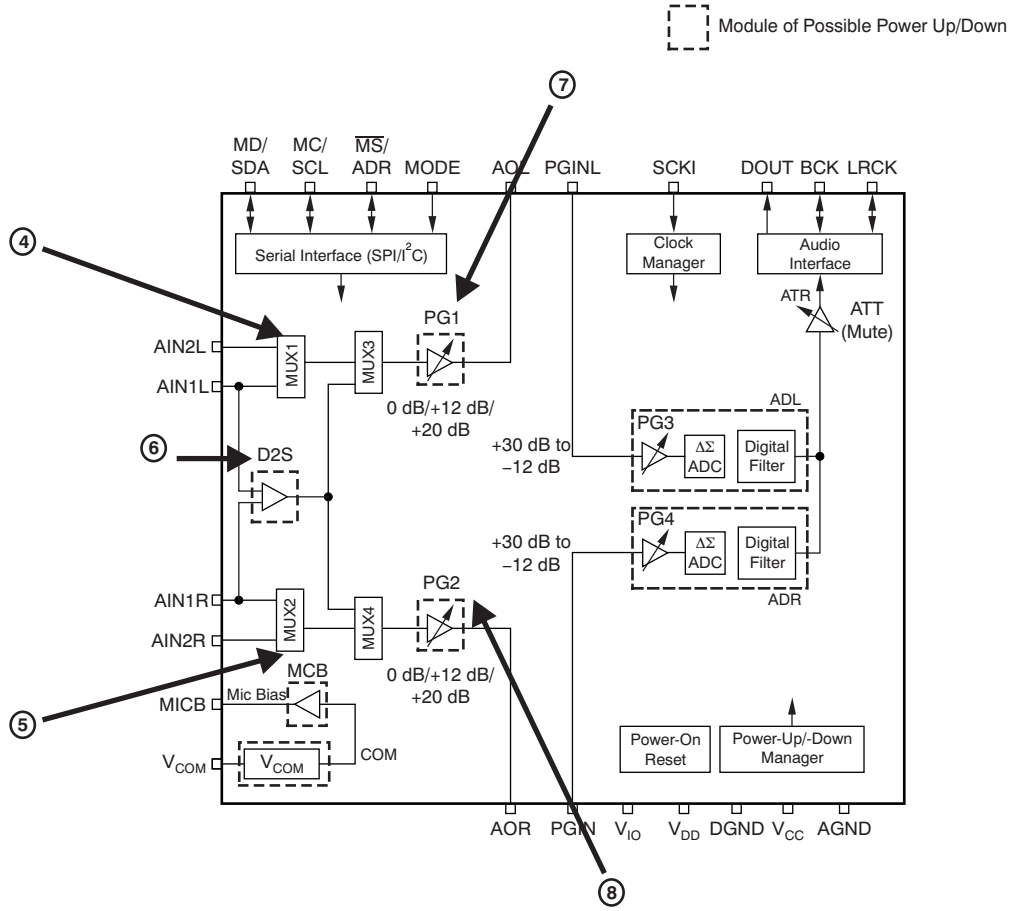


Figure 3-15. Modules Corresponding to Analog Path Function

Analog Input Options

This option selects the appropriate MUX for the respective left or right channel.

- MUX1 selects the L-channel source (AIN1L/AIN2L).
- MUX2 selects the R-channel source (AIN1R/AIN2R).

D2S Select Options

The analog input can be configured as single-end or differential. Select the *D2S* drop-down menu to choose between differential or single-ended inputs. If differential is selected, AIN1L and AIN1R are used as differential inputs.

Mic Boost Options

This checkbox sets (or resets) the microphone pre-amp PG1 (L-ch) or PG2 (R-ch). The gain can be set to 0 dB (flat), +12 dB, or +20 dB.

3.2.3.7 Audio Interface

Figure 3-16 shows the Audio Interface Function menu.

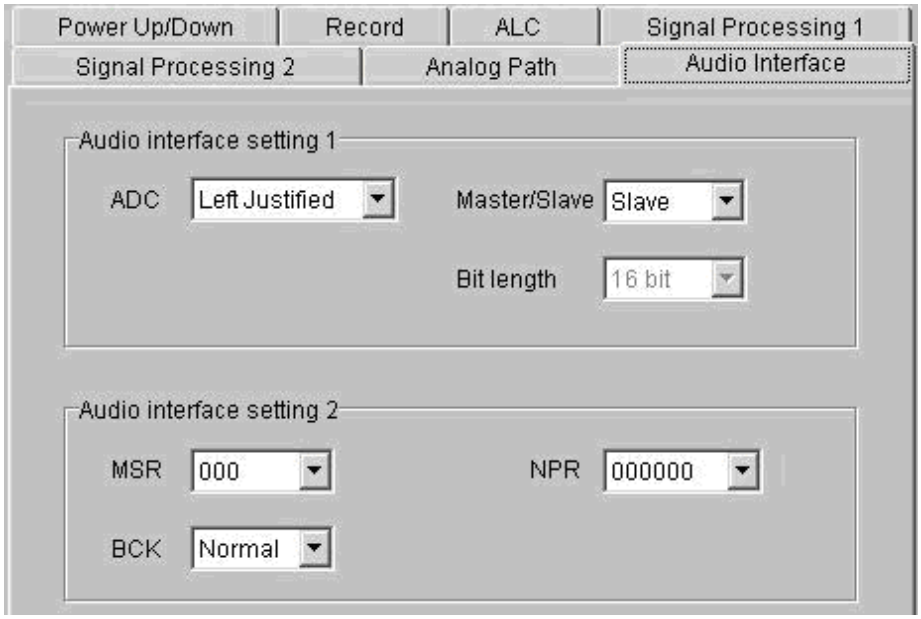


Figure 3-16. Audio Interface Function Menu Tab

Audio Interface Setting 1 Options

Use this section of the menu to set the audio data format for the ADC output. Set the operating mode as Master or Slave.

Audio Interface Setting 2 Options

Use this section of the menu when working in Master mode.

- **MSR:** sets system clock rate
- **NPR:** sets system clock divider rate
- **BCK:** chooses between normal and burst BCK output

  Burst operation of BCK in master mode will contribute to greater overall reduction in power consumption. See the PCM1870 data sheet for the possible combinations of these register settings.

3.2.4 LC89052T (DIR: Digital Audio I/F Receiver) Control Window

Figure 3-17 illustrates the LC89052 Interface format choices.

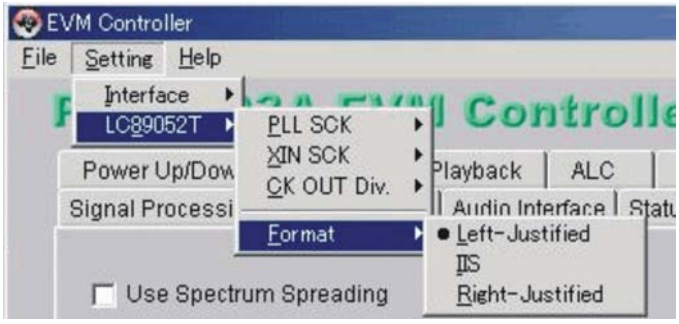


Figure 3-17. LC89052 Interface Format Selection Options

3.2.4.1 Audio Clock/Data Control Options

There are several options available for the audio clock and data control features in the DEM-DAI1870 EVM software.

For the system audio clock control, users can select any of these options:

- PLL SCK: Selects the system clock rate for the PCM1870
- XIN SCK or E-SCK: Selects the crystal oscillator frequency on Daughter Card #2
- CKOUT Div: Selects the dividing rate for CKOUT

The serial audio data format is controlled by the other part of the drop-down menu; see Figure 3-17. Select the data format for the DAC interface of the PCM1870 (it should match with the *DAC* setting on the *Audio Interface* tab).

3.2.5 Register Setting History

When any checkboxes are selected on any tab of the software GUI (including power up/down operation, corresponding resistor address, and so forth), the register value is automatically written into the register setting history panel. These parameters can then be saved, allowing users to identify a particular sequence setting that was sent to the device under test.

Any operating sequence settings can be saved as a comma-separated value (*.csv) file, with an identifiable name. This archive feature is useful when the same sequence settings are required for continued testing. The list of available *.csv files refreshes and displays when the *Clear* button is clicked.

Figure 3-18 shows the Register Setting History display window.

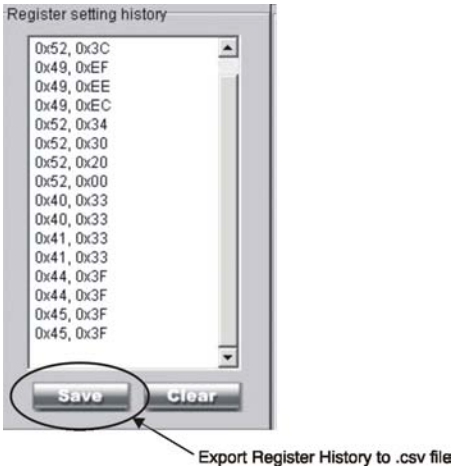


Figure 3-18. Register Setting History Window

3.2.5.1 Modifying a .csv File

The .csv file stores a sequence of register settings for the PCM1870. To load a given register setting, it should be written in hex code, as shown in Figure 3-19; use the left row for resistor addresses and the right row for resistor values.

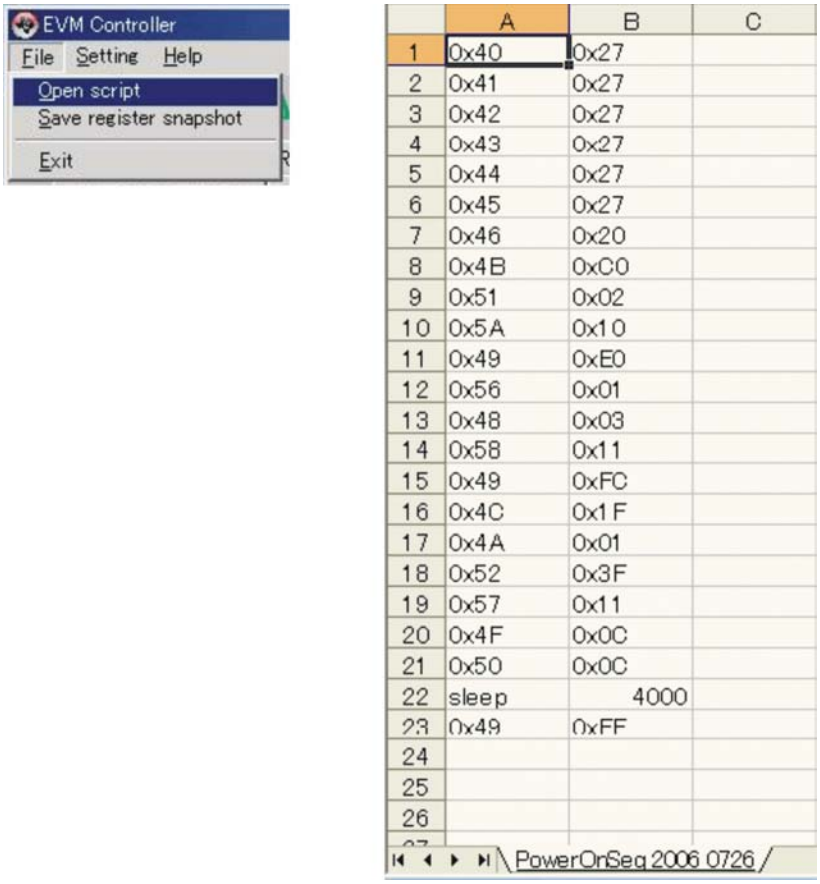


Figure 3-19. Opening and Modifying a .csv File

A *sleep* line can be inserted for implementing an interval (or wait) time until executing the next line of the file. If the cell is blank, no wait time will be executed. Files can be imported and exported using the *Open script* and *Save register snapshot* options.

3.2.6 Register Direct Access

Figure 3-20 illustrates the register direct access dialog.

Read function:

The *Read* function is only available in I^2C mode. The register value can be read in I^2C mode. To read the value, enter the Address number (in hex code format) in the left box and click the *Read* button. Data corresponding to the address appears.

Write function:

This window also enables the user to write the register value directly. Enter the Address number and data (both in hex code format) in the respective fields and click the *Write* button.

Figure 3-20. Register Direct Access Dialog

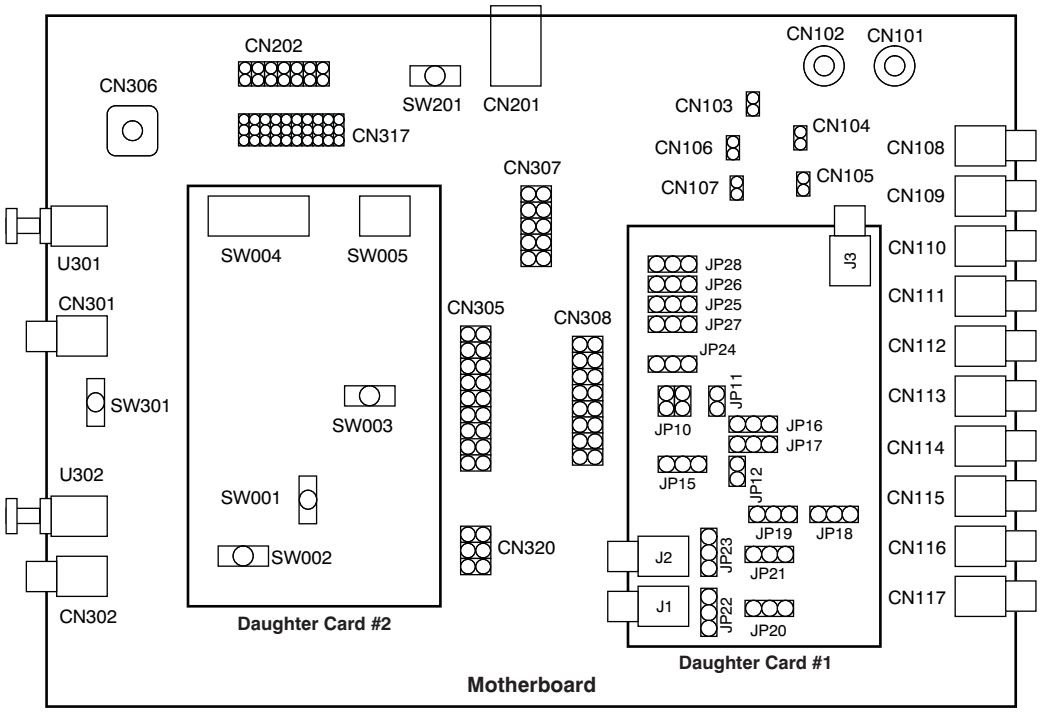
Switches and Connectors

This chapter reviews the DEM-DAI1870 EVM switch and jumper configuration.

Topic **Page**

4.1 Overview

Figure 4-1 shows the location of the switches and connectors on the EVM board.



Note: Silkscreen symbol ***CN320*** is not printed on the motherboard, but it is located in the position described.

Figure 4-1. EVM Configuration (RHF Package)

Note: See Section A.2.2 for an illustration of the EVM package for the wafer chip-scale package (WCSP) version of the PCM1870. The jumper locations on Daughter Card #1 are slightly different on this version of the EVM because of WCSP pin assignments.

4.2 Motherboard

Table 4-1 through Table 4-4 list the connector references for the DEM-DAI1870 EVM motherboard.

Table 4-1. Main Power Supply and Regulator

Connectors	Main Power Supply and Regulator
CN101	+6 V to 10 V Main Power Supply
CN102	GND

Table 4-2. Power-Supply Terminals for PCM1870 Power-Supply Pins

Connectors	PCM1870 Power-Supply Pins
CN103, CN104	Not used. Do not care about short or open.
CN105	V_{CC}
CN106	V_{DD}
CN107	V_{IO}

Table 4-3. Audio I/O

Connectors	Audio I/O Pins
CN108	Analog audio input for PCM1870 AIN1L and AIN2L (Selected by JP18:1-2 for AIN1L, 2-3 for AIN2L on Daughter Card #1)
CN109	Analog audio input for PCM1870 AIN1R and AIN2R (Selected by JP21:1-2 for AIN1R, 2-3 for AIN2R on Daughter Card #1)
CN110	Analog audio output for PCM1774 HPOL/LOL
CN111	Analog audio output for PCM1774 HPOR/LOR
CN112	Analog audio output for PCM1870 AOL (Selected by JP17:1-2 for PGINL, 2-3 for AOL on Daughter Card #1)
CN113	Analog audio output for PCM1870 AOR (Selected by JP16:1-2 for PGINR, 2-3 for AOR on Daughter Card #1)
CN114	Analog audio input for PCM1870 PGINL
CN115	Analog audio input for PCM1870 PGINR
CN116	Not used
CN117	Not used
U301	TOSLINK™. S/PDIF Optical output
CN301	S/PDIF coaxial output
SW301	Toggle switch. Opt/Coax selector for S/PDIF output
U302	TOSLINK. S/PDIF Optical output
CN302	S/PDIF coaxial input
CN305	2x9 header pins to connect digital audio I/F for ADC/DAC. If using external signal source, all shorting plugs should be removed.
CN306	BNC connector to provide external clock for LC89052T (DIR: S/PDIF receiver) on Daughter Card or PCM1774 directly as E-SCK.
CN307	2x5 header pins. System clock and bit clock selection to provide DIT4096 (DIT: S/PDIF transmitter).*SCK* and *BCK* should be provided from LC89052T as initial setting.
CN308, CN309–CN316	2x9 header pins and SMA connectors (x8) for connecting digital audio I/F with external devices or equipment. If using this feature, all shorting plugs on CN305 should be removed.
CN317	3x10 header pins. Path of I^2C/SPI-interface selection (via USB or parallel port). Selected USB port for initial configuration. (Parallel port is not available.)
CN320	2x3 header pins. Word (L/R) clock selection (Master or Slave mode). Selected Slave mode as initial.

Table 4-4. I/F Controller (MSP430, TUSB3410)

Connectors	I/F Controller (MSP430, TUSB3410)
CN201	USB connector type-B
CN202	JTAG port
SW201	Push switch. RESET for MSP430/TUSB3410

4.3 Daughter Card #1 (PCM1870)

Table 4-5 lists the connector references for the first DEM-DAI1870 EVM daughter card.

Table 4-5. Analog Input and Output—Daughter Card #1

Connectors	Analog Input and Output of Daughter Card #1
J1	Stereo microphone input
J2	Monaural microphone input
J3	Headphone output
JP1-9	Not used
JP10	System clock select. 1-2: External clock; 3-4: SPDIF
JP11	Short jumper for C21 Capacitor between AOR to PGINR
JP12	Short jumper for C20 Capacitor between AOL to PGINL
JP13, 14	Not used
JP15	1-2: Digital loop back from PCM1870 DOUT to PCM1774 DIN; 2-3: DIN from CN302 or U301 to PCM1774
JP16	1-2: AOR to PGINR signal path; 2-3: AOR signal out to CN113
JP17	1-2: AOL to PGINL signal path; 2-3: AOL signal out to CN112
JP18	Analog input select L-channel. 1-2: AIN1L; 2-3: AIN2L
JP19	Analog input select R-channel. 1-2: AIN1R; 2-3: AIN2R
JP20	Analog input source select. 1-2: CN108; 2-3: JP22
JP21	Analog input source select. 1-2: CN109; 2-3: JP23
JP22	1-2: Stereo mic (J1) L-channel; 2-3: Mono mic (J2) L-channel
JP23	1-2: Stereo mic (J1) R-channel; 2-3: Mono mic (J2) R-channel
JP24	PCM1870 TEST pin control jumper. 1-2: External control; 2-3: GND short
JP25	PCM1774 $\overline{MS}$ /ADRcontrol. 1-2: connected to motherboard; 2-3: JP26
JP26	1-2: shorted to GND; 2-3: connected to V_{DD}.
JP27	PCM1870 $\overline{MS}$/ADR control. 1-2: connected to motherboard; 2-3: JP28
JP28	1-2: shorted to GND; 2-3: connected to V_{DD}.
JP29	Not used

Simplified descriptions of the analog input and output configuration for Daughter Card #1 are shown in Figure 4-2. Figure 4-3 illustrates the $\overline{MS}$/ADR control configuration for I^2C communication for Daughter Card #1.

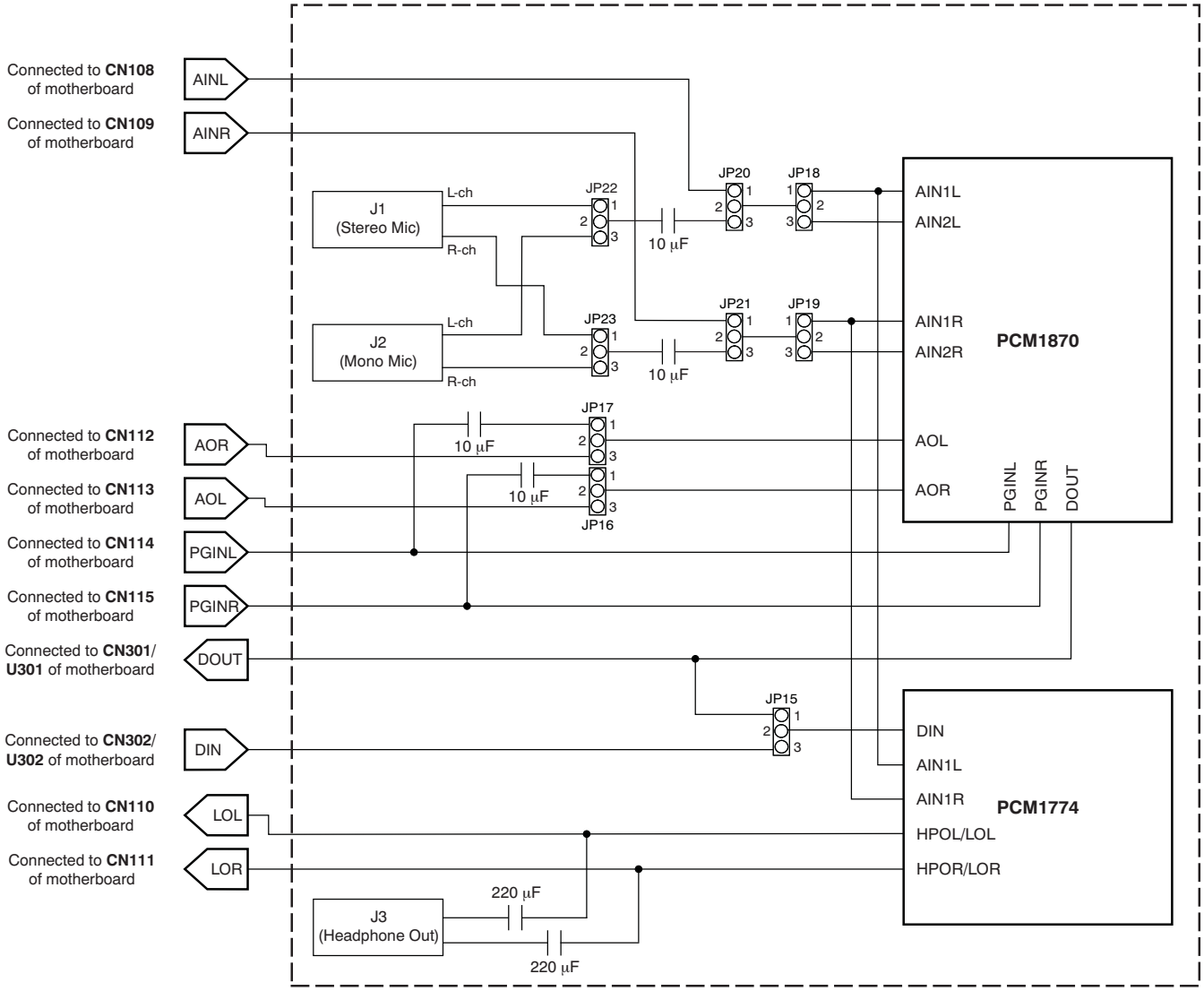


Figure 4-2. Analog Input/Output Configuration (Daughter Card #1)

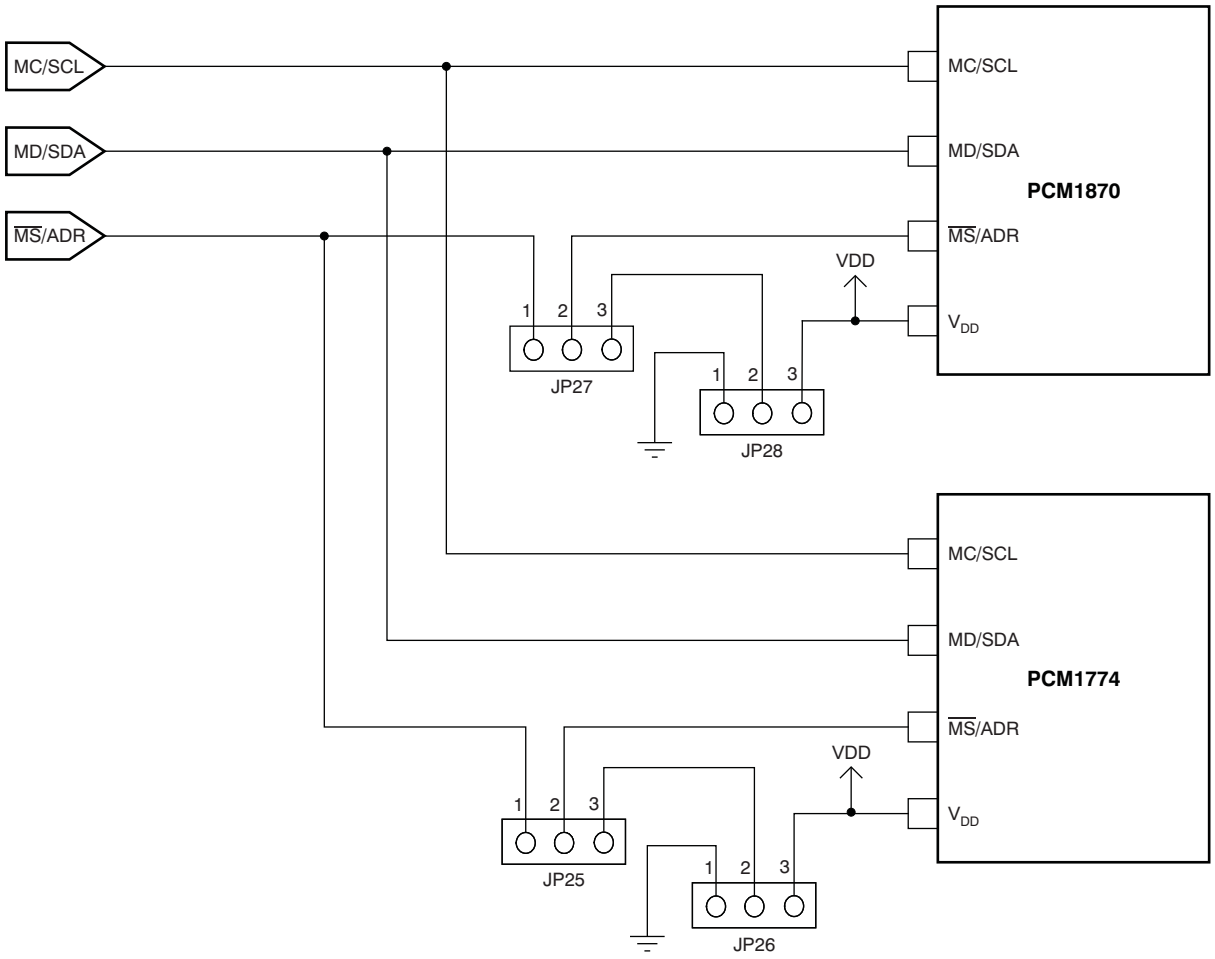


Figure 4-3. $\overline{MS}$/ADR Control Configuration for I^2C Communication (Daughter Card #1)

4.4 Daughter Card #2 (DIR: LC89052T and DIT: DIT4096)

Table 4-6 lists the connector references for the second DEM-DAI1870 EVM daughter card.

Table 4-6. Analog Input and Output—Daughter Card #2

Connectors	Analog Input and Output of Daughter Card #2
SW001	Toggle switch. Opt/Coax selector for S/PDIF input
SW002	Toggle switch. Reset/Power-down LC89052T and DIT4096
SW003	Clock source selection for LC89052T (Onboard crystal oscillator or external source from CN306 of motherboard)
SW004	DIP switch. Sets channel-status data of the DIT4096(1). Note that the OFF state of this switch sets a HIGH level. Channel-status data can be set up if needed. It is also possible to connect a microcontroller.
SW005	DIP switch. Sets the DIT4096 system clock and data format. Note that the OFF state of this switch sets a HIGH level.

(1) See the DIT4096 product data sheet (TI literature number SBOS225, available for download from the TI web site) for further information.

Table 4-7 describes the audio clock and data control format options for Daughter Card #2.

Table 4-7. Audio Clock and Input Data Control Format—Daughter Card #2

CLK0	CLK1	System Clock
L	L	Not used
L	H	$256f_S$ (initial setting)
H	L	$384f_S$
H	H	$512f_S$
FMT0	**FMT1**	**Input Data Format**
L	L	24-bit, left-justified, MSB-first
L	H	24-bit, I^2S (initial setting)
H	L	24-bit, right-justified, MSB-first
H	H	16-bit, right-justified, MSB-first

Evaluation and Measurements

This chapter discusses how to set up jumpers on the DEM-DAI1870 EVM motherboard for performance evaluation using the Audio Precision SYS-2722® or PSIA-2722® audio analyzers. (The PSIA-2722 is the programmable serial interface adapter that connects the Audio Precision 2700 series and enables connections directly to the ADC and DAC devices.) The process of measuring dynamic characteristics is then presented, along with example characteristic data.

Topic **Page**

5.1 Slave Mode With Audio Precision SYS-2722 (Default Setting)

These jumper configurations for the DEM-DAI1870 EVM motherboard are the default device settings. Simple evaluation using the Audio Precision SYS-2722 (as shown in Figure 5-1) is easily accomplished. First of all, the connect S/PDIF input and output to either optical U302 (or coaxial CN302) and U301 (or CN301). Then, select either SW301 or SW001, respectively.

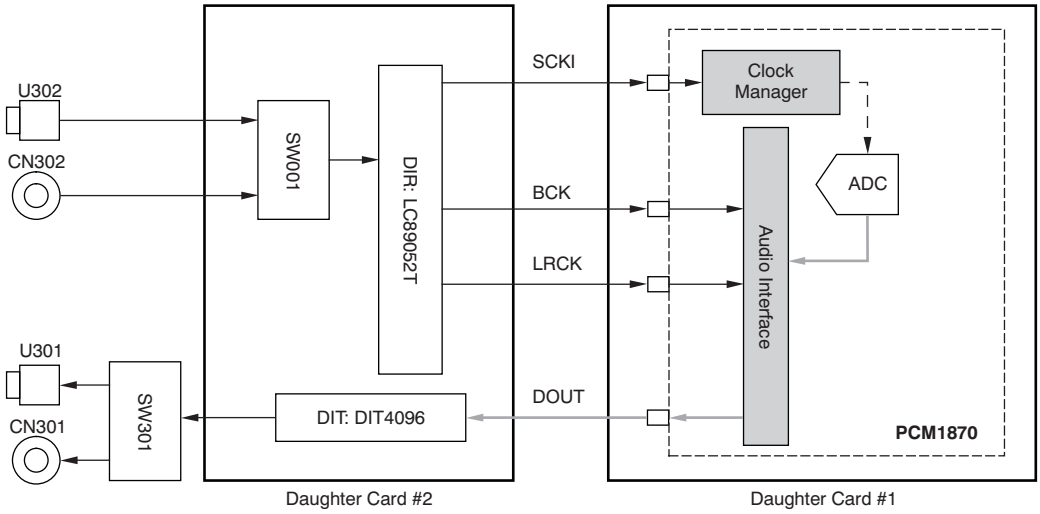


Figure 5-1. Slave Mode Configuration With SYS-2722

To put the DEM-DAI1870 EVM motherboard into the default slave mode configuration, refer to the jumper combination shown in Figure 5-2.

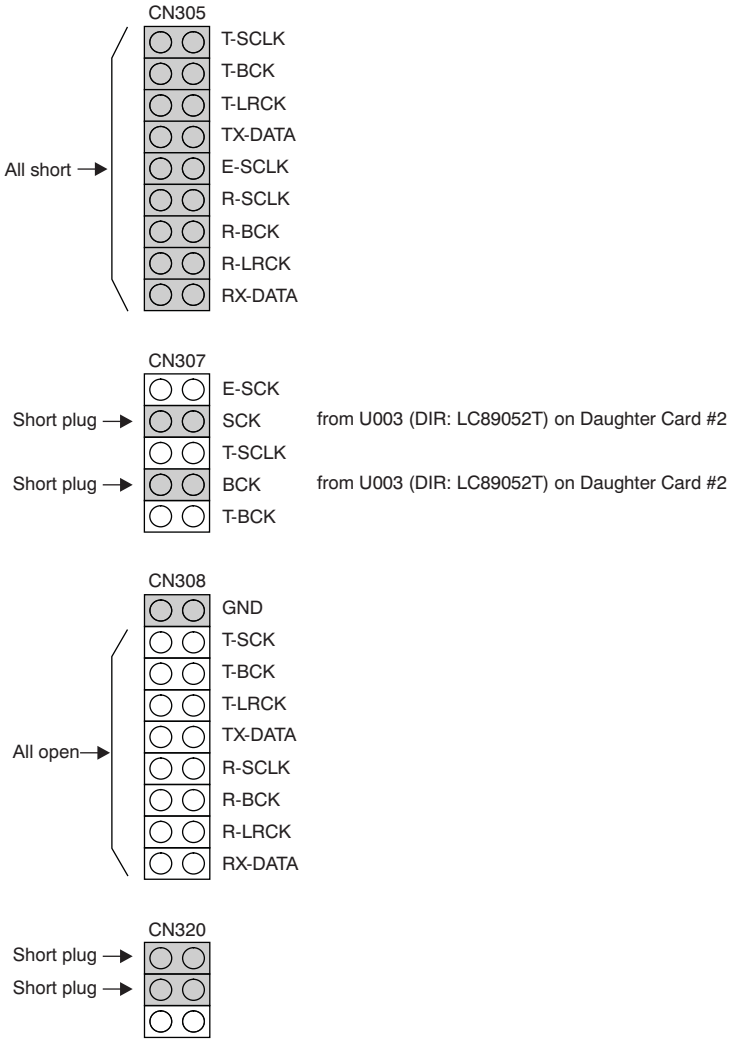


Figure 5-2. Jumper Configuration for Slave Mode (Default)

5.2 Master Mode with Audio Precision SYS-2722

To enable the DEM-DAI1870 EVM motherboard for use in Master mode, the path of the S/PDIF input to the PCM1870 through DIR is not available for use. LRCK and BCK change the respective output states at the PCM1870 side in master mode; the respective jumpers of R-BCK, R-LRCK, and RX-DATA should be removed from CN305 to avoid conflict between the input and output of these clocks.

Furthermore, in this situation, DIN to the PCM1870 is also invalid because the DIR LC89052T does not receive clocks (the LC89052T cannot work in slave mode). Therefore, any analog output from the DAC is invalid because there is no data input.

However, in this configuration, users ***can*** confirm master mode operation of both LRCK and BCK from the PCM1870 with a digital oscilloscope. Users can easily identify master mode without the use of other external equipment such as the PSIA-2722 analyzer.

The PCM1870 has no integrated internal PLL. However, the clock manager function can provide LRCK (f_S) and BCK in master mode, as described in Figure 5-3.

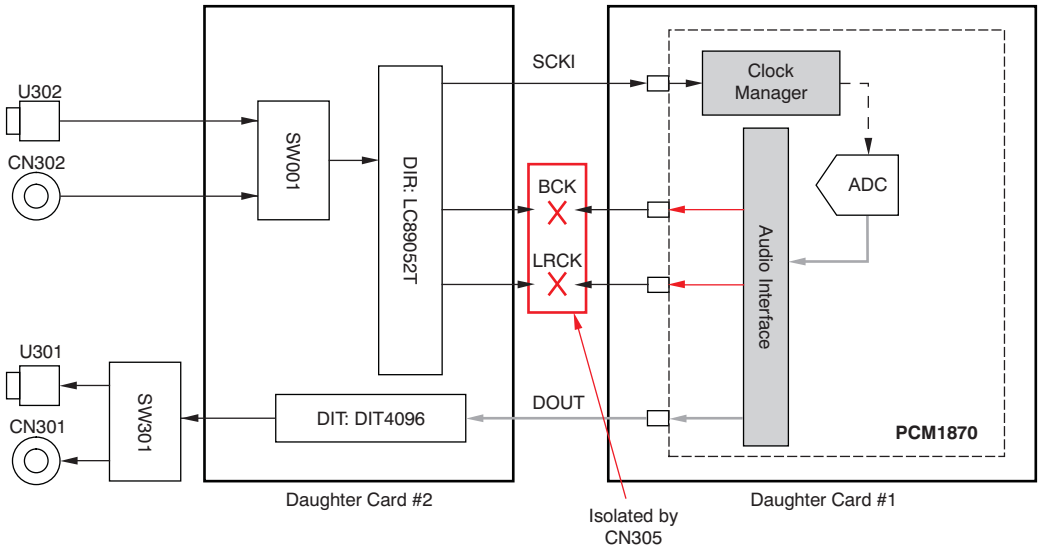


Figure 5-3. Master Mode Configuration With SYS-2722

Refer to the jumper combination shown in Figure 5-4 to put the DEM-DAI1870 EVM motherboard into master mode configuration.

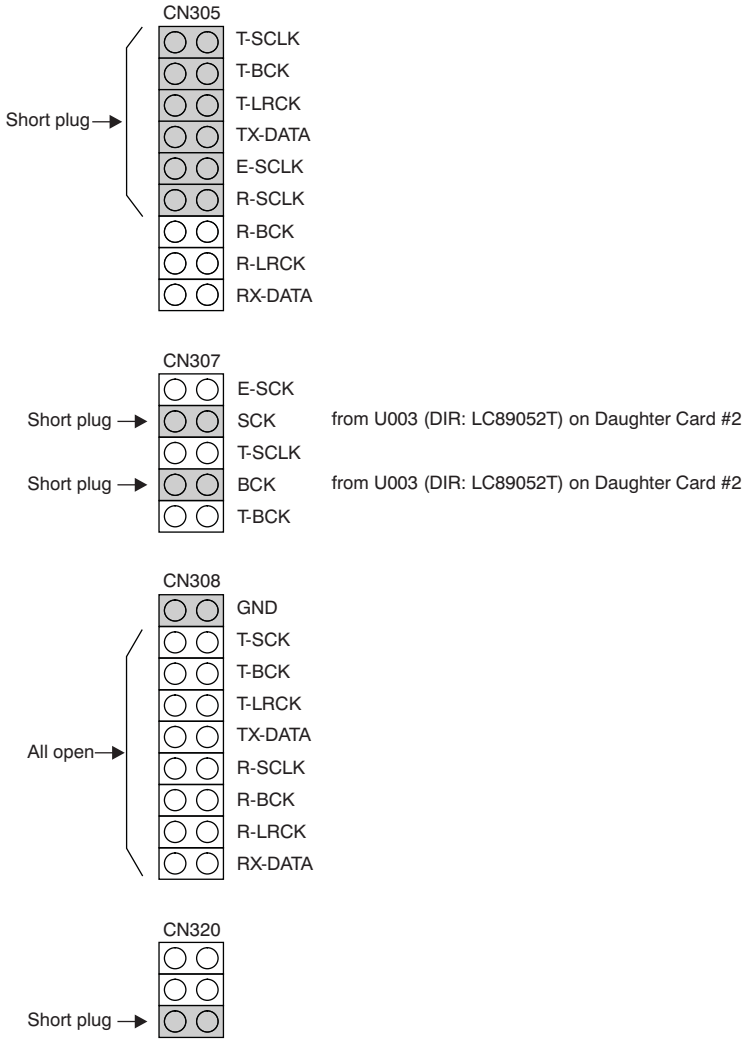


Figure 5-4. Jumper Configuration for Master Mode

5.3 Combined Master and Slave Modes With PSIA-2722

As shown in Figure 5-5, the DEM-DAI1870 EVM can provide evaluation for both slave and master modes of the PCM1870 at the same time without setup jumpers on the motherboard if the user has access to the PSIA-2722 analyzer.

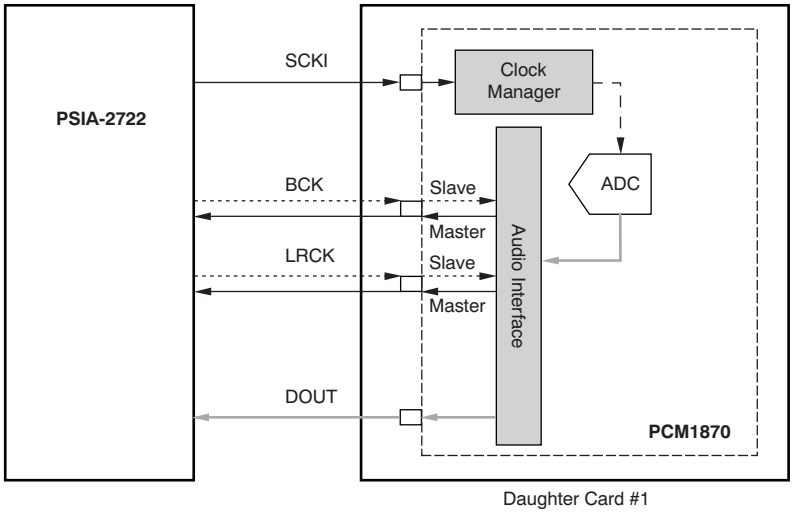


Figure 5-5. Combined Master and Slave Mode Configuration with SYS-2722

Refer to the jumper combination shown in Figure 5-6 to set up the combined master and slave modes configuration.

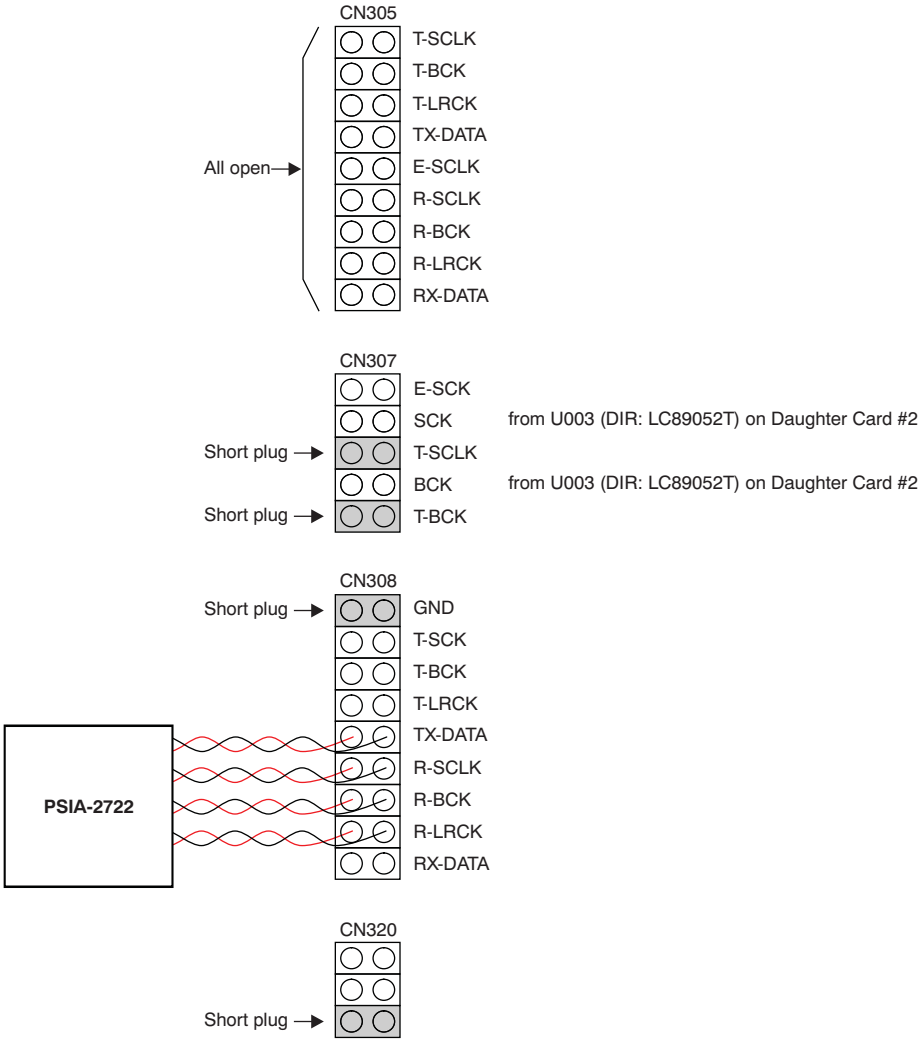


Figure 5-6. Jumper Configuration for Combined Master and Slave Modes

5.4 Measurements for Dynamic Characteristics

Typical dynamic performance graphs for analog-to-digital converters (ADCs) generally represent four performance characteristics (in addition to other specifications): total harmonic distortion and noise (THD+N); signal-to-noise ratio (SNR); dynamic range (DR); and channel separation. These graphs also specify the test environment and measurement conditions required in order to meet typical performance values defined in the product data sheet.

For the DEM-DAI1870 EVM, the evaluation environment specifications are:

- Equipment used: Audio Precision, System Two Cascade
- Audio Data format: 16-bit Left-Justified
- SCKI / BCK / LRCK (f_S): $256f_S$ / $64f_S$ / 48 kHz
- Power supply: $V_{DD} = V_{IO} = V_{CC} = 3.3$ V (Regulated down from 10 V applied to the motherboard)
- Temperature: Room/ambient

Once the lab or test environment is configured according to these parameters, start the EVM software (as discussed in Section 3.2). Click *All Power On* in the startup window or execute *power_on.csv*, and then execute the .csv file that corresponds to the appropriate measurement path discussed in the subsequent sections of this chapter.

The PCM1870 (U1) is soldered onto Daughter Card #1, DEM-PCM1870RHF/1774RGP-A. .CSV files bundled with the EVM kit are available to measure dynamic performance. These .CSV files will help users determine the appropriate register settings for the PCM1870 under various conditions. The Appendix A of this user guide also includes a block diagram that corresponds to each respective .CSV file.

5.4.1 Analog-to-Digital (A/D) Performance

Measurement path: 01.Line Input (AIN2L/AIN2R)
.csv file: 01_ADC_Line_Input.csv

Table 5-1. A/D Line Input Parameters

Power Supply	Parameter	Filter Setting	Left Channel	Right Channel
3.3V	THD+N (–1 dB at 1 kHz)	400 Hz—20 kHz AES-17	0.009%	0.009%
	SNR (BPZ input)	22 Hz—20 kHz SPCL + A-weighting	90.1 dB	89.8 dB
	DR (–60 dBFS input)	22 Hz—20 kHz AES-17 + A-weighting	90.3 dB	90.1 dB
	Channel Separation (BPZ input for target channel)	22 Hz—20 kHz AES-17	87.6 dB	87.5 dB

To obtain the performance results shown in Table 5-1, the functions should be set with these parameters:

- ALC: Off
- Mic boost: 0 dB
- All PGA: 0 dB

The bundled .csv file automatically sets the device to these conditions.

See Appendix A for a signal flow block diagram.

5.4.2 Amplitude Versus Frequency Performance

Measurement path: 01.Line Input (AIN2L/AIN2R)

.csv file: 01_ADC_Line_Input.csv

Note that an unweighted filter and an AES-17 bandwidth of 22 Hz to 20 kHz should be set to obtain precise spectrum results.

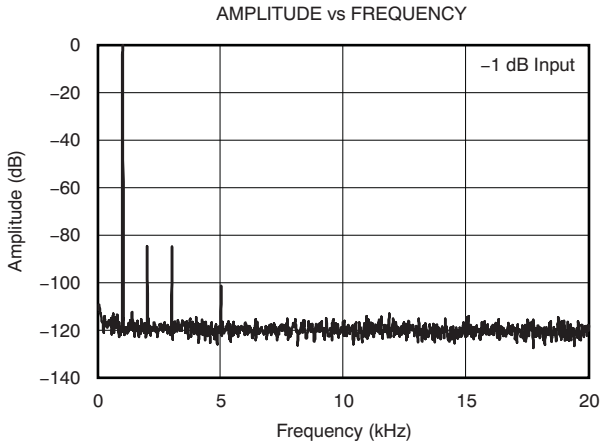


Figure 5-7. ADC Amplitude vs Frequency Result: –1dB Input

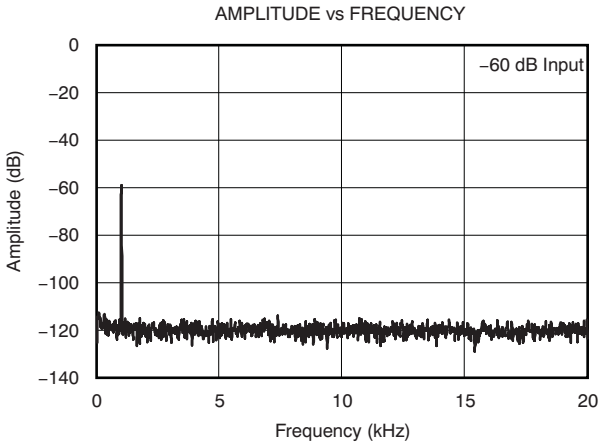


Figure 5-8. ADC Amplitude vs Frequency Result: –60dB Input

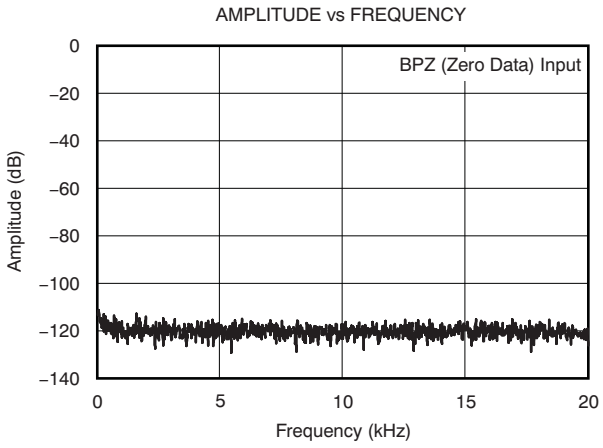


Figure 5-9. ADC Amplitude vs Frequency Result: BPZ (Zero Data) Input

See Appendix A for a signal flow block diagram.

5.5 Connection Diagram for Practical Applications

The PCM1870 Daughter Card has been configured to measure dynamic audio performance by common audio analyzer equipment.

In a practical application (such as portable audio player or cellular phone), simple components set up as shown in Figure 5-10 will be reasonable to save assembly and test spaces. Specific component values are listed in Table 5-2.

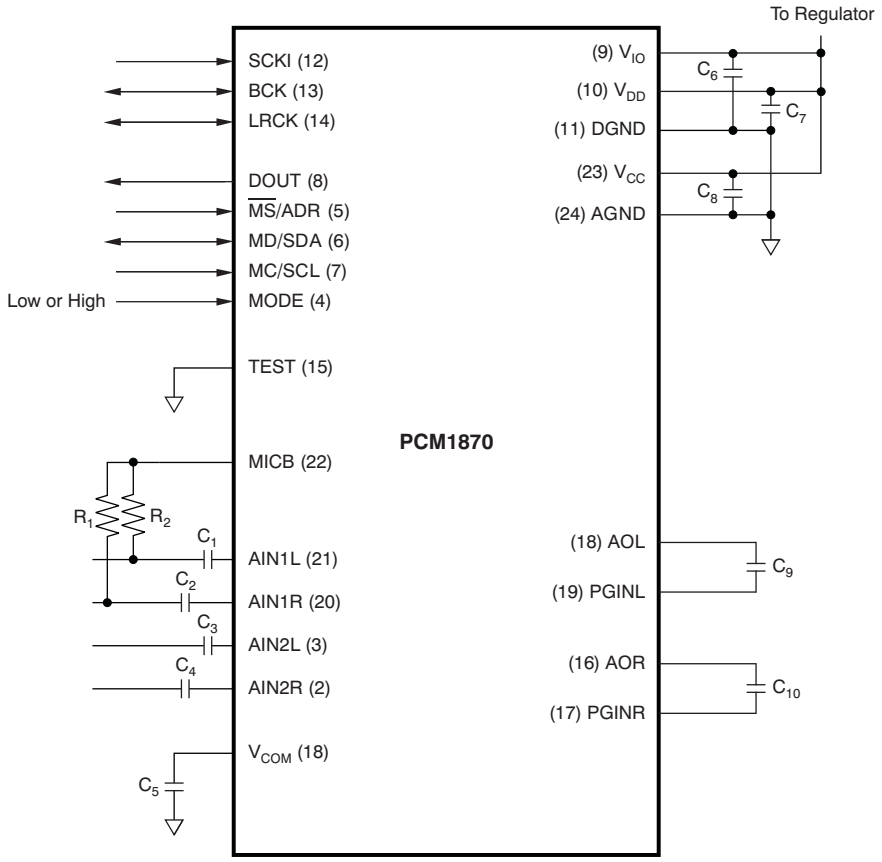


Figure 5-10. Basic Connection Diagram

Table 5-2. Recommended External Parts for Basic Connection Diagram

Component	Recommended Value	Component	Recommended Value
C_1—C_4	1 µF to 10 µF	C_8	1 µF to 4.7 µF
C_5	1 µF to 4.7 µF	R_1, R_2	2.2 kΩ
C_6	0.1 µF	C_9, C_{10}	1 µF to 10 µF
C_7	1 µF		

Schematic, PCB Layout, and Bill of Materials

This chapter provides the electrical and physical layout information for the DEM-DAI1870 EVM. The bill of materials is included for component and manufacturer reference.

Topic **Page**

6.1 Schematics

Figure 6-1 and Figure 6-2 illustrate the schematics for the DEM-DAI1870 EVM.

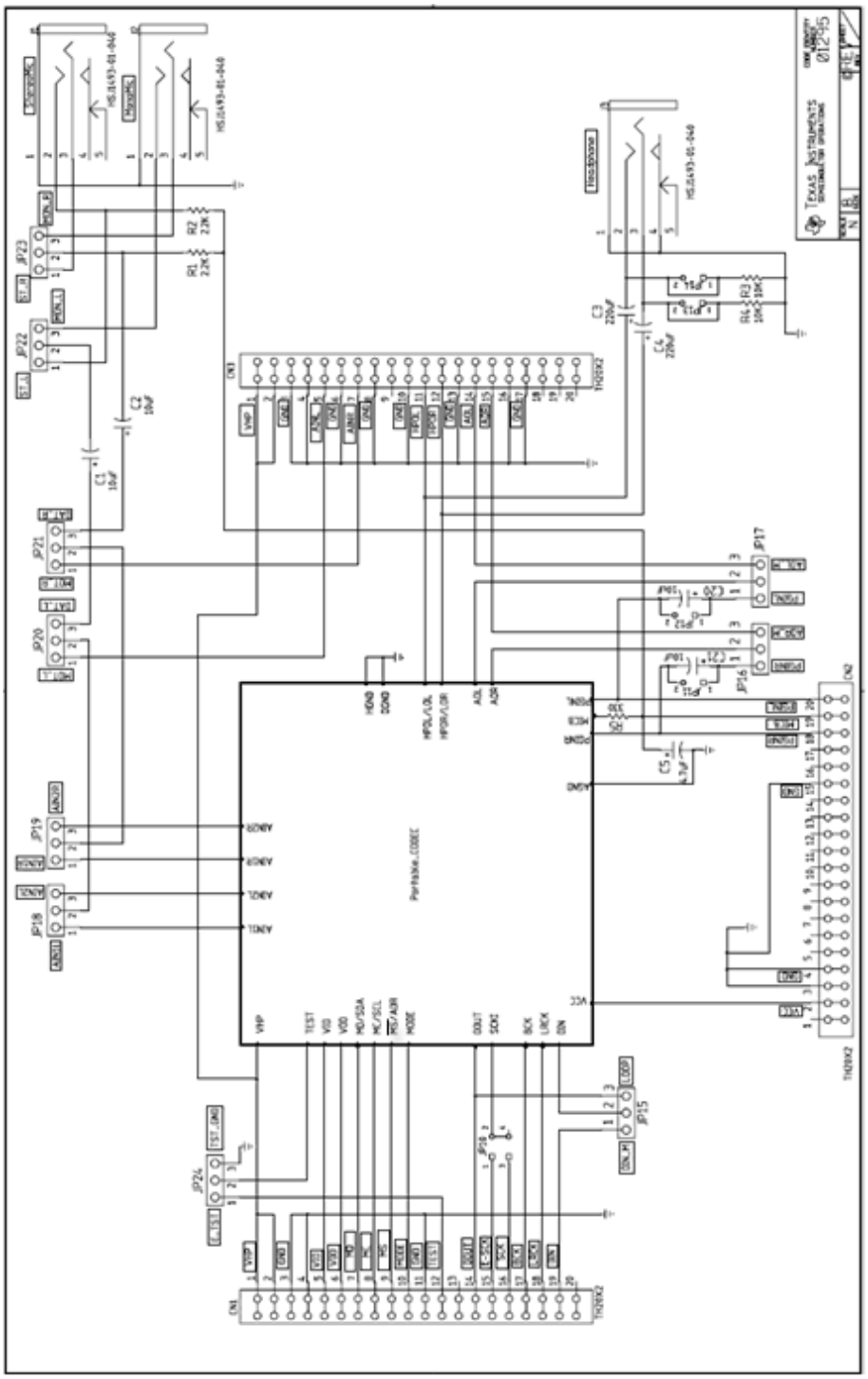


Figure 6-1. DEM-PCM1870RHF/1774RGP-A Part 1 (Daughter Card #1)

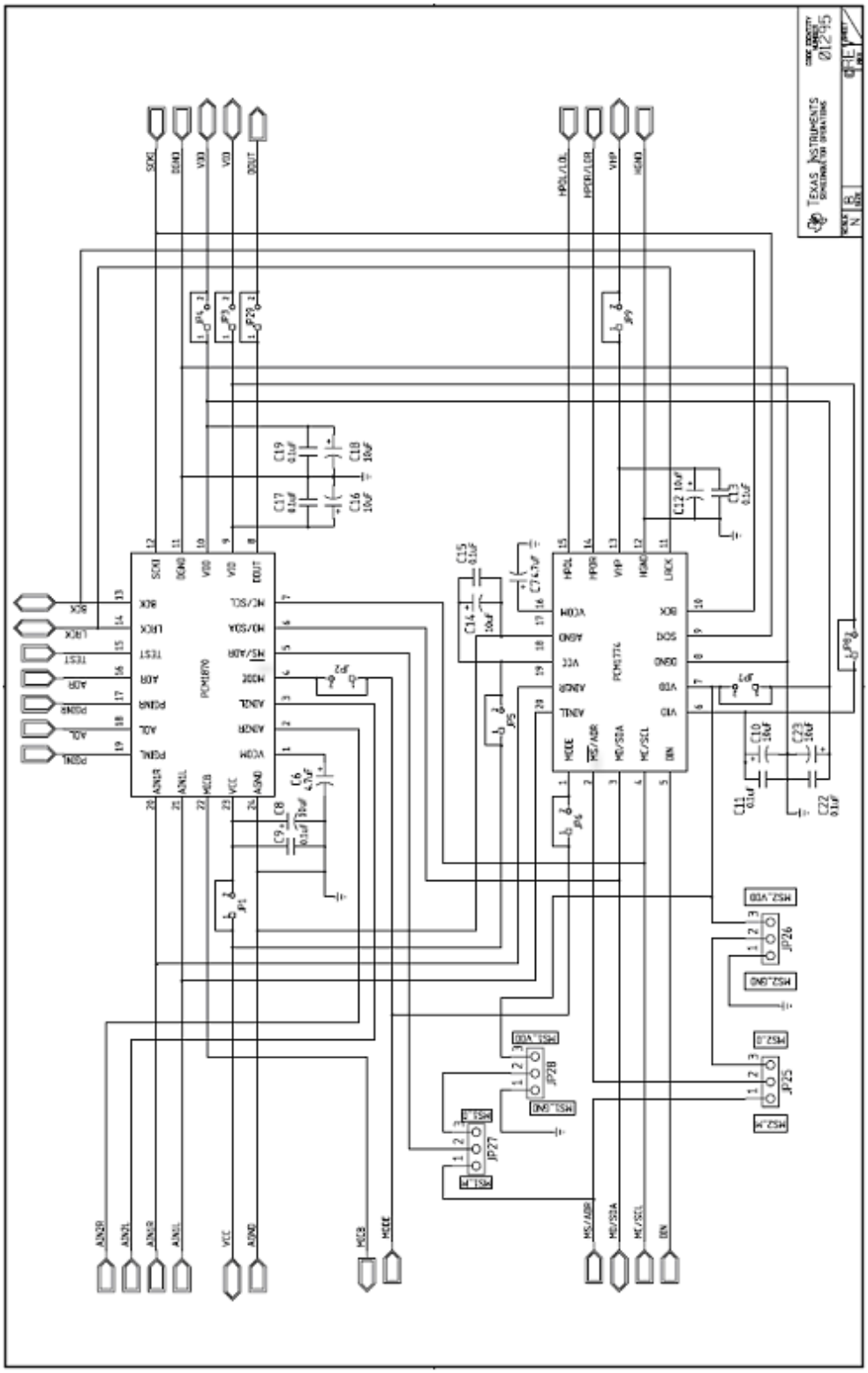


Figure 6-2. DEM-PCM1870RHF/1774RGP-A Part 2 (Daughter Card #1)

6.2 Printed Circuit Board Layout

Figure 6-3 through Figure 6-7 illustrate the printed circuit board (PCB) layout for the DEM-DAI1870 EVM.

Note: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing DEM-DAI1870 EVM PCBs.

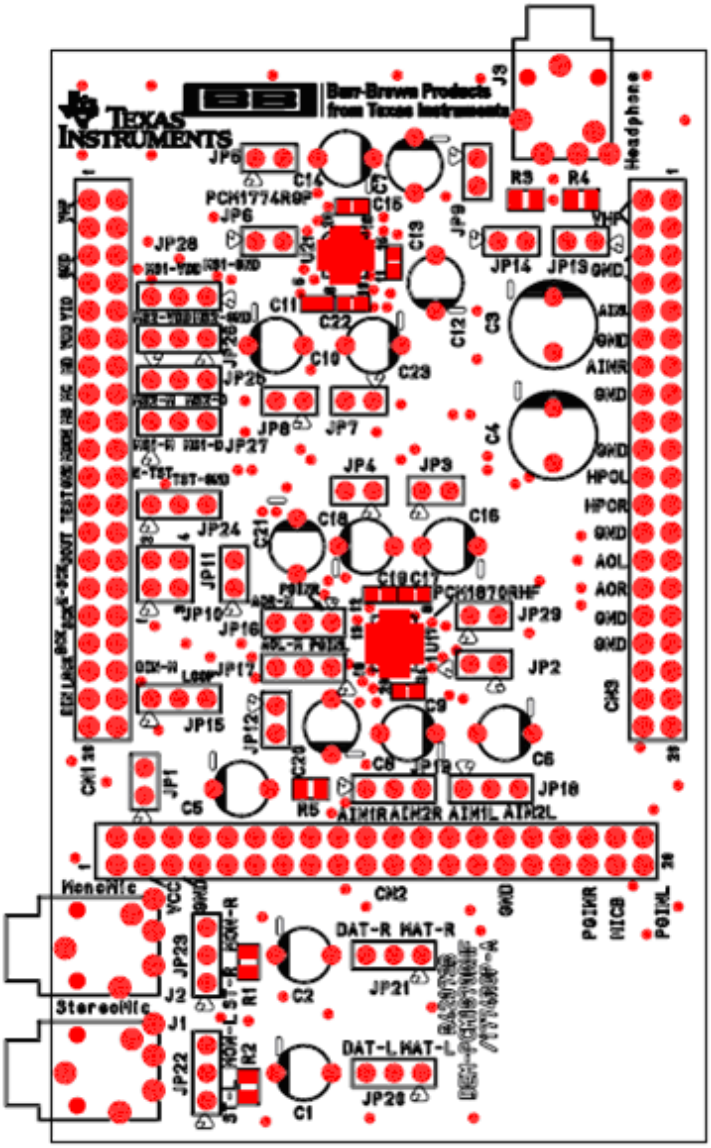


Figure 6-3. DEM-PCM1870RHF/1774RGP-A Board Layout—Silkscreen Side

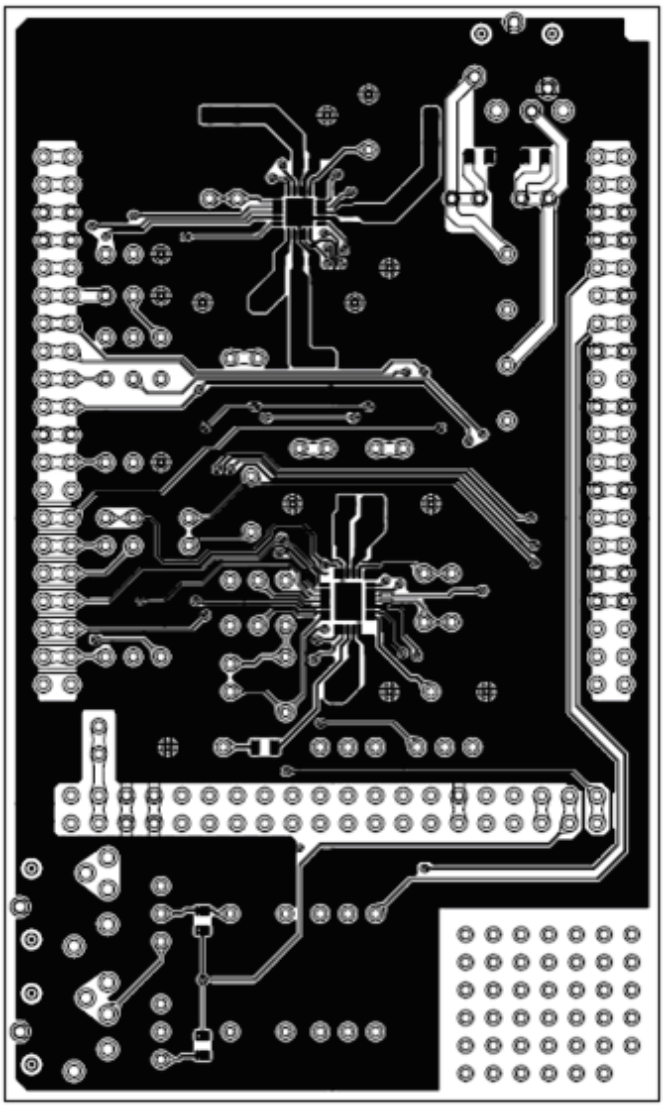


Figure 6-4. DEM-PCM1870RHF/1774RGP-A Board Layout—Component Side

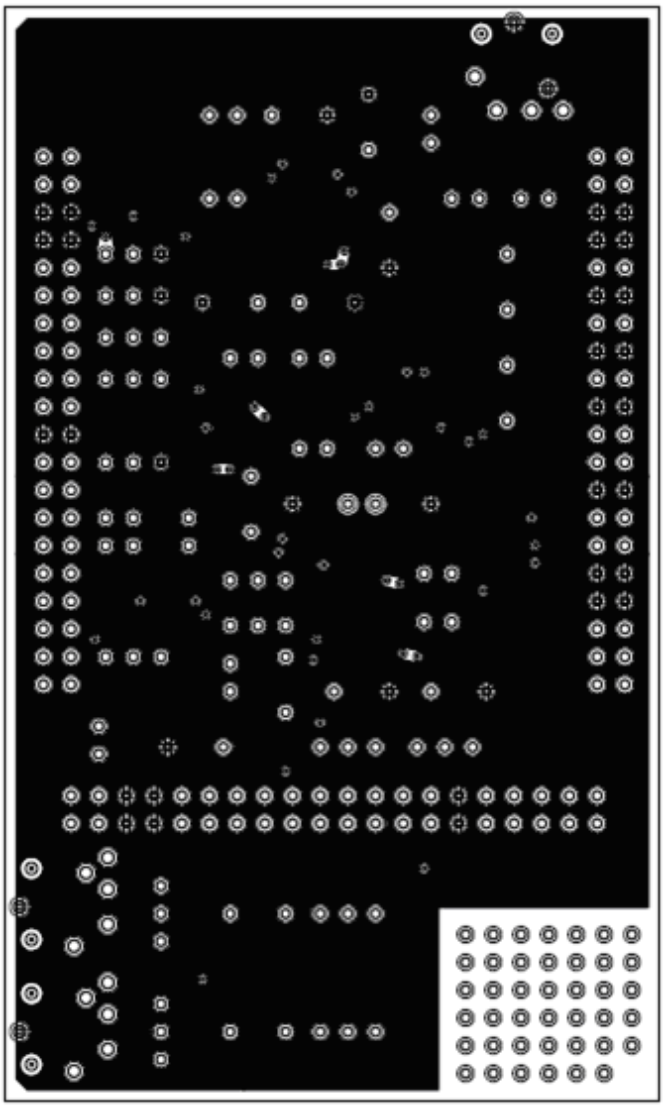


Figure 6-5. DEM-PCM1870RHF/1774RGP-A Board Layout—Inner Layer 2

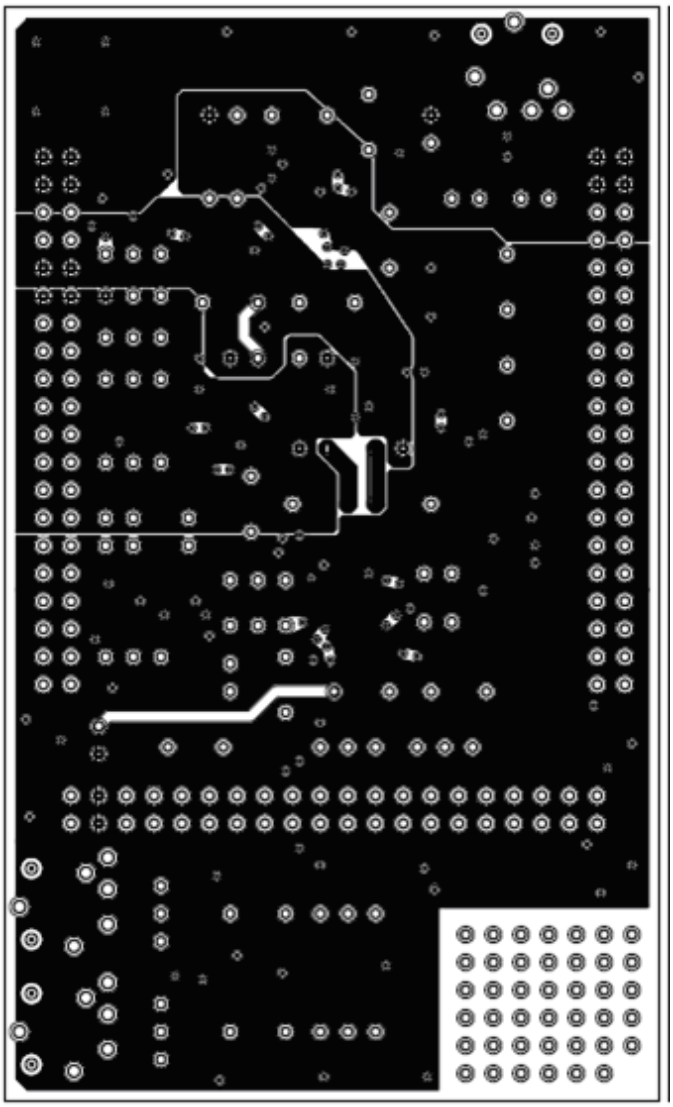


Figure 6-6. DEM-PCM1870RHF/1774RGP-A Board Layout—Inner Layer 3

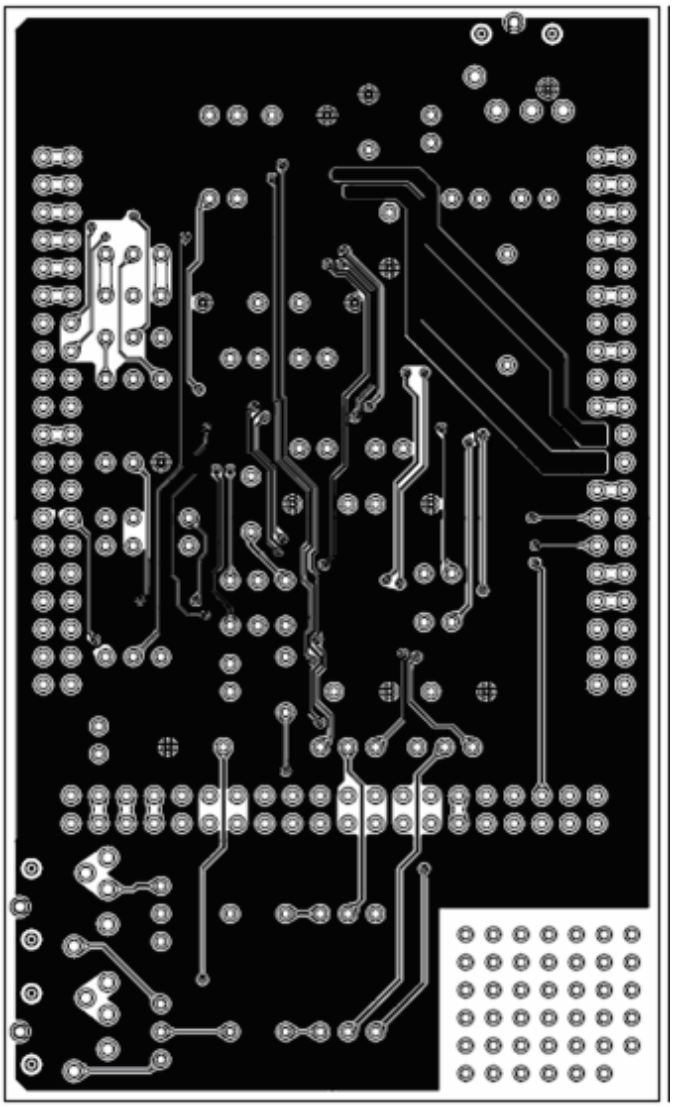


Figure 6-7. DEM-PCM1870RHF/1774RGP-A Board Layout—Solder Side

6.3 Component List

Table 6-1 lists the Bill of Materials for the DEM-DAI1870 EVM.

Table 6-1. Bill of Materials

Reference Designator	Quantity	Description
R1, R2	2	2.2 kΩ, Rohm, MCR10EZHJ222
R5	1	330 Ω, Rohm, MCR10EZHJ331
C9, C17, C19	4	0.1 µF, Murata, GRM188R71H104Z
C1, C2, C8, C16, C18, C20, C21	4	10 µF, Nippon Chemi-con, EKMG160ELL100ME11D
C5, C6	1	4.7 µF, Nippon Chemi-con, EKMG500ELL4R7ME11D
JP10	1	OMRON, 2×2 Pin, XJ8C-0411
JP11, JP12	2	OMRON, 2-Pin, XJ8B-0211
JP15, JP16, JP17, JP18, JP19, JP20, JP21, JP22, JP23, JP24, JP27, JP28	12	OMRON, 3-Pin, XJ8B-0311
J1, J2	2	HOSIDEN, HSJ1493-01-040
U1	1	16-bit Stereo Audio ADC, 4×5 mm QFN 24-pin, Texas Instruments, PCM1870

Reference .csv Files, Interfacing to DSPs, and Package Information

Topic **Page**

A.1 Reference .csv Files

The .csv files are bundled with the DEM-DAI1870 EVM Controller. These files enable users to execute register settings corresponding to the specific operating modes discussed in the product data sheet by importing them into the software.

Note that each .csv file (listed in Table A-1) must be implemented ***after*** an *All Active* operation is performed with the *power_on.csv* command; otherwise, these files will not work properly.

An *All Active* operation is recommended to start up the device, and can be executed by just clicking the *All Power On* button, as discussed in Section 3.2.

Table A-1. .CSV Files

Operating Mode		.CSV File Name
All Power Down		power_off.csv
All Active		power_on.csv
Recording		
01	Line Input (AIN2L/AIN2R)	01_ADC_Line_Input.csv
02	Mic Input (AIN1L/AIN1R, +20 dB)	02_ADC_Mic_Input.csv
03	Mic Input (AIN1L/AIN1R, +20 dB) with ALC	03_ADC_Mic_Input_with_ALC.csv
04	Mono Mic Input (AIN1L, +20 dB)	04_ADC_Mono_Mic_Input.csv
05	Mono Mic Input (AIN1L, +20 dB) with ALC	05_ADC_Mono_Mic_Input_with_ALC.csv
06	Mono Diff Mic Input (AIN1L/AIN1R, +20 dB)	06_ADC_Mono_Diff_Mic_Input.csv
07	Mono Diff Mic Input (AIN1L/AIN1R, +20 dB) with ALC	07_ADC_Mono_Diff_Mic_Input_with_ALC.csv

A Related Signal Flow Diagrams

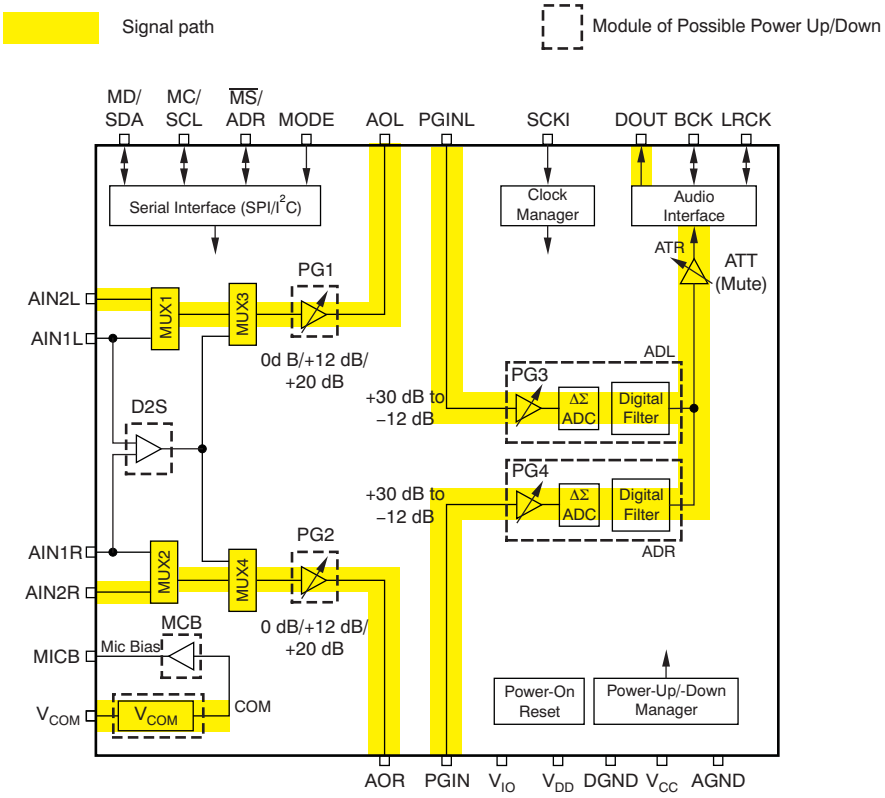


Figure A-1. Line Input (AIN2L/AIN2R)

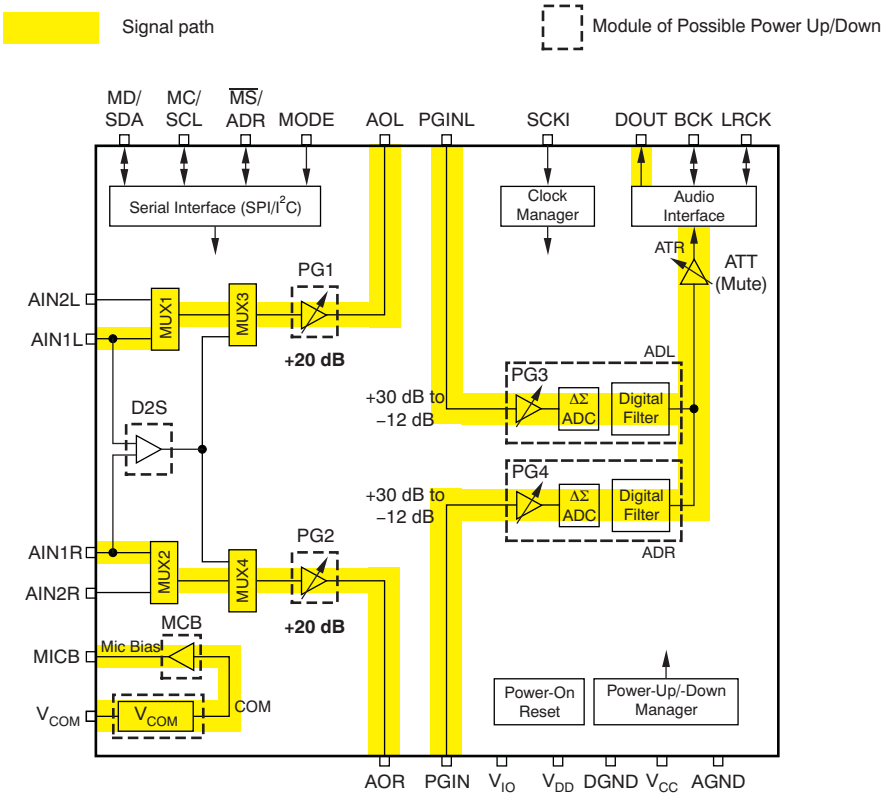


Figure A-2. Microphone Input (AIN1L/AIN1R, +20 dB)

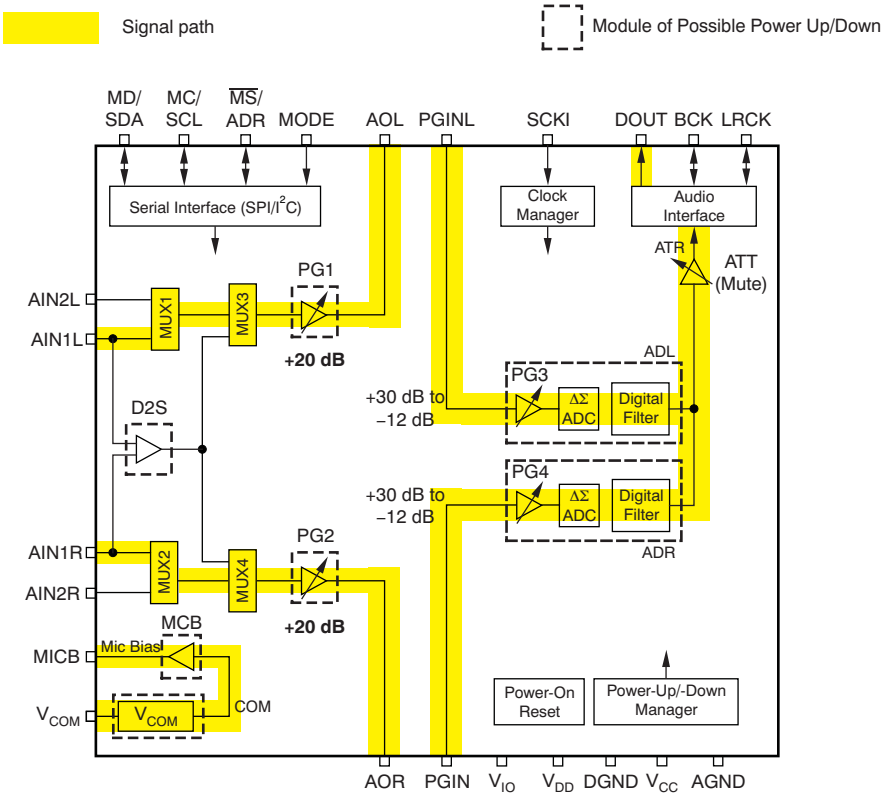


Figure A-3. Microphone Input (AIN1L/AIN1R, +20 dB) with ALC

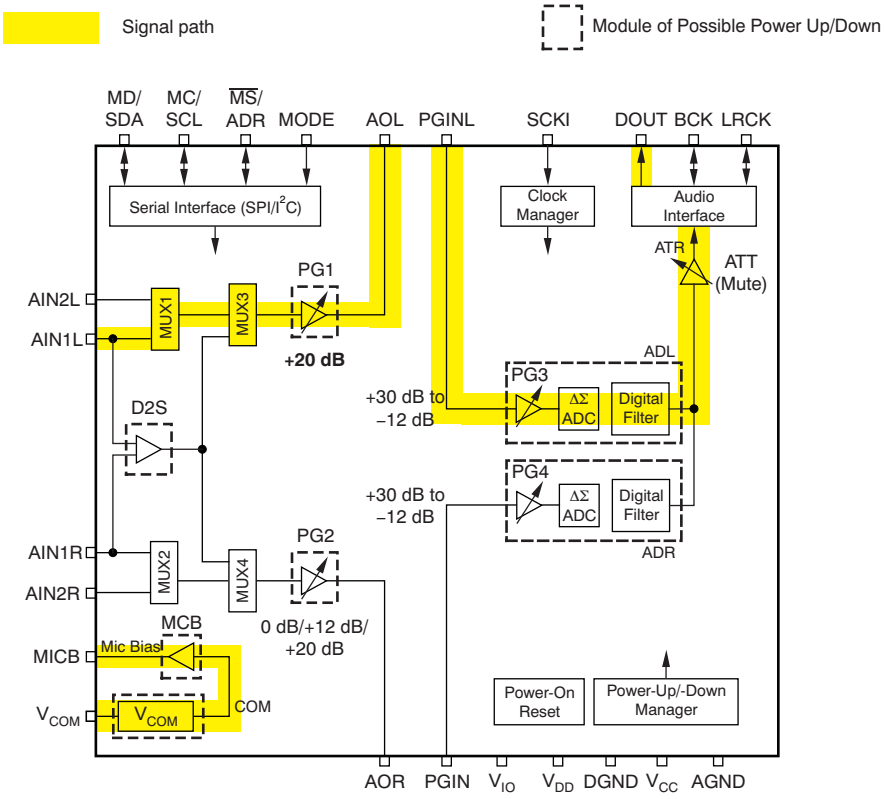


Figure A-4. Mono Microphone Input (AIN1L, +20 dB)

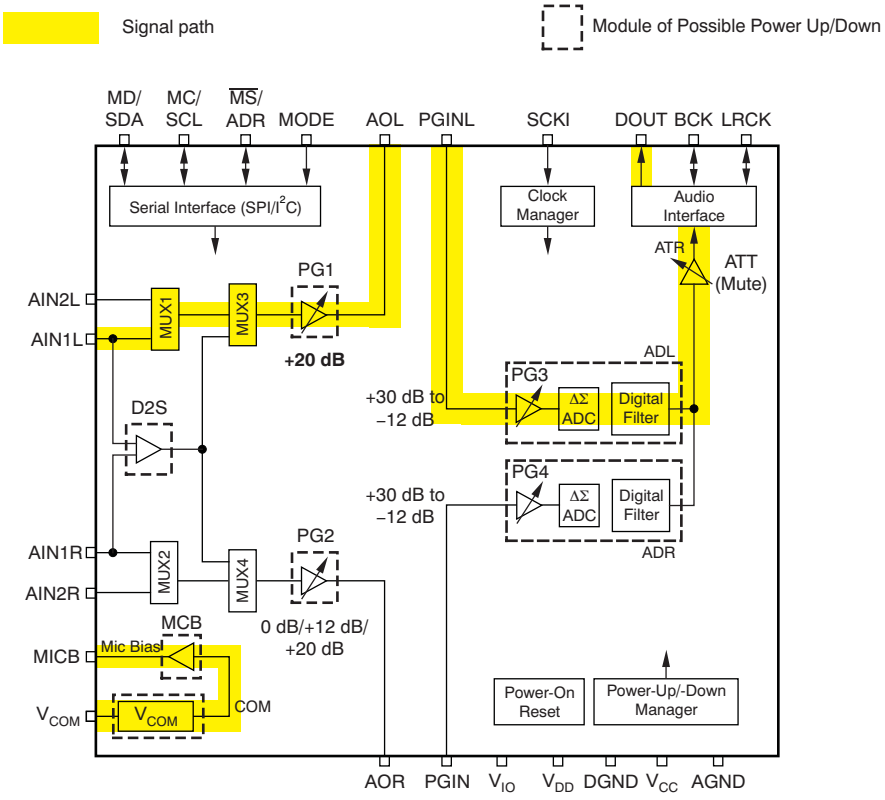


Figure A-5. Mono Microphone Input (AIN1L, +20 dB) with ALC

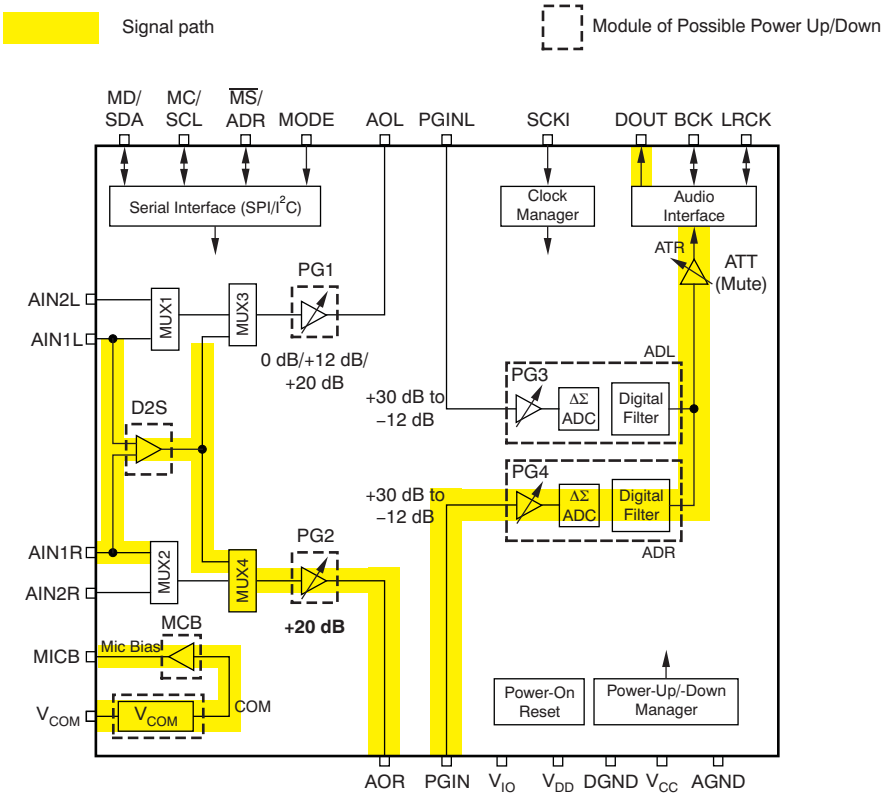


Figure A-6. Mono Differential Microphone Input (AIN1L/AIN1R, +20 dB)

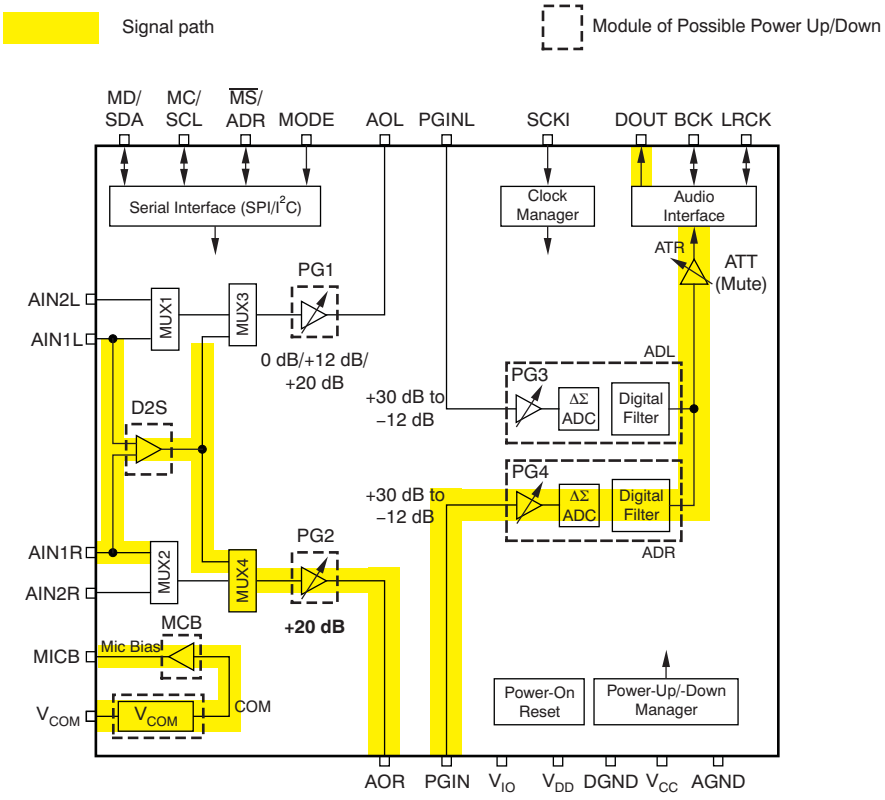


Figure A-7. Mono Differential Microphone Input (AIN1L/AIN1R, +20 dB) with ALC

A.2 Interfacing to DSPs

Refer to the following examples for interfacing the PCM1870 to a digital signal processor (DSP) in either slave or master mode. To implement master mode, MSTR = 1 of register 84 (54h) enables master mode operation as discussed in the product data sheet. Insert 5440h to the recommended power-on sequence after ADC power-up (52h) of the PCM1870, as noted in Table A-2.

These conditions apply for both modes of operation as illsutrated in Figure A-8 and Figure A-9:

- SCKI: Audio Clock ($256f_S/384f_S$)
- BCK:Clock for Audio Transfer ($32f_S/48f_S/64f_S$ in I^2S, LJ, and RJ; $32f_S/48f_S/64f_S/128f_S/256f_S$ in DSP)
- LRCK: Sampling Rate Clock (f_S)
- DIN: Audio Data Input for DAC (I^2S, LJ, RJ, DSP)
- DOUT: Audio Data Output from ADC (I^2S, LJ, RJ, DSP)

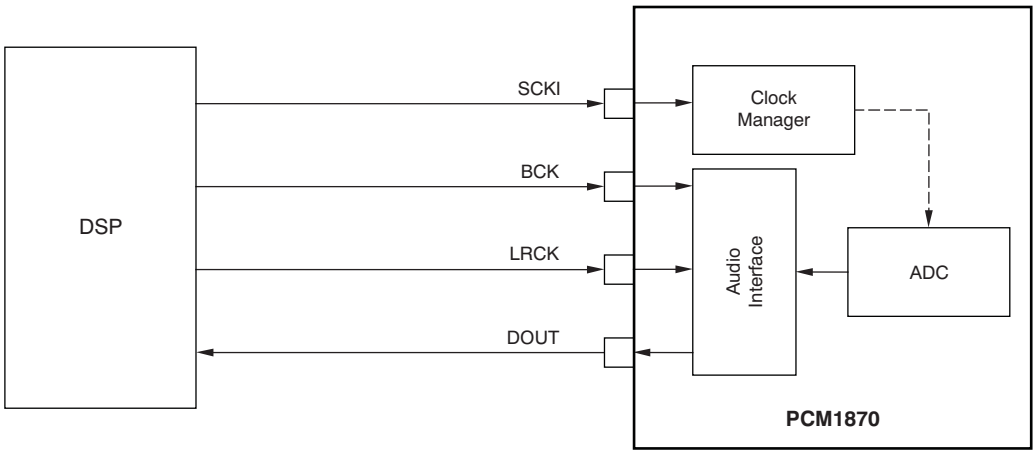


Figure A-8. Slave Mode Operation

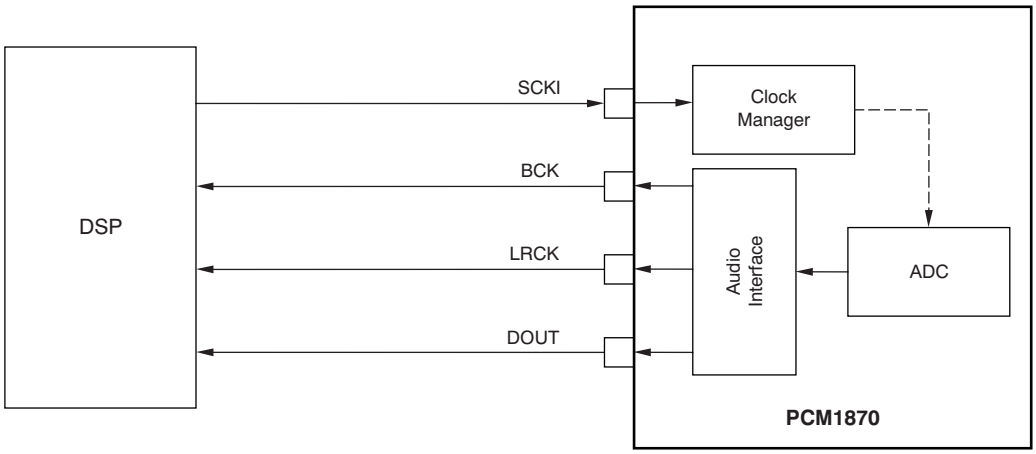


Figure A-9. Master Mode Operation

A.2.1 Register Control with DSP Interface

Table A-2 summarizes the recommended power-on sequence for the PCM1870. The shaded cells within the table indicate specific register settings that must be configured for the device to properly operate with a DSP interface.

Table A-2. Recommended Power-On Sequence for PCM1870

Step	Register Settings	Notes
1	–	Turn on all power supplies.(1)
2(2)	5102h	ADC audio interface format (left-justified)(3)
3	5A00h	PG1, PG2 gain control (0 dB)
4	4980h	Analog bias power up
5	5601h	Zero-cross detection enable
6	4A01h	V_{COM} power up
7(4)	523Fh	Analog front end (ADL, ADR, D2S, MCB, PG1, 2, 5, 6) power up
8(4)	5711h	Analog input (MUX3, MUX4) select. Analog input (MUX1, MUX2) select
9	4F0Ch	Analog input L-channel (PG3) volume (0 dB)(5)
10	500Ch	Analog input R-channel (PG4) volume (0 dB)(5)

(1) V_{DD} should be turn on prior to or simultaneously with the other power supplies. It is recommended to set register data with the system clock input after turning all power supplies on.
(2) I^2S: 4620h; Left-Justified: 4601h; Right-Justified: 4602h; DSP: 4603h.
(3) Audio interface format should be set to match the DSP or decoder being used.
(4) Between steps 7 and 8, add this value for slave configuration: 5400h. For master configuration, add: 5440h.
(5) Any level is acceptable for volume or attenuation. Level should be resumed by register data recorded when system power off.

A.2.2 WCSP Configuration

Figure A-10 illustrates the WCSP configuration for the DEM-DAI1870. Note that the the jumper locations on Daughter Card #1 are slightly different on this version of the EVM because of WCSP pin assignments.

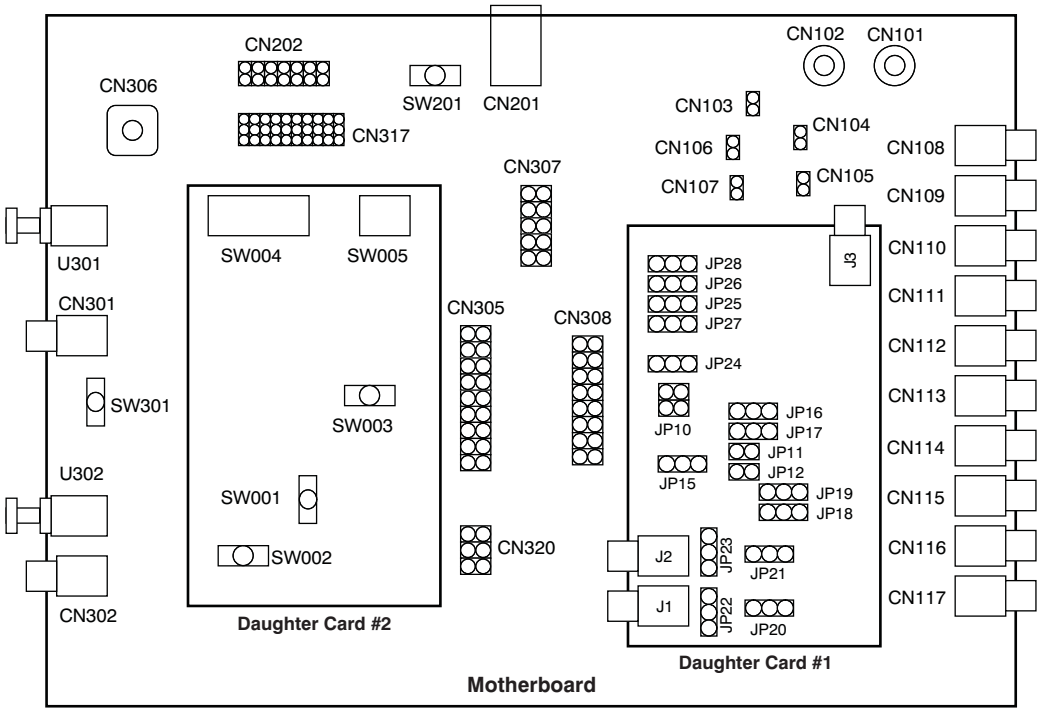


Figure A-10. EVM Configuration (WCSP)

A.2.3 Package Information

Packaging information includes a thermal pad mechanical drawing and an example board layout. These examples are taken from the PCM1870 product data sheet (available for download at www.ti.com).

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of –2.0V to +4.0V and the output voltage range of –2.0V to +4.0V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +60°C. The EVM is designed to operate properly with certain components above +60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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