TEXAS INSTRUMENTS

DEM-DAI1774 EVM

User's Guide

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About This Manual

This document provides the information needed to set up and operate the DEM-DAI1774 EVM evaluation module, a test platform for the 16-bit, low-power PCM1774 stereo digital-to-analog converter (DAC). For a more detailed description of the PCM1774 product line, please refer to the product data sheet available from the Texas Instruments web site at http://www.ti.com. Support documents are listed in the section of this guide entitled ***Related Documentation from Texas Instruments***.

How to Use This Manual

Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the DEM-DAI1774 EVM.

Chapter 1 gives an overview of the PCM1774 DAC and the DEM-DAI1774 EVM. The EVM block diagram and primary features are also discussed.

Chapter 2 provides general information regarding EVM handling and unpacking, absolute operating conditions, and the default switch and jumper configuration. This chapter also discusses the EVM controller software

Chapter 3 is the hardware setup guide for the EVM, providing all of the necessary information needed to configure the EVM switches and jumpers for product evaluation.

Chapter 4 reviews the DEM-DAI1774 EVM switch and jumper configuration.

Chapter 5 discusses how to set up jumpers on the DEM-DAI1774 EVM motherboard for performance evaluation using an audio analyzer. It also presents the process for measuring dynamic characteristics and provides example characteristic data.

Chapter 6 includes the EVM electrical schematics, printed circuit board (PCB) layout, and the bill of materials.

Information About Cautions and Warnings

This document contains caution statements.

CAUTION

This is an example of a caution statement. A caution statement describes a situation that could potentially damage your software or equipment.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

The following documents provide information regarding Texas Instruments integrated circuits used in the assembly of the DEM-DAI1774 EVM. These documents are available from the TI web site. The last character of the literature number corresponds to the document revision that is current at the time of the writing of this User's Guide. Newer revisions may be available from the TI web site at http://www.ti.com/ or call the Texas Instruments Literature Response Center at (800) 477–8924 or the Product Information Center at (972) 644–5580. When ordering, identify the document(s) by both title and literature number.

Data Sheet	Literature Number
PCM1870 Product data sheet	SLAS544
PCM1774 Product data sheet	SLAS551
DIT4096 Product data sheet	SBOS225B

If You Need Assistance

If you have questions regarding either the use of this evaluation module or the information contained in the accompanying documentation, please contact the Texas Instruments Product Information Center at (972) 644–5580 or visit the TI web site at www.ti.com.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense is required to take whatever measures may be required to correct this interference.

Trademarks

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Description

The DEM-DAI1774 EVM is a complete evaluation platform for the 16-bit, low-power PCM1774 DAC with headphone output. All necessary connectors and circuitry are provided for interfacing to audio test systems and commercial audio equipment.

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1.1 Introduction—PCM1774

The PCM1774 is a low-power stereo DAC designed for portable digital audio applications. This DAC integrates a headphone amplifier, line amplifier, boost amplifier, programmable gain control, analog mixing, and sound effects.

It is available in a 4 mm × 4 mm QFN package to reduce the overall device footprint. The PCM1774 accepts Right-Justified, Left-Justified, I^{2}S™, and digital signal processing (DSP) formats, providing an easy interface to audio DSPs and decoder chips. Sampling rates up to 50 kHz are supported. The user-programmable functions are accessible through a two- or three-wire serial control port.

1.1.1 Key Features

Major features of the PCM1774 include:

- Analog Front End:
  - Stereo single-ended input
  - Microphone amplifier (+12 dB, +20 dB)
- Analog Back End:
  - Stereo/Mono line output with volume
  - Stereo/Mono headphone amplifier with volume
- Analog Performance:
  - Dynamic range: 93 dB (DAC)
  - 40-mW + 40-mW headphone output at R_L = 16 Ω
- Power-Supply Voltage
  - 1.71 V to 3.6 V for digital I/O section
  - 1.71 V to 3.6 V for digital core section
  - 2.4 V to 3.6 V for analog section
  - 2.4 V to 3.6 V for power amplifier section
- Low Power Dissipation:
  - 7 mW in playback, 1.8 V/2.4 V, 48 kHz
  - 3.3 μW in power down
- Sampling Frequency: 5 kHz to 50 kHz
- Operation from a Single Clock Input without PLL
- System Clock:
  - Common-audio clock (256 f_S/384 f_S), 12 MHz/24 MHz, 13 MHz/26 MHz, 13.5 MHz/27 MHz, 19.2 MHz/38.4 MHz, 19.68 MHz/39.36 MHz
- Two- (I^{2}C™) or Three- (SPI™) Wire Serial Control
- Programmable Function by Register Control:
  - Digital attenuation of DAC: 0 dB to –62 dB
  - Power up/down control for each module
  - +6-dB to –70-dB gain for analog outputs
  - 0-dB/12-dB/20-dB boost for microphone input
  - 0-dB to –21-dB gain for analog mixing
  - Three-band tone control and 3D sound
  - Analog mixing control

- Pop-Noise Reduction Circuit
- Short Protection Circuit
- Package: 4-mm × 4-mm QFN Package
- Register compatible with PCM3793A/94A and PCM1870
- Operating Temperature Range: –40°C to +85°C

1.2 Pin Assignments and Terminal Functions

Figure 1-1 shows the pin assignments for the PCM1774. Table 1-1 lists the terminal functions.

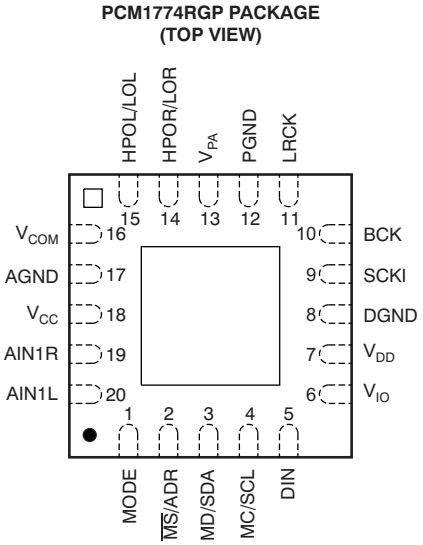

Figure 1-1. PCM1774 Pin Assignments

Table 1-1. PCM1774 Terminal Functions

Name	QFN-20 Terminal	I/O	Description
MODE	1	I	Two-wire or three-wire interface selection (LOW: SPI, HIGH: I^2C)
$\overline{MS}$/ADR	2	I	Mode control select for three-wire/two-wire interface
MD/SDA	3	I/O	Mode control data for three-wire/two-wire interface
MC/SCL	4	I	Mode control clock for three-wire/two-wire interface
DIN	5	I	Serial audio data input
V_{IO}	6	–	Power supply for digital I/O
V_{DD}	7	–	Power supply for digital core
DGND	8	–	Ground for digital
SCKI	9	I	System clock
BCK	10	I/O	Serial bit clock
LRCK	11	I/O	Left and right channel clock
PGND	12	–	Ground for speaker power amplifier
V_{PA}	13	–	Power supply for power amplifier
HPOR/LOR	14	O	Headphone/line out for L-channel
HPOL/LOL	15	O	Headphone/line out for R-channel
V_{COM}	16	–	Common voltage for analog
AGND	17	–	Ground for analog
V_{CC}	18	–	Power supply for analog
AIN1R	19	I	Analog input 1 for R-channel
AIN1L	20	I	Analog input 1 for L-channel

1.3 DEM-DAI1774 EVM Description

The DEM-DAI1774 evaluation module permits user control of the entire PCM1774 system. The EVM allows users to play back stereo headphone audio output with or without digital input in a variety of system configurations, using either an optical cable or RCA jacks, as shown in Figure 1-2.

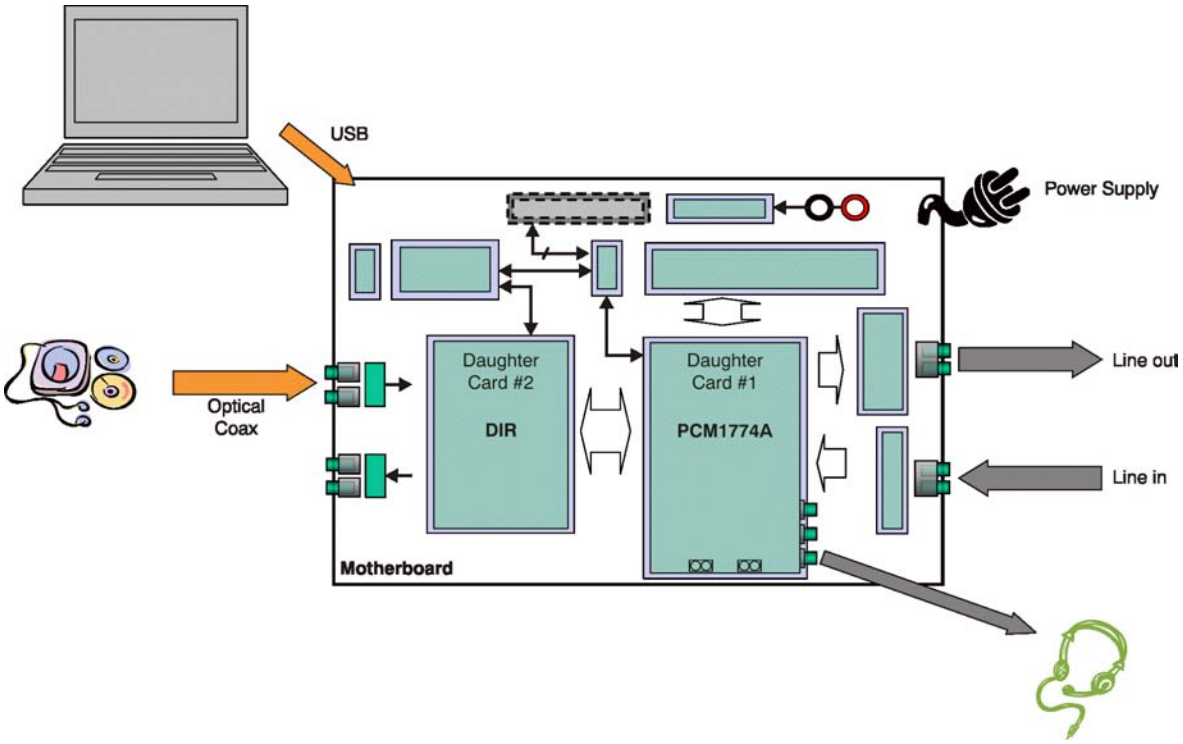

Figure 1-2. DEM-DAI1774 EVM System Diagram

Getting Started

This chapter provides information regarding handling and unpacking the DEM-DAI1774 EVM, as well as the EVM absolute operating conditions and a description of the factory default switch and jumper configurations.

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2.1 Electrostatic Discharge Warning

Many of the components on the DEM-DAI1774 EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

CAUTION

Failure to observe ESD handling procedures may result in damage to EVM components.

2.2 Unpacking the EVM

Upon opening the DEM-DAI1774 EVM package, please check to make sure that the following items are included:

- One DEM-DAI/LPC-USB (Motherboard)
- One DEM-PCM1870RHF/1774RGP-A (Daughter Card #1)
- One DEM-TRCV/LPC (Daughter Card #2)

If any of these items are missing, please contact the Texas Instruments Product Information Center nearest you to inquire about a replacement.

2.3 Default Configuration

Figure 2-1 and Figure 2-2 illustrate the default EVM configuration and the default external equipment connection configuration, respectively.

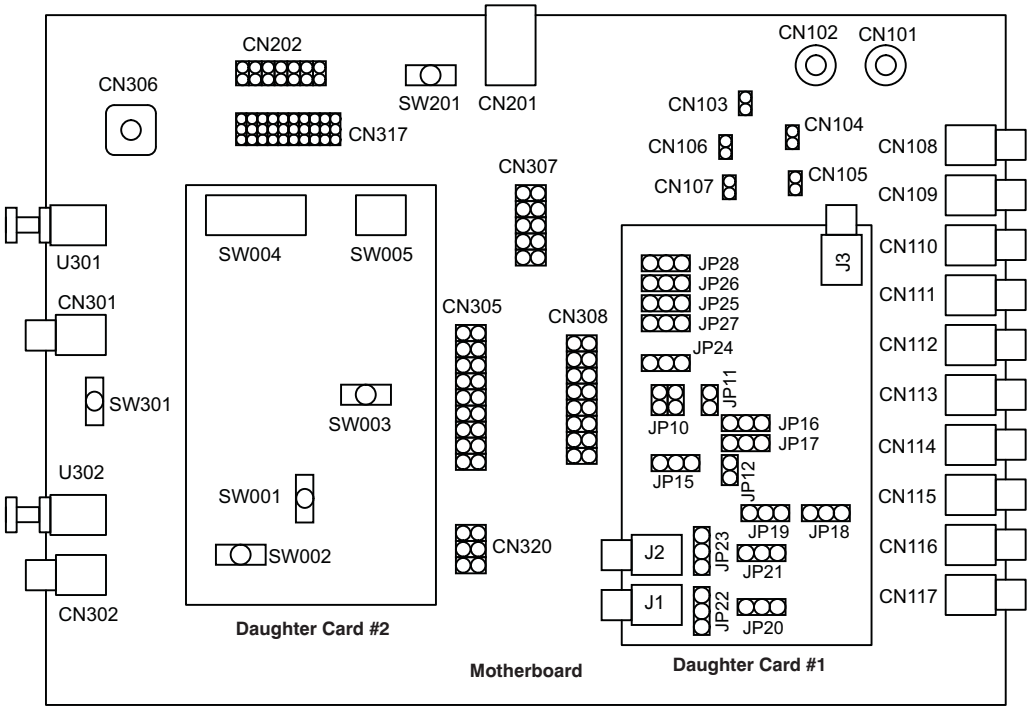

Figure 2-1. EVM Configuration

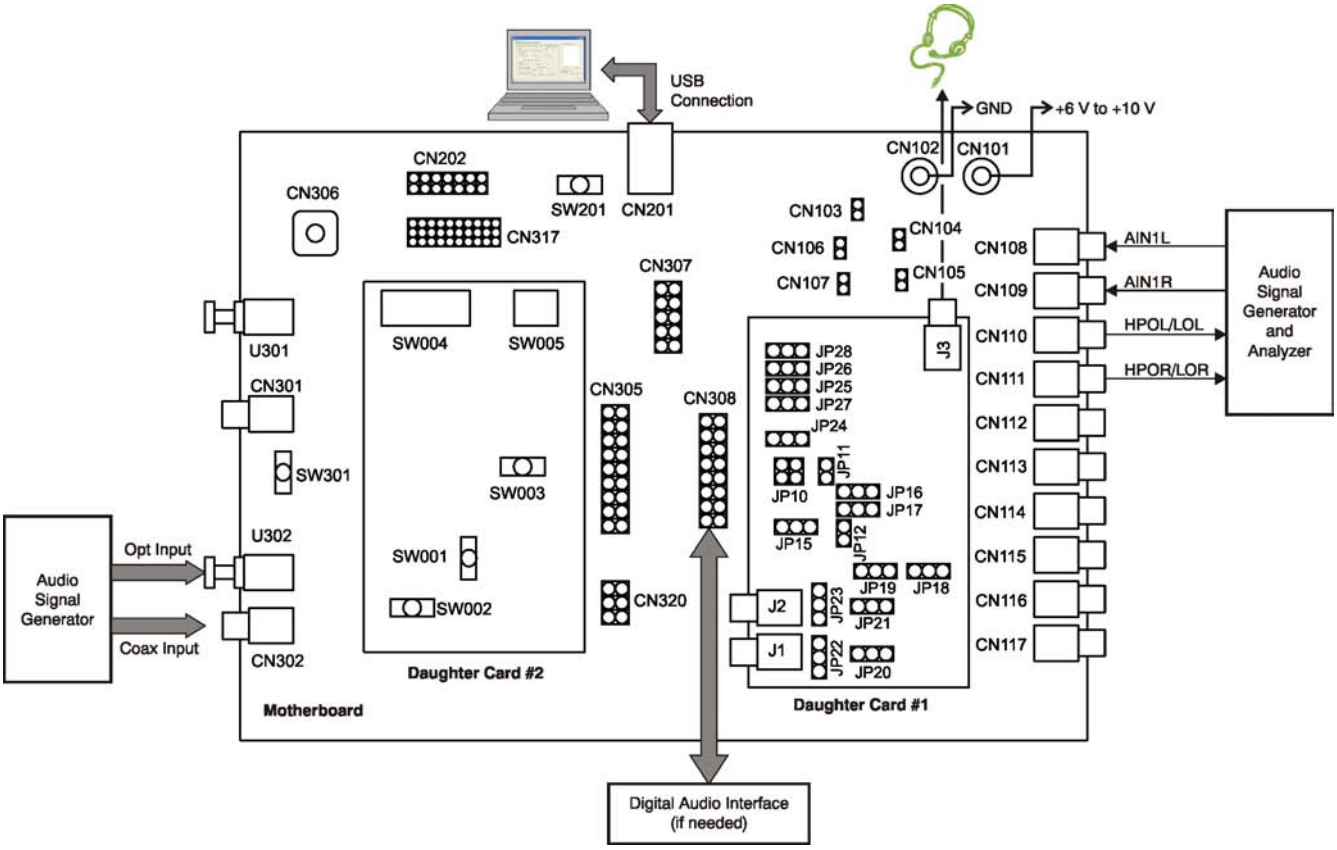

Figure 2-2. EVM and External Equipment Connections

The factory default configuration for the DEM-DAI1774 EVM is listed below.

Motherboard:

- CN101, CN102: Connect dc power supply positive lead (+) to CN101 and negative lead (–) to CN102
- SW301: Set *Opt* or *Coax* output for the proper cable connection

Daughter Card #1 (DEM-PCM1774RHF/1774RGP-A):

- JP1-9, JP13, JP14, and JP29: these jumper pins are not used
- For other jumper settings, please refer to the chapter, Switches and Connectors.

Daughter Card #2 (DEM-TRVC/LPC):

- SW001: Set *Opt* or *Coax* for S/PDIF input to DIR:LC89052T
- SW002: Set to silkscreen *SW002 RESET* side (releasing reset)
- SW003: Set *X'tal* to use onboard crystal oscillator

There is no need to change the setting of the shorting plugs for basic operation. Jumper settings strongly depend on the audio interface.

Set-Up Guide

This chapter discusses how to set up the DEM-DAI1774 EVM and describes the EVM software.

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3.1 Basic Operating Set-Up

Follow these steps to set up the DEM-DAI1774 EVM for operation.

Step 1. When using the kit for the first time, install the TUSB3410 VCP (Virtual COM Port) driver to the host PC. To install the driver, refer to the *Virtual COM Port Driver Installation Instructions.pdf* located in the DEM-DAI1774 folder of the software CD or available for download through the TI web site.

Step 2. Connect the audio signal sources and/or receiver, using one of these connections:

- S/PDIF cable (optical or coaxial)
- Analog input/output (RCA)

Step 3. Connect microphone, headphone, audio amplifier, or measurement equipment, if necessary.

Step 4. Confirm that jumpers CN103–CN107 are shorted.

Step 5. Connect the USB cable between the host PC and the motherboard (CN201).

Step 6. Apply +6 V to +10 V to the motherboard (CN101, CN102 for power supply).

Step 7. Execute *EVM1774A.exe*.

When the installation is complete, the EVM software is ready to use.

3.2 Software Control and Operation

This section of the user's guide reviews the operation and configuration of the EVM controller software.

3.2.1 User Interface Panel

After finishing the installation process (as explained in Section 3.1), the user interface panel shown in Figure 3-1 appears.

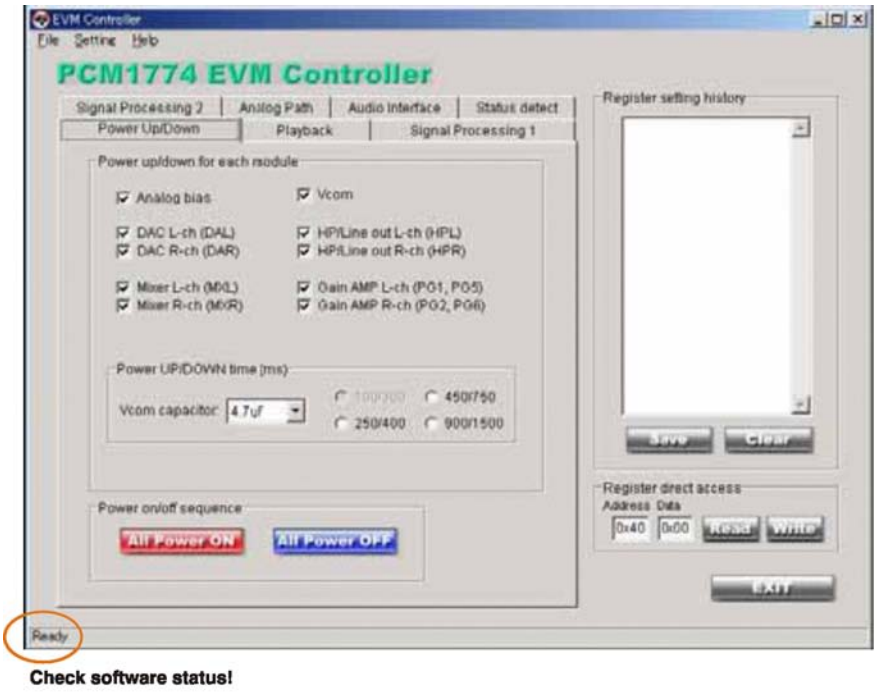


Figure 3-1. User Interface Window

Check to see that a ***Ready*** notation appears in the lower left-hand corner after successful I^2C communication is established. Otherwise, you will see an error box showing a communication error (as shown in Figure 3-2).

Figure 3-2. Communication Error Message

If you receive this error message, confirm the set-up procedures and restart the software. Shut it down and then execute *EVM1774.exe* a second time.

There are four primary sections of the user interface panel (see Figure 3-1):

- Module controller, for functions such as record, signal processing, audio format, and so forth;
- Power on/off sequence controller
- Register setting history controller
- Register direct access controller

3.2.2 Power On/Off Sequence

By default, each module is set without any of the checkboxes toggled in the Power Up/Down menu. All modules are set to a power-down condition.

Click *All Power On* (the red box, as shown in Figure 3-3) to easily start EVM operation, instead of powering up the module manually.

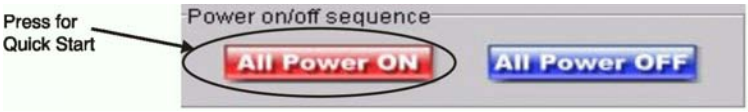


Figure 3-3. Power On/Off Sequence Function Buttons

Note: If pressing the Power On/Off sequence button has no effect, check to see that the two files *power_on.csv* and *power_off.csv* are located in the same folder on the PC as the EVM software (EVM1774A.exe).

3.2.3 Module Function Control

The PCM1774 EVM controller software contains seven tabs:

- Power Up/Down: to power up and power down each module
- Playback: executes headphone gain control and digital attenuation
- Signal Processing 1: adjusts the tone control and notch filter coefficient
- Signal Processing 2: adjusts DAC oversampling and de-emphasis
- Analog Path: controls analog mixer
- Audio Interface: selects the audio interface for the DAC
- Status Detect: controls headphone short detection

3.2.3.1 Power Up/Down

This menu (shown in Figure 3-4) allows users to manually power up or power down each module. Click the appropriate checkboxes to power up or power down a specific module. Table 3-1 shows the register mapping for each module setting.

Abbreviations such as *ADL/ADR*, *D2S*, and *PG1, PG2* stand for corresponding modules that are described in the block diagram of the PCM1774 (see Figure 3-8).

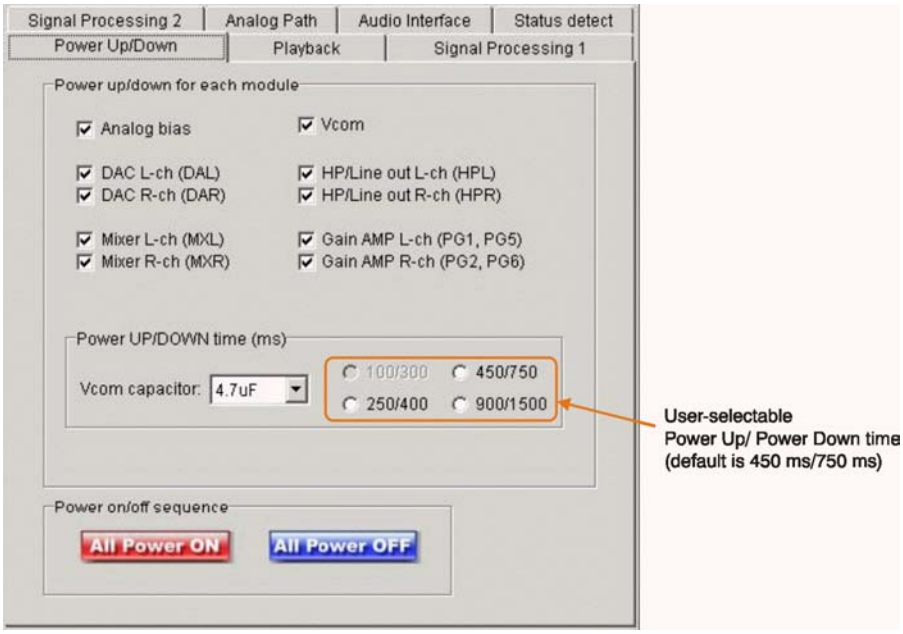


Figure 3-4. Internal Module Power Up/Down Function Menu Tab

Table 3-1. Register Mapping for Power Up/Down Module

Check Box	Internal Module	Register
Analog Bias	Analog bias	Reg#73 bit7 [PBIS]
V_{COM}	Analog common voltage	Reg#74 bit0 [PCOM]
HP/Line out L-ch (HPL)	Headphone/Line out amp L-channel	Reg#73 bit2 [PHPL]
HP/Line out R-ch (HPR)	Headphone/Line out amp R-channel	Reg#73 bit3 [PHPR]
DAC L-ch (DAL)	DAC and interpolation filter L-ch	Reg#73 bit5 [PDAL]
DAC R-ch (DAR)	DAC and interpolation filter R-ch	Reg#73 bit6 [PDAR]
Gain AMP L-ch (PG1, PG5)	Gain amp L-channel (PG1 and PG5)	Reg#82 bit4 [PAIL]
Gain AMP R-ch (PG2, PG6)	Gain amp R-channel (PG2 and PG6)	Reg#82 bit5 [PAIR]

Power UP/DOWN Time (ms) Options

It is possible to select the V_{COM} ramp up/down time (from GND level to common-level voltage or from common-level voltage to GND level), in milliseconds. It is also possible to choose a V_{COM} capacitor value and time by clicking the appropriate check boxes. A 4.7 µF V_{COM} capacitor value is the default setting (this value is also mounted on the EVM fixture).

A 4.7 µF V_{COM} capacitor is the recommended value. In this configuration, users do not need to change the recommended power-on sequence discussed in the PCM1774 datasheet on pages 15 and 16. However, values other than a 4.7 µF V_{COM} capacitor that are application-specific can be used. Select the appropriate value from the V_{COM} capacitor drop-down menu if the default capacitor value on the EVM (4.7 µF) is changed to 1.0 µF, 2.2 µF, or 10 µF.

The combination of PTM[1:0] and RES[4:0] determines the V_{COM} ramp up/down time as described in Table 3-2 and Table 3-3.

Table 3-2. PCM1774 Resistor 125(7dh) RES[4:0]: Resistor Value Control

RES [4:0]	V_{COM} Resistor Value
10000	60 kΩ
11000	24 kΩ
11100	12 kΩ
11110	6 kΩ
Others	Reserved

Table 3-3. PCM1774 Resistor 125(7dh) PMT[1:0]:Power Up/Down Time Control and Register Direct Access

V_{COM} Capacitor (μF)	RES [4:0]	PTM [1:0]	Power Up Time (ms)	Power Down Time (ms)	Resistor Direct Access
10	11110	00	450	750	0x7D1E
	11100	11	900	1500	0x7D7C
	11000	Do not set	-	-	-
	10000	Do not set	-	-	-
4.7	11110	01	250	400	0x7D3E
	11100	00	450	750	0x7D1C (default)
	11000	11	900	1500	0x7D78
	10000	Do not set	-	-	-
2.2	11110	10	100	300	0x7D5E
	11100	01	250	400	0x7D3C
	11000	00	450	750	0x7D18
	10000	11	900	1500	0x7D70
1.0	11110	Do not set	-	-	-
	11100	10	100	300	0x7D5C
	11000	01	250	400	0x7D38
	10000	00	450	750	0x7D10

As a reference, Figure 3-5 and Figure 3-6 show example ramp-up and ramp-down waveforms, resepctively, measured with the default setting.

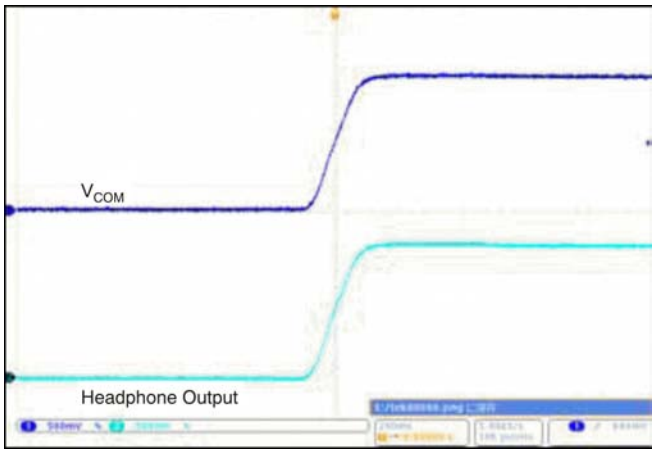


Figure 3-5. Example Ramp-Up Waveform

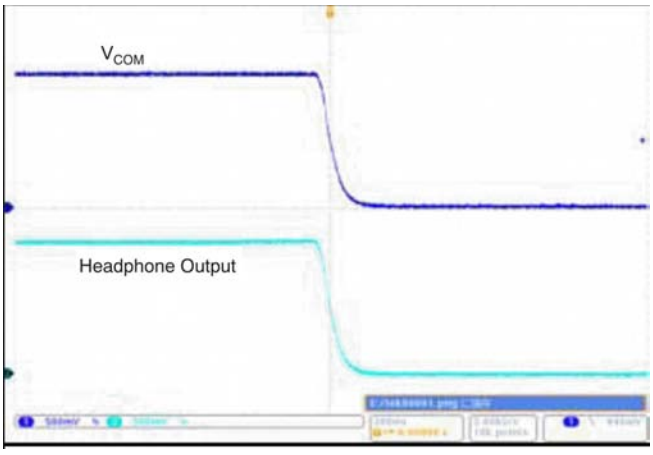


Figure 3-6. Example Ramp-Down Waveform

3.2.3.2 Playback

Figure 3-7 shows the Playback function tab options.

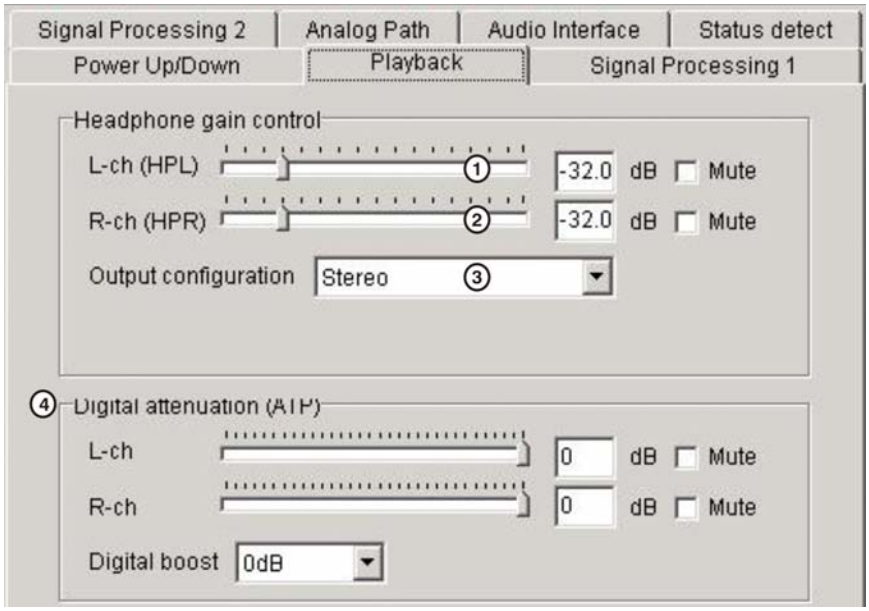


Figure 3-7. Playback Function Menu Tab

Figure 3-8 shows the EVM modules that correspond to the playback function.

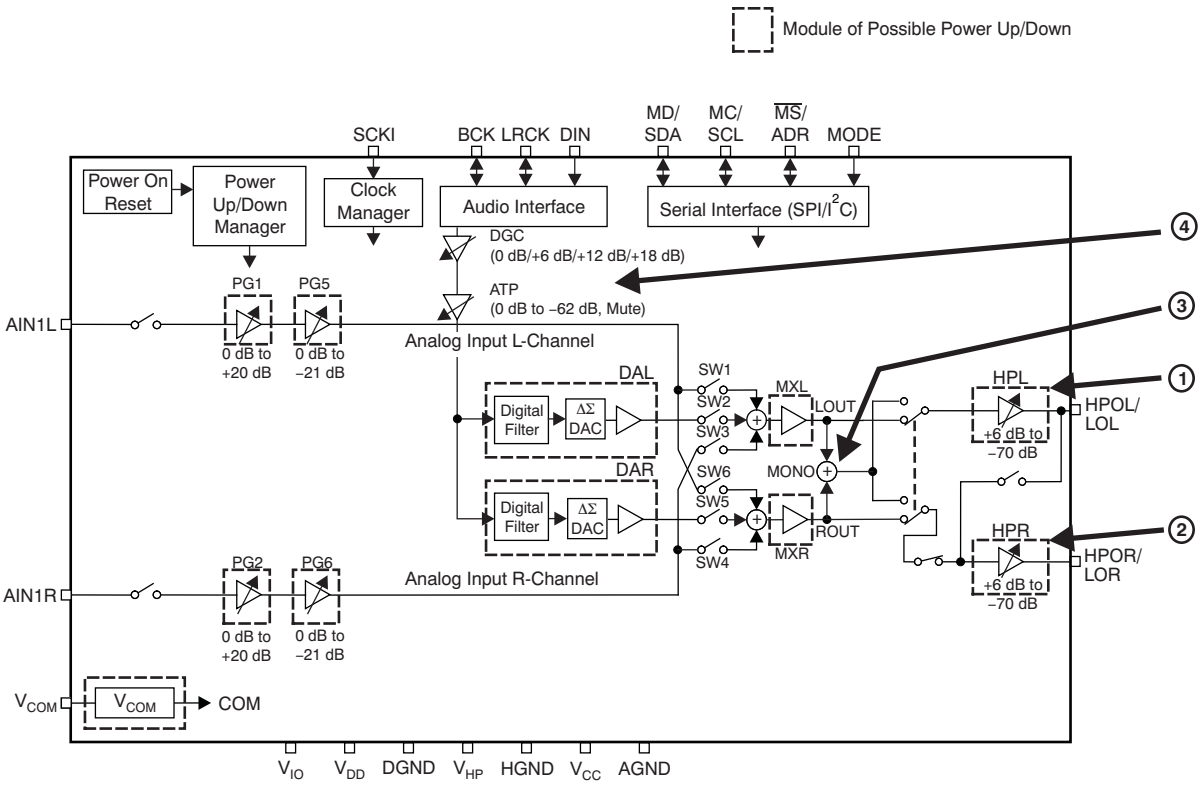


Figure 3-8. EVM Modules Corresponding to Playback Function

Headphone Gain Control Options

Move the L-channel (HPL) and R-channel (HPR) to adjust the gain of the analog output from the headphone amplifier.

Use the *Output configuration* drop-down menu to select from either stereo or mono output.

- The L-ch slider controls the headphone/line amp gain
- The R-ch slider controls the headphone/line amp gain
- Select the Output configuration from stereo/mono (single-ended)/mono (differential) for the desired channel
- The HP com drop-down list determines the HPCOM/MONO pin function

Digital Attenuation (ATP) Options

Move the L-ch and R-ch sliders to adjust the gain of the incoming digital signals prior to conversion by the DAC.

- The L-ch slider controls the DAC digital attenuator level
- The R-ch slider controls the DAC digital attenuator level
- Select the Output configuration from stereo or mono
- The Digital boost enables gain control of 0 dB, +6 dB, +12 dB, or +18 dB for the DAC digital input

3.2.3.3 Signal Processing 1

Figure 3-9 illustrates the Signal Processing 1 function menu tab.

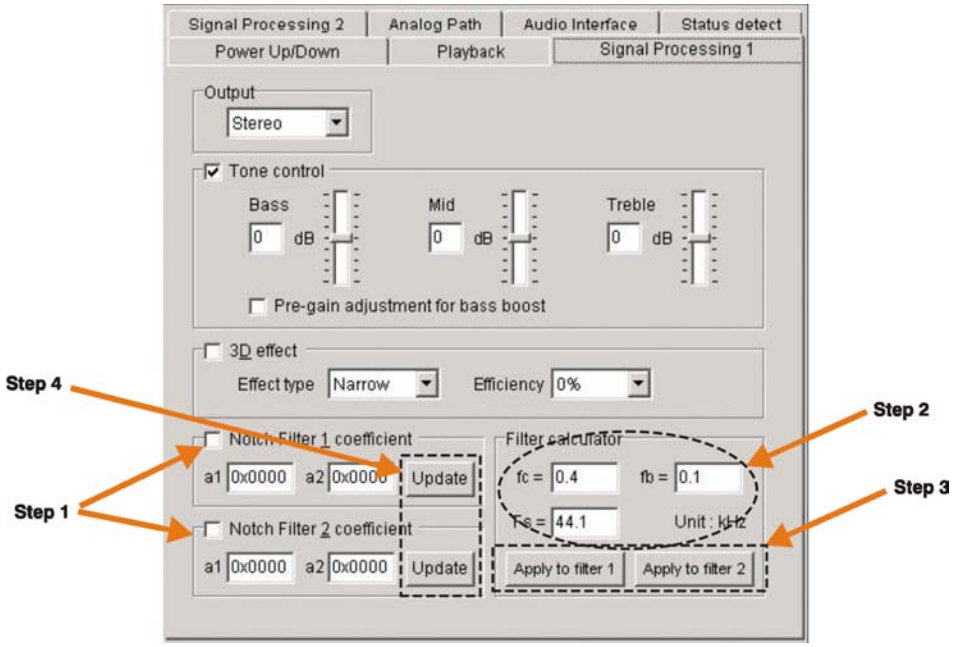


Figure 3-9. Signal Processing 1 Function Menu Tab

Output Options

Select the *Source* drop-down menu to choose between a stereo or mono output configuration.

Tone Control Options

Move the Bass, Mid, and Treble sliders to adjust the tone control gain. The tones are controlled by the respective tone sliders. A three-band tone control characteristic plot is shown in Figure 3-10.

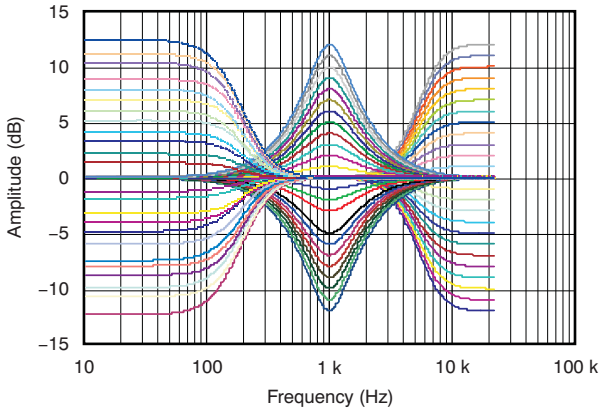


Figure 3-10. Three-Band Tone Control (Bass, Mid, Treble)

3D Effect Options

By implementing a 3D effect in this option box, the PCM1774 provides 3D sound to the headphone and speaker outputs with low power consumption during DAC operation. Check the *3D effect*, then select an *Effect* type and an *Efficiency* drop-down menu to obtain the desired 3D enhancement.

Effect type means the selection of a band-pass filter (BPF); the BPF filters the sound, and enables a high percentage of heavy 3D enhancements to be applied to the signal.

Effect type and efficiency are controlled through the use of checkboxes.

Notch Filter 1 Coefficient, Notch Filter 2 Coefficient Options

In some applications, incoming noise such as motor control noise, CCD noise and other mechanical noise may not be negligible. The PCM1774 provides a very useful function to reduce such interference with the notch filter function.

When the checkbox of Notch Filter 1 Coefficient or Notch Filter 2 Coefficient is checked, coefficient a_1 and a_2 of the notch filter can be programmed at each edit box. (Note that not all users need to calculate these coefficients for a given application.)

Load the values of f_c, f_b and f_S into the Filter Calculator group box.

Click *Apply to Filter 1* or *Apply to Filter 2*. The calculated coefficient will then appear in the a_1 and a_2 edit box.

Finally, click the *Update* button for each Notch filter coefficient. To complete the notch filter operation, the *Update* button must be clicked.

Note that Update step is required each time new or different parameters are loaded to the dialog box.

Follow these steps to update the notch filter coefficient:

Step 1. Click the checkbox of Notch Filter 1 Coefficient or Notch Filter 2 Coefficient.

Step 2. Input the parameter values f_c, f_b and f_S.

Step 3. Click *Apply to Filter 1* or *Apply to Filter 2*.

Step 4. Update for each notch filter coefficient.

Each coefficient is calculated using the following equations.

$a_1 = –(1 + a_2)\cos(\omega_o)$

$a_2 = [1 – \tan(\omega_b/2)] / [1 + \tan(\omega_b/2)]$

where:

- f_S = sampling frequency
- f_c = center frequency
- f_b = bandwidth
- $\omega_o = 2\pi f_c/f_S$ represents the angular center frequency
- $\omega_b = 2\pi f_b/f_S$ is the parameter to adjust bandwidth

Here are several example coefficient calculations using Equation 3-1 and Equation 3-2. These measurements are also shown in Figure 3-12.

Given: f_S = 16 kHz, f_c = 0.5 kHz, f_b = 0.2 kHz

a_2 = 0.924390492 (converted decimal to hex: 3B29h)

a_1 = –1.887413868 (converted decimal to hex: 8735h)

a_2: F[215:208] = 3Bh, F[207:200] = 29h

a_1: F[115:108] = 87h, F[107:100] = 35h

Figure 3-11 illustrates the notch filter characteristic. All users can select any frequencies that can be used by the application system based on the notch filter coefficient theory discussed here.

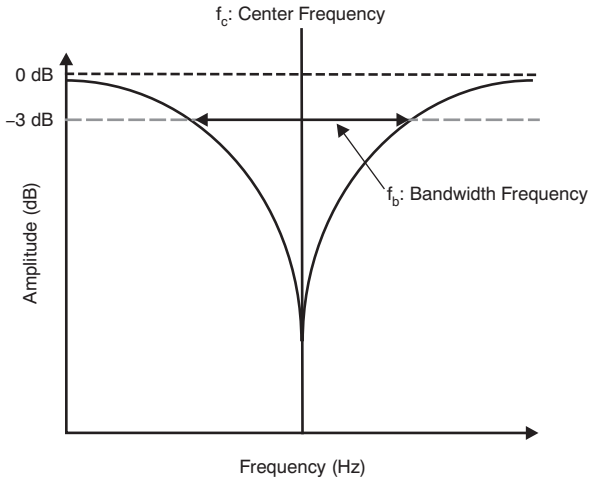


Figure 3-11. Notch Filter Characteristic Model

In some applications, incoming noise such as motor control noise, CCD noise, and other mechanical noise may not be negligible. The PCM1774 provides a very useful function to reduce these types of noise with the notch filter function.

Users can select any interference frequency that is generated by the end application system based on the theory of the notch filter coefficient discussed previously.

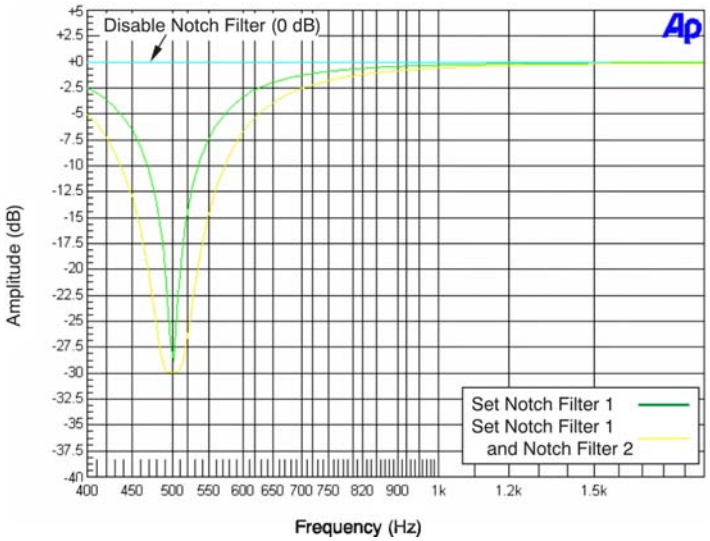


Figure 3-12. Example of Measured Notch Filter Characteristic

3.2.3.4 Signal Processing 2

The Signal Processing 2 Function menu tab is shown in Figure 3-13.

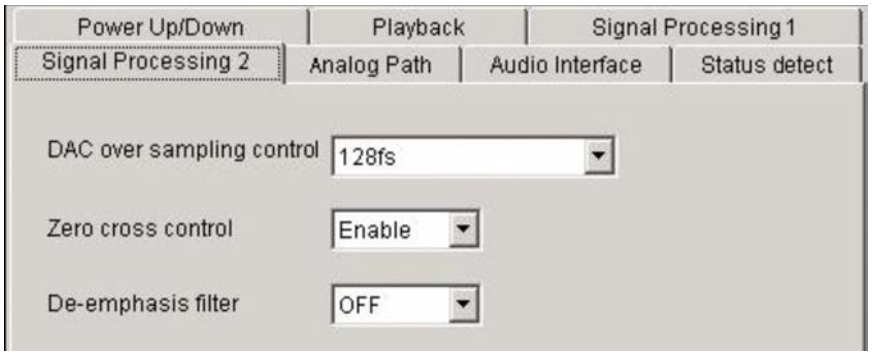


Figure 3-13. Signal Processing 2 Function Menu Tab

DAC Oversampling Control Options

Select the *DAC Oversampling control* to determine the DAC oversampling ratio.

The oversampling ratio can be set at a sampling frequency of $128f_S$, $192f_S$, $256f_S$, or $384f_S$. The oversampling rate of $192f_S$, $256f_S$, or $384f_S$ will be selected when sampling frequency of the input data is lower than 24 kHz. These oversampling ratios will move the out-of-band noise caused by the delta-sigma modulator to a higher frequency domain.

Zero Cross Control Options

Choose the *Zero Cross Control* menu to turn on the zero crossing function.

When zero crossing control is enabled, the digital attenuation and analog volume level change at the zero crossing point to avoid the audible zipper noise.

De-Emphasis Filter Options

Select the *De-emphasis filter* drop-down menu to enable the de-emphasis filter.

De-emphasis can be disabled or enabled for a given sampling frequency.

3.2.3.5 Analog Path

Figure 3-14 shows the Analog Path Function menu.

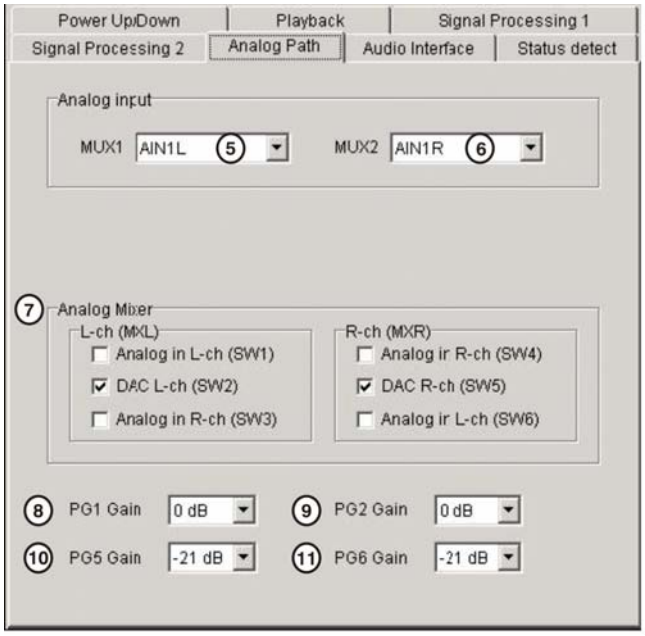


Figure 3-14. Analog Path Function Menu Tab

Figure 3-15 illustrates the modules that correspond to the analog path function.

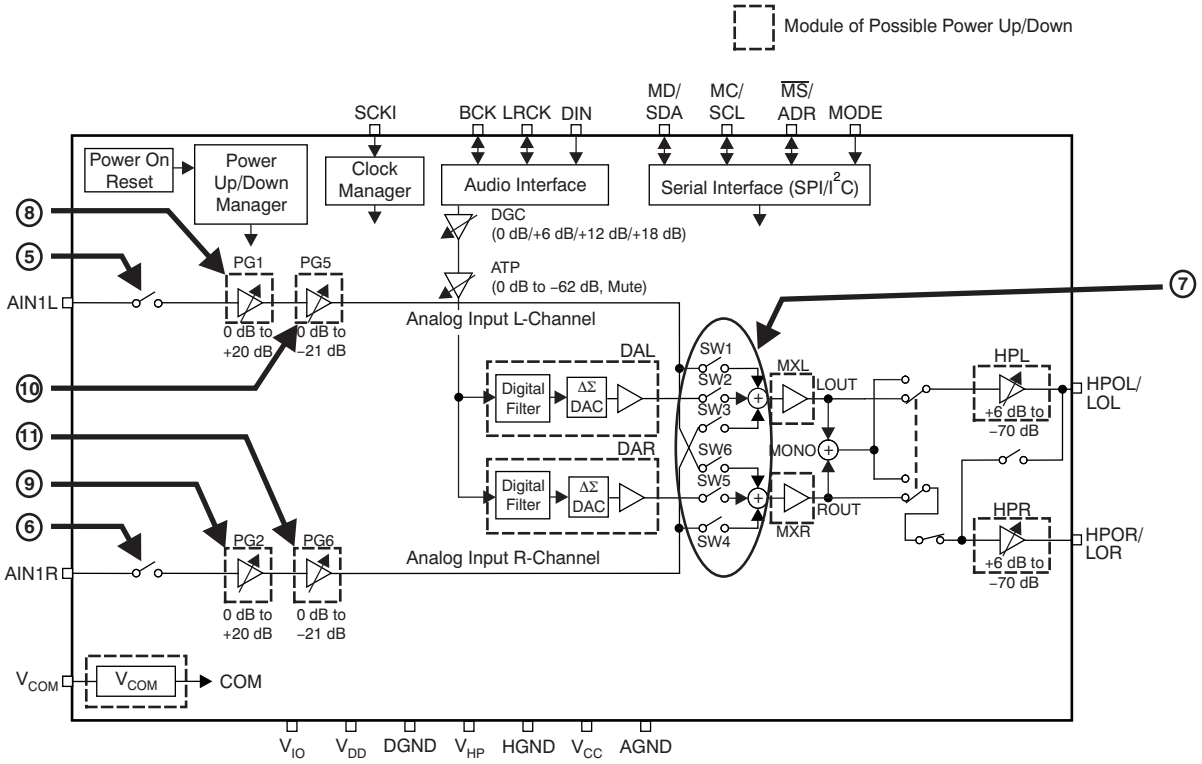


Figure 3-15. Modules Corresponding to Analog Path Function

Analog Mixer Options

Select the *Analog Mixer* drop-down menu to combine the DAC output and the incoming stereo or mono analog signal input through PG1/PG5 or PG2/PG6.

- The analog input, DAC output, and the other channel of the analog input can be combined as the analog mixer source.

PG1/PG5 Gain and PG2/PG6 Gain Options

Adjust the left channel gain for PG1/PG5 from the drop-down menu. Adjust the right channel gain for PG2/PG6 from the drop-down menu.

3.2.3.6 Audio Interface

Figure 3-16 shows the Audio Interface Function menu.

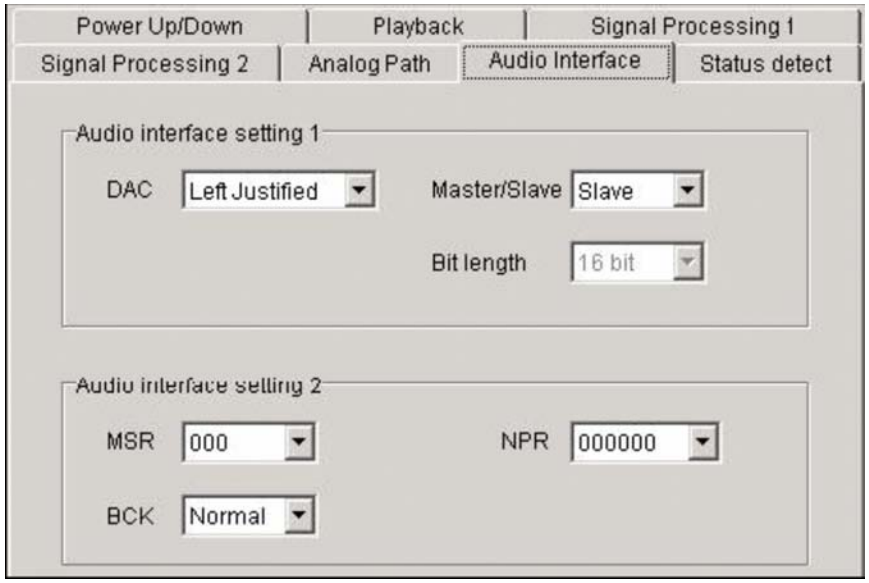


Figure 3-16. Audio Interface Function Menu Tab

Audio Interface Setting 1 Options

Use this section of the menu to set the audio data format for the DAC output. Set the operating mode as Master or Slave.

Audio Interface Setting 2 Options

Use this section of the menu when working in Master mode.

- **MSR:** sets system clock rate
- **NPR:** sets system clock divider rate
- **BCK:** chooses between normal and burst BCK output

  Burst operation of BCK in master mode will contribute to greater overall reduction in power consumption. See the PCM1774 data sheet for the possible combinations of these register settings.

3.2.3.7 Status Detect

Figure 3-17 shows the Status Detect Function menu.

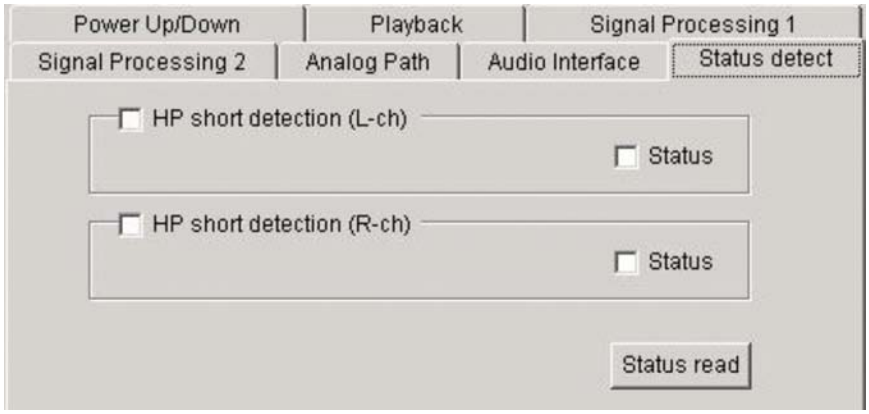


Figure 3-17. Status Detect Function Menu Tab

HP Short Detection Options

These checkboxes enable or disable the headphone L-channel and R-channel short detection, respectively.

When short detection recovery is set to *Release*, the status bit automatically resets to '0'.

The *Status Read* button enables the user to read back the current status of the headphone short detection via the I^2C interface.

3.2.4 LC89052T (DIR: Digital Audio I/F Receiver) Control Window

Figure 3-18 illustrates the LC89052 Interface format choices.

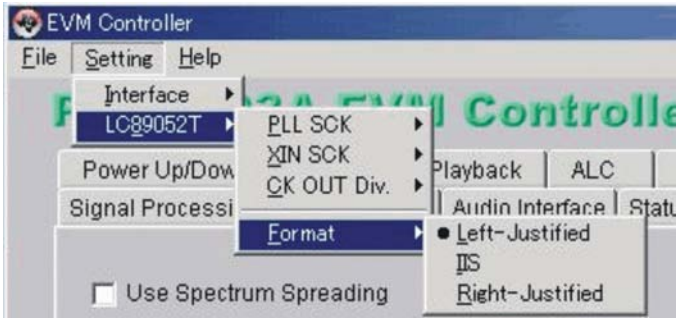


Figure 3-18. LC89052 Interface Format Selection Options

3.2.4.1 Audio Clock/Data Control Options

There are several options available for the audio clock and data control features in the DEM-DAI1774 EVM software.

For the system audio clock control, users can select any of these options:

- PLL SCK: Selects the system clock rate for the PCM1774
- XIN SCK or E-SCK: Selects the crystal oscillator frequency on Daughter Card #2
- CKOUT Div: Selects the dividing rate for CKOUT

The serial audio data format is controlled by the other part of the drop-down menu; see Figure 3-18. Select the data format for the DAC interface of the PCM1774 (it should match with the *DAC* setting on the *Audio Interface* tab).

3.2.4.2 Register Setting History

When any checkboxes are selected on any tab of the software GUI (including power up/down operation, corresponding resistor address, and so forth), the register value is automatically written into the register setting history panel. These parameters can then be saved, allowing users to identify a particular sequence setting that was sent to the device under test.

Any operating sequence settings can be saved as a comma-separated value (*.csv) file, with an identifiable name. This archive feature is useful when the same sequence settings are required for continued testing. The list of available *.csv files refreshes and displays when the *Clear* button is clicked.

Figure 3-19 shows the Register Setting History display window.

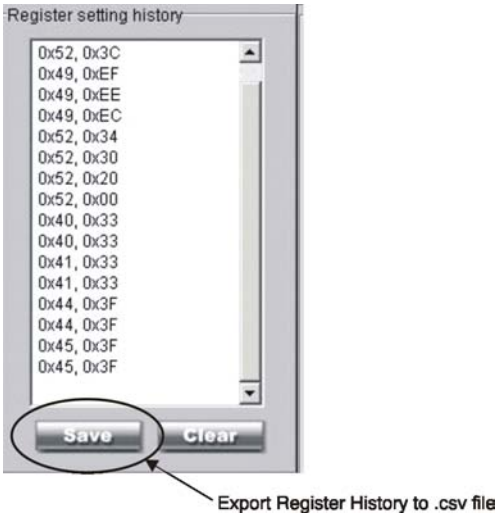


Figure 3-19. Register Setting History Window

3.2.4.2.1 Modifying a .csv File

The .csv file stores a sequence of register settings for the PCM1774. To load a given register setting, it should be written in hex code, as shown in Figure 3-20; use the left row for resistor addresses and the right row for resistor values.

	A	B	C
1	0x40	0x27	
2	0x41	0x27	
3	0x42	0x27	
4	0x43	0x27	
5	0x44	0x27	
6	0x45	0x27	
7	0x46	0x20	
8	0x4B	0xC0	
9	0x51	0x02	
10	0x5A	0x10	
11	0x49	0xE0	
12	0x56	0x01	
13	0x48	0x03	
14	0x58	0x11	
15	0x49	0xFC	
16	0x4C	0x1F	
17	0x4A	0x01	
18	0x52	0x3F	
19	0x57	0x11	
20	0x4F	0x0C	
21	0x50	0x0C	
22	sleep	4000	
23	0x49	0xFF	
24			
25			
26			

PowerOnSeq 2006 0726

Figure 3-20. Opening and Modifying a .csv File

A *sleep* line can be inserted for implementing an interval (or wait) time until executing the next line of the file. If the cell is blank, no wait time will be executed. Files can be imported and exported using the *Open script* and *Save register snapshot* options.

3.2.4.3 Register Direct Access

Figure 3-21 illustrates the register direct access dialog.

Read function:

The *Read* function is only available in I^2C mode. The register value can be read in I^2C mode. To read the value, enter the Address number (in hex code format) in the left box and click the *Read* button. Data corresponding to the address appears.

Write function:

This window also enables the user to write the register value directly. Enter the Address number and data (both in hex code format) in the respective fields and click the *Write* button.

Figure 3-21. Register Direct Access Dialog

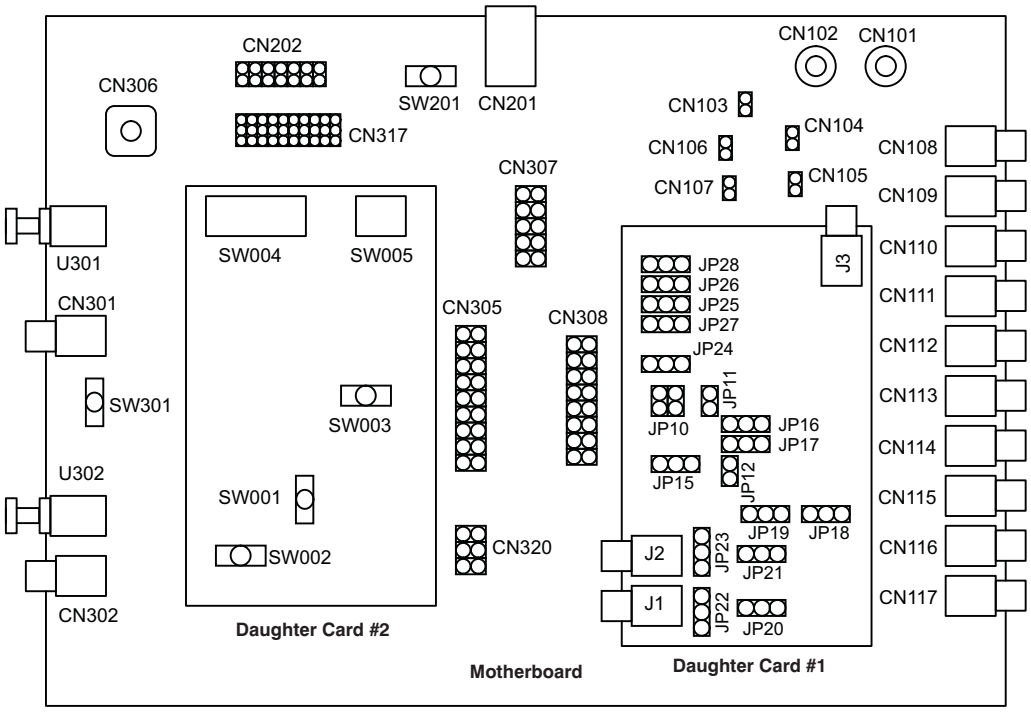
Switches and Connectors

This chapter reviews the DEM-DAI1774 EVM switch and jumper configurations.

Topic **Page**

4.1 Overview

Figure 4-1 shows the location of the switches and connectors on the EVM board.



Note: Silkscreen symbol ***CN320*** is not printed on the motherboard, but it is located in the position described in Figure 5-3.

Figure 4-1. EVM Configuration

4.2 Motherboard

Table 4-1 through Table 4-4 list the connector references for the DEM-DAI1774 EVM motherboard.

Table 4-1. Main Power Supply and Regulator

Connectors	Main Power Supply and Regulator
CN101	+6 V to 10 V Main Power Supply
CN102	GND

Table 4-2. Power-Supply Terminals for PCM1774 Power-Supply Pins

Connectors	PCM1774 Power-Supply Pins
CN103	V_{HP}
CN104	Not used. Do not care about short or open.
CN105	V_{CC}
CN106	V_{DD}
CN107	V_{IO}

Table 4-3. Audio I/O

Connectors	Audio I/O Pins
CN108	Analog audio input for PCM1870 AIN1L and AIN2L (Selected by JP18:1-2 for AIN1L, 2-3 for AIN2L on Daughter Card #1)
CN109	Analog audio input for PCM1870 AIN1R and AIN2R (Selected by JP21:1-2 for AIN1R, 2-3 for AIN2R on Daughter Card #1)
CN110	Analog audio output for PCM1774 HPOL/LOL
CN111	Analog audio output for PCM1774 HPOR/LOR
CN112	Analog audio output for PCM1870 AOL (Selected by JP17:1-2 for PGINL, 2-3 for AOL on Daughter Card #1)
CN113	Analog audio output for PCM1870 AOR (Selected by JP16:1-2 for PGINR, 2-3 for AOR on Daughter Card #1)
CN114	Analog audio input for PCM1870 PGINL
CN115	Analog audio input for PCM1870 PGINR
CN116	Not used
CN117	Not used
U301	TOSLINK™. S/PDIF Optical output
CN301	S/PDIF coaxial output
SW301	Toggle switch. Opt/Coax selector for S/PDIF output
U302	TOSLINK. S/PDIF Optical output
CN302	S/PDIF coaxial input
CN305	2x9 header pins to connect digital audio I/F for ADC/DAC. If using external signal source, all shorting plugs should be removed.
CN306	BNC connector to provide external clock for LC89052T (DIR: S/PDIF receiver) on Daughter Card or PCM1774 directly as E-SCK.
CN307	2x5 header pins. System clock and bit clock selection to provide DIT4096 (DIT: S/PDIF transmitter).*SCK* and *BCK* should be provided from LC89052T as initial setting.
CN308, CN309–CN316	2x9 header pins and SMA connectors (x8) for connecting digital audio I/F with external devices or equipment. If using this feature, all shorting plugs on CN305 should be removed.
CN317	3x10 header pins. Path of I^2C/SPI-interface selection (via USB or parallel port). Selected USB port for initial configuration. (Parallel port is not available.)
CN320	2x3 header pins. Word (L/R) clock selection (Master or Slave mode). Selected Slave mode as initial.

Table 4-4. I/F Controller (MSP430, TUSB3410)

Connectors	I/F Controller(MSP430, TUSB3410)
CN201	USB connector type-B
CN202	JTAG port
SW201	Push switch. RESET for MSP430/TUSB3410

4.3 Daughter Card #1 (PCM1774)

Table 4-5 lists the connector references for the first DEM-DAI1774 EVM daughter card.

Table 4-5. Analog Input and Output—Daughter Card #1

Connectors	Analog Input and Output of Daughter Card #1
J1	Stereo microphone input
J2	Monaural microphone input
J3	Headphone output
JP1-9	Not used
JP10	System clock select. 1-2: External clock; 3-4: SPDIF
JP11	Short jumper for C21 Capacitor between AOR to PGINR
JP12	Short jumper for C20 Capacitor between AOL to PGINL
JP13, 14	Not used
JP15	1-2: Digital loop back from PCM1870 DOUT to PCM1774 DIN; 2-3: DIN from CN302 or U301 to PCM1774
JP16	1-2: AOR to PGINR signal path; 2-3: AOR signal out to CN113
JP17	1-2: AOL to PGINL signal path; 2-3: AOL signal out to CN112
JP18	Analog input select L-channel. 1-2: AIN1L; 2-3: AIN2L
JP19	Analog input select R-channel. 1-2: AIN1R; 2-3: AIN2R
JP20	Analog input source select. 1-2: CN108; 2-3: JP22
JP21	Analog input source select. 1-2: CN109; 2-3: JP23
JP22	1-2: Stereo mic (J1) L-channel; 2-3: Mono mic (J2) L-channel
JP23	1-2: Stereo mic (J1) R-channel; 2-3: Mono mic (J2) R-channel
JP24	PCM1870 TEST pin control jumper. 1-2: External control; 2-3: GND short
JP25	PCM1774 $\overline{MS}$/ADR control. 1-2: connected to motherboard; 2-3: JP26
JP26	1-2: shorted to GND; 2-3: connected to V_{DD}.
JP27	PCM1870 $\overline{MS}$/ADR control. 1-2: connected to motherboard; 2-3: JP28
JP28	1-2: shorted to GND; 2-3: connected to V_{DD}.
JP29	Not used

Simplified descriptions of the analog input and output configuration for Daughter Card #1 are shown in Figure 4-2. Figure 4-3 illustrates the $\overline{MS}$/ADR control configuration for I^2C communication for Daughter Card #1.

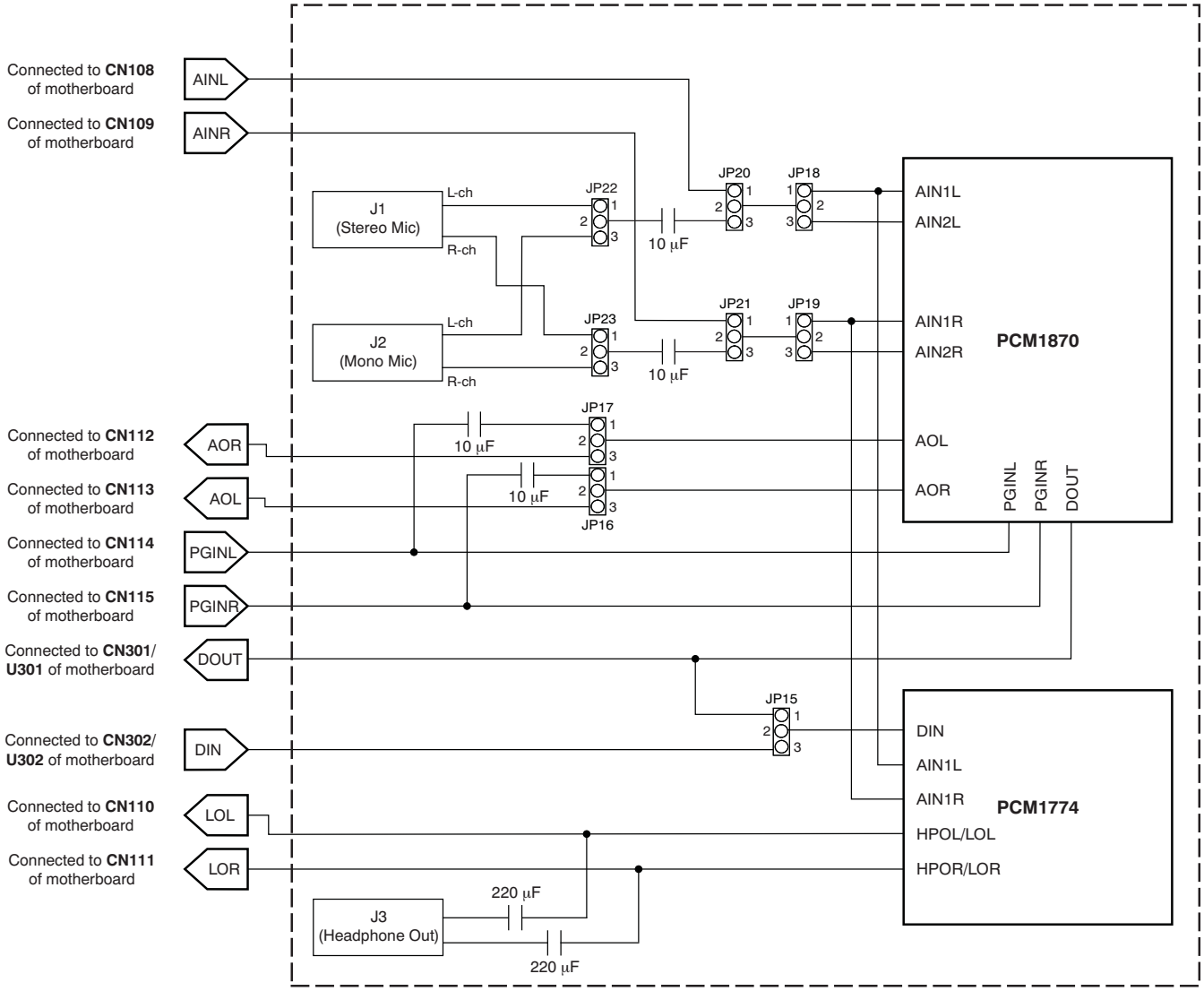


Figure 4-2. Analog Input/Output Configuration (Daughter Card #1)

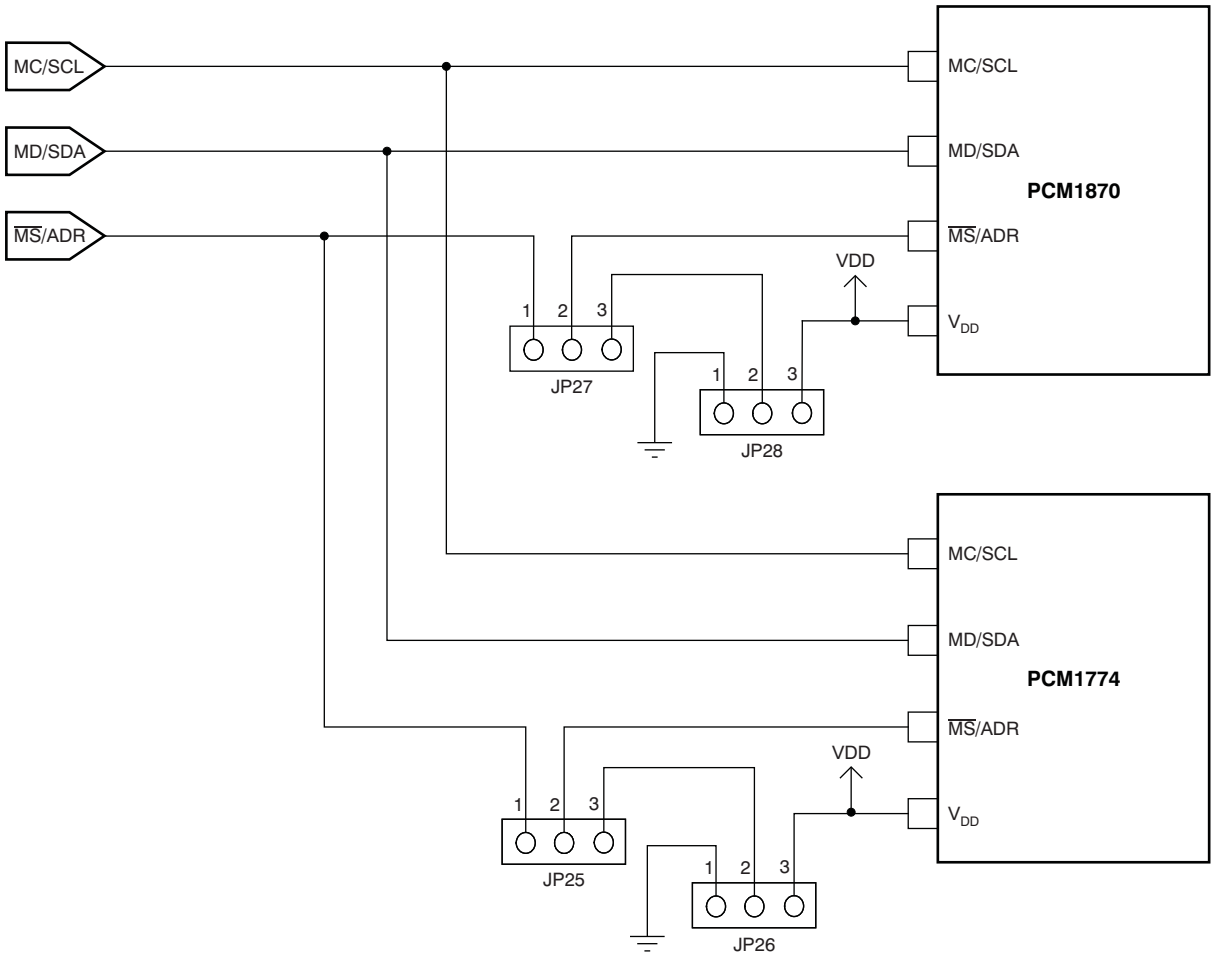


Figure 4-3. $\overline{MS}$/ADR Control Configuration for I²C/SPI Communication (Daughter Card #1)

4.4 Daughter Card #2 (DIR: LC89052T and DIT: DIT4096)

Table 4-6 lists the connector references for the second DEM-DAI1774 EVM daughter card.

Table 4-6. Analog Input and Output—Daughter Card #2

Connectors	Analog Input and Output of Daughter Card #2
SW001	Toggle switch. Opt/Coax selector for S/PDIF input
SW002	Toggle switch. Reset/Power-down LC89052T and DIT4096
SW003	Clock source selection for LC89052T (Onboard crystal oscillator or external source from CN306 of motherboard)
SW004	DIP switch. Sets channel-status data of the DIT4096(1). Note that the OFF state of this switch sets a HIGH level. Channel-status data can be set up if needed. It is also possible to connect a microcontroller.
SW005	DIP switch. Sets the DIT4096 system clock and data format. Note that the OFF state of this switch sets a HIGH level.

(1) See the DIT4096 product data sheet (TI literature number SBOS225, available for download from the TI web site) for further information.

Table 4-7 describes the audio clock and data control format options for Daughter Card #2.

Table 4-7. Audio Clock and Input Data Control Format—Daughter Card #2

CLK0	CLK1	System Clock
L	L	Not used
L	H	$256f_S$ (initial setting)
H	L	$384f_S$
H	H	$512f_S$
FMT0	**FMT1**	**Input Data Format**
L	L	24-bit, left-justified, MSB-first
L	H	24-bit, I^2S (initial setting)
H	L	24-bit, right-justified, MSB-first
H	H	16-bit, right-justified, MSB-first

Evaluation and Measurements

This chapter discusses how to set up jumpers on the DEM-DAI1774 EVM motherboard for performance evaluation in both slave mode and master mode using the Audio Precision SYS-2722® or PSIA-2722® audio analyzers. (The PSIA-2722 is the programmable serial interface adapter that connects the Audio Precision 2700 series and enables connections directly to the ADC and DAC devices.) The process of measuring dynamic characteristics is then presented, along with example characteristic data.

Topic **Page**

5.1 Slave Mode With Audio Precision SYS-2722 (Default Setting)

These jumper configurations for the DEM-DAI1774 EVM motherboard are the default device settings. Simple evaluation using the Audio Precision SYS-2722 (as shown in Figure 5-1) is easily accomplished. Connect the S/PDIF input and output to an optical cable at jacks U302 and U301 (for a coaxial cable, use jacks CN302 and CN301, respectively). For optical cable connections, select switch SW301; for a coaxial cable connection, select switch SW302.

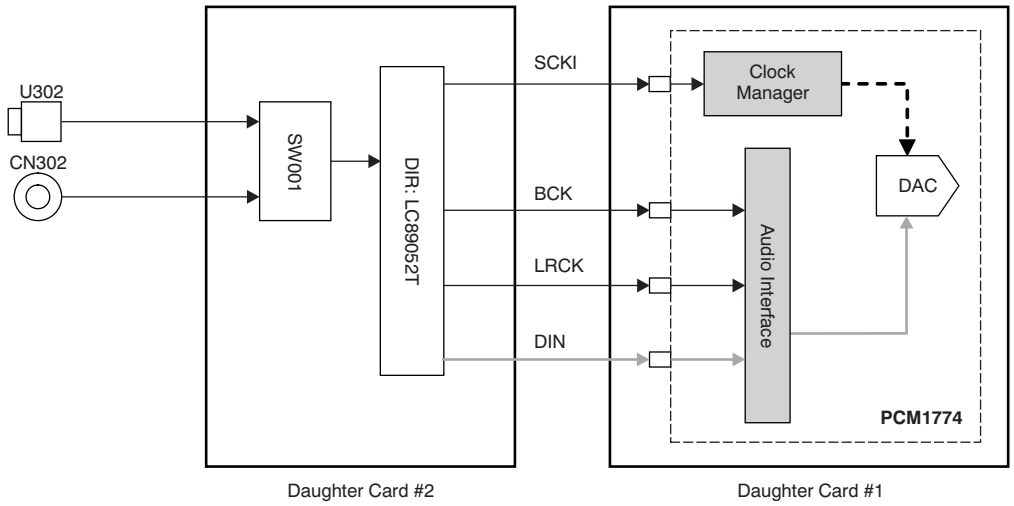


Figure 5-1. Slave Mode Configuration With SYS-2722

To put the DEM-DAI1774 EVM motherboard into the default slave mode configuration, refer to the jumper combination shown in Figure 5-2.

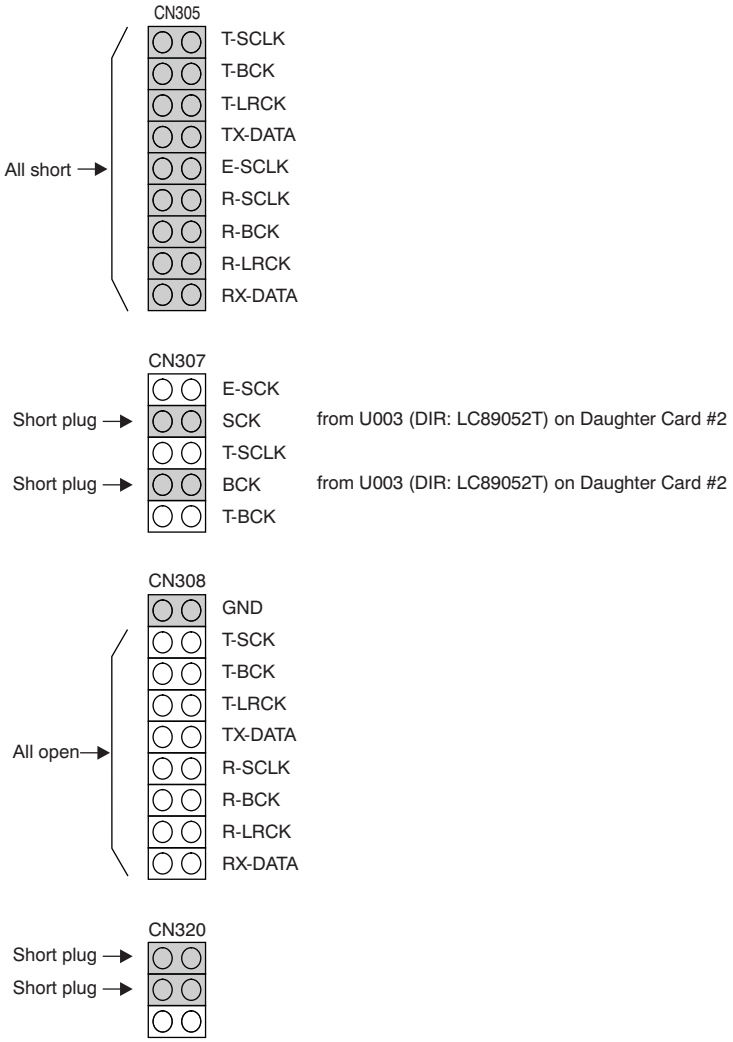


Figure 5-2. Jumper Configuration for Slave Mode (Default)

5.2 Master Mode with Audio Precision SYS-2722

To enable the DEM-DAI1774 EVM motherboard for use in Master mode, the path of the S/PDIF input to the PCM1774 through DIR is not available for use. LRCK and BCK change the respective output states at the PCM1774 side in master mode; the respective jumpers of R-BCK, R-LRCK, and RX-DATA should be removed from CN305 to avoid conflict between the input and output of these clocks.

Furthermore, in this situation, DIN to the PCM1774 is also invalid because the DIR LC89052T does not receive clocks (the LC89052T cannot work in slave mode). Therefore, any analog output from the DAC is invalid because there is no data input.

However, in this configuration, users ***can*** confirm master mode operation of both LRCK and BCK from the PCM1774 with a digital oscilloscope. Users can easily identify master mode without the use of other external equipment such as the PSIA-2722 analyzer.

The PCM1774 has no integrated internal PLL. However, the clock manager function can provide LRCK (f_S) and BCK in master mode, as illustrated in Figure 5-3.

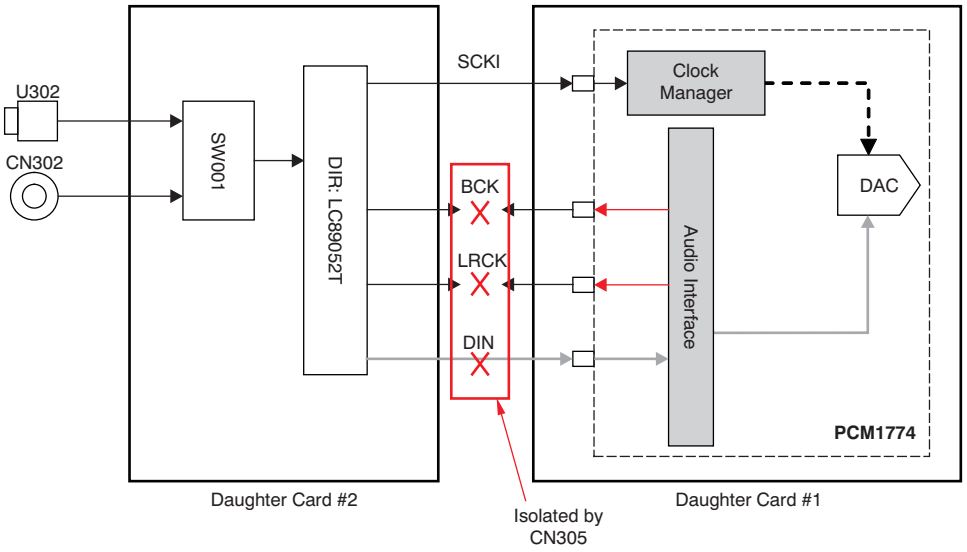


Figure 5-3. Master Mode Configuration With SYS-2722

Refer to the jumper combination shown in Figure 5-4 to put the DEM-DAI1774 EVM motherboard into master mode configuration.

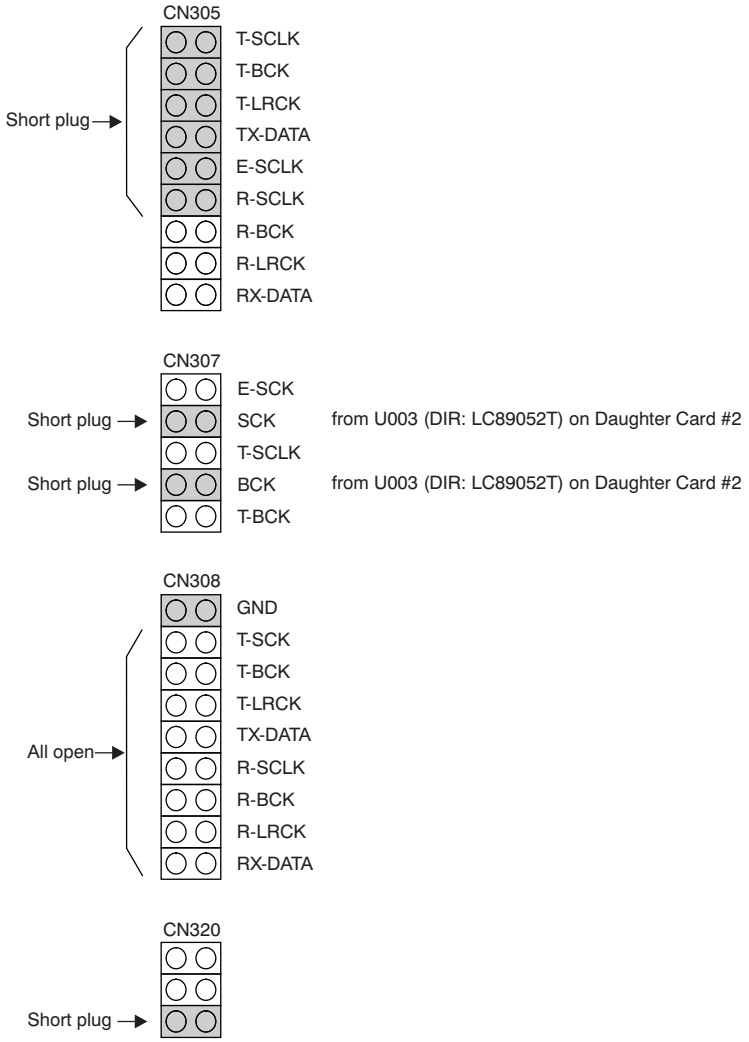


Figure 5-4. Jumper Configuration for Master Mode

5.3 Combined Master and Slave Modes With PSIA-2722

As shown in Figure 5-5, the DEM-DAI1774 EVM can provide evaluation for both slave and master modes of the PCM1774 at the same time without setup jumpers on the motherboard if the user has access to the PSIA-2722 analyzer.

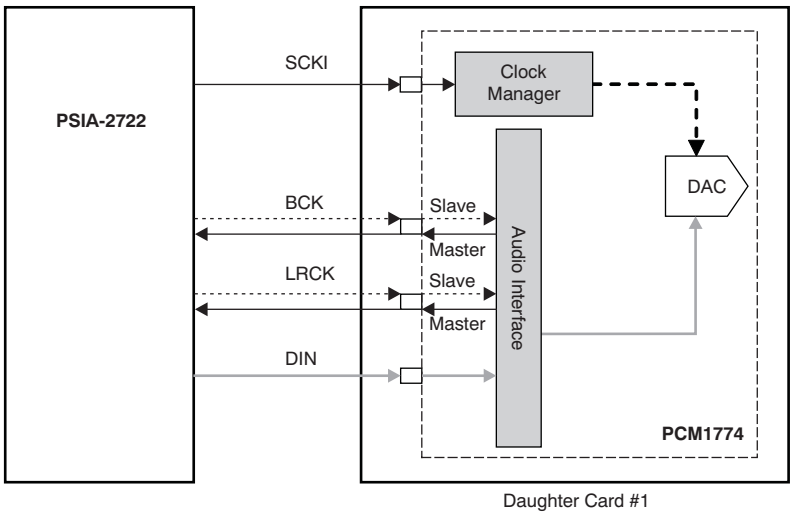


Figure 5-5. Combined Master and Slave Mode Configuration with SYS-2722

Refer to the jumper combination shown in Figure 5-6 to set up the combined master and slave modes configuration.

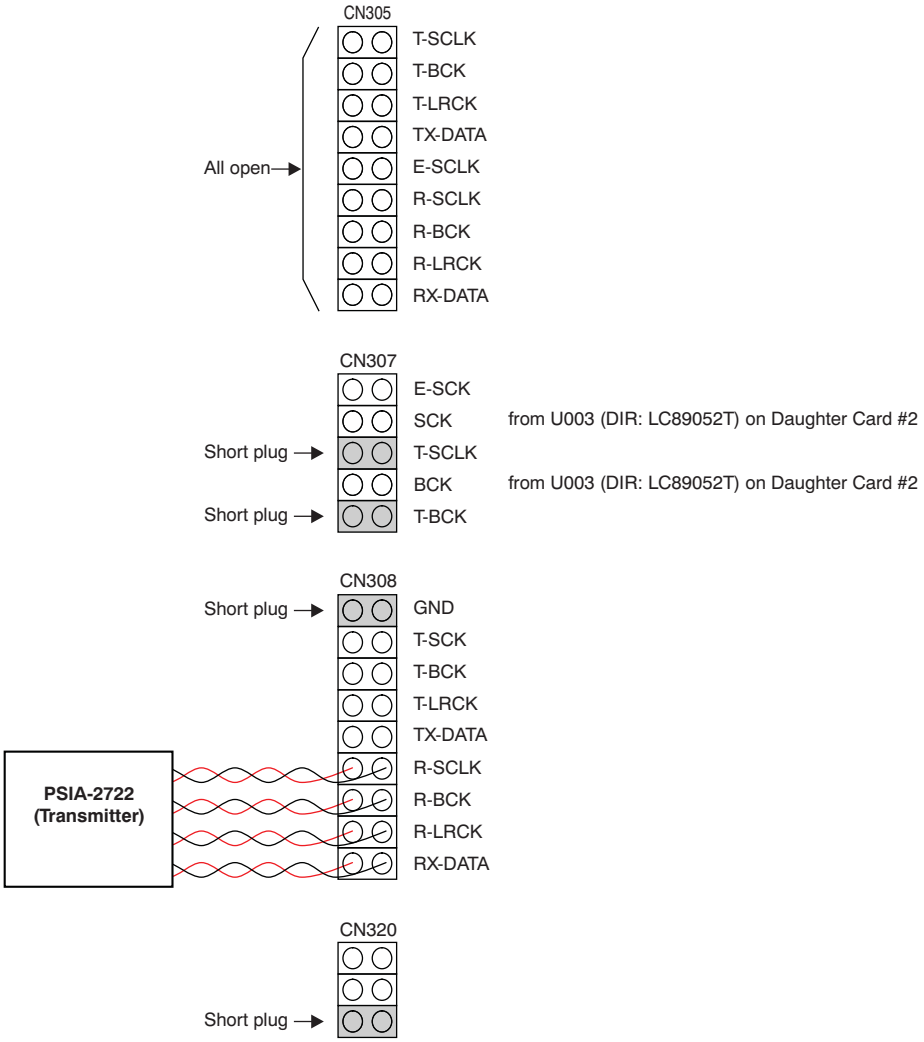


Figure 5-6. Jumper Configuration for Combined Master and Slave Modes

5.4 Measurements for Dynamic Characteristics

Typical dynamic performance graphs for digital-to-analog converters (DACs) generally represent four performance characteristics (in addition to other specifications): total harmonic distortion and noise (THD+N); signal-to-noise ratio (SNR); dynamic range (DR); and channel separation. These graphs also specify the test environment and measurement conditions required in order to meet typical performance values defined in the product data sheet.

For the DEM-DAI1774 EVM, the evaluation environment specifications are:

- Equipment used: Audio Precision, System Two Cascade
- Audio Data format: 16-bit Left-Justified
- SCKI / BCK / LRCK (f_S): $256f_S$ / $64f_S$ / 48 kHz
- Power supply: $V_{DD} = V_{IO} = V_{CC} = V_{HP}$ = 3.3 V (Regulated down from 10 V applied to the motherboard)
- Temperature: Room/ambient

Once the lab or test environment is configured according to these parameters, start the EVM software (as discussed in Section 3.2). Click *All Power On* in the startup window or execute *power_on.csv*, and then execute the .csv file that corresponds to the appropriate measurement path discussed in the subsequent sections of this chapter.

The PCM1774 (U2) is soldered onto Daughter Card #1, DEM-PCM1870RHF/1774RGP-A. .CSV files bundled with the EVM kit are available to measure dynamic performance. These .csv files will help users determine the appropriate register settings for the PCM1774 under various conditions. Appendix A of this user guide also includes a block diagram that corresponds to each respective .csv file.

5.4.1 Digital-to-Analog (D/A) Performance

Measurement path: 01.01.Line Output and Headphone Output
.csv file: 01_DAC_Line_Output_and_Headphone_Output.csv

Table 5-1. Line Output Parameters

Power Supply	Parameter	Filter Setting	R_L	Left Channel	Right Channel
3.3 V	THD+N (0 dBFS at 1 kHz)	400 Hz—20 kHz AES-17	10 kΩ	0.008%	0.009%
	SNR (BPZ input)	22 Hz—20 kHz SPCL + A-weighting	10 kΩ	93.3 dB	93.2 dB
	DR (–60 dBFS input)	22 Hz—20 kHz SPCL + A-weighting	10 kΩ	93.4 dB	93.1 dB
	Channel Separation (BPZ input for target channel)	22 Hz—20 kHz AES-17	10 kΩ	90.5 dB	90.7 dB

Table 5-2. 16-Ω Headphone Output Inserted to Headphone Jack J3 Parameters

Power Supply	Parameter	Filter Setting	R_L	Left Channel	Right Channel
3.3 V	THD+N (40 mW; HP volume: –1 dB)	400 Hz—20 kHz AES-17	16 Ω	0.026%	0.025%
	SNR (BPZ input)	22 Hz—20 kHz SPCL + A-weighting	16 Ω	93.0 dB	89.8 dB
	DR (–60 dBFS input)	22 Hz—20 kHz SPCL + A-weighting	16 Ω	93.1 dB	93.0 dB
	Channel Separation (BPZ input for target channel)	22 Hz—20 kHz AES-17	16 Ω	84.6 dB	84.3 dB

To obtain the performance results shown in Table 5-1, the other functions should be set with these parameters:

- Volume: 0 dB
- R_L: 10 kΩ for line output
- R_L: 16 Ω inserted to headphone jack J3 for headphone output
- All PGA: 0 dB

The bundled .csv file automatically sets the device to these conditions.

Please note that the headphone volume should be changed from 0 dB to –1 dB and the signal input level of the Audio Precision signal analyzer configured to meet the 40-mW target output power when THD+N is measured at 16 Ω.

See Appendix A for a signal flow block diagram.

5.4.2 Amplitude Versus Frequency Performance

Measurement path: 01.Line Output and Headphone Output

.csv file: 01_DAC_Line_Output_and_Headphone_Output.csv

Note that an unweighted filter and an AES-17 bandwidth of 22 Hz to 20 kHz should be set to obtain precise spectrum results.

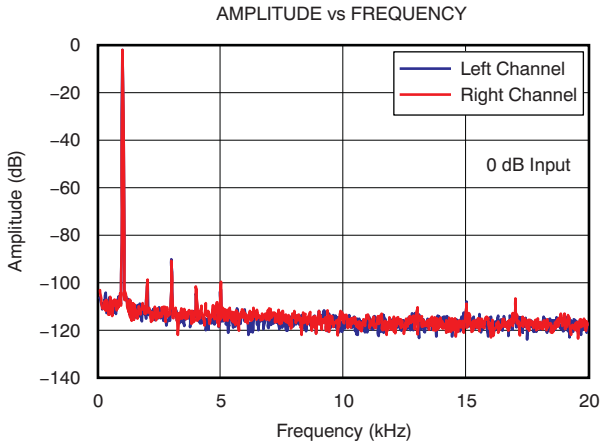


Figure 5-7. DAC Amplitude vs Frequency Result: 0 dB Input

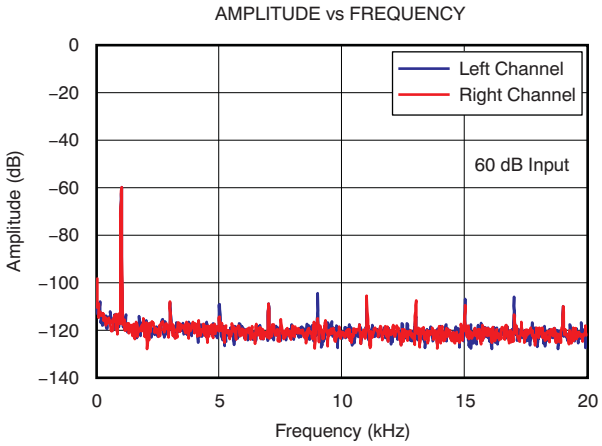


Figure 5-8. DAC Amplitude vs Frequency Result: –60 dB Input

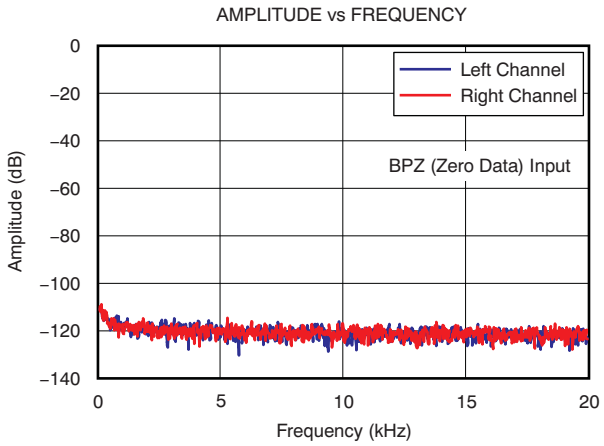


Figure 5-9. DAC Amplitude vs Frequency Result: BPZ (Zero Data) Input

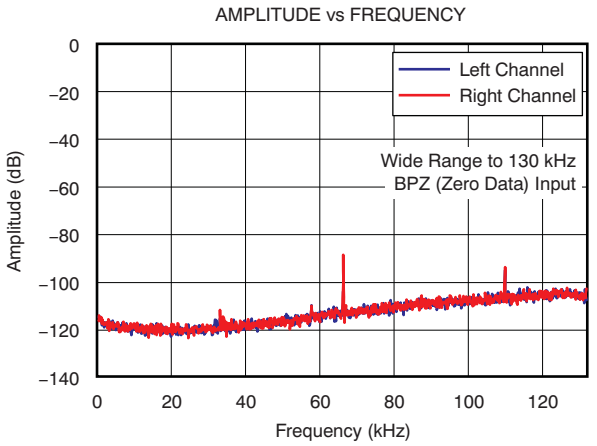


Figure 5-10. DAC Amplitude vs Frequency Result: Wide Range to 130 kHz, BPZ (Zero Data)

See Appendix A for a signal flow block diagram.

5.5 Connection Diagram for Practical Applications

The PCM1774 Daughter Card has been configured to measure dynamic audio performance by audio standard analyzer equipment.

In a practical application (such as a portable audio player or cellular phone), simple components set up as shown in Figure 5-11 will be reasonable to save assembly and test spaces. Specific component values are listed in Table 5-3.

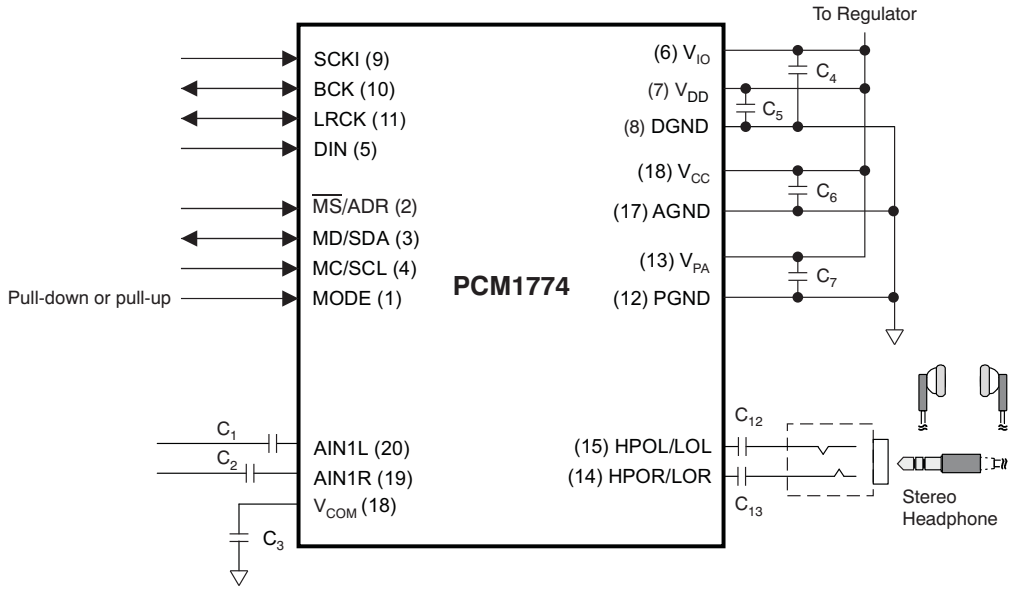


Figure 5-11. Basic Connection Diagram

Table 5-3. Recommended External Parts for Basic Connection Diagram

Component	Recommended Value	Component	Recommended Value
C_1, C_2	1 µF	C_5, C_6, C_7	1 µF to 4.7 µF
C_3	1 µF to 4.7 µF	C_9, C_{10}	10 µF to 220 µF
C_4	0.1 µF		

Schematic, PCB Layout, and Bill of Materials

This chapter provides the electrical and physical layout information for the DEM-DAI1774 EVM. The bill of materials is included for component and manufacturer reference.

Topic **Page**

6.1 Schematics

Figure 6-1 and Figure 6-2 illustrate the schematics for the DEM-DAI1774 EVM.

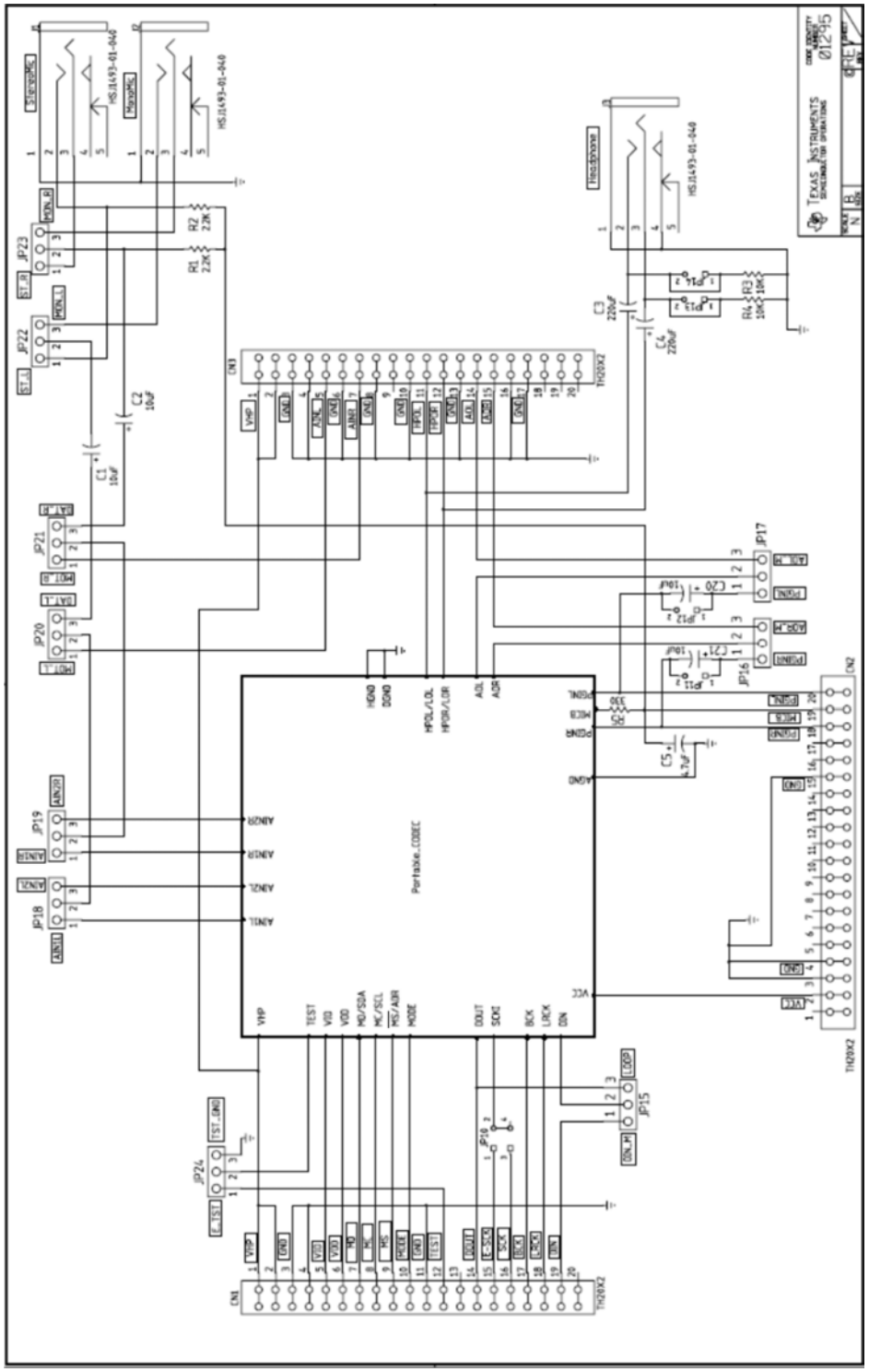


Figure 6-1. DEM-PCM1870RHF/1774RGP-A Part 1 (Daughter Card #1)

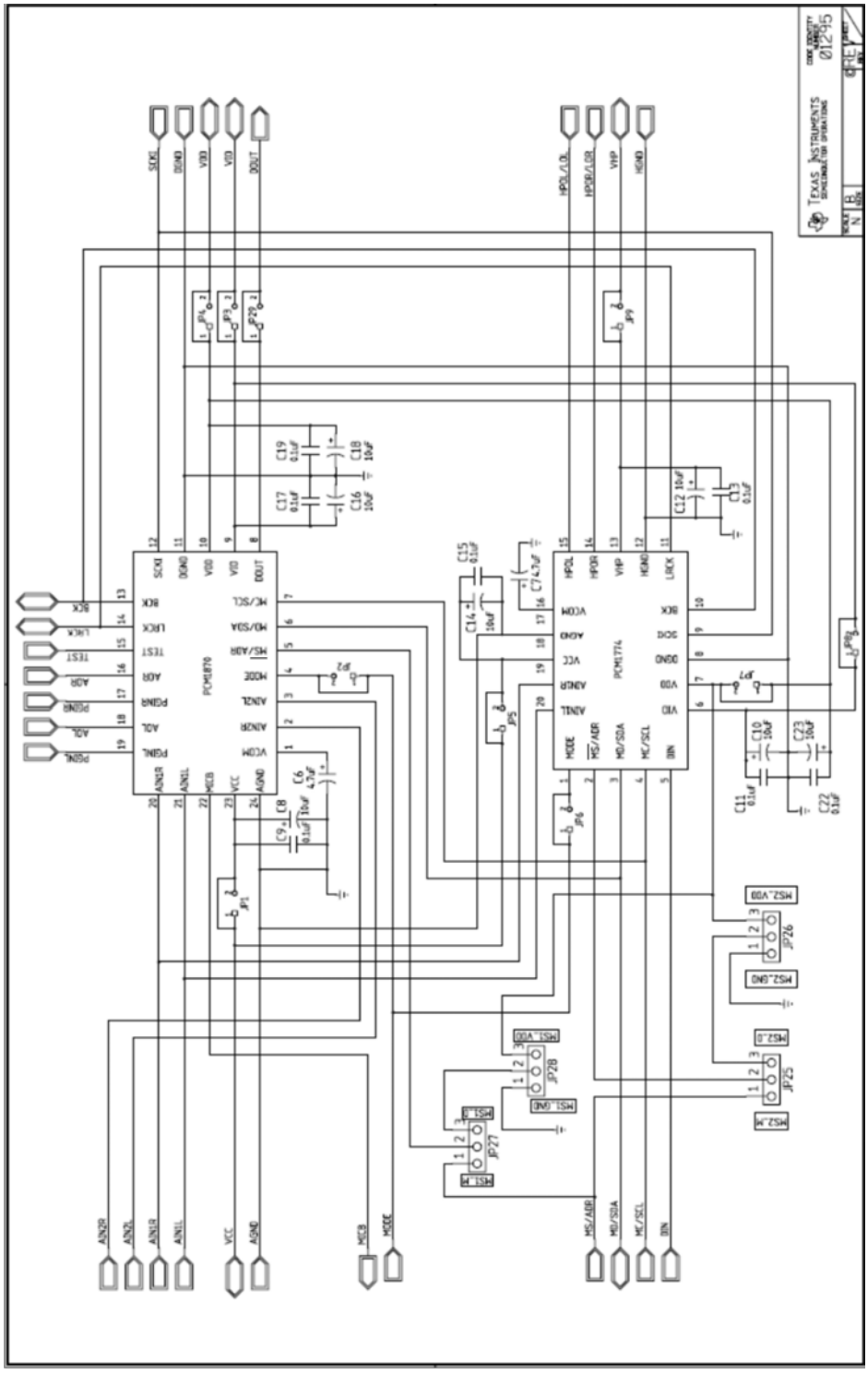


Figure 6-2. DEM-PCM1870RHF/1774RGP-A Part 2 (Daughter Card #1)

6.2 Printed Circuit Board Layout

Figure 6-3 through Figure 6-7 illustrate the printed circuit board (PCB) layout for the DEM-DAI1774 EVM.

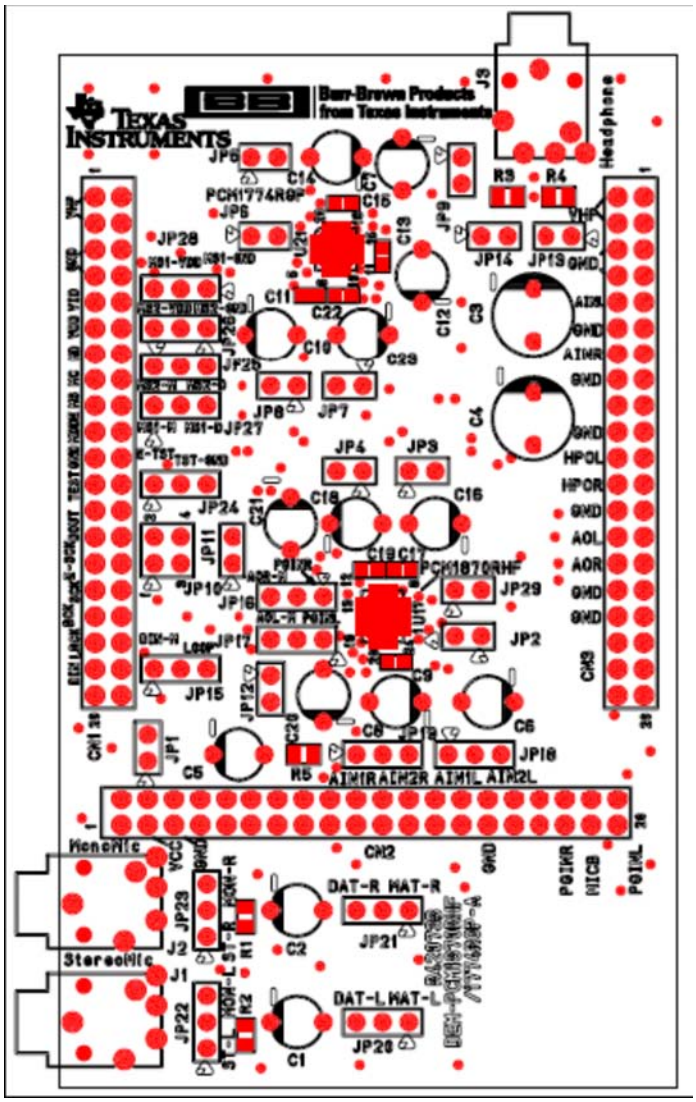


Figure 6-3. DEM-PCM1870RHF/1774RGP-A Board Layout—Silkscreen Side

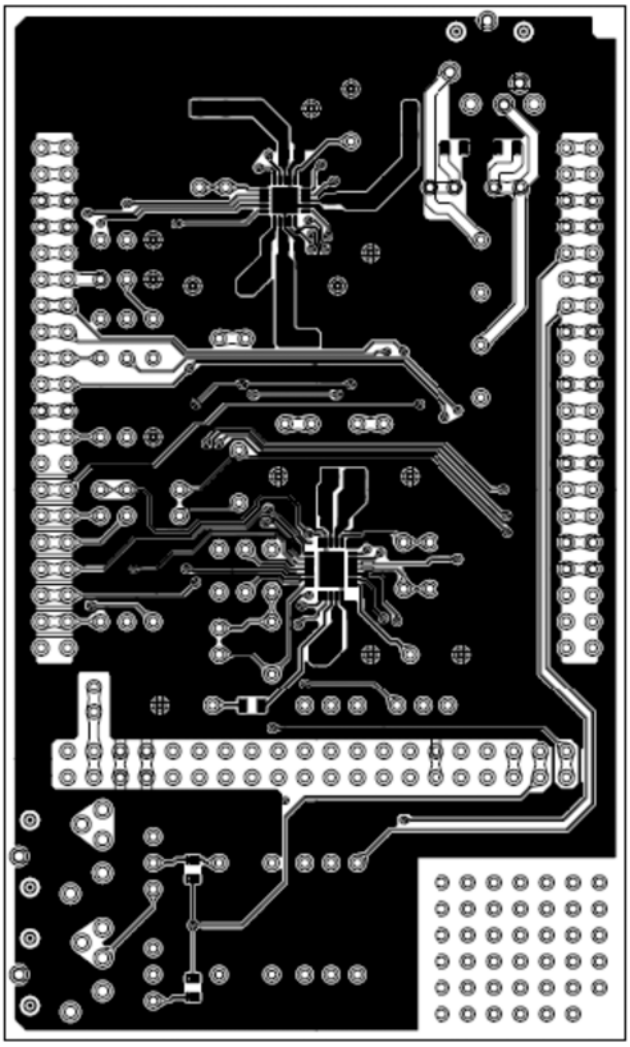


Figure 6-4. DEM-PCM1870RHF/1774RGP-A Board Layout—Component Side

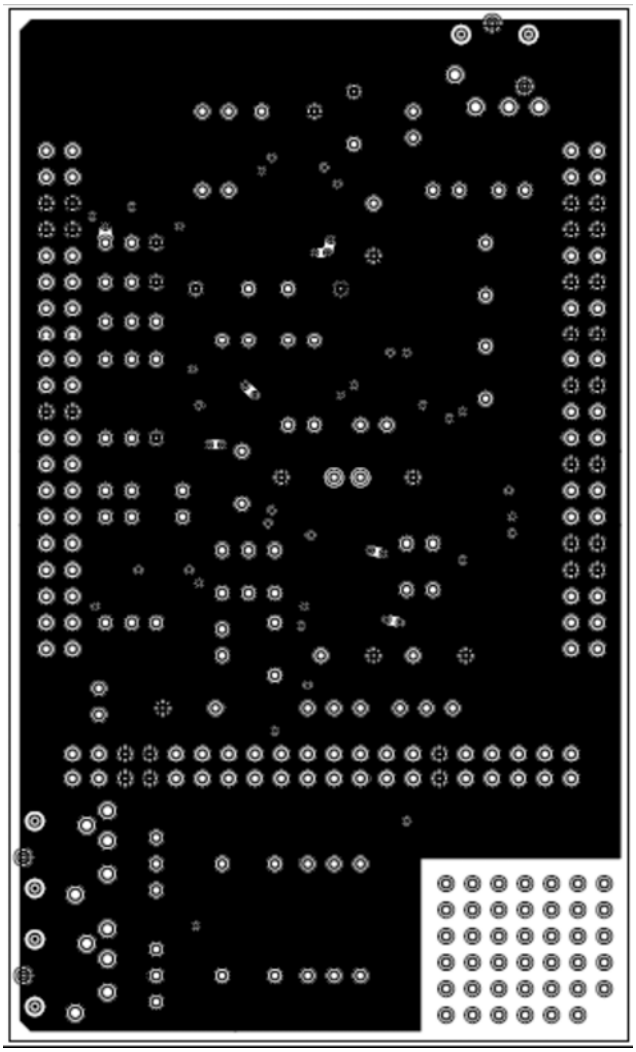


Figure 6-5. DEM-PCM1870RHF/1774RGP-A Board Layout—Inner Layer 2

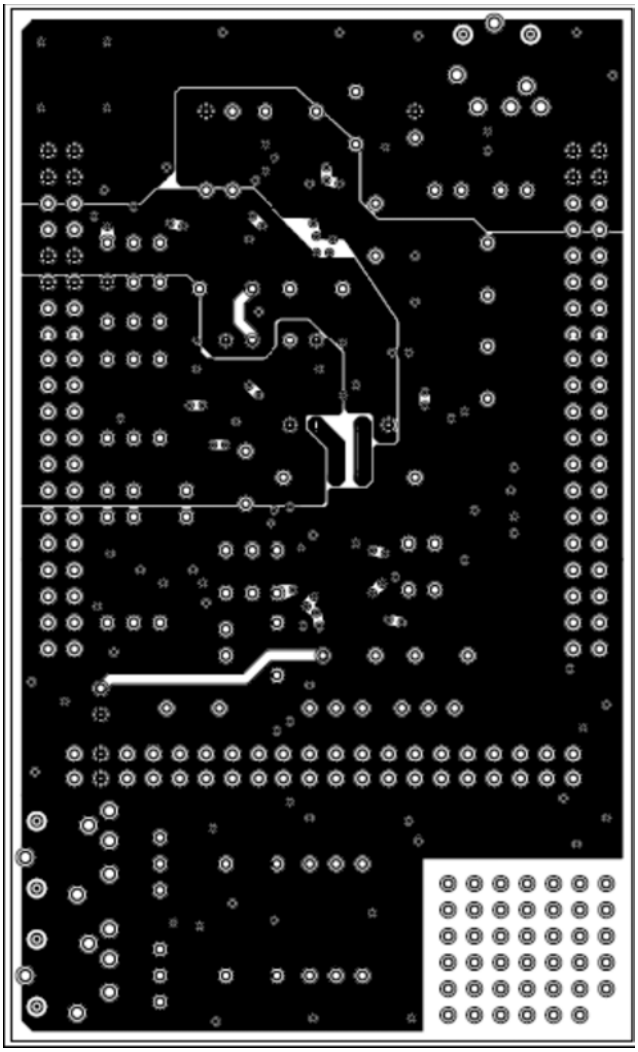


Figure 6-6. DEM-PCM1870RHF/1774RGP-A Board Layout—Inner Layer 3

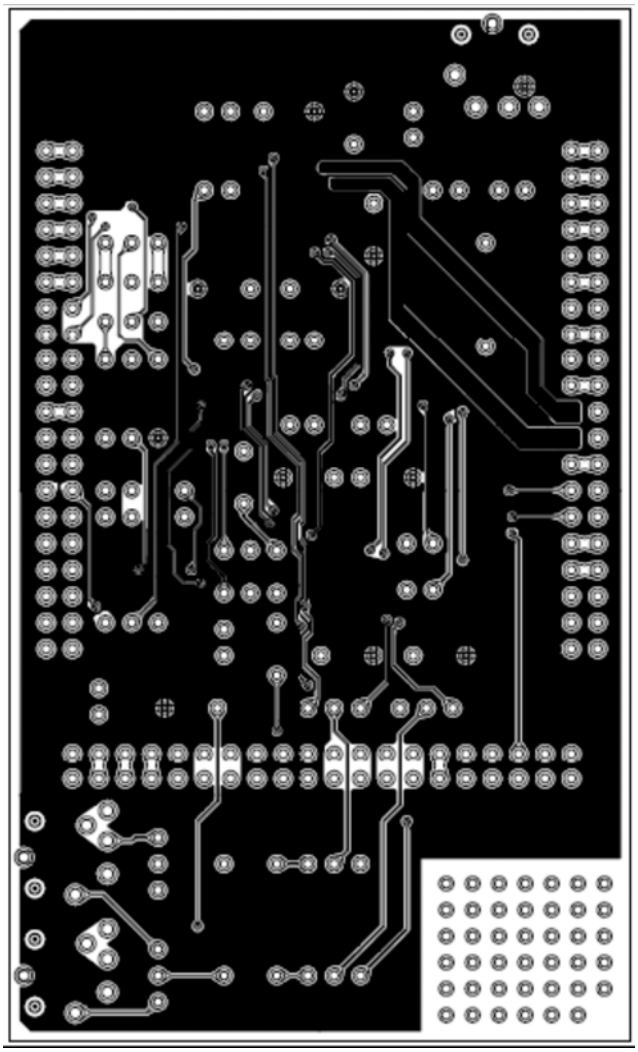


Figure 6-7. DEM-PCM1870RHF/1774RGP-A Board Layout—Solder Side

6.3 Component List

Table 6-1 lists the Bill of Materials for the DEM-DAI1774 EVM.

Table 6-1. Bill of Materials(1)

Reference Designator	Quantity	Description
R3, R4	2	10 kΩ, Rohm, MCR10EZHJ103
C11, C13, C15, C22	4	0.1 µF, Murata, GRM188R71H104Z
C10, C12, C14, C23	4	10 µF, Nippon Chemi-con, EKMG160ELL100ME11D
C7	1	4.7 µF, Nippon Chemi-con, EKMG500ELL4R7ME11D
C3, C4	2	220 µF, Nippon Chemi-con, EKMG350ELL221MHB50
JP10	1	OMRON, 2-Pin, XJ8C-0411
JP15, JP18, JP19, JP20, JP21, JP25, JP26	7	OMRON, 3-Pin, XJ8B-0311
J3	1	HOSIDEN, HSJ1493-01-040
U2	1	16-bit Stereo Audio DAC, 4×4 mm QFN 20-pin, Texas Instruments, PCM1774

(1) This list is specifically related to the PCM1774 components.

Reference .csv Files, Interfacing to DSPs, and Package Information

Topic Page

A.1 Reference .csv Files

The .csv files are bundled with the DEM-DAI1774 EVM Controller. These files enable users to execute register settings corresponding to the specific operating modes discussed in the product data sheet by importing them into the software.

Note that each .csv file (listed in Table A-1) must be implemented ***after*** an *All Active* operation is performed with the *power_on.csv* command; otherwise, these files will not work properly.

An *All Active* operation is recommended to start up the device, and can be executed by just clicking the *All Power On* button, as discussed in Section 3.2.

Table A-1. .CSV Files

Operating Mode		.CSV File Name
All Power Down		power_off.csv
All Active		power_on.csv
Playback with Digital Input		
01	Line Output or Headphone Output	01_DAC_Line_Output_and_Headphone_Output.csv
02	Headphone Output with Sound Effect	02_DAC_Headphone_Output_with_Sound_Effect.csv
03	Headphone Output with Line Input (AIN1L/AIN1R)	03_DAC_Headphone_Output_with_Line_Input.csv
04	Headphone Output with Mono Mic Input (AIN1L, +20 dB)	04_DAC_Headphone_Output_with_Mono_Mic_Input.csv
Playback without Digital Input		
05	Line Input (AIN2L/AIN2R) to Headphone Output	05_Line_Input_to_Headphone_Output.csv
06	Mono Mic Input (AIN1L, +20 dB) to Headphone Output	06_Mono_Mic_Input_to_Headphone_Output.csv

A.1.1 Related Signal Flow Diagrams

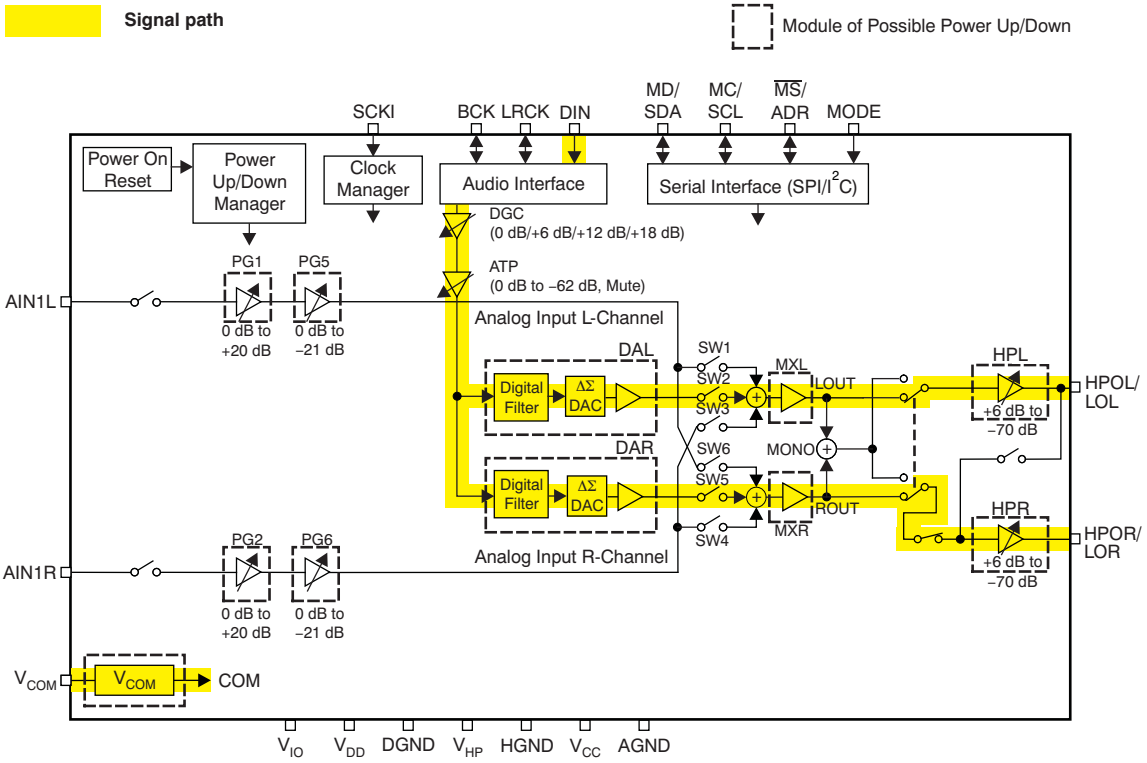


Figure A-1. Line Output or Headphone Output

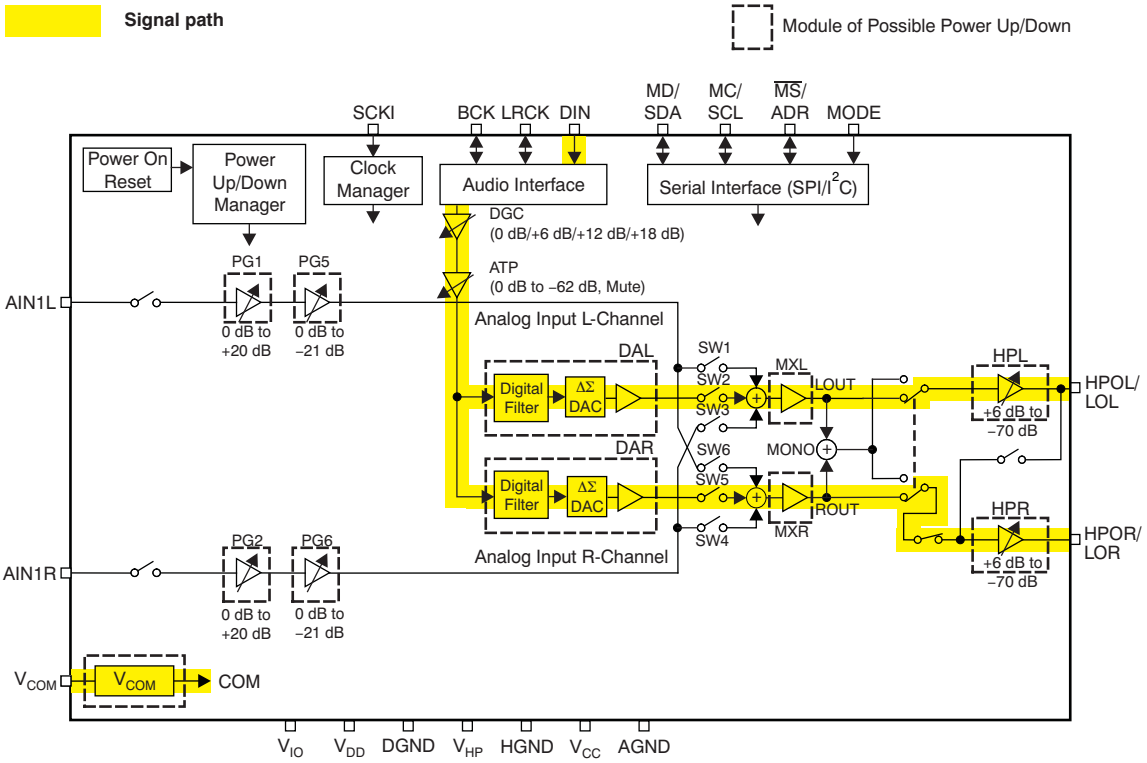


Figure A-2. Headphone Output with Sound Effects

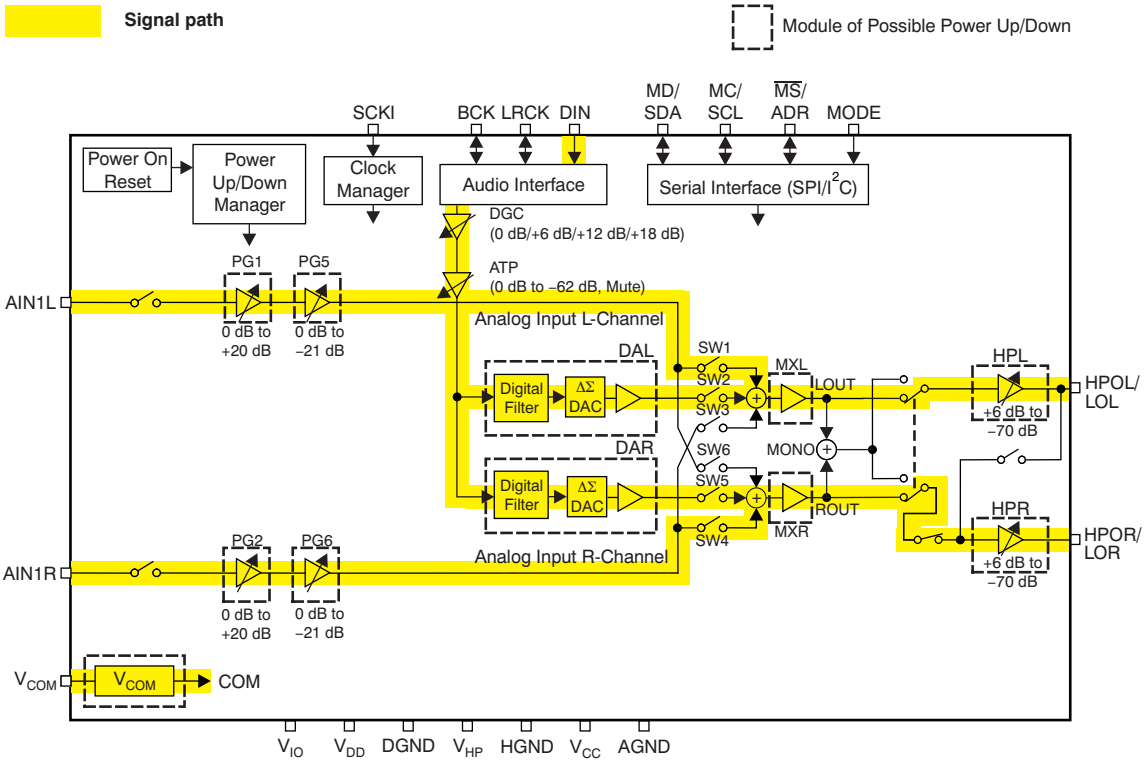


Figure A-3. Headphone Output with Line Input (AIN1L/AIN1R)

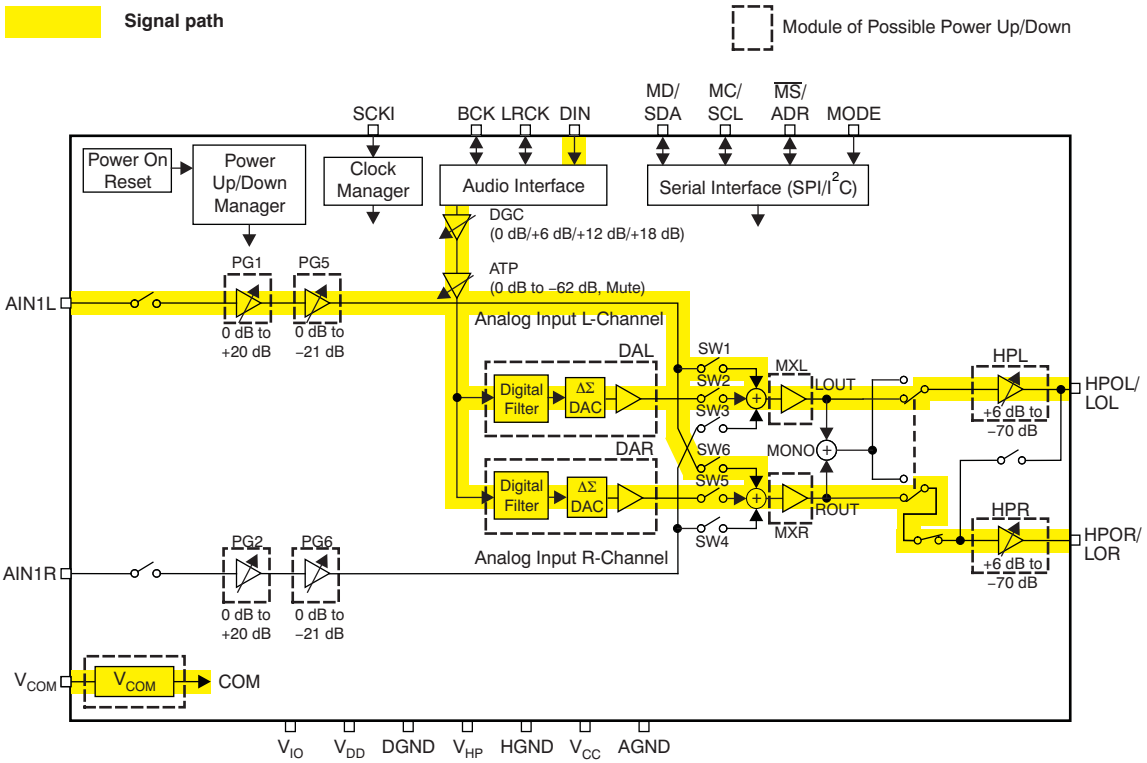


Figure A-4. Headphone Output with Mono Mic Input (AIN1L, +20 dB)

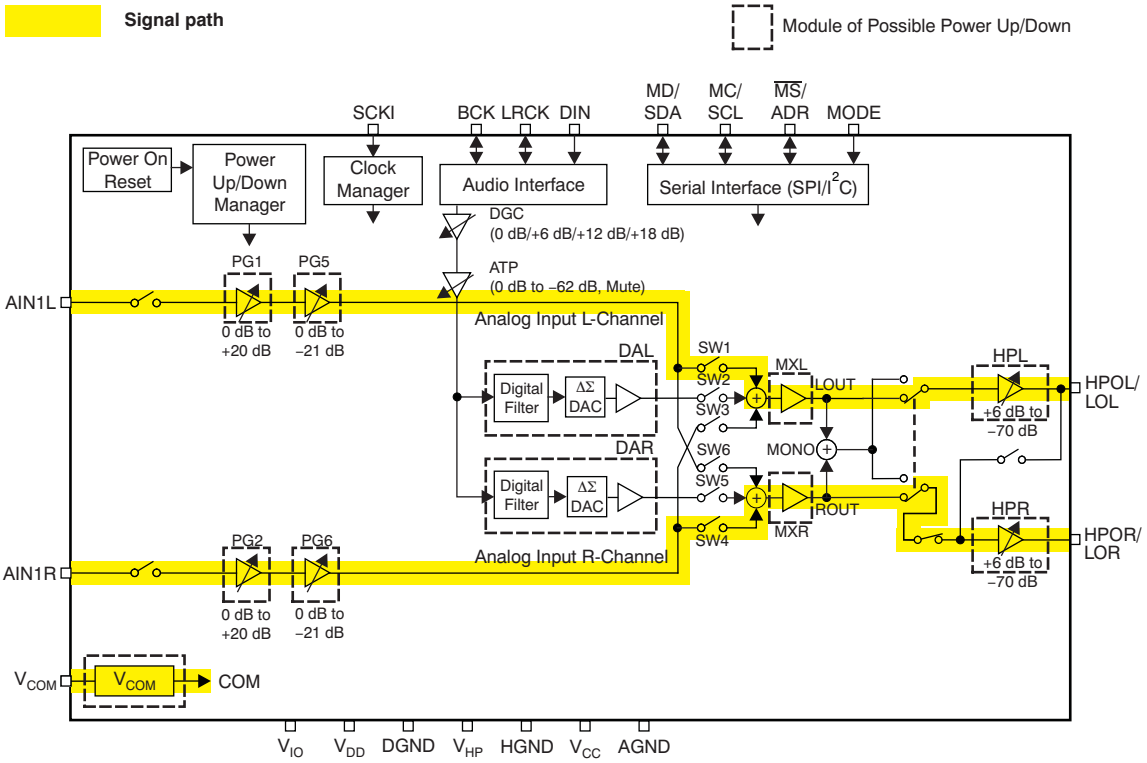


Figure A-5. Line Input (AIN1L/AIN1R) to Headphone Output

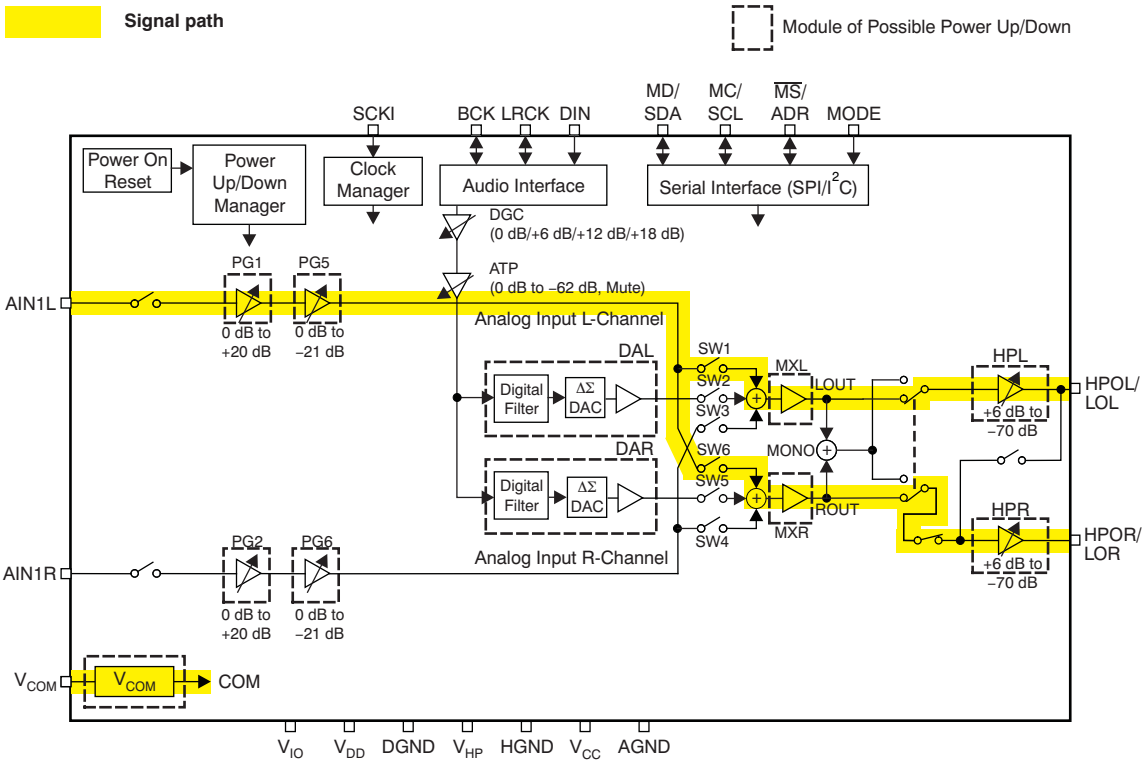


Figure A-6. Mono Line Input (AIN1L) to Headphone Output

A.2 Interfacing to DSPs

Refer to the following examples for interfacing the PCM1774 to a digital signal processor (DSP) in either slave or master mode. To implement master mode, MSTR = 1 of register 84 (54h) enables master mode operation as discussed in the product data sheet. Insert 5440h to the recommended power-on sequence after DAC power-up (49h) of the PCM1774, as noted in Table A-2.

These conditions apply for both modes of operation as illustrated in Figure A-7 and Figure A-8:

- SCKI: Audio Clock ($256f_S/384f_S$)
- BCK:Clock for Audio Transfer ($32f_S/48f_S/64f_S$ in I^2S, LJ, and RJ; $32f_S/48f_S/64f_S/128f_S/256f_S$ in DSP)
- LRCK: Sampling Rate Clock (f_S)
- DIN: Audio Data Input for DAC (I^2S, LJ, RJ, DSP)
- DOUT: Audio Data Output from ADC (I^2S, LJ, RJ, DSP)

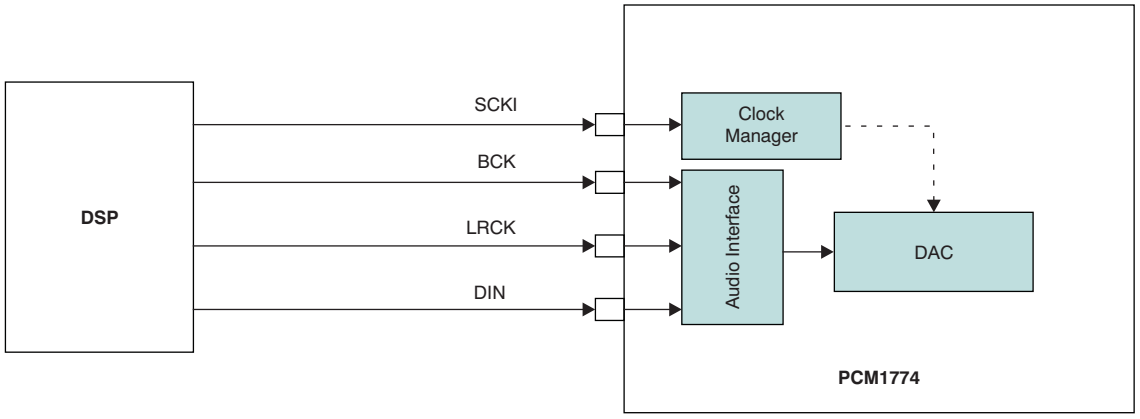


Figure A-7. Slave Mode Operation

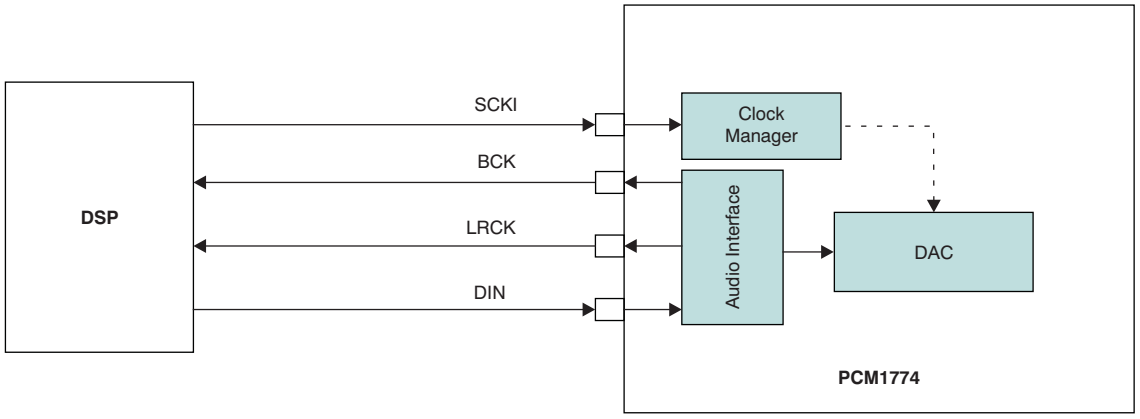


Figure A-8. Master Mode Operation

A.2.1 Register Control with DSP Interface

Table A-2 summarizes the recommended power-on sequence for the PCM1774. The shaded cells within the table indicate specific register settings that must be configured for the device to properly operate with a DSP interface.

Table A-2. Recommended Power-On Sequence for PCM1774

STEP	REGISTER SETTINGS	NOTE
1	–	Turn on all power supplies.(1)
2	4027h	Headphone amp L-channel volume (–6 dB)
3	4127h	Headphone amp R-channel volume (–6 dB)
4(2)	4427h	Digital attenuator L-channel (–6 dB)
5	4527h	Digital attenuator R-channel (–6 dB)
6	4620h	DAC audio interface format (left-justified)
7(3)	49E0h	DAC (DAL, DAR) and analog bias power-up
8(3)	5601h	Zero-cross detection enable
9	4903h	Analog mixer (MXL, MXR) power-up
10	5811h	Analog mixer input (SW2, SW5) select
11	4QFCh	Headphone amp (HPL, HPR, HPC) power-up
12	4A01h	V_{COM} power up
13	523Ch	Analog front-end (D2S, MCB, PG1, 2, 5, 6) power-up
14	5711h	Analog input (MUX3, MUX4) select; analog input (MUX1, MUX2) select

(1) V_{DD} should be turned on prior to or simultaneously with the other power supplies. It is recommended to set register data with the system clock input after turning all power supplies on.
(2) I^2S: 4620h; Left-Justified: 4601h; Right-Justified: 4602h; DSP: 4603h.
(3) Between steps 12 and 13, add this value for slave configuration: 5400h. For master configuration, add: 5440h.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of –2.0 V to +4.0 V and the output voltage range of –2.0 V to +4.0 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +60°C. The EVM is designed to operate properly with certain components above +60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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