



## ABSTRACT

This user's guide provides a walkthrough of hardware and software setup with supplemental images as a visual representation, followed by bringup steps.

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## 1 Introduction

This guide is intended to be used in conjunction with the document ID PC-004159-DC version 3 from Picocom.

This user's guide introduces a small cell application using Texas Instruments' AFE7769D evaluation module (EVM) in collaboration with Picocom, a semiconductor company that provides industry-standard systems on chips (SoCs) for small cell wireless infrastructure. This reference solution serves to help customers ramp system integration of the analog front-end (AFE), and allows for seamless interfacing with the Picocom PC802 system-on-chip (SoC).

The AFE7769D is a 4T4R2F RF-sampling transceiver with integrated digital pre-distortion (DPD) that serves to linearize power amplifiers (PA's) for improved wireless coverage to the end customer. The small cell 5-watt radio unit (RU) utilizes the EVM version of the device that connects with Picocom's component of the solution for seamless interfacing. The Picocom PC802 is a SoC that is designed for "5G NR/LTE small cell disaggregated and integrated RAN architectures", per Picocom's website.

## 2 Basic EVM Test Procedures

### 2.1 Safety

- Safety glasses must be worn.
- This test must be performed by qualified personnel trained in electronics theory and understand the risks and hazards of the assembly to be tested.
- ESD precautions must be followed while handling electronic assemblies while performing this test.
- Precautions should be taken to avoid touching areas of the assembly that may get hot or present a shock hazard during testing.
- No ESD wrist strap shall be worn for Hi Voltage testing ( $\Rightarrow$ 50 Vrms or  $\Rightarrow$ 75 VDC) use Ionizer.

### 2.2 Quality

Test data or reports are made available upon request by Texas Instruments.

### 2.3 Apparel

- Safety glasses
- Electrostatic smock
- Electrostatic gloves or finger cots
- Ground ESD wrist strap

### 2.4 Hardware and Software Requirements

#### 2.4.1 Test Equipment Required

- DC power supply at 5.5 V, 5A
- DC multimeter
- USB mini-B cable
- USB 3.0 cable
- PC with USB port
- Intel USB Blaster or USB Blaster II
- Signal generator
- 1:8 relay
- Spectrum analyzer
- BNC cables, splitter
- USB hub
- TSW14J58 Rev A5

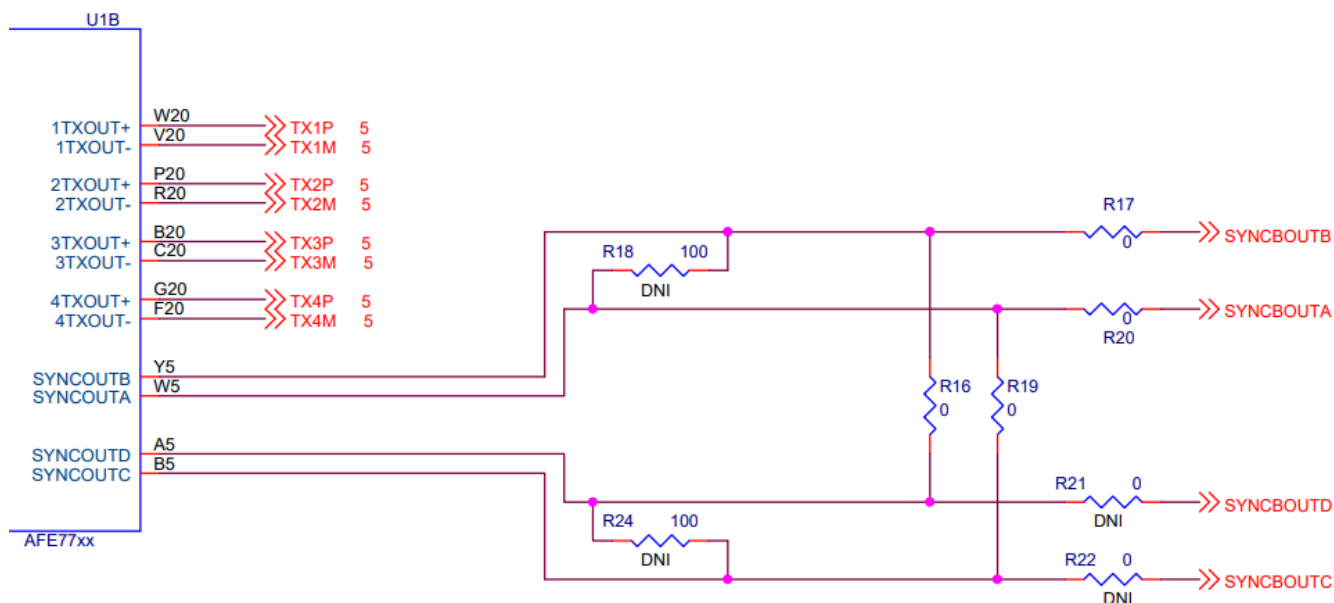
#### 2.4.2 Software Required

- AFE77xxD Latte v0.4

### 3 AFE7769DEVM Setup

#### 3.1 AFE7769D Hardware Changes

Make the following changes to the AFE7769DEVM to separate the SYNCOUT pins as shown in [Figure 3-1](#).



**Figure 3-1. Separating the SYNCOUT Pins**

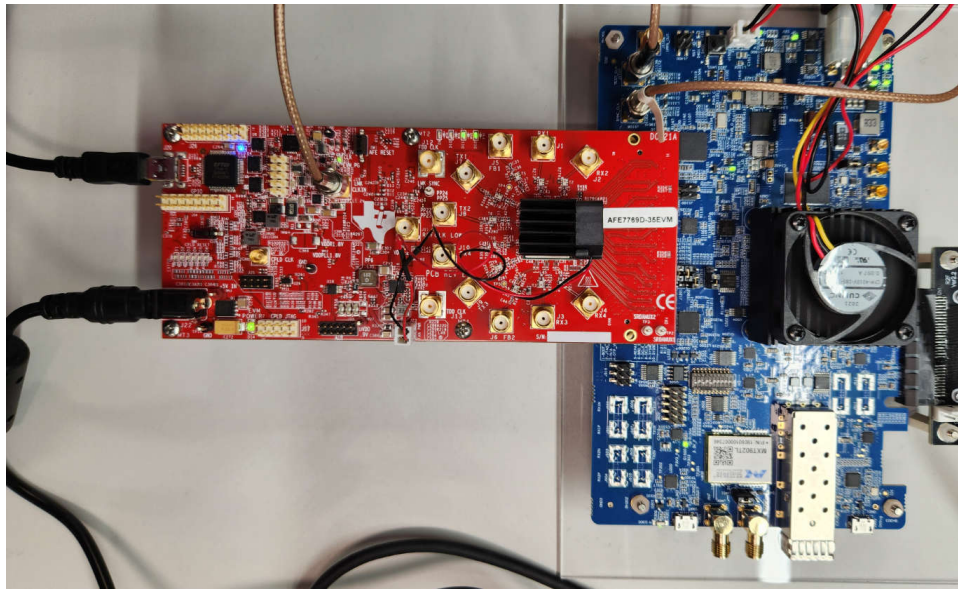
In conjunction to the schematic, see [Table 3-1](#) for the list of switches to make.

**Table 3-1. List of Pin Changes, AFE7769DEVM**

| AFE Reference Designator | Change From | Change To  |
|--------------------------|-------------|------------|
| R16                      | 0 $\Omega$  | DNI        |
| R19                      | 0 $\Omega$  | DNI        |
| R3                       | 0 $\Omega$  | DNI        |
| R5                       | 0 $\Omega$  | DNI        |
| R1                       | DNI         | 0 $\Omega$ |
| R2                       | DNI         | 0 $\Omega$ |
| R21                      | DNI         | 0 $\Omega$ |
| R22                      | DNI         | 0 $\Omega$ |

#### 3.2 AFE7769D Connections

- Connect the 5.5 V power supply to power jack connector (J22) of the AFE7769D EVM.
  - Check: D14 (POWER) LED should light up.
- Connect the USB Type Mini-B Cable from PC to the USB port (J20) of the AFE7769D EVM.
  - Check: D13 (USB\_PWR) LED should light up.
- Connect the AFE7769DEVM to the PC802 through the FMC connector.
- Connect the 122.88MHz reference clock (SYNC\_CLOCK) from the PC802 (J1106) to the LMK\_CLKIN (J19) of the AFE7769DEVM, as shown in [Figure 3-2](#).



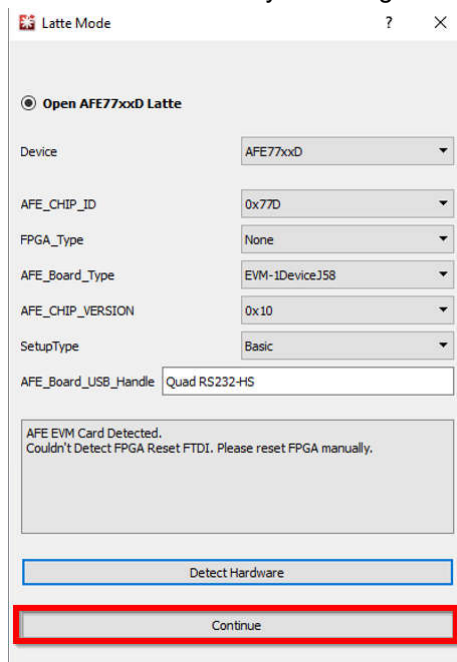
**Figure 3-2. Hardware Setup and Connections AFE7769DEVM-PC802**

### 3.3 AFE7769D Software Setup

1. Install the AFE77xxD Latte GUI from zipped folder called “V0p4.zip” in the TI drive.
2. After installing the AFE77xxD GUI, copy the PC802\_LMKDIV.py script and paste it under the following directory “...\Documents\Texas Instruments\AFE77xxDLatte\projects\AFE77xxD\AFE7769D”.
3. Copy the “AFE77xxD\_Picocom\_pc802\_K1L.xlsx” file and paste it under “\Documents\Texas Instruments\AFE77xxDLatte\lib\configs”.

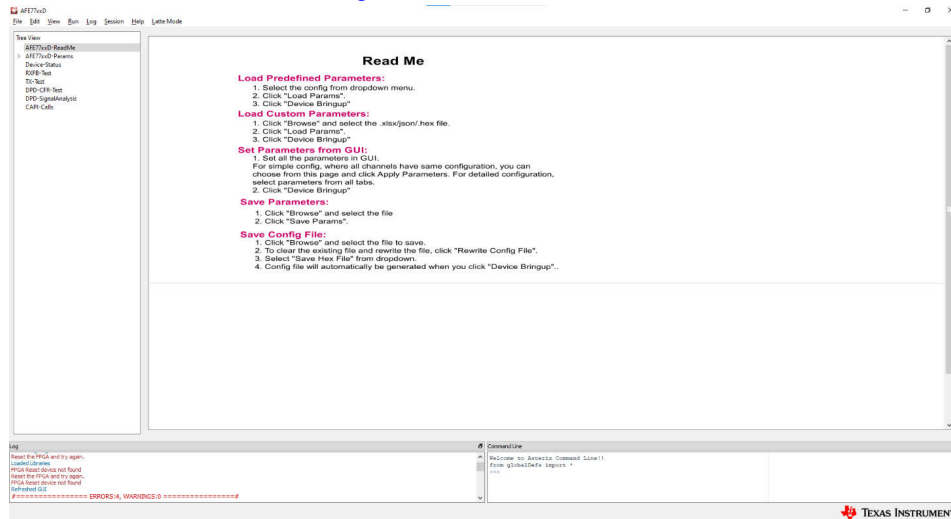
### 3.4 AFE7769D Programming Method 1: Automated

1. Open the AFE77xxD GUI version 0.4. Make sure it looks like [Figure 3-3](#), then click Continue. The “Couldn’t Detect FPGA Reset FTDI. Please reset FPGA manually.” message is expected and can be ignored.



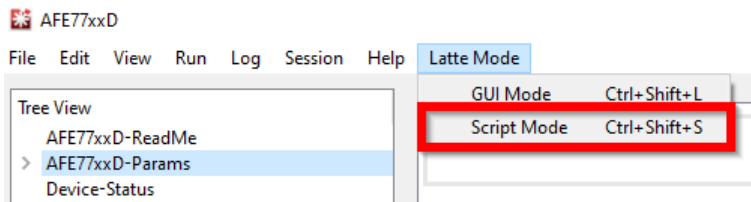
**Figure 3-3. Launching AFE77xxD Latte Software**

2. Wait until the GUI loads. It will look like [Figure 3-4](#).



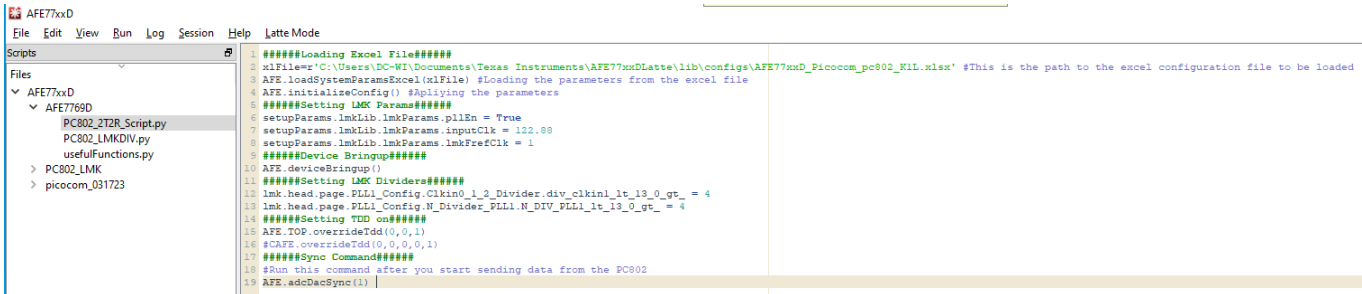
**Figure 3-4. ReadMe AFE77xxD Latte Software**

3. At the top, click on Latte Mode and navigate to Script Mode, as shown in [Figure 3-5](#).



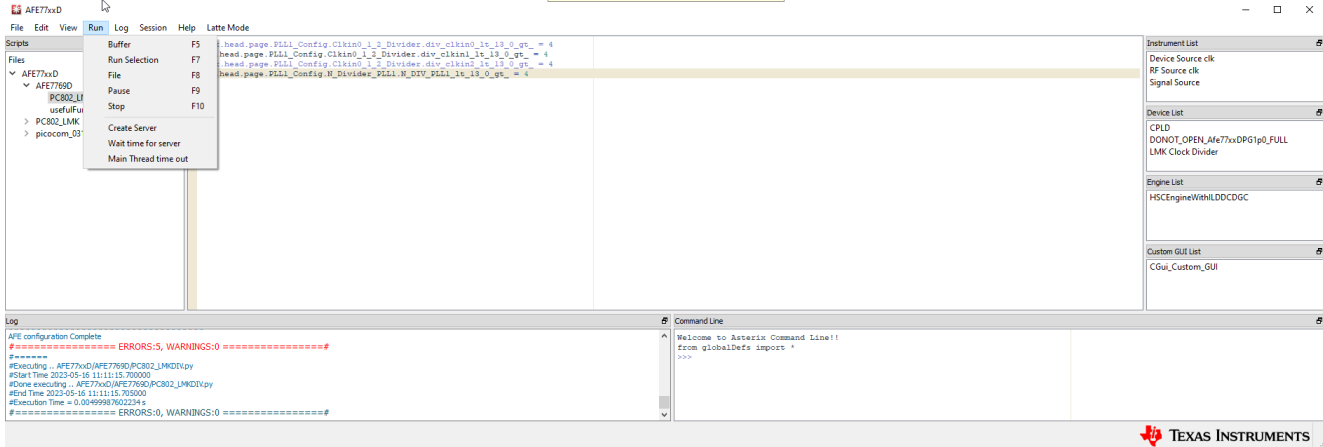
**Figure 3-5. Switching to Script Mode**

4. Open the PC802\_2T2R\_Script.py script on the tree view on the left as shown in [Figure 3-6](#).



**Figure 3-6. PC802 Script**

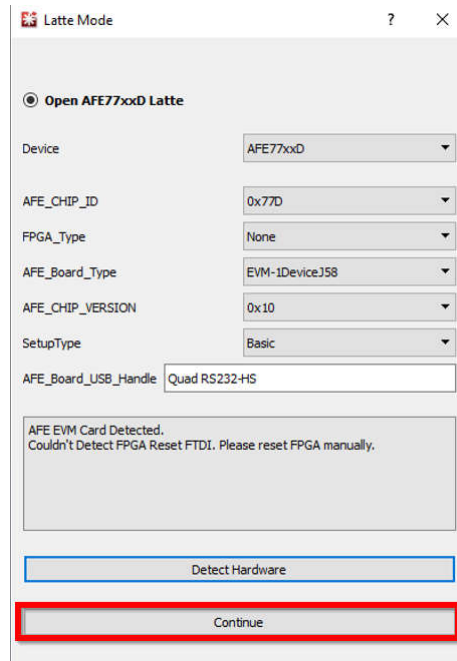
- Run the script by pressing F5 or by clicking Run > Buffer. You should see an output in the log window like that shown in [Figure 3-7](#) signaling the script was run with no errors. After running this script, the LMK\_LOCKED LED (D11) turns on if the 122.88 MHz reference from the PC802 is connected after programming the PC802.



**Figure 3-7. Running the PC802 Script**

### 3.5 AFE7769D Programming Method 2: Using GUI Mode

- Open the AFE77xxD GUI version 0.4. Make sure it looks like [Figure 3-8](#), then click Continue. The “Couldn’t Detect FPGA Reset FTDI. Please reset FPGA manually.” message is expected and can be ignored.



**Figure 3-8. Launching AFE77xxD Latte Software**

- Wait until the GUI loads. It will look like Figure 9. Click on “AFE77xxD-Device” tab under the tree view on the left for the main parameters screen.



Figure 3-9. ReadMe AFE77xxD Latte Software

- Click on “Browse” under “Load System Parameters” and select the “AFE77xxD\_Picocom\_pc802\_K1L.xlsx” config file under “\Documents\Texas Instruments\AFE77xxDLatte\lib\configs”. After selecting the file, click “LOAD”, and the screen should look like Figure 3-10. You should also see a message saying that the configuration was loaded in the log window.

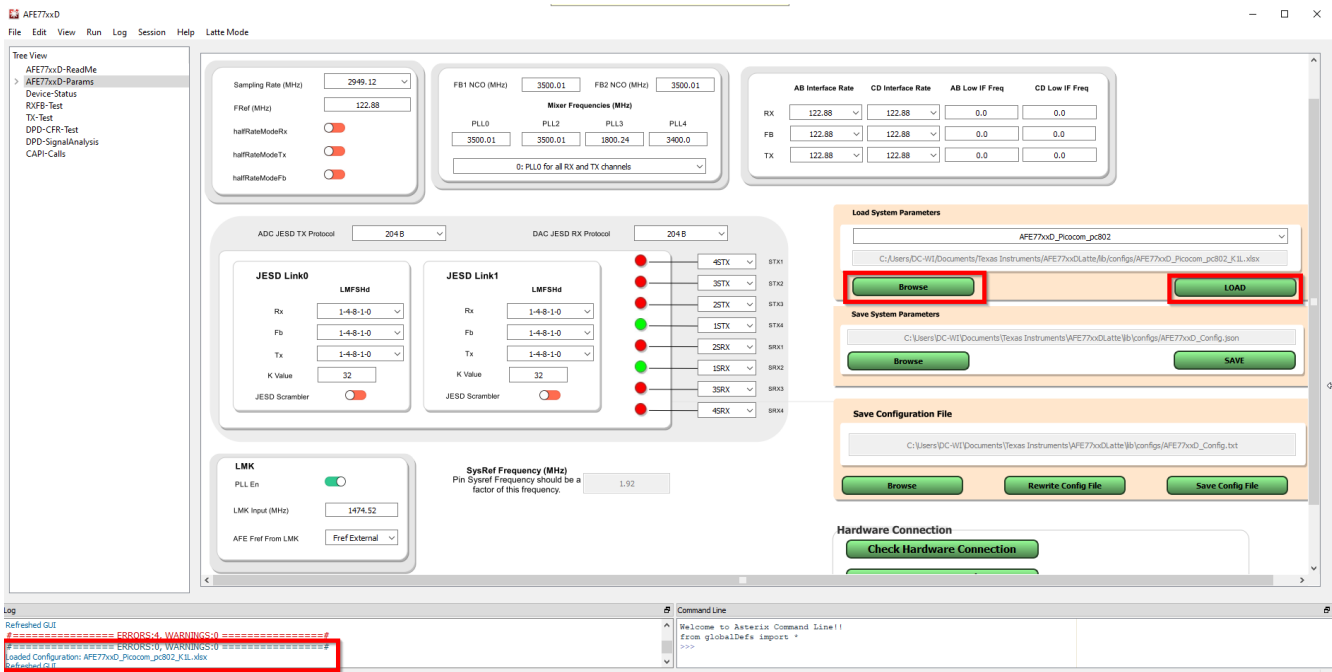
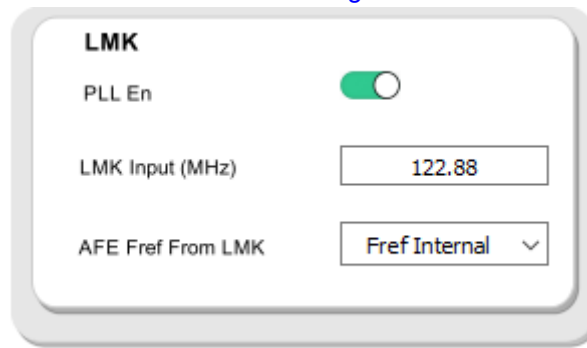


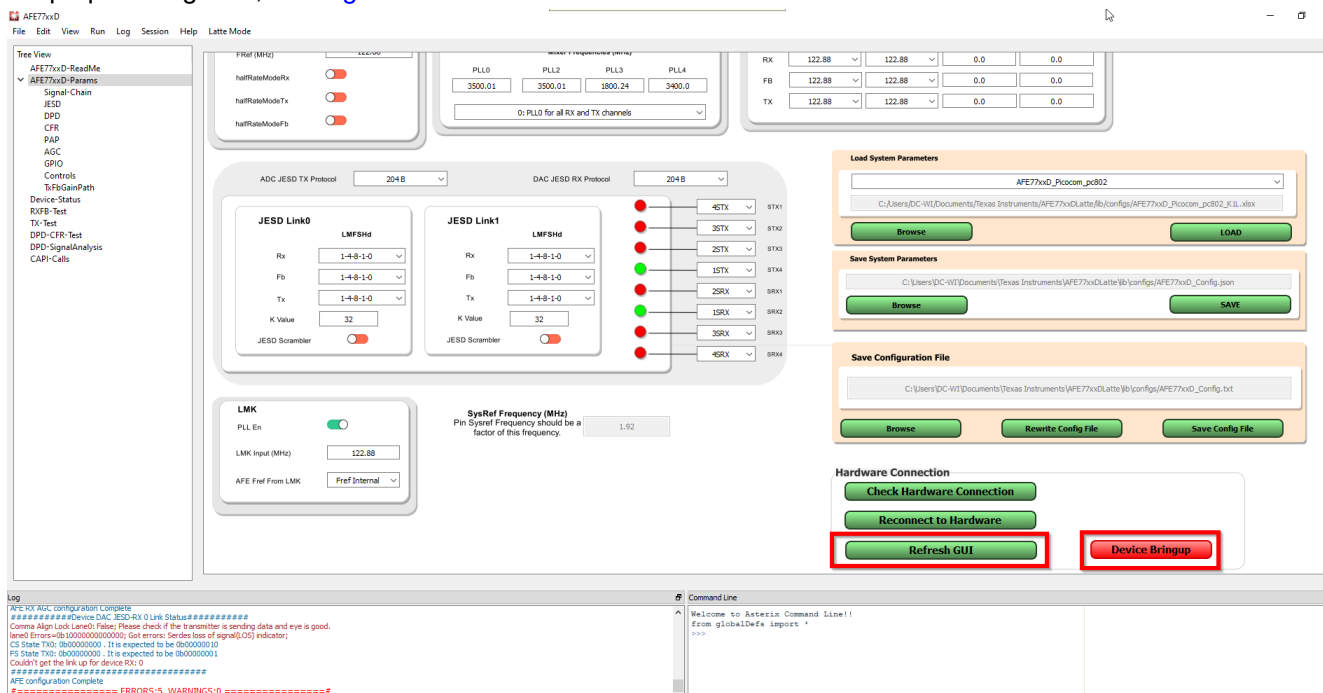
Figure 3-10. Main Window: GUI Mode

- Set the LMK parameters on the bottom left corner like [Figure 3-11](#).



**Figure 3-11. Setting LMK Parameters**

- After that, under “Hardware Connection”, click the refresh GUI button and you will see a message on the log window saying “Refreshed GUI”. Then click on “Device Bringup” this will start the bring up for the device. For proper navigation, see [Figure 3-12](#).



**Figure 3-12. Device Bringup**

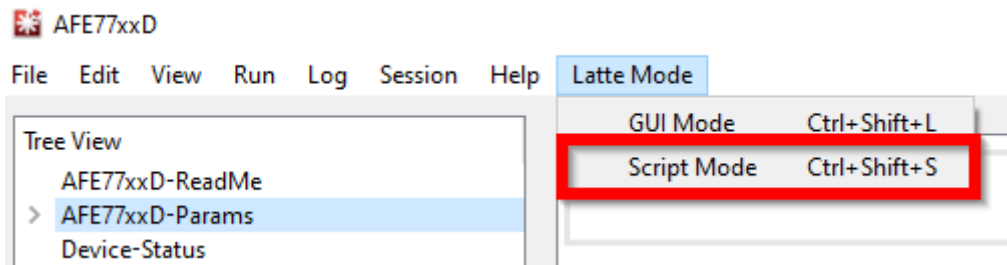


- After the device bringup is done, you will see some errors on the log window (shown in [Figure 3-13](#)). Two of these errors should be “FPGA Reset device not found” and the rest should be under the “Device DAC JESD-RX 0 Link Status” line. These errors are expected since the JESD link is not up.

```
Log
LMK Configured.
Fuse farm load autoloading done successful
No autoloading error
Fuse farm load autoloading done successful
No autoloading error
AFE Reset Done.
pll1: True; LO Frequency: 2949.12
FPGA Reset device not found
FPGA Reset device not found
FPGA Configured.
AFE MCU Wake up done.
pll0: True; LO Frequency: 3500.01
pll1: True; LO Frequency: 2949.12
AFE all PLLs configured.
FB DSA 3.5G Band
AFE SerDes configured.
AFE Digital Chains configured.
AFE DAC Analog Writes configured.
AFE RX Analog Writes configured.
AFE FB Analog Writes configured.
AFE JESD configured.
AFE GPIO configured.
AFE TX IQMC-LOL Correction configuration Complete
AFE DPD Block configuration
AFE DPD Block configuration Complete
AFE RX IQMC configuration Complete
AFE RX AGC configuration Complete
#####Device DAC JESD-RX 0 Link Status#####
Comma Align Lock Lane0: False; Please check if the transmitter is sending data and eye is good.
lane0 Errors=0b10000000000000; Got errors: Serdes loss of signal(LOS) indicator;
CS State TX0: 0b00000000 . It is expected to be 0b00000010
FS State TX0: 0b00000000 . It is expected to be 0b00000001
Couldn't get the link up for device RX: 0
#####
AFE configuration Complete
#===== ERRORS:5, WARNINGS:0 =====#
```

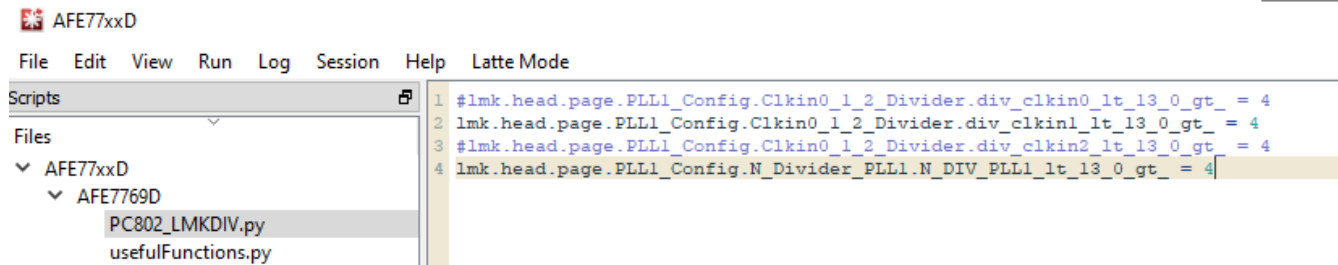
**Figure 3-13. Latte Log Qindow Post-Bringup**

- At the top, click on Latte Mode and navigate to Script Mode as shown in [Figure 3-14](#).



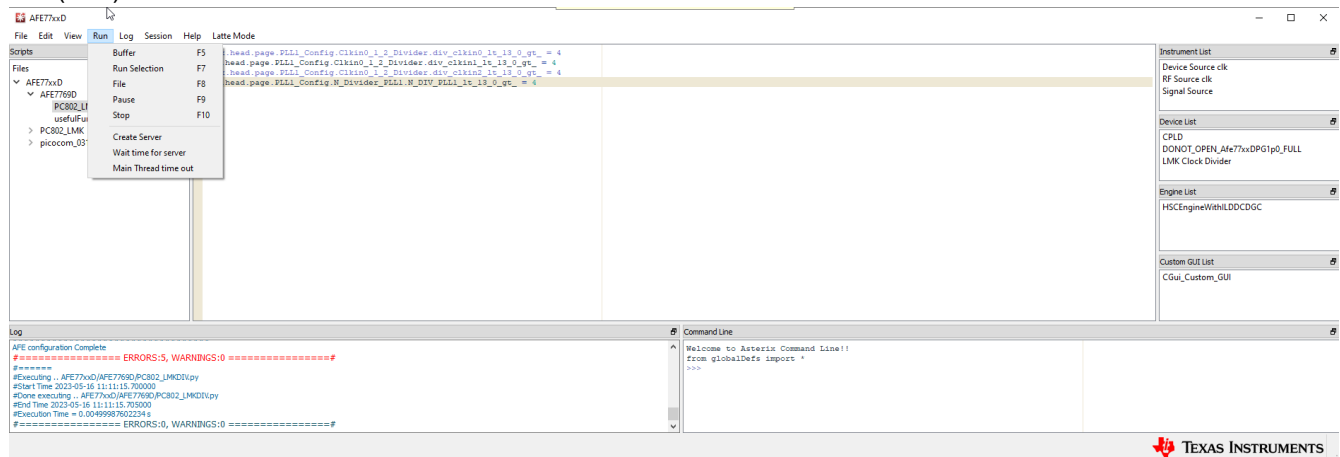
**Figure 3-14. Switching to Script Mode**

- Open the PC802\_LMKDIV.py script on the tree view on the left, as shown in [Figure 3-15](#).



**Figure 3-15. PC802 LMK Script**

- Run the script by pressing F5 or by clicking Run > Buffer. You should see an output in the log window like [Figure 3-16](#), signaling the script was run with no errors. After running this script, the LMK\_LOCKED LED (D11) turns on if the 122.88 MHz reference from the PC802 is connected.



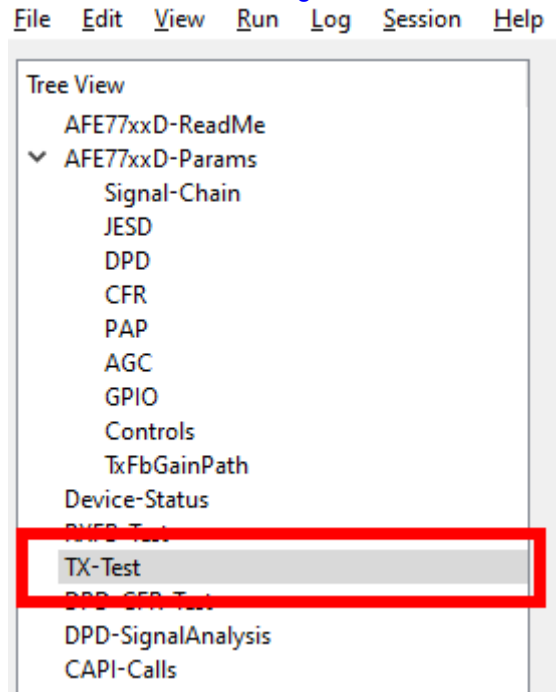
**Figure 3-16. Running the LMK Script**

- Click on Latte Mode and navigate to GUI Mode as shown in [Figure 3-17](#).



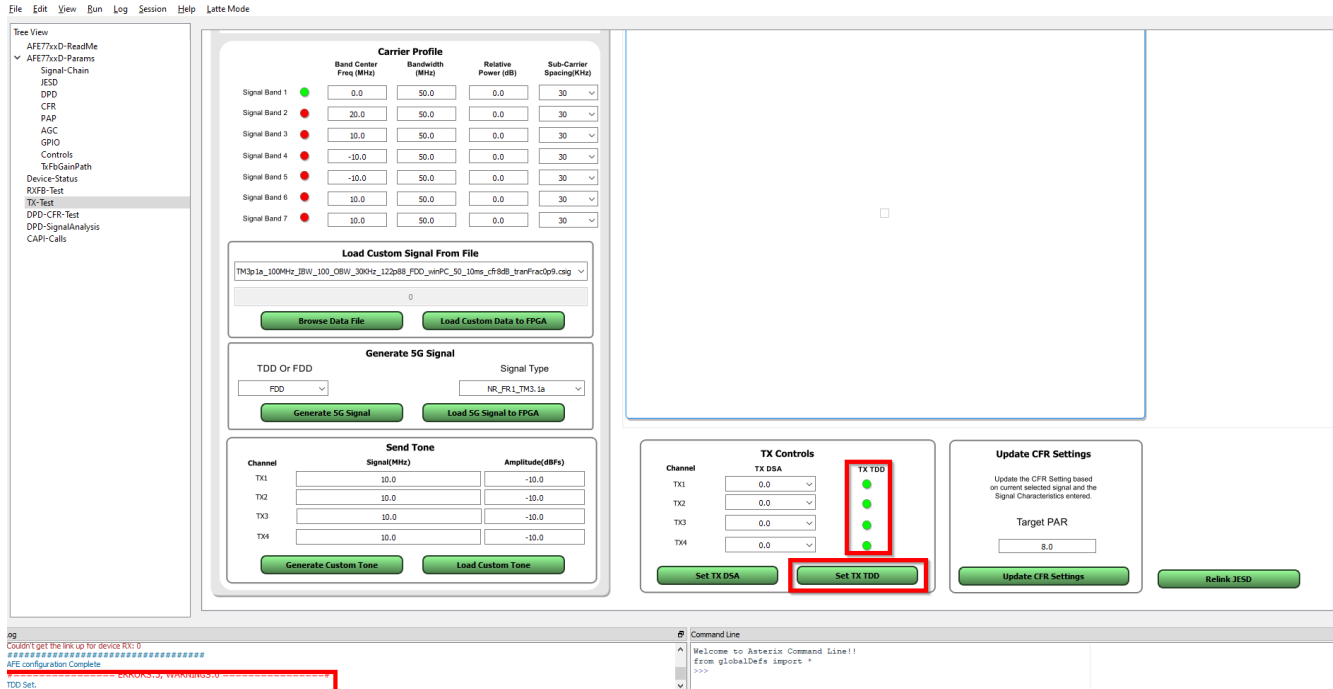
**Figure 3-17. Switching to GUI Mode**

- Click on “TX-Test” under the tree view, as shown in [Figure 3-18](#).



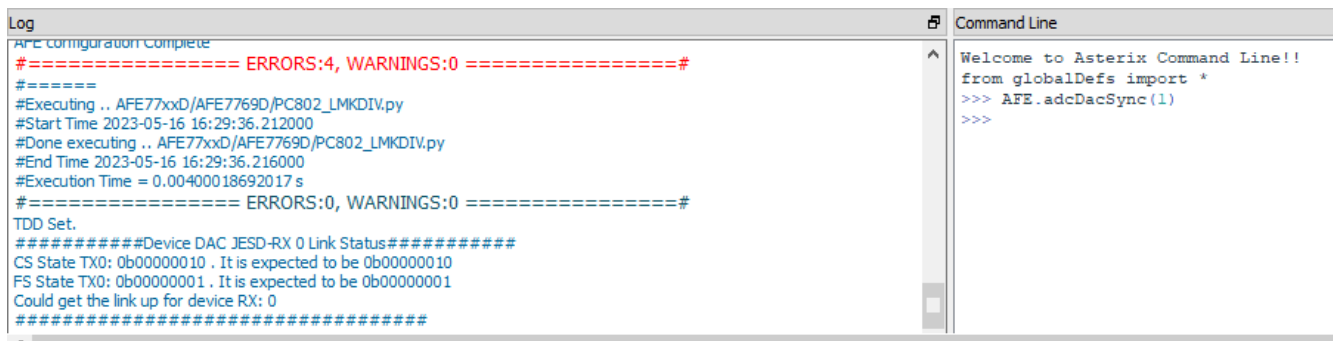
**Figure 3-18. Switching to TX-Test Tab in Latte**

12. Enable the TDD for the TX channels by setting them to green like in [Figure 3-19](#). Then, click “Set TX TDD”, and a message should appear on the log window that says “TDD set”.



**Figure 3-19. Enabling TDD Mode**

13. Proceed to set up the PC802 by following the [PC802 EVB RFIC Demonstration User Guide](#) (Version 3) (where is this doc located or what is the lit number?) from section 2.2. Once you get to section 2.2.5, after you enter the “start” command on the test mode tool to start sending data, type the “AFE.adcDacSync(1)” command in the Command line in the AFE77xxD GUI. You should now be able to see a report in the log window that the JESD link is up with no errors like in [Figure 3-20](#). Data will be going out of the AFE TX channel.



**Figure 3-20. JESD Link Bringup**

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