Analog Engineer's Circuit

Full-Wave Rectifier Circuit

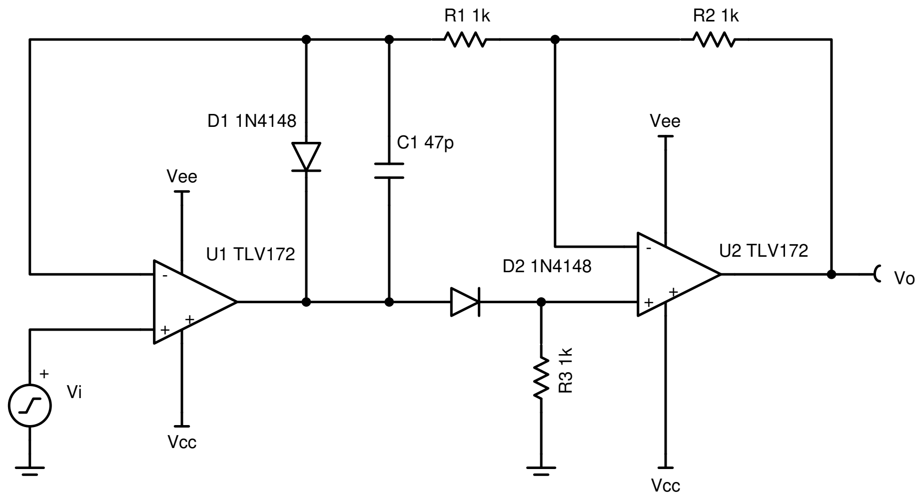
TEXAS INSTRUMENTS

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
±25 mV	±10 V	25 mV	10 V	15 V	–15 V	0 V

Design Description

This absolute value circuit can turn alternating current (AC) signals to single polarity signals. This circuit functions with limited distortion for ±10 V input signals at frequencies up to 50 kHz and for signals as small as ±25 mV at frequencies up to 1 kHz.



Design Notes

1. Be sure to select an op amp with sufficient bandwidth and a high slew rate.
2. For greater precision look for an op amp with low offset voltage, low noise, and low total harmonic distortion (THD).
3. The resistors were selected to be 0.1% tolerance to reduce gain error.
4. Selecting too large of a capacitor C_1 will cause large distortion on the transition edges when the input signal changes polarity. C_1 may not be required for all op amps.
5. Use a fast switching diode.

Design Steps

1. Select gain resistors.
   a. Gain for positive input signals.

   $$\frac{V_o}{V_i} = 1\frac{V}{V}$$

   b. Gain for negative input signals.

   $$\frac{V_o}{V_i} = -\frac{R_2}{R_1} = -1\frac{V}{V}$$

2. Select R_1 and R_2 to reduce thermal noise and to minimize voltage drops due to the reverse leakage current of the diode. These resistors will appear as loads to U_1 and U_2 during negative input signals.

   $$R_1 = R_2 = 1\ \text{k}\Omega$$

3. R_3 biases the non-inverting node of U_2 to GND during negative input signals. Select R_3 to be the same value as R_1 and R_2. U_1 must be able to drive the R_3 load during positive input signals.

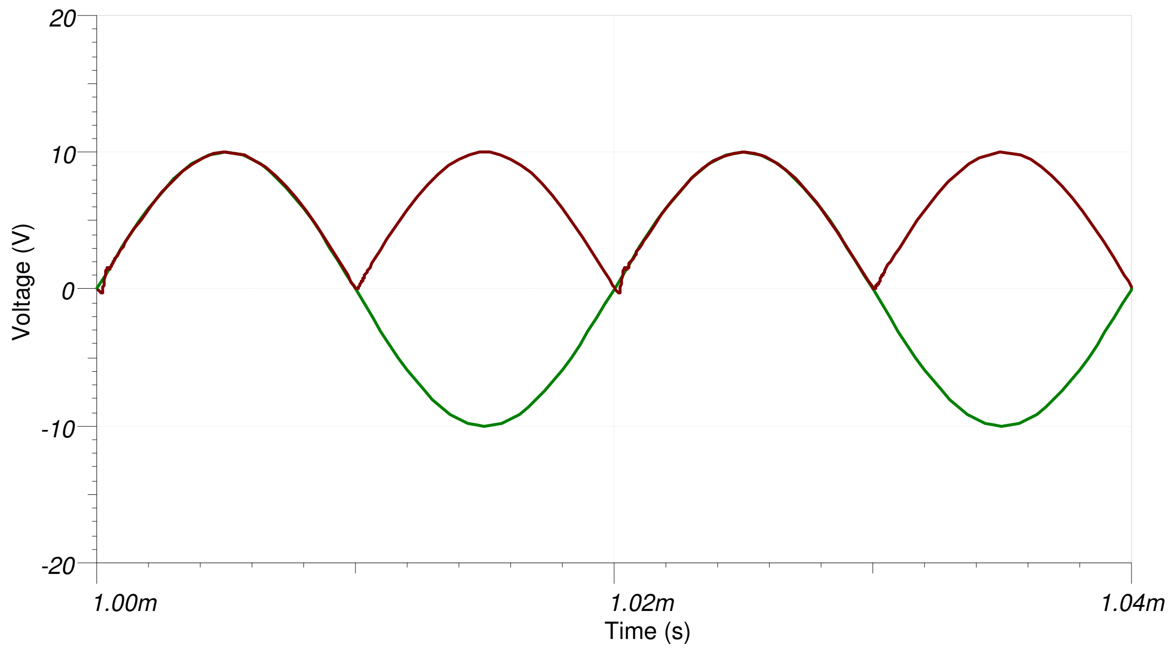
   $$R_3 = 1\ \text{k}\Omega$$

4. Select C_1 based on the desired transient response. See the *Design Reference* section for more information.

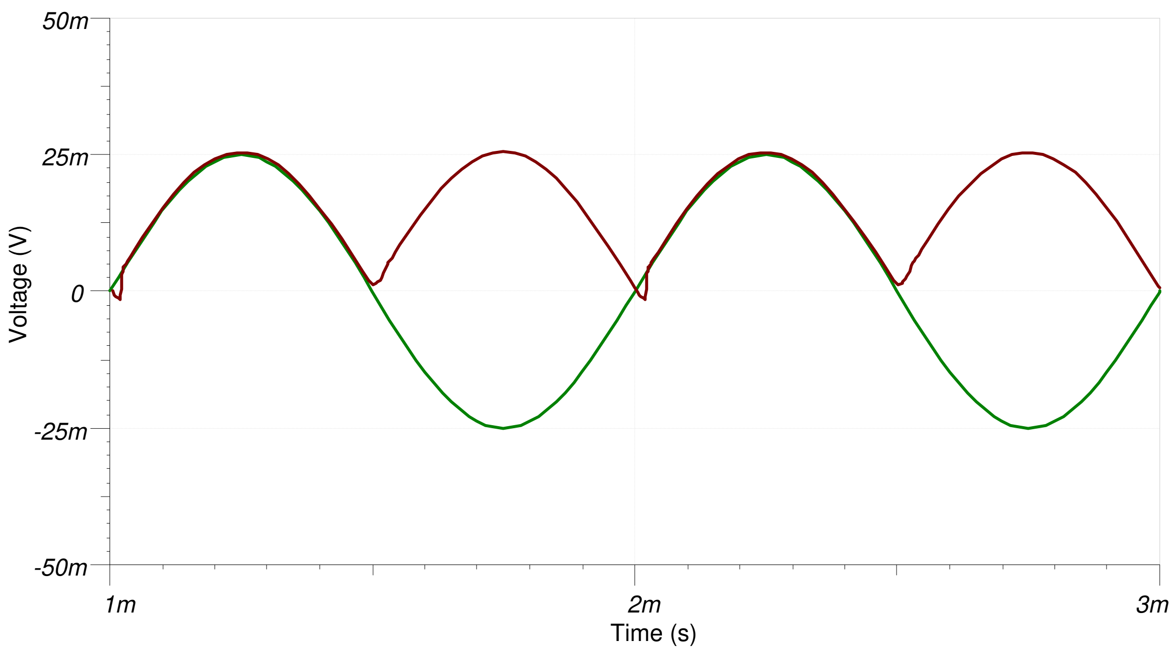
   $$C_1 = 47\text{pF}$$

Design Simulations

Transient Simulation Results



±10 V at 50 kHz Input



±25 mV at 1 kHz Input

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC517.

See TIPD139, Prevision Full-Wave Rectifier, Dual-Supply.

Design Featured Op Amp

TLV172	
V_{cc}	4.5 V to 36 V
V_{inCM}	V_{ee} to (V_{cc}–2 V)
V_{out}	Rail-to-rail
V_{os}	0.5 mV
I_q	1.6 mA/Ch
I_b	10 pA
UGBW	10 MHz
SR	10 V/µs
#Channels	1, 2, and 4
TLV172	

Design Alternate Op Amp

OPA197	
V_{cc}	4.5 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	25 µV
I_q	1 mA/Ch
I_b	5 pA
UGBW	10 MHz
SR	20 V/µs
#Channels	1, 2, and 4
OPA197	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 1, 2019 **Page**

- Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page and Spice simulation file. 1