Technical White Paper

Op Amp Offset Voltage and Bias Current Limitations

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ABSTRACT

Input offset voltage is a DC error source that adds to or subtracts from the input signal. Input bias current is a DC current on op amp input terminals that converts to an offset voltage when it flows through the source resistance and/or feedback resistors. These error sources are affected by temperature, power supply voltage, input common mode voltage, and output voltage. This document shows how to calculate errors associated with input offset voltage and input bias current. It also covers the impact of offset and bias current in op amp technologies. It includes internal IC-design methods used to minimize offset and bias current Understanding this material helps you select the best amplifier for your specific system requirements.

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1 Input Offset Voltage (V_{OS}) Definition

Input offset voltage can be modeled as an error voltage source in series with the non-inverting input of the op amp (see Figure 1-1). This offset voltage can range from microvolts to millivolts (see Table 1-1). For amplifiers, the term *precision* is generally used to describe amplifiers with input offset voltage less than 1mV.

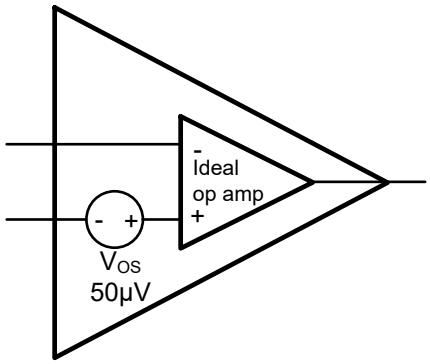


Figure 1-1. Offset Voltage Model

Because the offset source is directly in series with the op amp input, the impact of offset voltage error is more significant for small input signal ranges. Figure 1-2, and Figure 1-3 illustrate the error introduced by a 1mV offset for an amplifier in a gain of 10 V/V and 100 V/V. Equation 1 through Equation 4 show the error calculation for gain of 10V/V and Equation 5 through Equation 8 show the calculation for 100V/V. The applied input signal drives the output to near full scale in both cases (4.5V on a 5V supply). Notice that the percentage error increased by a factor of 10 when the gain is increased by a factor of 10. Thus, offset voltage is often a greater concern in higher gain systems.

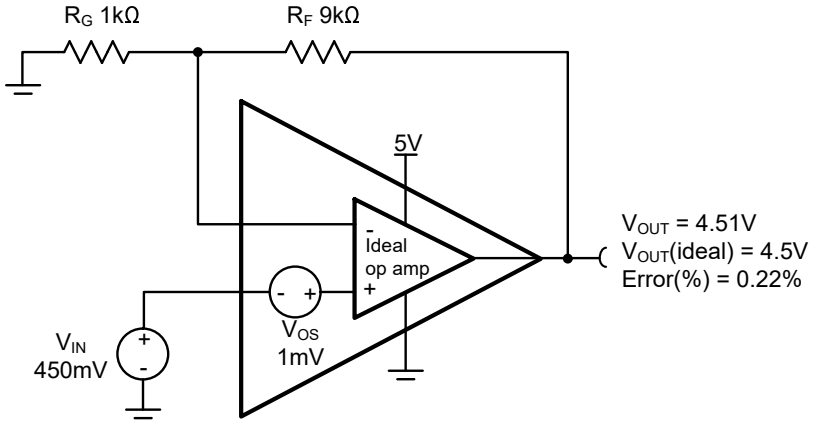


Figure 1-2. Output Offset and Percent Error In Low Gain

$$G = \frac{R_F}{R_G} + 1 = \frac{9k\Omega}{1k\Omega} + 1 = 10V/V \quad (1)$$

$$V_{OUT} = (V_{IN} + V_{OS})G = (450mV + 1mV)(10V/V) = 4.51V \quad (2)$$

$$V_{OUT(Ideal)} = (V_{IN})G = (450mV + 1mV)\left(10V/V\right) = 4.50V \quad (3)$$

$$Error\left(\%\right) = 100\left(\frac{V_{OUT} - V_{OUT(Ideal)}}{V_{OUT(Ideal)}}\right) = 100\left(\frac{4.51V - 4.50V}{4.50V}\right) = 0.22\% \quad (4)$$

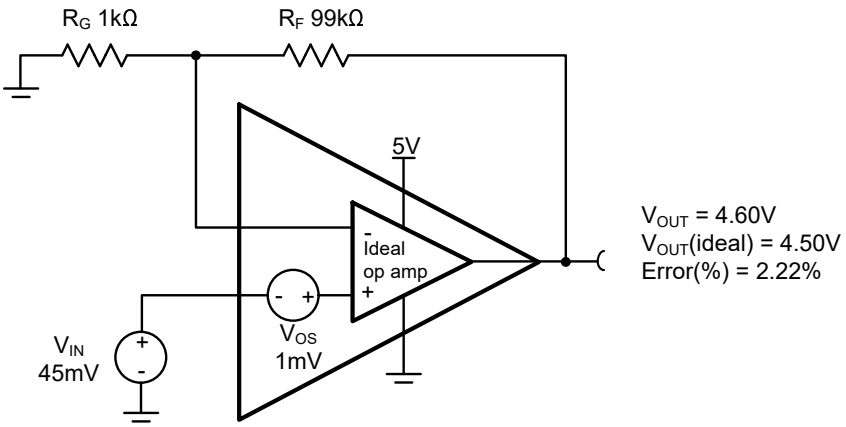


Figure 1-3. Output Offset And Percent Error in High Gain

$$G = \frac{R_F}{R_G} + 1 = \frac{99k\Omega}{1k\Omega} + 1 = 100V/V \quad (5)$$

$$V_{OUT} = (V_{IN} + V_{OS})G = (45mV + 1mV)(100V/V) = 4.60V \quad (6)$$

$$V_{OUT(Ideal)} = (V_{IN})G = (45mV + 1mV)\left(100V/V\right) = 4.50V \quad (7)$$

$$Error\left(\%\right) = 100\left(\frac{V_{OUT} - V_{OUT(Ideal)}}{V_{OUT(Ideal)}}\right) = 100\left(\frac{4.60V - 4.50V}{4.50V}\right) = 2.22\% \quad (8)$$

1.1 Input Offset Voltage Drift (dV_{OS}/dT) Definition

The input offset voltage is specified at room temperature (25°C), and across temperature (V_{OS} drift, or dV_{OS}/dT). For precision devices, typical V_{OS} drift maximum specifications range from 0.001 µV/°C to 5 µV/°C. Cost optimized and high-speed devices are generally not optimized for input offset voltage and V_{OS} temperature drift, so they can have drifts as high as 100 µV/°C (see Table 1-1). The change in offset due to V_{OS} drift can be estimated by multiplying the change in temperature relative to 25°C by the V_{OS} drift term, ΔV_{OS} = (dVos/dT)(T - 25°C). The change in offset due to temperature drift adds to the initial room temperature V_{OS}. This calculation assumes that the amplifier V_{OS} drift is linear over temperature which may not be true for all amplifiers. Some amplifier data sheets provide a graph of V_{OS} versus temperature, which is useful to understand the linearity of the drift. Figure 1-4 shows this calculation at a temperature of 125°C for OPA2205 using the maximum specified offset and drift. In this example, the room temperature V_{OS} is 15 µV and the V_{OS} drift is 20 µV for a total V_{OS} of 35 µV at 125°C.

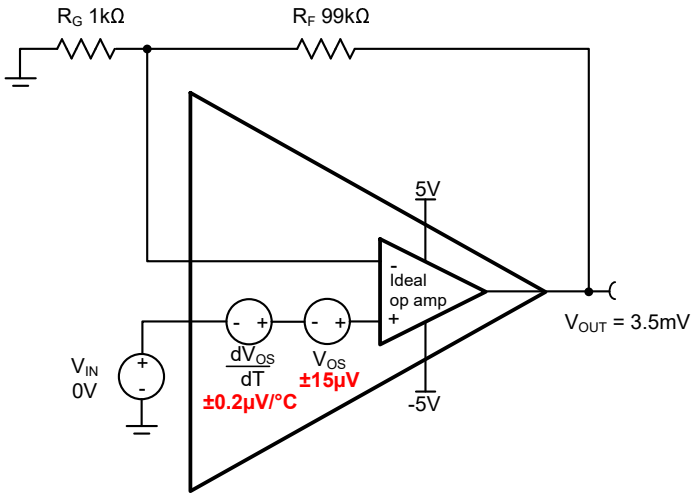


Figure 1-4. Maximum Input Offset Voltage Drift Model And Calculation for OPA2205

$$T = 125°C \quad (9)$$

$$G = \frac{R_F}{R_G} + 1 = \frac{99k\Omega}{1k\Omega} + 1 = 100V/V \quad (10)$$

$$V_{OS}(T) = V_{OS}(25°C) - \frac{dV_{OS}}{dT}(T - 25°C) \quad (11)$$

$$V_{OS}(125°C) = 15\mu V - (0.2\mu V/°C)(125°C - 25°C) = 35\mu V \quad (12)$$

$$V_{OUT} = (V_{OS})G = (35\mu V)(100V/V) = 3.5mV \quad (13)$$

Table 1-1. Range of V_{OS} and V_{OS} Drift for Different Amplifier Types

Op Amp	$V_{OS\ (max)}$ (high grade)	V_{OS} Drift (max)(high grade)	Technology
OPA387	2µV	0.012µV/°C	Low voltage Zero-Drift CMOS
OPA182	4µV	0.012µV/°C	High Voltage Zero-Drift CMOS
OPA2186	10µV	0.04µV/°C	24V Zero-Drift CMOS
OPA192	25µV	0.5µV/°C	e-Trim™ High Voltage CMOS
OPA210	35µV	0.5µV/°C	Super-Beta Bipolar
OPA827	150 µV	1.5 µV/°C	JFET input, Laser Trim, Bipolar
OPA828	300µV	1.3µV/°C	DiFET (JFET), Laser trimmed
LMV841	500µV	5µV/°C	12V CMOS
OPA835	1.85mV	13.5µV/°C	High Speed Bipolar
LM741	3mV	15µV/°C	Bipolar commodity (lower cost)

1.2 V_{OS} and V_{OS} Temperature Drift Inside the Amplifier

Both bipolar and CMOS op amps have an input differential pair used as the first stage of the amplifier (see Figure 1-5, and Figure 1-6). For bipolar devices, the offset voltage is mainly due to the mismatch of the base to emitter junction voltages (Vbe1 and Vbe2). This mismatch is due to photo-lithography effects, doping gradients, and stress introduced during packaging of the device. Similarly, the offset in CMOS devices is from the gate-to-source voltage mismatch, and the mismatch is due to the same types of fabrication issues as with bipolar.

The V_{OS} in bipolar and CMOS op amps can be reduced by adjusting the value of Ros1 or Ros2. This process is called *trimming* and can be accomplished through *laser-trim* or *package-level-trim* (e-Trim®). In both cases the V_{OS} is measured and resistors are adjusted to minimize the offset. In laser-trimming, sections of a thin film resistor are physically cut away to increase the resistance (see Section 1.3). Package-level-trim uses digital communications to open switches or fuses in a binary weighted resistor network (see Section 1.4). A third way that op amp V_{OS} can be minimized is by using an internal self-calibration circuit. These types of amplifiers are called zero-drift amplifiers and are covered in Section 4.

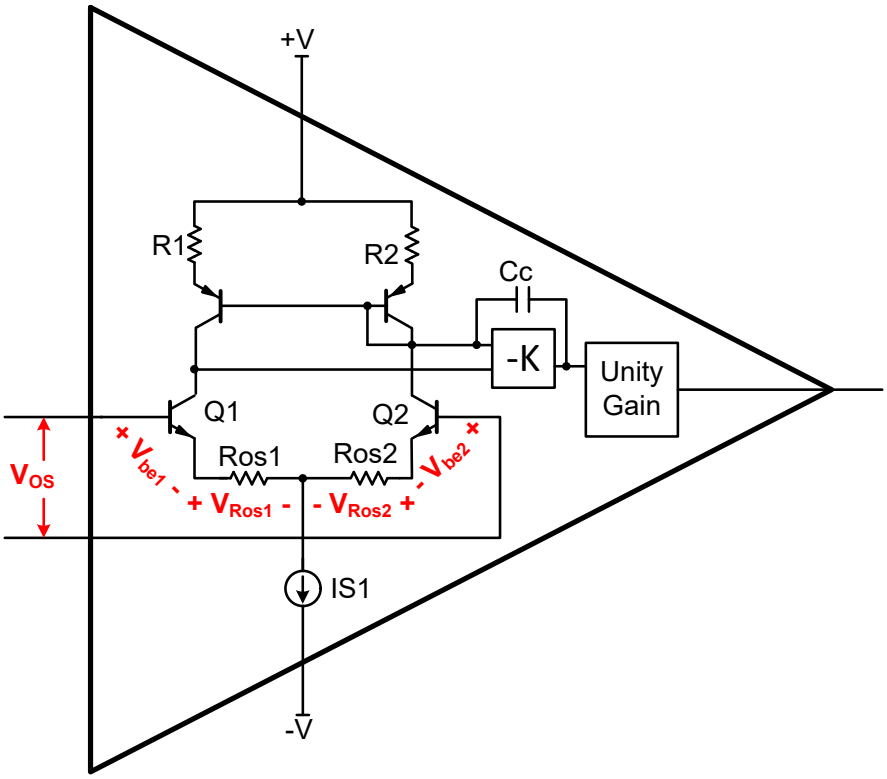


Figure 1-5. Bipolar differential input, simplified op amp model

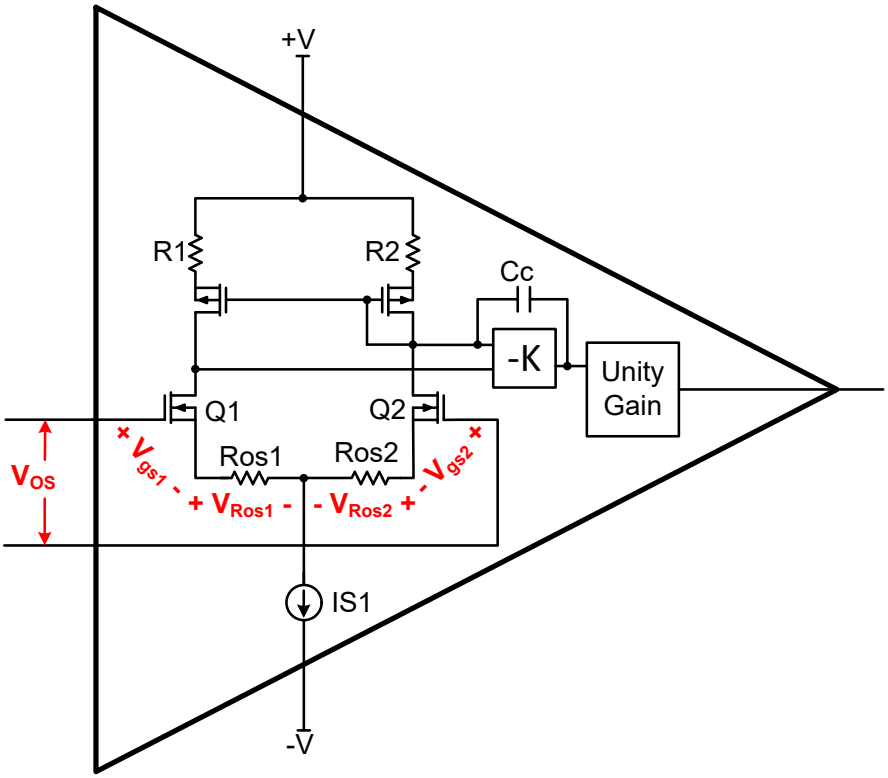


Figure 1-6. CMOS differential input, simplified op amp model

The temperature drift of a bipolar op amp is linear and is directly proportionate to offset (see Figure 1-7). In fact, each millivolt of offset yields about 3.3µV/C of offset drift. Thus, trimming the offset to zero on a bipolar op amp also trims the drift close to zero (see Figure 1-7). Conversely, the drift of CMOS devices is nonlinear and is not proportional to offset as with the bipolar (see Figure 1-8). Trimming the temperature drift on a CMOS device requires adjustment of resistors R_1, R_2, and offset is trimed with R_{OS1}, and R_{OS2} (see Figure 1-6). Furthermore, the CMOS op amp offset must be measured at multiple temperatures in order to trim the temperature drift, whereas the bipolar device temperature drift can be trimmed at a single temperature. The additional complexity of the CMOS V_{OS} and the V_{OS}-drift trim makes it challenging to achieve the same performance as the bipolar device.

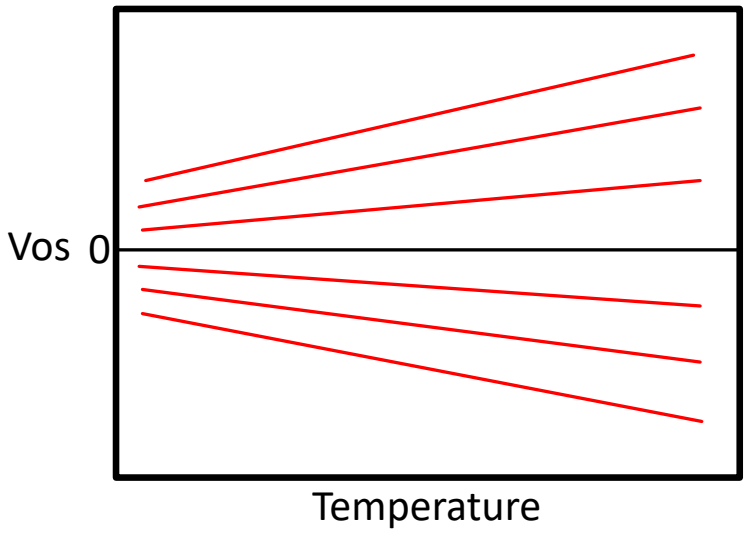


Figure 1-7. Bipolar V_{OS} vs Temperature

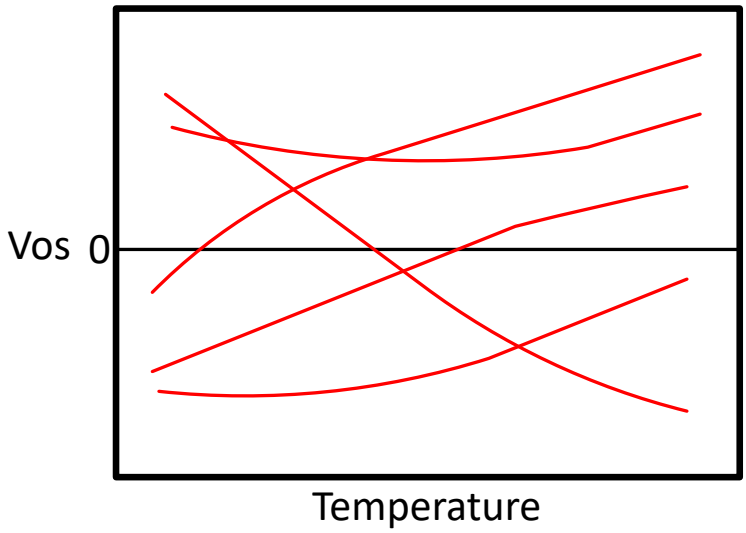


Figure 1-8. CMOS V_{OS} vs Temperature

1.3 Laser Trim to Adjust Performance

Both laser trimming and package trimming are methods for adjusting the value of resistors on the die for op amp and other semiconductor devices. Laser trimming adjusts the resistors by cutting away material on the resistors using a laser beam. Normally laser trimming is used on thin film resistors. Figure 1-9 shows a picture of an op amp die that uses laser trimming to adjust V_{OS}, and quiescent current (I_Q). The coarse laser trim adjustment effectively makes the current path longer which significantly increases the resistance. The fine laser trim adjustment makes the resistor width narrower and consequently introduces a smaller more gradual increase in resistance.

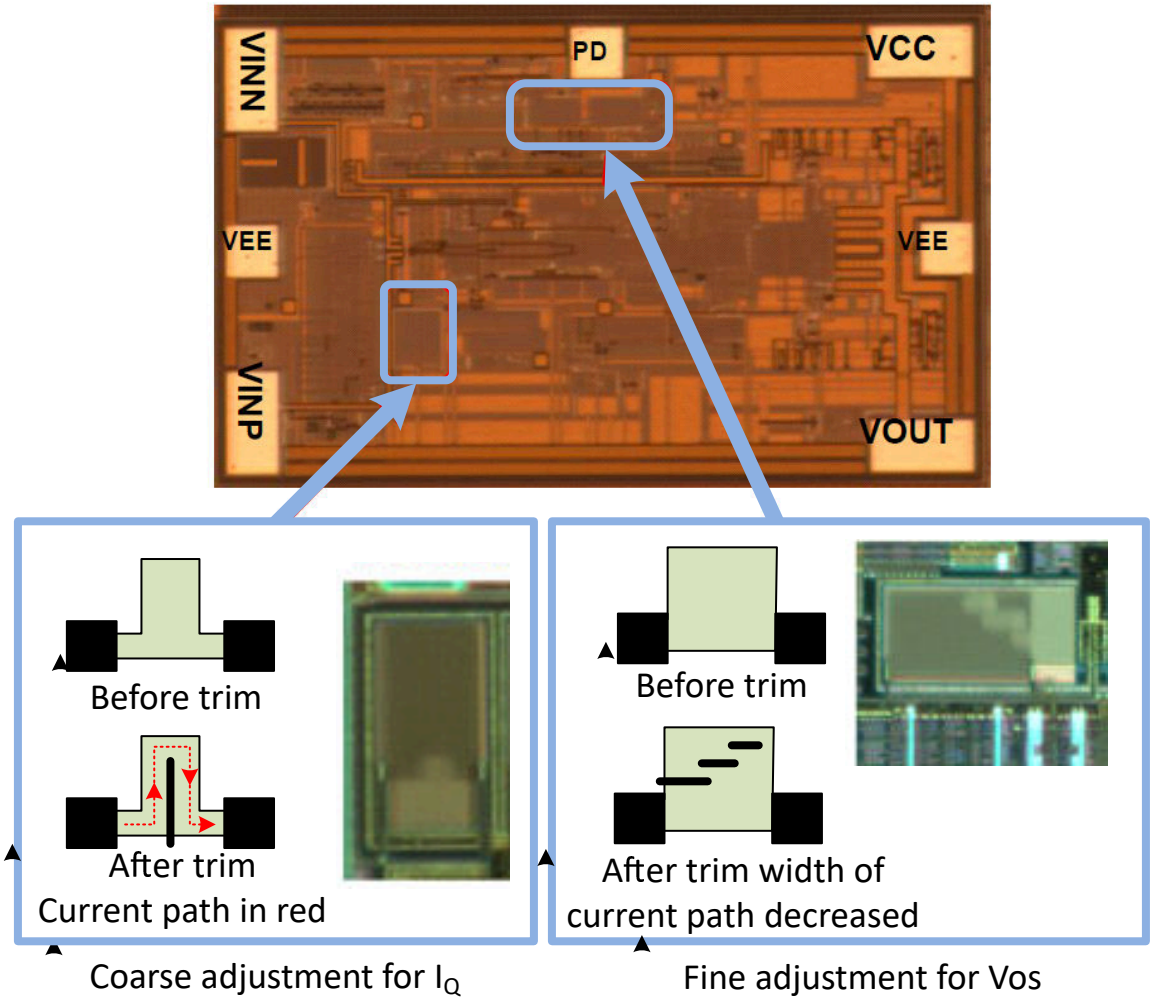


Figure 1-9. Coarse and Fine Laser Trim of Thin Film Resistors

Laser trimming is done when the device is in wafer form before packaging. A typical op amp wafer has tens of thousands of devices on it. Each device, or die, is tested by applying the electrical signals through probes that contact the pads. During the test various parameters such as V_{OS} are measured and the laser is used to reduce the offset by making the appropriate adjustments in the trim resistors. Figure 1-10 illustrates a simplified view of the wafer, probe card, and laser. The wafer is brought into contact with the probes by moving the wafer chuck up and down. Different die on the wafer are selected by moving the chuck right and left. Figure 1-11 shows a zoomed in view of the probes in contact with a single die.

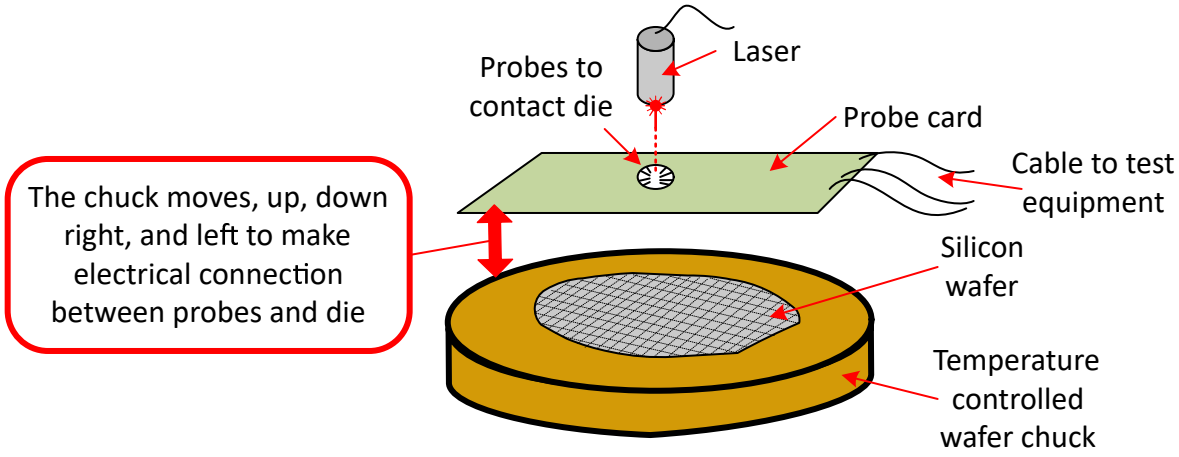


Figure 1-10. Laser Probe Hardware (side view)

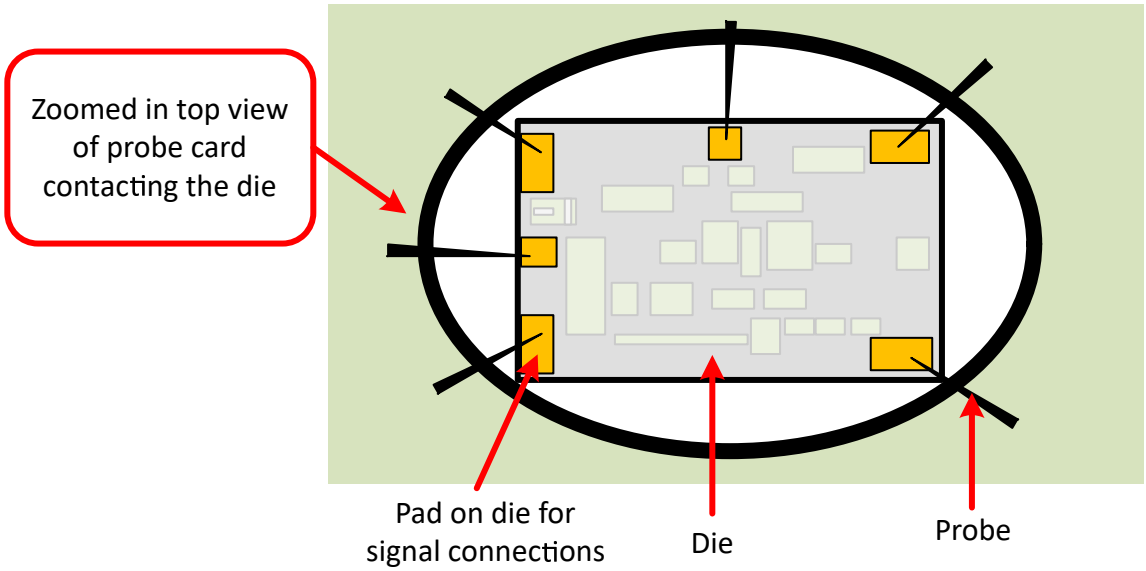


Figure 1-11. Laser Probe Card in Contact with Die (zoomed in, top view)

After wafer probing is complete the wafer is sawed into individual die which would then be glued to a lead frame, its pads wire bonded to appropriate pins, and finally encapsulated in plastic (see Figure 1-12). The packaging process introduces physical stress (bending, warping) on the die that causes shifts in device performance. For example, during laser trim the offset might be trimmed to a level of 10 µV, but the packaging introduces stress that shifts the offset to 100 µV. This package shift can be somewhat mitigated by careful symmetrical layout and inter-digitation of key components, however, it is not possible to completely eliminate this error source. Thus, laser trimming has inherent accuracy limitations and is the main reason why wafer trimmed parts cannot achieve single digit microvolts offset.

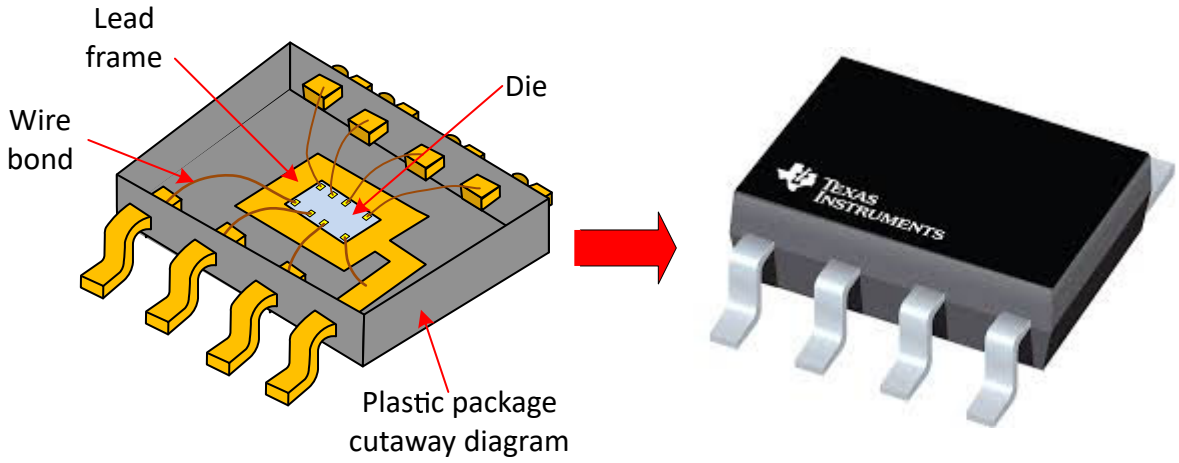


Figure 1-12. Cutaway Diagram of Die Packaged in SOIC

1.4 Package Trim (e-Trim™) to Adjust Performance

Every amplifier at Texas Instruments undergoes a final test of the device in package form. The final test applies power and electrical signals to the device and measures performance. This measurement compares against the specifications given in the product data sheet. Devices that do not meet specifications are discarded. For devices that use package level trimming (e-Trim®), parameters such as V_{OS} are adjusted during final test to optimize performance. This adjustment is done by measuring the offset and adjusting a resistance value to minimize the error. In package trimming the internal trim resistors are divided into binary weighted segments. These segments can be added to the resistor by opening a fusible link or by using a one-time-programable (OTP) nonvolatile memory. Modern designs at Texas Instruments are mainly done using OTP.

Figure 1-13 shows a simplified view of how the resistor value is adjusted with package trimming. During final test the initial V_{OS} is measured, and the desired trim resistor value is calculated based on the measurement. A digital signal is applied to the device through the output pin to program the OTP memory. The OTP is used to open switches in parallel with the resistor segments. The example shows that the binary weighted resistor can have a value from 0 Ω to 15 kΩ in 1 kΩ increments. When the test procedure completes, the signal sends a write protect command the device to disable the digital interface so that in the future it is not possible to accidentally re-program the OTP. After programming, the op amp reads the OTP during the startup period and the device configures the switches to set the trim resistor to its target value.

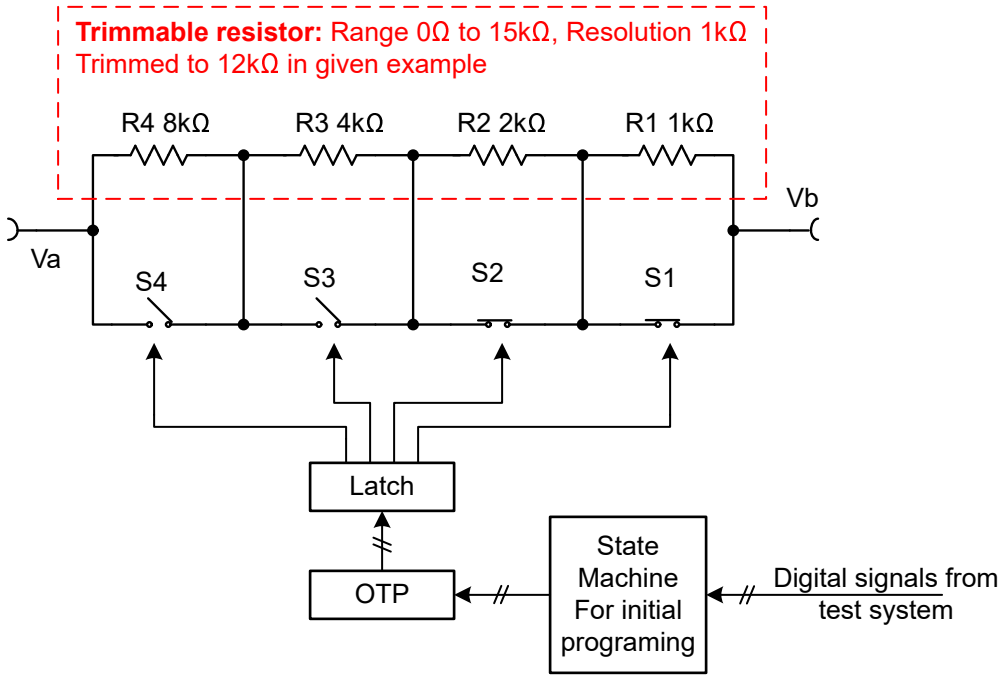


Figure 1-13. Package trim resistor configuration

Figure 1-14 shows a simplified view of how the digital signals are applied to the device. Remember, the device is packaged and op amps normally do not have any pins for a digital interface. For op amps, the output pin is initially used to apply the digital signal. The device places the output in one of three states: sourcing 5 mA, sinking 5 mA, or floating. A comparator circuit detects these output current loads and creates two digital signal patterns. The digital signals drive the state machine which is used to program the OTP.

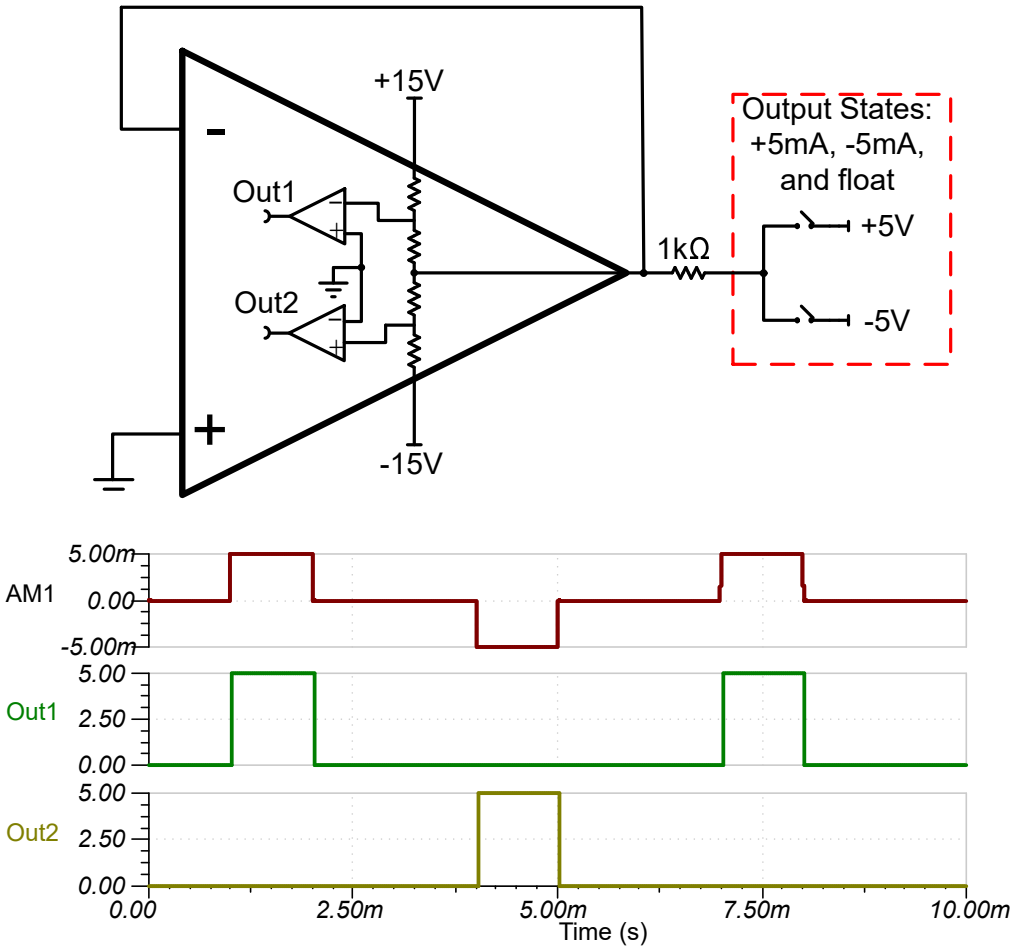


Figure 1-14. Package Trim Communication

2 Input bias current (I_B) definition

Input bias current (I_B) can be modeled as DC current sources on both the inverting and non-inverting input terminals (see Figure 2-1). This bias current develop an error voltage when it flows through the feedback network and source impedance. The error voltage can be referred to the input so that it adds to the V_{OS} and V_{OS} drift error sources. Equation 14 and Equation 15 shows the calculation for converting bias current into an offset voltage. Figure 2-2 and Equation 17 show how the input bias current translates into offset voltage sources.

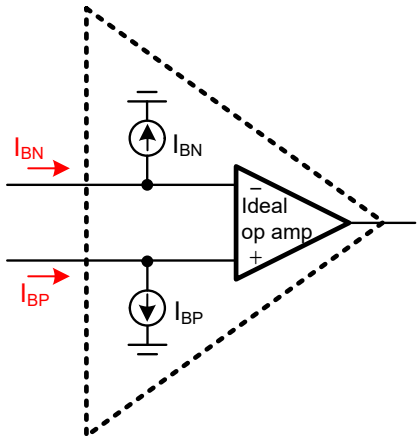


Figure 2-1. Bias Current Model

$$V_{IBP} = -I_{BP}R_S \quad (14)$$

$$V_{IBN} = I_{BN}(R_F \,||\, R_G) \quad (15)$$

$$\left(R_F \,\middle|\middle|\, R_G\right) = \frac{R_F R_G}{R_F + R_G} \quad (16)$$

$$V_{IB} = I_{BN}(R_F \,||\, R_G) - I_{BP}R_S \quad (17)$$

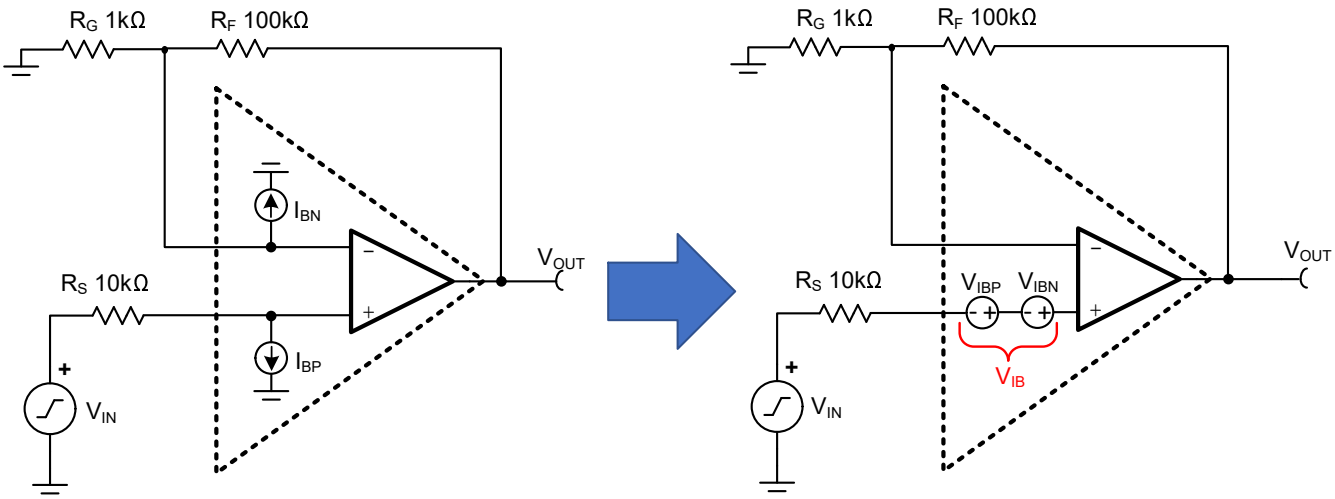


Figure 2-2. Bias Current Translated to Input Offset Voltage

The amplifier data sheet normally does not specify the bias current for the inverting and non-inverting input separately, but rather specifies the difference between the bias currents as bias current offset ($I_{OS} = I_{BP} - I_{BN}$). If the bias currents are equal and the source impedance is equal to the feedback network impedance ($R_S = R_F \parallel R_G$), then the bias current offset voltages cancel (see Equation 19). However, in most modern precision amplifiers the bias currents have significant offset ($I_{OS} \neq 0$). In fact, for most CMOS amplifiers and many bipolar amplifiers the bias currents and bias offset are comparable in magnitude ($I_B \approx I_{OS}$). Thus, the approach of balancing the source and feedback impedance frequently is not a practical way to minimize input offset voltage due to bias current. When $I_{OS} \geq I_B$, the best approach to minimizing V_{IB} is by minimizing R_S, and $R_F \parallel R_G$, not by balancing the source and feedback impedance. Equation 20 shows V_{IB} where I_{OS} is equal on both inputs ($I_{BP} = I_B + I_{OS}/2$, and $I_{BN} = I_B - I_{OS}/2$). The second term in this equation highlights how the I_{OS} effects are not canceled when $R_S = R_F \parallel R_G$.

$$I_{OS} = I_{BP} - I_{BN} \tag{18}$$

$$V_{IB} = I_B((R_F \parallel R_G) - R_S), \text{ for } I_{OS} = 0 \tag{19}$$

$$V_{IB} = I_B((R_F \parallel R_G) - R_S) + \frac{I_{OS}}{2}((R_F \parallel R_G) + R_S), \text{ for } I_{OS} \text{ equal on each input} \tag{20}$$

Equation 21 and Equation 22 are a good way to estimate the offset voltage due to bias current. These equations assume that half of the bias current offset is equally distributed between the inverting and non-inverting input. The two equations calculate the offset due to I_B considering the polarity of the bias current offset (I_{OS} is negative in Equation 21 and positive in Equation 22). For worst case error analysis calculate both values and select the largest absolute value (see Equation 23). Example 1 uses these equations in a calculation for maximum input offset voltage due to bias current for OPA205A.

$$V_{IB1} = \left(I_B + \frac{I_{OS}}{2}\right)\left(R_F \parallel R_G\right) - \left(I_B - \frac{I_{OS}}{2}\right)R_S \tag{21}$$

$$V_{IB2} = \left(I_B - \frac{I_{OS}}{2}\right)\left(R_F \parallel R_G\right) - \left(I_B + \frac{I_{OS}}{2}\right)R_S \tag{22}$$

$$V_{IB} = \max(|V_{IB1}|, |V_{IB2}|) \tag{23}$$

Example 1: Calculation for OPA205 Maximum Bias Current to Input Offset Voltage

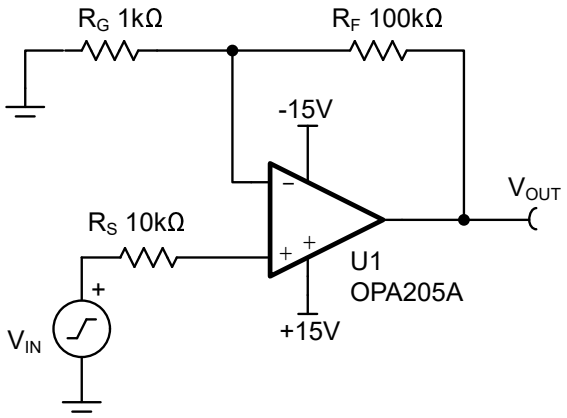


Figure 2-3. Circuit for I_B Example Calculation

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_B	Input bias current	OPA205A	25°C		±0.1	±0.5	nA
I_{OS}	Input offset current	OPA205A	25°C		±0.1	±0.4	nA

$$V_{IB1} = \left(0.5\text{nA} + \frac{0.4\text{nA}}{2}\right)\left(0.99\text{k}\Omega\right) - \left(0.5\text{nA} - \frac{0.4\text{nA}}{2}\right)\left(10\text{k}\Omega\right) = -2.31\mu\text{V} \quad (24)$$

$$V_{IB2} = \left(0.5\text{nA} - \frac{0.4\text{nA}}{2}\right)\left(0.99\text{k}\Omega\right) - \left(0.5\text{nA} + \frac{0.4\text{nA}}{2}\right)\left(10\text{k}\Omega\right) = -6.70\mu\text{V} \quad (25)$$

$$V_{IB} = \max(|-6.70\mu\text{V}|, |-2.31\mu\text{V}|) = 6.70\mu\text{V} \quad (26)$$

2.1 Input Bias Current (I_B) and I_B Temperature Drift Inside the Amplifier

The choice of transistor technology (bipolar, CMOS, or JFET) has a significant effect on input bias current. Bipolar transistors are current controlled devices, whereas CMOS and JFET are voltage controlled. The bipolar transistor collector current is equal to base current multiplied by a current gain. Thus, it is required to have a minimum base current for all bipolar transistors to operate. Because CMOS devices are voltage controlled, the drain current is controlled by a voltage from gate to source. Also, the gate is insulated from the drain-to-source channel with a layer of metal-oxide so the input impedance is very high and there is effectively no leakage current. A JFET device is also a voltage-controlled device. The JFET transistor uses a reverse-biased gate to source P-N junction voltage to control the drain current. Thus, there will be a very small reverse bias leakage current. However, compared to the base current of a bipolar transistor, the JFET gate current is negligible (see Figure 2-4).

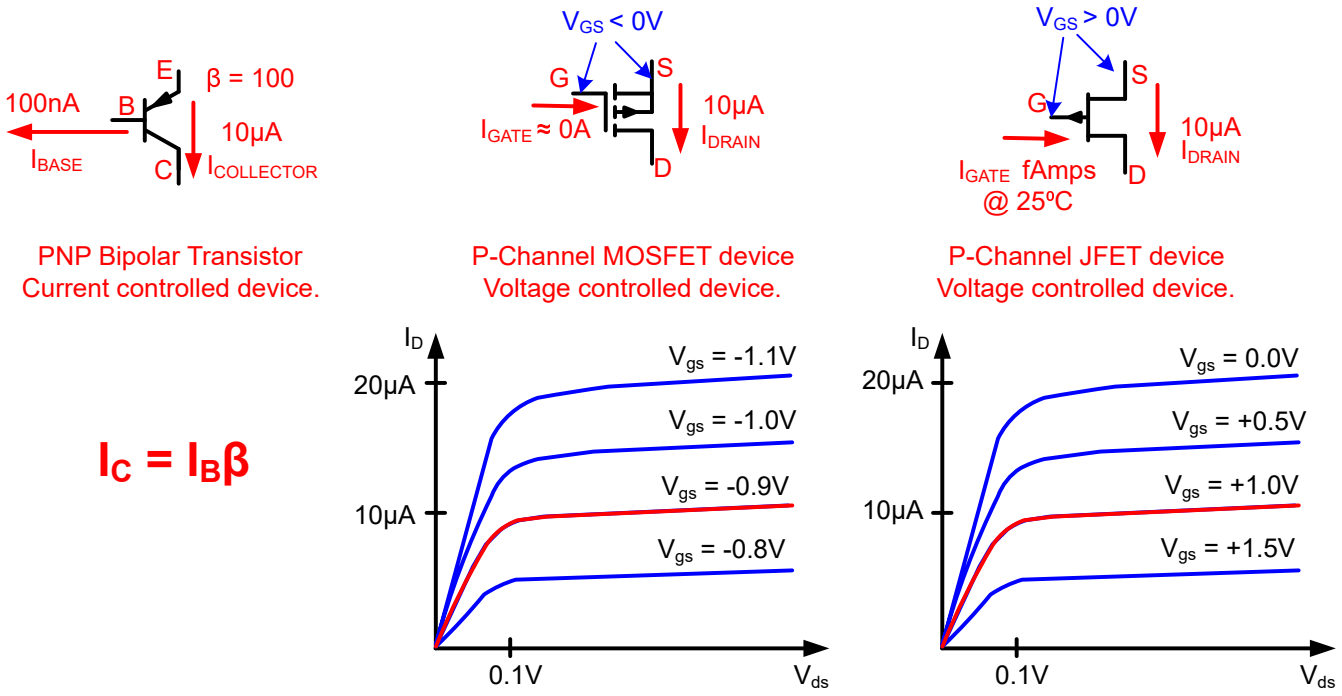


Figure 2-4. Bipolar, MOSFET, and JFET Biasing Summary

The base current of the input stage is the input bias current (I_B) in a bipolar op amp. Depending on the bandwidth, slew rate, and process technology the input bias current of uncorrected bipolar op amps can range from nano-amps to micro-amps. The two inputs also have some leakage current due to ESD structures but this current is generally negligible compared to the base current (see Figure 2-5). Also, the input transistors are not perfectly matched, so the I_B flowing into each amplifier differs slightly. This difference is referred to is bias current offset (I_{OS}). Conversely, the I_B of CMOS and JFET devices, is primarily due to the leakage of the ESD structures and will generally be in the pico-amp or femto-amp range at room temperature (see Figure 2-6).

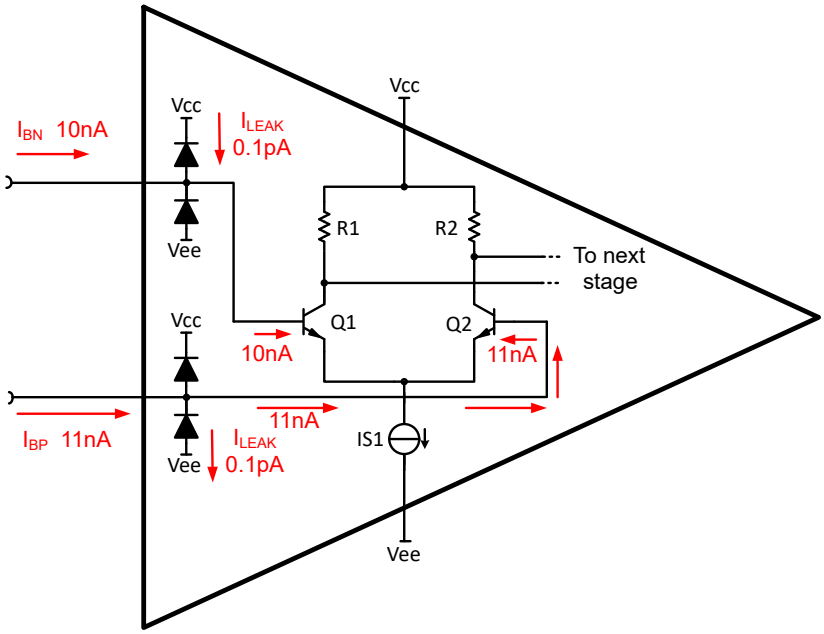


Figure 2-5. Input Bias Current on Input of Bipolar Op Amp

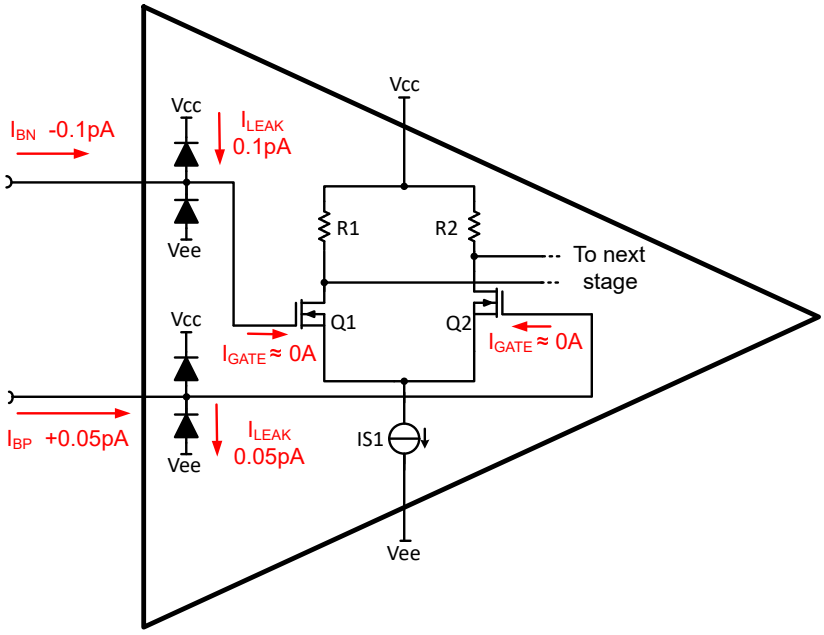


Figure 2-6. Input Bias Current on Input on Input of CMOS Op Amp

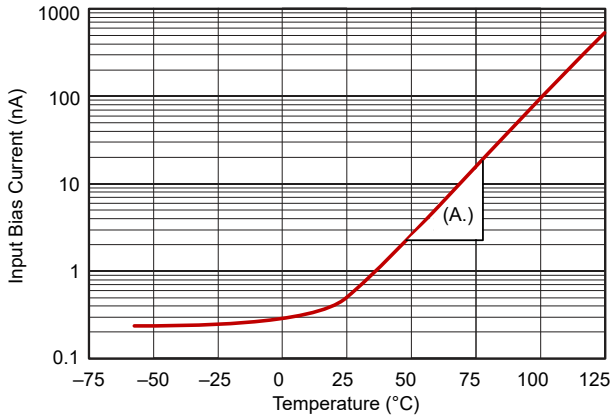
I_B is generally specified in the data sheet table at room temperature and across different temperature ranges (see Table 2-1). The data sheet table generally only tells the maximum bias current over temperature. The characteristic curves provide additional detail to help understand the shape of the I_B vs temperature curve (see Figure 2-7). This relationship is quite different when comparing bipolar to CMOS/JFET devices. Because I_B in CMOS and JFET devices is mainly from the leakage of the input ESD diodes, the I_B drift over temperature is the change in leakage current over temperature. In general, the leakage of a silicon diode doubles every 10°C. Thus, at room temperature the I_B for a CMOS device is typically in the low pico-amp level, and at high temperatures the I_B can increase to nano-amp levels (see Figure 2-7).

For bipolar devices the I_B versus temperature relationship is more complex. It depends on the overall biasing temperature coefficient of the input stage and also on the relationship between current gain and temperature. Thus, the input bias current of some bipolar devices is constant over temperature (in zero-TC biasing), some devices increase over temperature in PTAT (*proportionate to absolute temperature*) biasing, and others decrease over temperature in CTAT (*counter to absolute temperature*) biasing. The temperature coefficient for these biasing schemes is mainly valid below 85°C. Above 85°C the input bias current for bipolar devices typically increase by a factor of 3× to 5× due to a decrease in the beta of the input transistors. In CMOS or JFET devices the input bias current usually increases by a factor of 1000× between room temperature and 125°C due to the ESD diode leakage doubling every 10°C (see Figure 2-7).

Figure 2-7 compares I_B over temperature for a CMOS device to the bipolar device shown in Figure 2-8. The CMOS graph vertical axis is logarithmic and I_B increases from about 200fA to 500pA across temperature (increases by 2,500×). Conversely, the bipolar amplifier bias current increases slightly at 85°C by a factor of 2× or 3×. Although the CMOS device current increases by a much higher factor than that of the bipolar device, the absolute magnitude of the I_B in bipolar is larger. In the example curve you can see the bipolar has I_B above 3nA at 125°C, whereas the CMOS device has I_B of 0.5 nA at 125°C. Thus, at high temperature the example CMOS device has lower bias current than the bipolar device. The key point here is that when performing error analysis for I_B on CMOS devices, it is very important to consider the operating temperature range of the application.

Table 2-1. Bias Current Over Temperature for OPA392

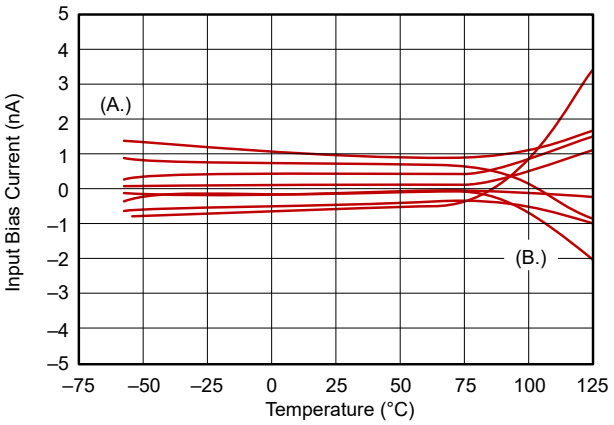
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_B	Input bias current	T_A = 25°C		±0.01	±0.8	pA
		T_A = -40°C to 125°C			±30	
I_{OS}	Input offset current	T_A = 25°C		±0.01	±0.8	pA
		T_A = -40°C to 125°C			±30	



OPA350

A. I_B doubles every 10°C.

Figure 2-7. CMOS Input Bias Current vs Temperature



OPA277

A. Curves represent typical production units.

B. I_B increases 2× or 3× at high temperature.

Figure 2-8. Bipolar Input Bias Current vs Temperature

2.2 Derivation of I_B Conversion to V_{OS}

Figure 2-9 shows the op amp model for bias current. Using the principle of superposition, you can determine the offset shift for each of the bias current sources separately, then combine the result. In superposition, only one source is considered at a time and the unused current sources are replaced with opens while the unused voltage sources are replaced with shorts. Figure 2-10 shows the superposition diagram for calculation of the output offset due to I_{BN}. Considering the amplifier to be ideal, there is a virtual short between the inverting and non-inverting input terminals. Since the non-inverting input is grounded, the inverting input is virtually grounded and the voltage across R_G is 0 V. Thus, there is no current through R_G so all the bias current flows through R_F. The output offset is $I_{BN}R_F$ (see Equation 27). This offset can be referred to the input by dividing its magnitude by the op amp closed loop gain. Simplifying this equation yields Equation 28. Thus, the offset referred to the input from I_{BN} is the bias current multiplied by the parallel combination of R_F and R_G.

$$V_{IBN\_RTO} = I_{BN}R_F \tag{27}$$

$$V_{IBN} = \frac{V_{IBN\_RTO}}{G} = \frac{I_{BN}R_F}{R_F/R_G + 1} = I_{BN}\left(\frac{R_F R_G}{R_F + R_G}\right) = I_{BN}(R_F \mid\mid R_G) \tag{28}$$

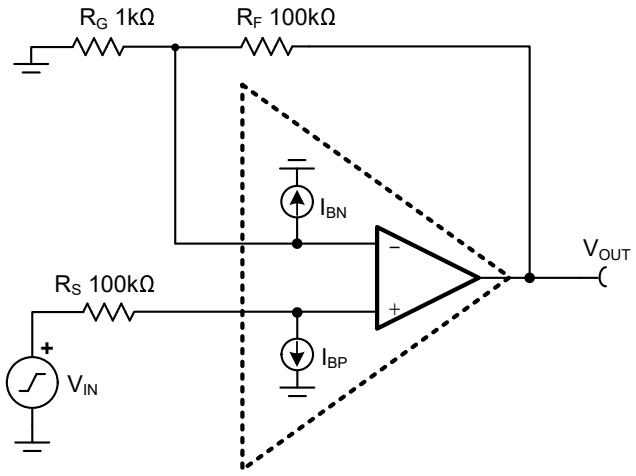


Figure 2-9. Op Amp Model for Bias Current

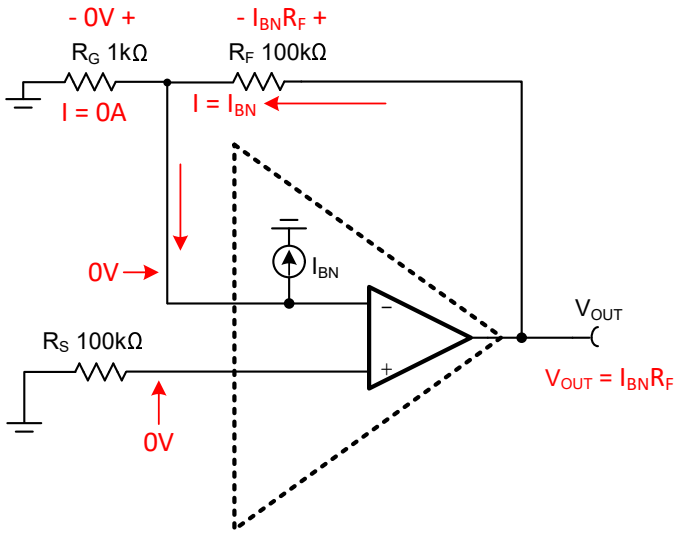


Figure 2-10. Offset Due to I_{BN} for Superposition Calculation

Figure 2-11 shows the superposition diagram for calculation of the output offset due to I_{BP}. In this case the offset calculation is simply the bias current multiplied by the source impedance, $V_{IBP} = -I_{BP}R_S$. Note that when the bias current from both the inverting and non-inverting input flow in the same direction, the polarity of the offset generated by inverting and non-inverting inputs oppose each other. In cases where $I_{BN} = I_{BP}$ and both currents flow in the same direction, the feedback network impedance and source impedance can be balanced to cancel the bias current effects, $R_S = (R_F \parallel R_G)$. However, in general two CMOS input bias currents and chopper transients are not equal, so balancing their impedances may not improve the bias current generated offset voltage error much and may actually make the error worse. Section 4 covers this topic in more detail.

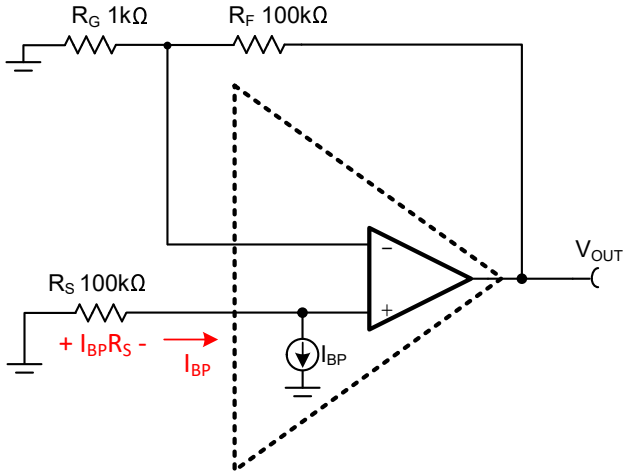


Figure 2-11. Offset Due to I_{BP} for Superposition Calculation

2.3 Internal Bias Current Cancelation

The op amp input pins are connected to the base of the transistors in the differential input pair. The bipolar transistors are current controlled devices, so base current is required to properly bias the input stage (see Section 2.1). The choice of input stage collector current biasing depends on the bandwidth, noise, and slew-rate requirement for the op amp. The base current of the input transistors will be the collector current divided by the current gain of the transistor (β). Thus, the input bias current, I_B, for bipolar devices will depend on the specific product requirements and process technology. Nevertheless, a typical range of uncorrected input bias currents is in hundreds of nano-amps to micro-amps. For some applications, the uncorrected bias current value would introduce large errors that would be considered unacceptable. To solve this issue, the integrated circuit design method *bias current cancellation* is used to significantly reduce bias current.

The input bias current cancellation is a method where the transistor base current is monitored and an equal but opposite current is summed into the op amp input terminal to cancel the base current (see Figure 2-12). If the cancellation circuit worked perfectly, the input bias current seen from outside of op amp would reduce to zero. However, there is a tolerance in the canceling current so that some residual bias current remains. Typically, the improvement due to input bias current cancellation reduces I_B by a factor of 100. Figure 2-12 shows the bias current reduced from 10 nA to about 1 nA. Also, without bias current cancellation the bias current of bipolar devices always flows in the same direction. For an NPN device, base current flows into the base, and for PNP it flows out of the base. However, when bias current cancellation is used, the residual current after the correction can flow in either direction.

Using bias current cancellation also has an impact on input bias current offset (I_{OS}). In general, for devices that do not use bias current cancellation the I_B tends to be much larger than I_{OS} (approximately 10x). This is because the input transistors are well matched. Conversely, when bias current cancellation is used the residual I_B left after the cancellation is an error term, and the two inputs is no longer well matched. Thus, for devices that use bias current cancellation I_B is approximately the same magnitude as I_{OS}. When $I_B >> I_{OS}$, the impact of I_B can be reduced by matching the impedance of the feedback network and non=inverting input of the op amp. Conversely, when $I_B \cong I_{OS}$, matching the impedances no longer helps reduce the effects of I_B and may in fact double the error.

Table 2-2, and Table 2-3 compare a device without I_B cancellation to one with I_B cancellation. Most important notice that the absolute magnitude of I_B is much lower when I_B cancellation is used (-35 nA vs ±4.5 nA). Also, notice that without I_B cancellation $I_B >> I_{OS}$, but with cancellation $I_B \approx I_{OS}$. Finally, notice that without I_B cancellation, the polarity of I_B is in one direction, whereas it is in both directions with I_B cancellation (-35 nA vs ±4.5 nA). The negative polarity for I_B without I_B cancellation indicates an PNP input structure.

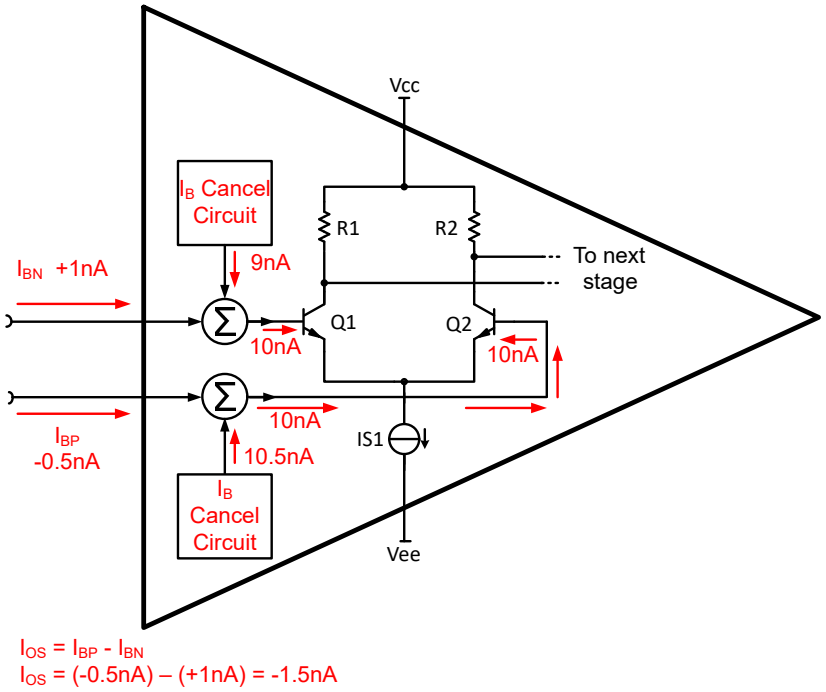


Figure 2-12. Internal Bias Current Cancellation

Table 2-2. I_B and I_{OS} for Device Without Bias Current Cancellation (LM358B)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LM358B | INPUT BIAS CURRENT						
I_B	Input bias current			-10	-35	nA
		T_A = -40°C to 85°C			-60	
I_{OS}	Input offset current			±0.5	±4	nA
		T_A = -40°C to 85°C			±5	

Table 2-3. I_B and I_{OS} for Device with Bias Current Cancellation (OPA209)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPAx209 | INPUT BIAS CURRENT							
I_B	Input bias current	V_{CM} = 0 V	T_A = 25°C		±1	±4.5	nA
			T_A = -40°C to 125°C			±15	
I_{OS}	Input offset current	V_{CM} = 0 V	T_A = 25°C		±0.7	±4.5	nA
			T_A = -40°C to 125°C			±15	

2.4 Super Beta Input Transistors

Bipolar transistor current gain (beta, β) is the ratio of collector current to base current ($\beta = I_C/I_B$). A typical bipolar transistor used for op amps IC designs has a beta of 50 to 150 A/A. Super-beta transistors undergo additional processing to achieve beta exceeding 1,000 A/A. Since super-beta transistors have high current gain, the base current required to achieve a target collector current can be much lower than traditional bipolar transistors. The collector current of the differential input pair determines the bandwidth, slew-rate, noise, and other parameters. Thus, bipolar op amps that use super beta transistors have lower base current than comparable traditional bipolar op amps. The lower I_B not only lowers the error caused by the conversion of I_B to input offset voltage, but additionally improves the input bias current noise ($i_n = \sqrt{2qI_B}$). The super-beta technology can also be used with input bias current cancellation to further reduce I_B. Figure 2-13 compares the base current of a bipolar transistors with and without I_B cancellation to a super-beta transistor with I_B cancellation. The combination of both super-beta and bias current cancellation reduce I_B by a factor of 100 when compared to traditional amplifiers. Super-beta Input Amplifiers: Features and Benefits provides more details on this technology.

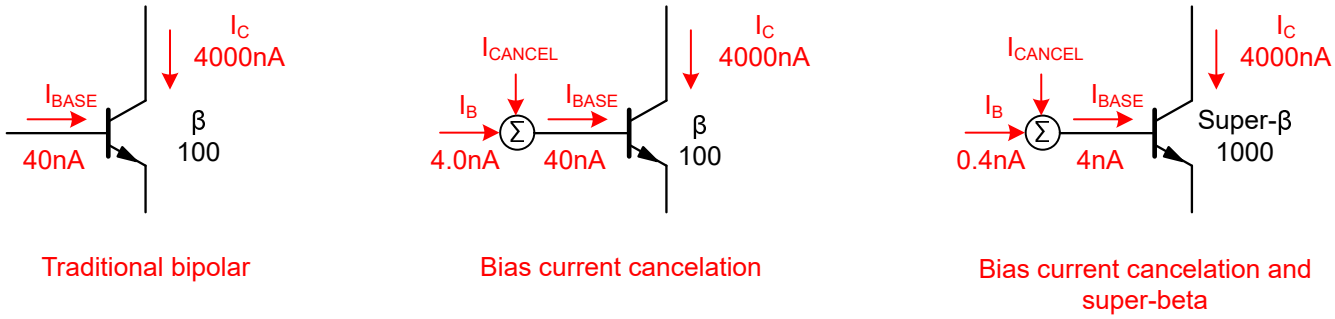


Figure 2-13. Super-beta vs Traditional Approaches

3 Other Factors Influencing Offset

This section covers several different factors that can cause a shift in V_{OS}. This section used OPA210 in calculations and simulations examples. Table 3-1 lists an excerpt of the OPA210 data sheet for use in the examples. Because Texas Instruments spice models use typical parameters, the calculations all use typical parameters for easy comparison.

Table 3-1. Electrical Specifications from OPA210 Data Sheet

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage			±5	±35	µV
A_{OL}	Open-loop voltage gain	R_L = 10 kΩ, T_A = 25°C	126	132		dB
		R_L = 10 kΩ, T_A = -40°C to 125°C	120			dB
		RL = 600Ω, T_A = 25°C	114	120		dB
		R_L = 600Ω, T_A = 25°C TO 125°C	110			dB
CMRR	Common-mode rejection ratio	(V–) + 1.5 V < V_{CM} < (V+) – 1.5 V	132	140		dB
PSRR	V_{OS}vs power supply	V_S = ±2.25 V to ±18 V		0.05	0.5	µV/V

3.1 Finite Open Loop Gain (A_{OL})

The open-loop-gain (A_{OL}) for an op amp is defined as the change in output over the change in the differential input of the op amp. For an ideal op amp the differential input is considered to be zero and the A_{OL} is infinite. For a practical op amp, however, the differential input is the input offset voltage (V_{OS}) and the open loop gain is typically on the order of 1 MV/V or 120 dB. The equation for A_{OL} is $A_{OL} = \Delta V_{OUT} / \Delta V_{OS}$ or $20\log(\Delta V_{OUT} / \Delta V_{OS})$ in decibels. Rearranging the equation shows that V_{OS} changes when the output signal changes by $\Delta V_{OS} = \Delta V_{OUT} / A_{OL}$. Figure 3-1 shows an inverting amplifier in a gain of –1 V/V where the output swings from -12 V to +12 V. Because the inverting configuration is used the common mode voltage (V_{CM}) is held constant at 0 V. Changing common mode also causes a shift in offset, so the inverting configuration is useful in illustrating the effect of A_{OL} on offset without compounding the effect with Vcm.

The specifications for the OPA210 example are shown in Table 3-1. Based on the specification, you would expect the typical offset to be ±5 µV. Notice the test condition listed at the top of the table indicates that the parameters all assume $V_{CM} = V_{OUT}$ = midsupply. However, the output voltage ranges from -12 V to +12 V, and the common mode is at 0 V. Thus, the 24 V change in output voltage will result in a corresponding 6 µV change in offset (see calculation Equation 30, and simulation Figure 3-2). In the simulation notice that V_{OS} = 5 µV specification when V_{OUT} = 0 V as expected based on the test condition.

$$A_{OL(lin)} = 10^{\left(A_{OL(dB)}/20\right)} = 10^{(132dB/20)} = 3.981 \cdot 10^{6}\,V/V \tag{29}$$

$$\Delta V_{OS} = \frac{\Delta V_{OUT}}{A_{OL(lin)}} = \frac{24\,V}{3.981 \cdot 10^{6}\,V/V} = 6.0\,\mu V \tag{30}$$

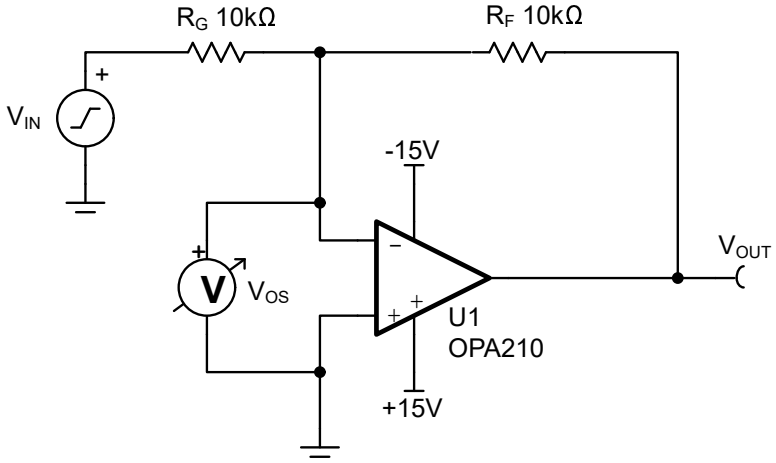


Figure 3-1. V_{OS} Shift Due to Finite A_{OL} on Inverting OPA210 Configuration

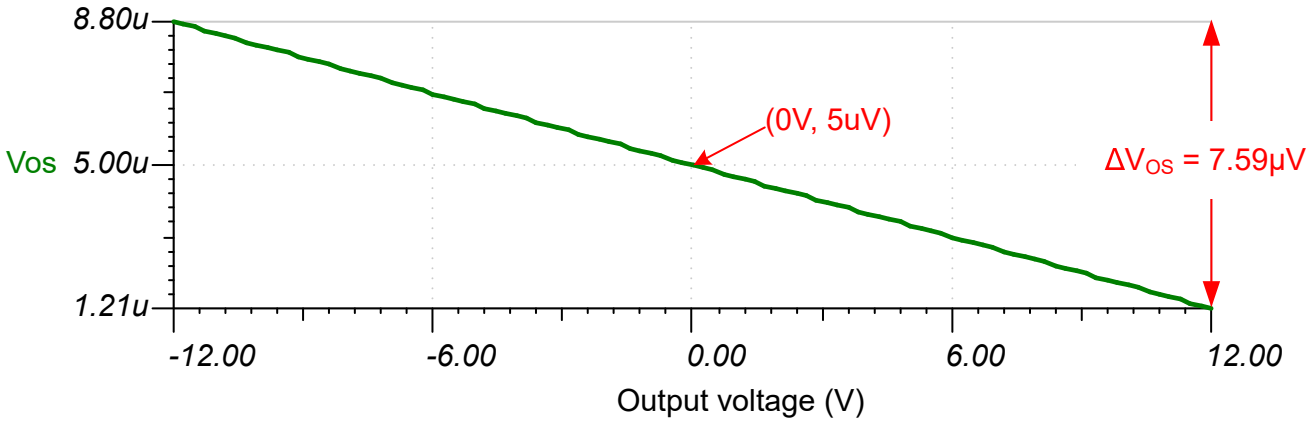


Figure 3-2. Simulated V_{OS} and Output Swing for Inverting OPA210 Circuit

3.2 Common Mode Rejection Ratio (CMRR)

The common-mode rejection ratio (CMRR) for an op amp is defined as the change in V_{OS} versus change in the common mode voltage of the op amp. For an ideal op amp, the common mode signal does not affect V_{OS} (that is, CMRR is infinite). For a practical op amp, however, the CMRR ranges from 60 dB to 170 dB. The equation for CMRR is CMRR = $\Delta V_{CM}/\Delta V_{OS}$ or $20\log(\Delta V_{CM}/\Delta V_{OS})$ in decibels.

Figure 3-3 shows a difference amplifier in a gain of 1V/V where the inputs are connected together to force the differential input voltage to zero. The voltage source (V_{IN}) swings from -24 V to +24 V, which causes the common mode voltage (V_{CM}) to swing from -12 V to +12 V. Because the differential input is 0 V (mid-supply), the output remain near zero volts. Finite A_{OL} does not affect the offset (see Section 3.1). Thus, the primary factor impacting the shift in offset voltage is change in the common mode voltage.

The specifications for the OPA210 example are shown in Table 3-1. Based on the specification, you would expect the typical offset to be ±5 µV. Notice the test condition listed at the top of the table indicates that the parameters all assume $V_{CM} = V_{OUT}$ = mid-supply. However, the common mode voltage ranges from -12 V to +12 V, and the output voltage is at 0V. The calculation for a 24V change in V_{CM} voltage shows a corresponding 2.4 µV change in offset (see calculation Equation 31). In this example, the simulated offset shift of 3.85 µV (CMRR = 136 dB) compares well to the calculated shift of 2.4 µV (CMRR = 140 dB). In the simulation notice that V_{OS} = 5 µV specification when V_{CM} = 0 V as you would expect based on the test condition.

$$\Delta V_{OS} = \frac{\Delta V_{CM}}{CMRR_{(lin)}} = \frac{24V}{10^{(140/20)}} = 2.4\ \mu V \tag{31}$$

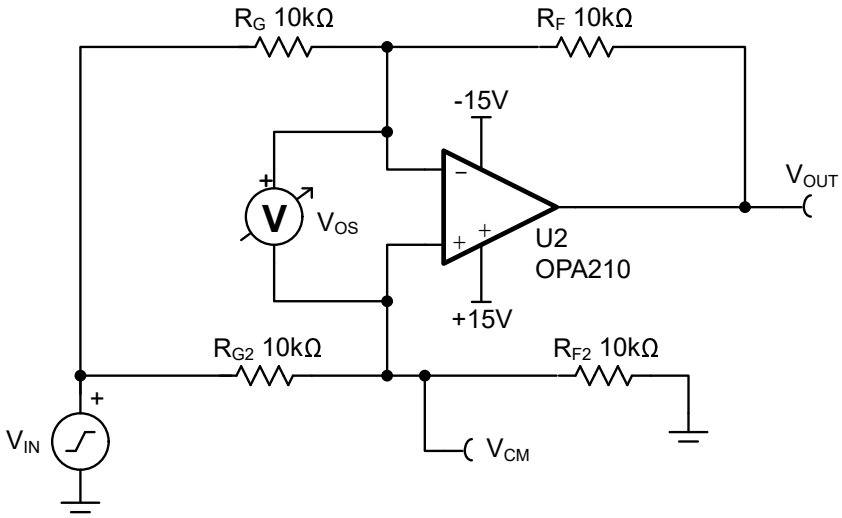


Figure 3-3. V_{OS} Shift Due to CMRR on OPA210 Difference Amp Configuration

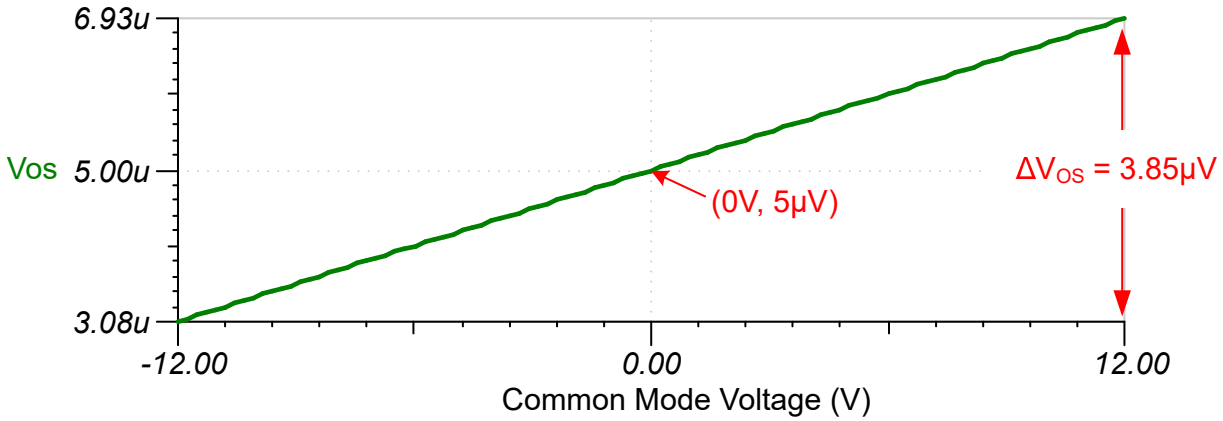


Figure 3-4. Simulated Vos and Output Swing for Difference Amp Configuration

In many cases, the effects of open loop gain and common mode rejection will be combined as in the case of unity-gain buffer (a follower with G = 1). From a calculation perspective the two calculations can be done separately and the results are combined. Simulation modela both effects and the output reflect the typical operation of the device. In this example, the model shows the slope of V_{OS} due to A_{OL} to be negative and the slope of V_{OS} vs Vcm to be positive. In general, the slope of V_{OS} vs V_{CM} can be either positive or negative, but V_{OS} due to A_{OL} will always have a negative slope. Thus, in this example the two effects are subtracted from each other.

$$\Delta V_{OS(\text{total calculated})} = \frac{\Delta V_{CM}}{CMRR_{(lin)}} - \frac{\Delta V_{OUT}}{A_{OL(lin)}} = \frac{24V}{10^{(140/20)}} - \frac{24V}{10^{(132/20)}} = -3.63\mu V \quad (32)$$

$$\Delta V_{OS(\text{total simulated})} = \Delta V_{OS(CMRR)} - \Delta V_{OS(AOL)} = 3.85\mu V - 7.59\mu V = -3.74\mu V \quad (33)$$

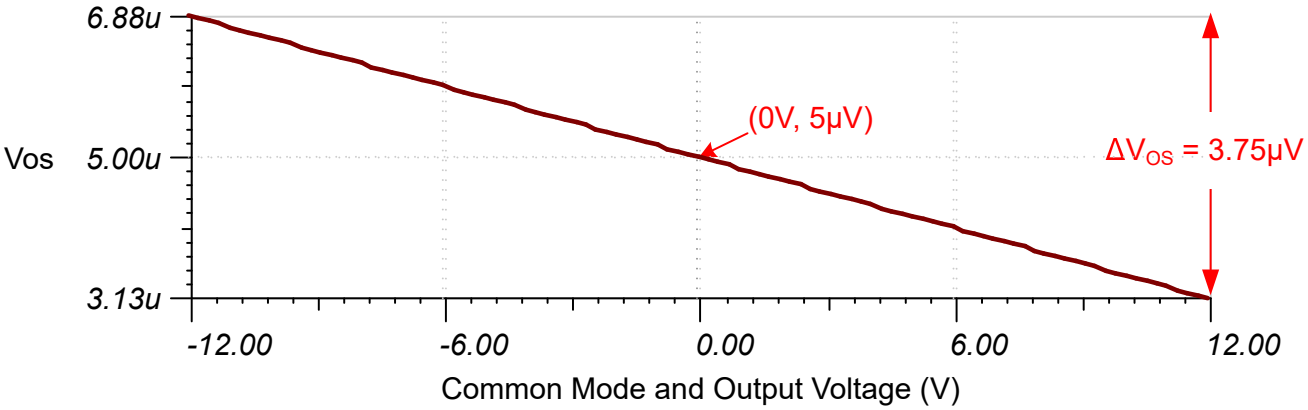


Figure 3-5. Combined Effects of A_{OL} and V_{CM} on V_{OS}

3.3 Power Supply Rejection Ratio (PSRR)

The power supply rejection ratio (PSRR) for an op amp is defined as the change in V_{OS} versus change in the power supply voltage of the op amp. For an ideal op amp, the power supply voltage do not affect V_{OS} (i.e. PSRR is infinite). For a practical op amp, however, the PSRR ranges from 60 dB to 166 dB (1000 µV/V to 0.005 µV/V). The equation for PSRR is PSRR = $\Delta V_{OS}/\Delta V_S$ or $20\log(\Delta V_{OS}/\Delta V_S)$ in decibels. Figure 3-6 shows a buffer amplifier in a gain of 1V/V where the noninverting input is grounded. Both the positive and negative supply are shifted in equal amounts to maintain a 0 V common mode voltage. Because V_{CM} = 0 V and V_{OUT} = 0 V, the CMRR and A_{OL} does not change the offset, so the power supply rejection is the only factor shifting offset.

The specifications for the OPA210 example are shown in Table 3-1. Based on the specification, you would expect the typical offset to be ±5 µV. Notice the test condition listed at the top of the table indicates that the parameters all assume V_S =±15 V, and V_{CM} = V_{OUT} = midsupply. In this case, V_{CM} and V_{OUT} are at midsupply (V_{CM} = V_{OUT} =0 V), but the supply is shifted from ±15 V to ±10 V. The 10V change in V_S voltage causes a corresponding 0.5µV change in offset (see calculation Equation 34, and simulation Figure 3-6).

$$\Delta V_{OS} = \frac{\Delta V_S}{PSRR_{(lin)}} = \frac{10V}{10^{(146/20)}} = 0.5\ \mu V \quad (34)$$

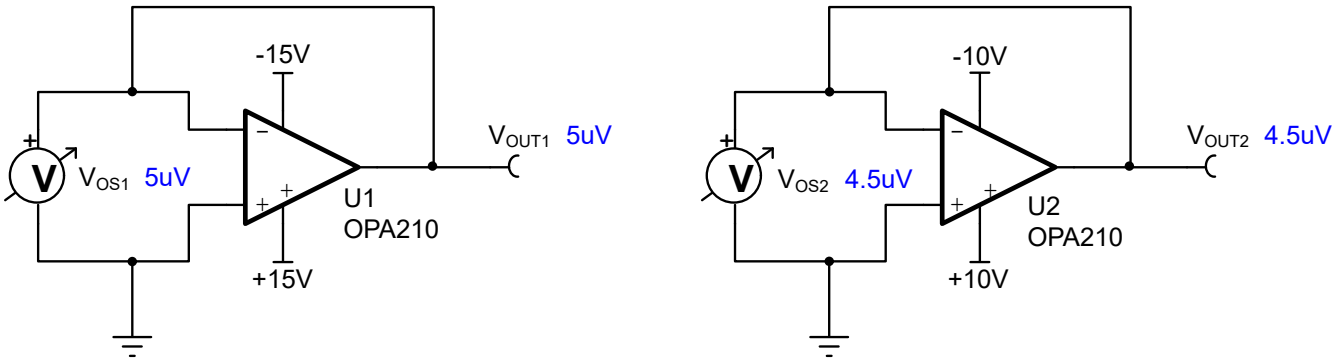


Figure 3-6. V_{OS} Shift Due to PSRR on OPA210 Difference Amp Configuration

Making an asymmetrical change in the power supply voltage causes a shift in V_{OS} due to both common mode rejection and power supply rejection. Remember, the test condition at the top of the specification table says that V_{CM} = V_{OUT} = mid-supply. For a ±15 V supply, midsupply is 0 V, so V_{CM} = 0 V meets the test condition. When an asymmetric change is made on the power supply, the common mode voltage shifts relative to the test condition. For example, if the supply changes from (+15 V, -15 V) to (+15 V, -5 V), midsupply value shifts from 0 V to 5 V. This is effectively a 5 V change in common mode and V_{OUT} as well as a 10 V change in power supply, so PSRR, A_{OL}, and CMRR must be considered. Conversely, if the supply changes from (+15 V, -15V) to (+10 V, -10 V), midsupply is 0 V, for both cases, and only PSRR impacts V_{OS}.

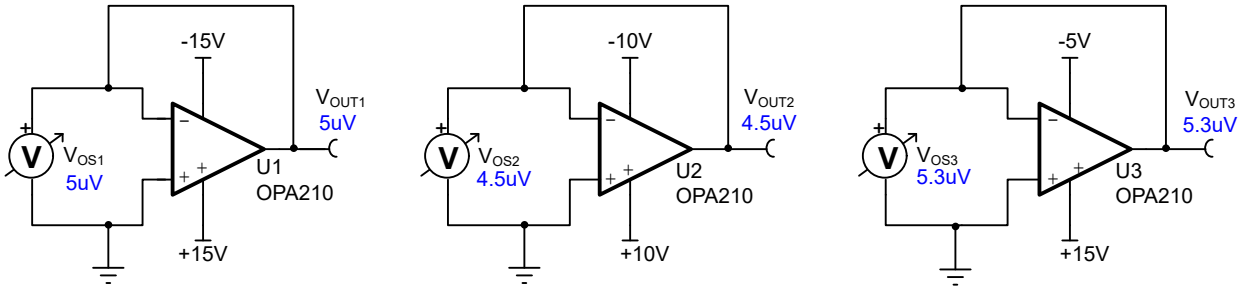


Figure 3-7. V_{OS} Shift Due to PSRR and CMRR When Supplies Are Asymmetrical

3.4 A_{OL}, CMRR, and PSRR Over Frequency

Open-loop gain, common mode rejection ratio, and power supply rejection all decrease over frequency. Generally, this frequency response is a first-order response. That is, the response is flat at low frequency then begin to roll-off at 20 dB/decade afterwards. This roll-off over frequency means that the offset introduced by these parameters increases at higher frequencies. Furthermore, these bandwidth limitations are small signal responses. A small signal generally means that the signal needs to be less than 10 mV, but the requirement can be different depending on the design or technology. For larger signals, the response may differ from the specified small-signal response because of slew-rate limitation of the amplifier. These slew-rate limitations are sometimes referred to as *full-power bandwidth* limits.

Figure 3-8 is a simulation example that adds an AC signal on the positive supply. This circuit condition simulates a noise signal on the amplifiers power supply. The AC signal causes variations in the power supply over frequency, so PSRR is being tested. However, because the power supply change is non-symmetrical, CMRR limitations is also being exercised. Finally, because the output signal is not held constant, A_{OL} limitations also affect the result. In addition to showing how A_{OL}, CMRR, and PSRR change over frequency, this simulation also illustrates how simulation can be used to solve a complex issue with many factors interacting. Figure 3-9 compares the PSRR curve from the data sheet to the PSRR simulation of Figure 3-8.

In general, bode plots such as the A_{OL}, CMRR, and PSRR curves apply to sinusoidal signals. Often, noise signals applied to the power supply are not sinusoidal. To understand how the rejection curves function on non-sinusoidal curves it is helpful to use the Fourier theorem. This theorem states that any non-sinusoidal signal can be built with a series of sinusoidal signals. For example, a square wave at 100 kHz is composed of a sine wav at 100 kHz, 300 kHz, 500 kHz and other odd multiples of 100 kHz. The various multiples of the square wave frequency are called harmonics. All of the sinusoidal components can be applied to the bode plot to see how each component is affected. The SPICE simulation does this automatically, but it is useful to think of the math behind the simulator because the response to the non-sinusoidal signals may not be intuitive otherwise.

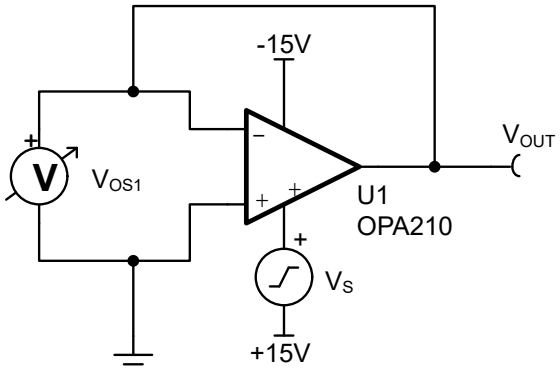


Figure 3-8. OPA210 with Noise Signal on Positive Power Supply

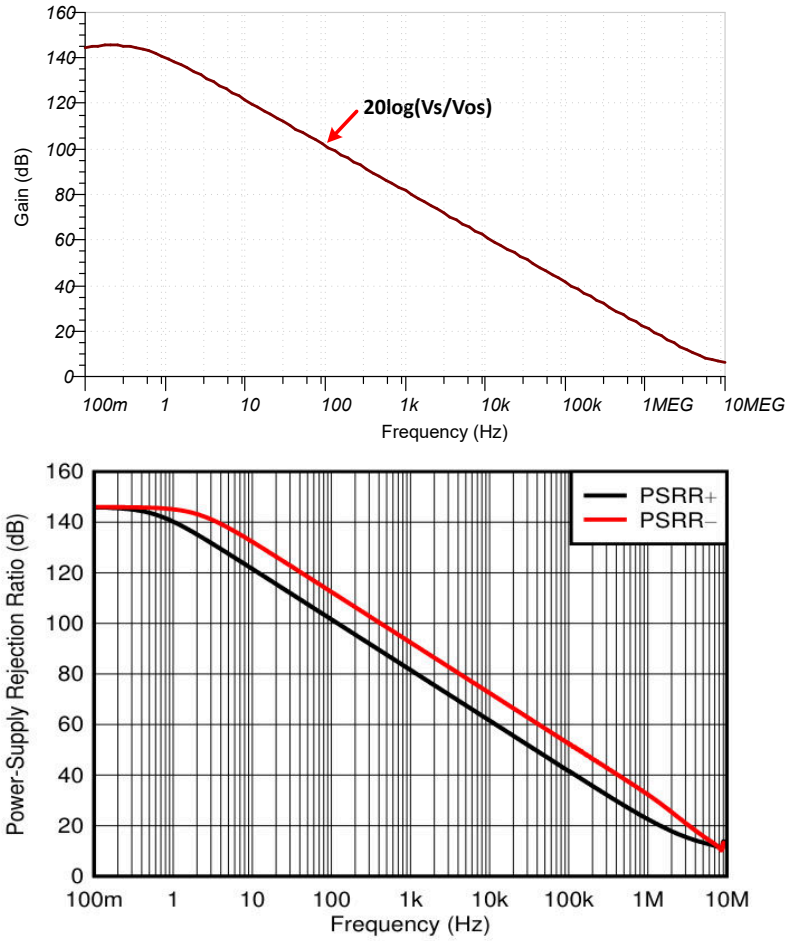


Figure 3-9. V_{OS} vs Frequency for Noise Signal on Power Supply

3.5 Electromagnetic Interference Ratio (EMIRR)

Electromagnetic interference rejection ratio (EMIRR) is a measure of how high frequency signals that are outside of the op amps bandwidth can impact V_{OS}. Specifically, the EMIRR test directly couples a sinusoidal waveform with frequency ranging from 10 MHz to 10 GHz and looks at the shift in V_{OS}. It may seem unusual that a DC parameter such as offset is affected by signals outside the bandwidth of the amplifier. However, this high-frequency AC input signal undergoes a rectification by internal diodes and is converted from a high frequency AC signal to a change in DC operation of the amplifier (V_{OS}). This test can be thought of as a conducted immunity test. The details of how the EMIRR is tested is covered in EMI Rejection Ratio of Operational Amplifiers .

Figure 3-10 shows the graph of EMIRR for OPA206. As an example, assume a 40 mVpk, 100 MHz noise signal is applied to the noninverting input of the amplifier. The shift in V_{OS} can be calculated to be 90 µV using Equation 35.

$$\Delta V_{OS} = \left(\frac{(V_{RF\_PEAK})^2}{100mVpk}\right) 10^{(-EMIRR/20)} = \left(\frac{(40mVpk)^2}{100mVpk}\right) 10^{(-45dB/20)} = 90\mu V \quad (35)$$

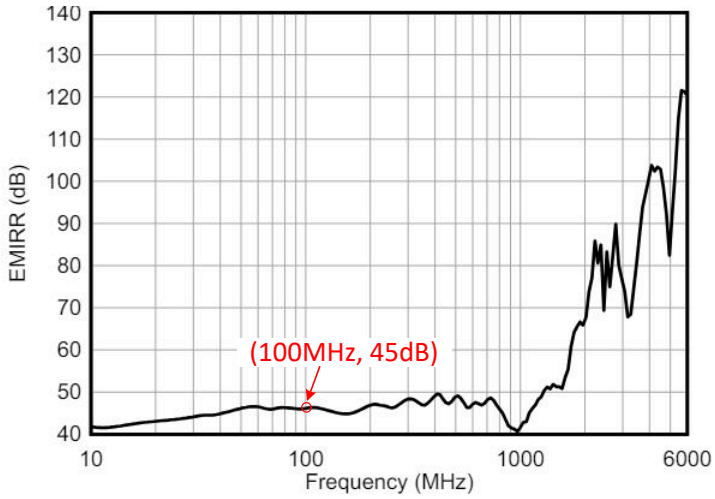


Figure 3-10. EMIRR vs Frequency for OPA206

3.6 Mechanical Stress Induced Offset Shift

Small amounts of mechanical stress applied to an integrated circuit can cause subtle shifts in operation due to the compression or tension applied to internal components. This stress can be from a flexing of the printed circuit board that the IC is mounted on or even from the soldering process. For op amps, mechanical stress is most often associated with a small shift in V_{OS}. The magnitude of offset shift depends on the amount of mechanical stress applied to the device and the devices susceptibility to stress. The internal op amp design sensitivity to stress can be improved using careful layout methods where the most sensitive internal input transistors are laid out in a symmetrical inter-digitated pattern away from the edges of the die. This symmetrical layout method minimizes the offset shift by maintaining the VBE shift on both input transistors equal ($V_{OS} = V_{BE1} - V_{BE2} \cong$ constant).

The process of soldering an op amp to a printed circuit board may also introduce a shift as large as 100 µV. However, the stresses introduced during the soldering process tend to relax over time and the device eventually returns to an offset near the pre-solder value (e.g. $\Delta V_{OS} < 10$ µV). However, at room temperature this process may take several weeks. One way to accelerate the stress relaxation process is to bake the printed circuit board at high temperature (100°C or greater) after cleaning the board. The baking softens rigidity of the IC package causing a dramatic reduction in the time required to relax the stress.

Aside from the stress introduced by solder reflow, most devices undergo parametric changes over time called long-term shift. These shifts are larger during the initial 1000 hrs of operation than later in the life of the device. Thus, the post clean baking process reduces the initial shift by curing of the molding compound of the device, so that the initial more significant effects are minimized. The long-term shift and soldering related stress effects are also important for voltage reference accuracy, and gain accuracy of instrumentation amplifiers. Long-Term Drift in Voltage References covers the background of long-term shift as well as the bake method to minimize the problem.

Flexing of the printed circuit board may also cause a shift in offset. Thus, the PCB thickness, mounting hardware, and stress introduced by connector tension can all cause shifts in offset performance. Therefore, the mechanical design, enclosure, and connections can all have some impact on electrical performance.

3.7 Parasitic Thermocouples

Whenever two dissimilar metals are connected together a thermocouple is formed. A thermocouple generates a small DC voltage that is proportionate to temperature. A parasitic thermocouple is an unintended junction of two different metals that may introduce errors. Printed circuit boards contain hundreds of parasitic thermocouples. For example, surface mount resistors normally have a tin-plated nickel end cap. This end cap is soldered to a copper trace. The copper junction with the nickel-tin end cap creates a thermocouple. There are potentially other thermocouples in this simple component where the end-cap contacts the film resistor (see Figure 3-11). Most PCB designs have hundreds if not thousands of similar components. The presence of hundreds of parasitic thermocouples may seem like a serious accuracy concern for precision DC circuits, but it generally is not a significant issue because the thermocouple voltages cancel each other when the PCB temperature is uniform. Thus, the parasitic thermocouple effect is a concern only for precision DC systems that have a temperature gradient on the PCB. This gradient may be due to high power dissipation on a localized portion of the PCB or an adjacent heat source that is not uniformly applied to the PCB.

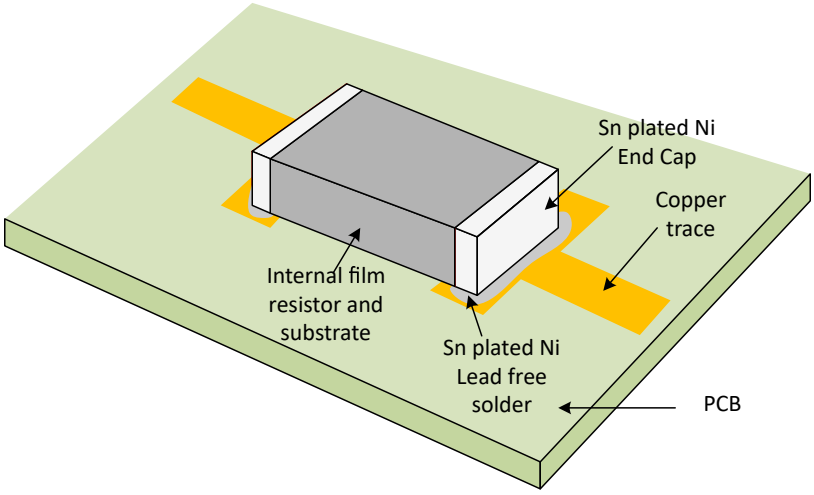


Figure 3-11. Mechanical Connections on a Resistor Showing Dissimilar Metal Junctions

Figure 3-12 and Figure 3-13 show a single horizontally modeled resistor with a vertical and horizontal temperature gradient. For the vertical temperature gradient, the parasitic thermocouples are at the same temperature, so the junction voltages cancel each other (Verror = 0 V). Conversely, with the horizontal temperature gradient the two junctions are no longer at the same temperature, so the errors do not fully cancel out (Verror = 20 µV).

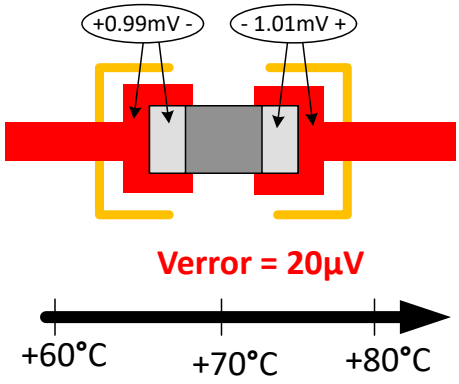


Figure 3-12. Horizontal Mounted Resistor with Vertical Temperature Gradient

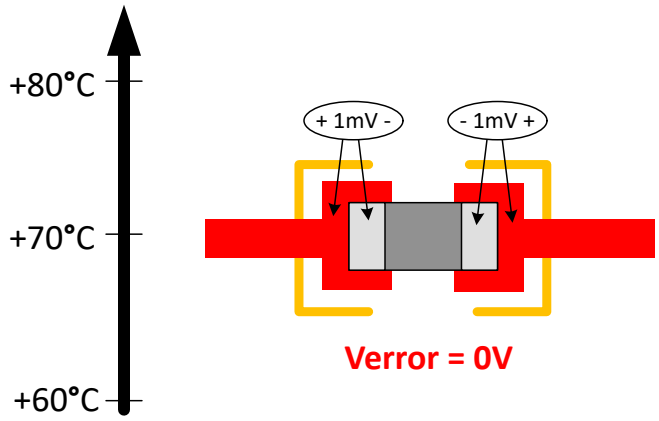


Figure 3-13. Vertical Mounted Resistor With Horizontal Temperature Gradient

Figure 3-14 and Figure 3-15 show a low thermal EMF resistor layout. This layout can be used in precision DC applications that have large temperature gradients to minimize the parasitic thermocouple effect. This two-resistor series layout can replace the single resistor shown in Figure 3-12 and Figure 3-15. Figure 3-14 shows that with a vertical temperature gradient the two resistors each develop an equal error voltage, but the two error voltages cancel out each other (Verror = +10 µV - 10 µV = 0 V). Figure 3-15 shows that with a horizontal temperature gradient the two resistors are each at a different temperature, but each resistor is at a constant temperature. That is, the resistor on the left is at approximately 65°C and the resistor on the right is at approximately 75°C. The important point here is that each individual resistor is at a uniform temperature so the thermocouples on that resistor cancel each other for a net error of 0 V.

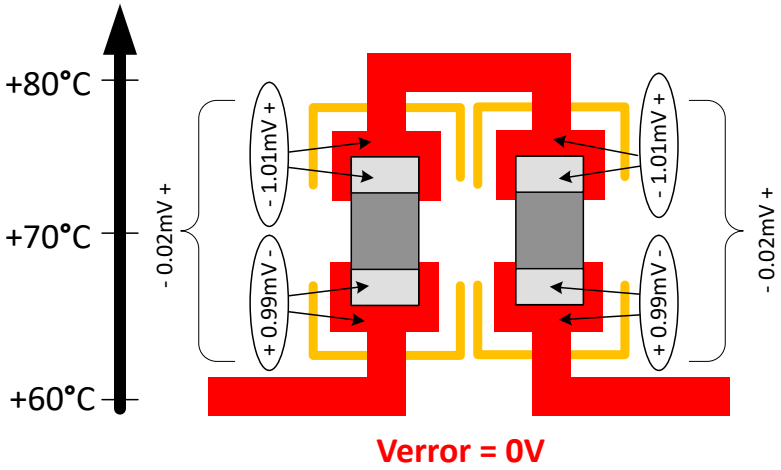


Figure 3-14. Two-resistor Low Thermal EMF Layout with Vertical Temperature Gradient

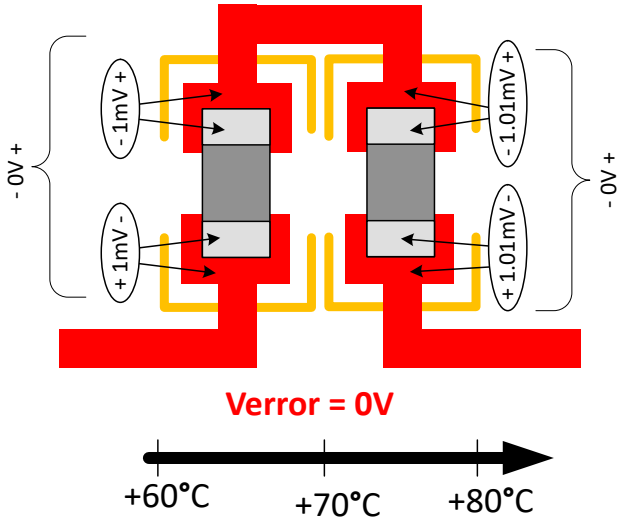


Figure 3-15. Two-resistor Low Thermal EMF Layout with Horizontal Temperature Gradient

3.8 Flux Residue and Cleanliness

Solder flux is a chemical that helps promote good solder junctions by cleaning the surface of oxidation and enhances the flow of solder connections. After completing the soldering process, it is important to properly clean the surface of the PCB to remove residual solder flux. Residual solder flux has a high impedance that changes over time, humidity, and temperature. Solder flux residue is most problematic in applications involving high impedance circuits. For example, a low power op amp might use 100 kΩ or larger feedback resistors to minimize power consumptions. In this case, the solder flux residue forms parasitic paths on the feedback network that introduce gain error. This error is more significant for larger value feedback resistors as the flux impedance is typically high. Different types of flux require different solvents and cleaning methods, so for best result refer to the solder flux manufacture recommendations. For example, water soluble solder flux is frequently cleaned in an ultrasonic water bath at 60°C. The ultrasonic vibrations help break free the flux material. For assemblies with mechanical devices (such as relays) an ultrasonic clean and immersion in fluid is not practical as this process could damage the mechanical components. In case fluid immersion is not practical, a spray type clean can be used.

Figure 3-16 shows a circuit with solder-flux residue that was not cleaned. The solder-flux residue looks like a clear thick substance resembling a syrup. The circuit impacted by the solder-flux is a bridge sensor amplified by an instrumentation amplifier (see Figure 3-17). Figure 3-18 and Figure 3-19 show how different levels of contamination can affect the amplifier inverting input and output over time. The no-clean results show very large drifting over time. This drift is affected by temperature and humidity. The graphs show qualitatively that flux can have a significant impact on performance and the effect is especially significant on high-impedance circuits.

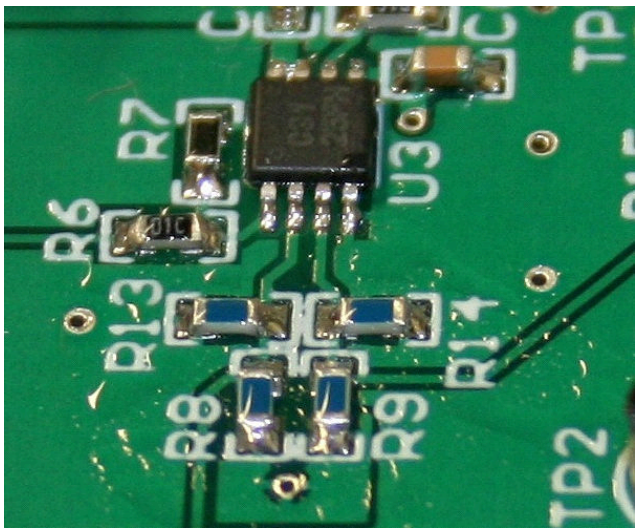


Figure 3-16. PCB Flux Residue

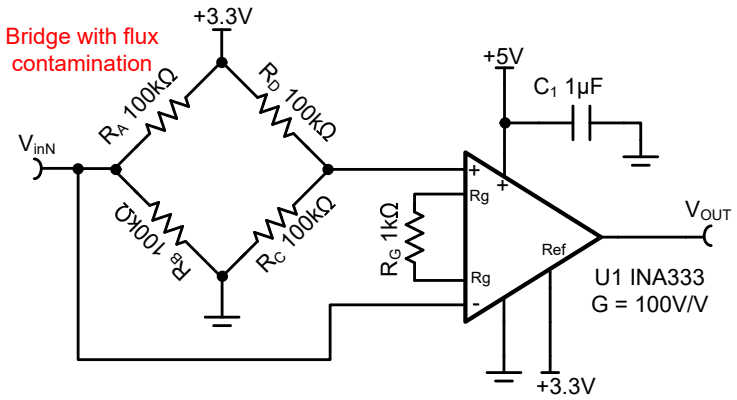


Figure 3-17. Bridge Amplifier with Flux Contamination

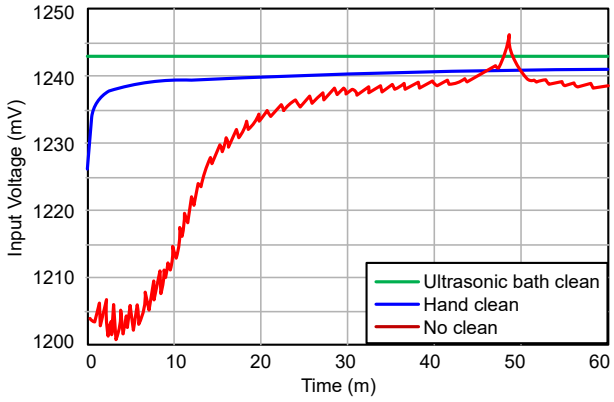


Figure 3-18. Flux Impact on Amplifier Input

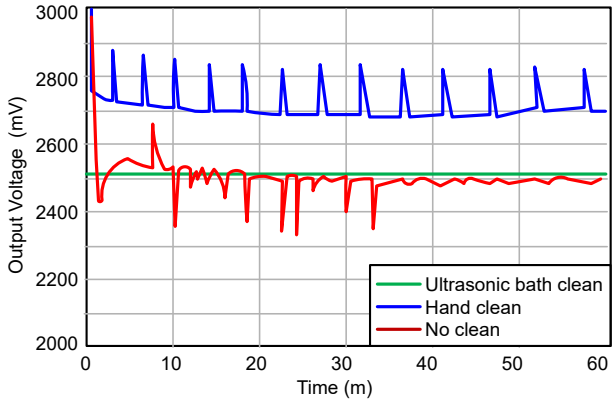


Figure 3-19. Flux Impact on Amplifier Output

Some very high impedance applications require and extremely thorough PCB clean as well as special handling requirements. In general, these very sensitive applications use very high-impedance sensors such as a pH sensor (R_S > 100MΩ). These types of applications generally require multiple cleans using different solvents. In ultra-high impedance applications it is important to avoid directly handling the PCB as oil, moisture, and salt from skin can introduce errors. Furthermore, these applications also may require the use of a PCB guard trace to minimize leakage currents. Details on these ultra-low bias current applications are covered in the low leakage design series Part 1, Part 2, and Part 3.

4 Zero-drift Amplifiers to Minimize V_{OS} and V_{OS} Drift

Zero-drift amplifiers use an internal circuitry to continuously correct the V_{OS} and V_{OS} drift. Chopper and auto-zero are two different architectures used to achieve the V_{OS} correction, so the terms zero-drift, chopper, and auto-zero are often used interchangeably. The internal offset correction generally reduces maximum V_{OS} to less than 10µV and V_{OS} drift to less than 0.05µV/°C. Other parameters such as A_{OL}, PSRR, CMRR, and EMIRR are also improved by the reduction in offset. The main limitation of zero-drift amplifiers are input bias current transients from switching charge injection and clock-feedthrough. These transients can translate into an additional V_{OS} when large feedback resistors are used. Also, this transient can introduce unwanted noise tones at the zero-drift auto-correction frequency. The application note, Optimizing Chopper Amplifier Accuracy covers details on using zero-drift amplifiers and minimizing the errors introduced by the I_B transients.

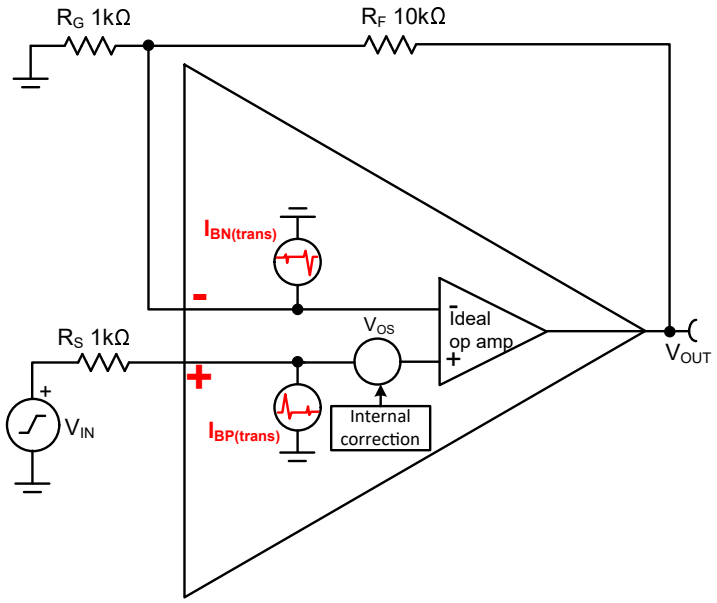


Figure 4-1. Zero-drift Amplifier V_{OS} Correction and I_B Transients

5 Calibration of V_{OS}, IB, and Gain Error

Calibration is the process where a system is measured to understand error sources and the errors are mathematically corrected. In many cases a micro-controller (where calibration coefficients are stored in a local EEPROM) performs the mathematical correction. The discovered errors are generally unique for each product, so each product needs to be individually calibrated. In the case of amplifiers, calibration can minimize the offset and gain error. For amplifiers, gain error is primarily due to resistor tolerance. Any deviation of the resistor value from the nominal value introduces a gain error.

Figure 5-1 shows a simple non-inverting op amp circuit and its associated DC transfer characteristic. To calibrate gain and offset of this circuit, two precision test signals need to be applied to the input. Generally, full system calibration includes error sources, multiple amplifier stages, as well as an analog to digital converter, but the same approach can be used as given in this simple example. The two calibration test signals need to be on the linear portion of the transfer function or the calculated gain and offset errors cannot be correct. In this example, an input signal of 0 V is not an acceptable calibration signal because the amplifier is nonlinear due to output swing limitations for a 0 V input signal. This example uses input signals of 0.25 V and 2.25 V to achieve an ideal output range of 0.5 V to 4.5 V. It is also important that the calibration signals are very accurate and low noise. Calibrating in non-linear regions or using noisy calibration signals can actually introduce additional error rather than correct the systems inherent error. See Op Amp Input and Output Swing Limitations for details on determining the linear range of amplifiers.

Equation 36 shows the general straight-line equation used in calibration of linear systems. Equation 37 and Equation 38 show the calculation of the gain and offset calibration coefficients. The ideal value for gain is 2.0 V/V, but 2.00088 V/V was measured due to resistor tolerance. Also, the ideal offset would be 0 V, but an offset of 31.25 µV was calculated. Equation 39 shows how the calibration coefficients can be used to correct the gain and

offset error to determine a more accurate value for V_{IN}. This approach can be used to correct any signal in the amplifiers linear range. The simulation results for this example show that when the output is at 2.5 V, the input is at 1.2494 V. A circuit input of 1.25 V for a 2.5 V output (G = 2 V/V, V_{OS} = 0 V) is best. The calibration calculation determines a more accurate value for the input signal by eliminating gain and offset errors.

Overall, calibration is an effective way of minimizing gain and offset error sources. However, calibrating temperature drift, and effects such as PSRR and CMRR can be challenging. The temperature drift and other secondary effects are generally minimized by selection of low error precision amplifiers and low drift precision resistor networks rather than through calibration. Chopper amplifiers, such as OPA182, have maximum V_{OS} in the low microvolt level (V_{OSMax} = ±4 µV, $V_{OSDrift}$ = ±0.012 µV/°C for OPA182). Resistor networks such as the RES11 can be used to minimize gain error and drift (gain error = ±0.05%, and gain drift = ±2 ppm/°C for RES11). Calibration can be costly as it increases the end-product manufacturing test time as well as requiring accurate calibration sources.

$$V_{OUT} = G \cdot V_{IN} + V_{Offset} \tag{36}$$

$$G = \frac{V_{OUT2} - V_{OUT1}}{V_{IN2} - V_{IN1}} = \frac{4.502 - 0.50025}{2.25 - 0.25} = 2.00088\ V/V \tag{37}$$

$$V_{Offset} = V_{OUT1} - G \cdot V_{IN1} = 0.50025 - 2.00088 \cdot 0.25 = 31.25\mu V \tag{38}$$

$$V_{IN} = \frac{V_{OUT} - V_{Offset}}{G} = \frac{2.5V - 31.25\mu V}{2.00088\ V/V} = 1.2494V \tag{39}$$

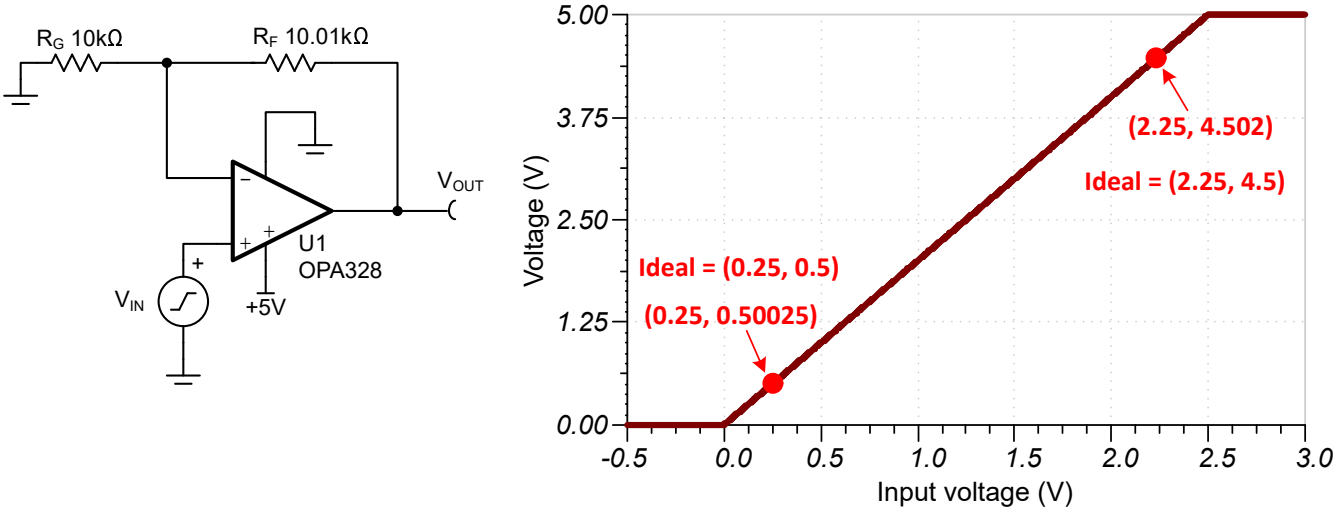


Figure 5-1. Op Amp DC Transfer Characteristic for Calibration

6 References

- Wiliams, I., "Why Should I Give a Flux?", Precision Hub Blog, September 2013, https://e2e.ti.com/blogs_/archives/b/precisionhub/posts/why-should-i-give-a-flux
- "Solder Flux - A Basic Introduce Is Here - NextPCB", www.nextpcb.com, Solder Flux - A Basic Introduce Is Here - NextPCB
- Blake, K., "Op Amp Precision Design: PCB Layout Techniques", 2009, https://ww1.microchip.com/downloads/en/AppNotes/01258B.pdf
- Grohe, P., "Design femtoampere circuits with low leakage, part 1", November 2011, https://www.edn.com/design-femtoampere-circuits-with-low-leakage-part-one/
- Grohe, P., "Design femtoampere circuits with low leakage, part 2: Component selection", November 2011, https://www.edn.com/design-femtoampere-circuits-with-low-leakage-part-2-component-selection/
- Grohe, P., "Design femtoampere circuits with low leakage, part 3: Low-current design techniques", September 2012, https://www.edn.com/design-femtoampere-circuits-with-low-leakage-part-3-low-current-design-techniques/

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2024	*	Initial Release

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