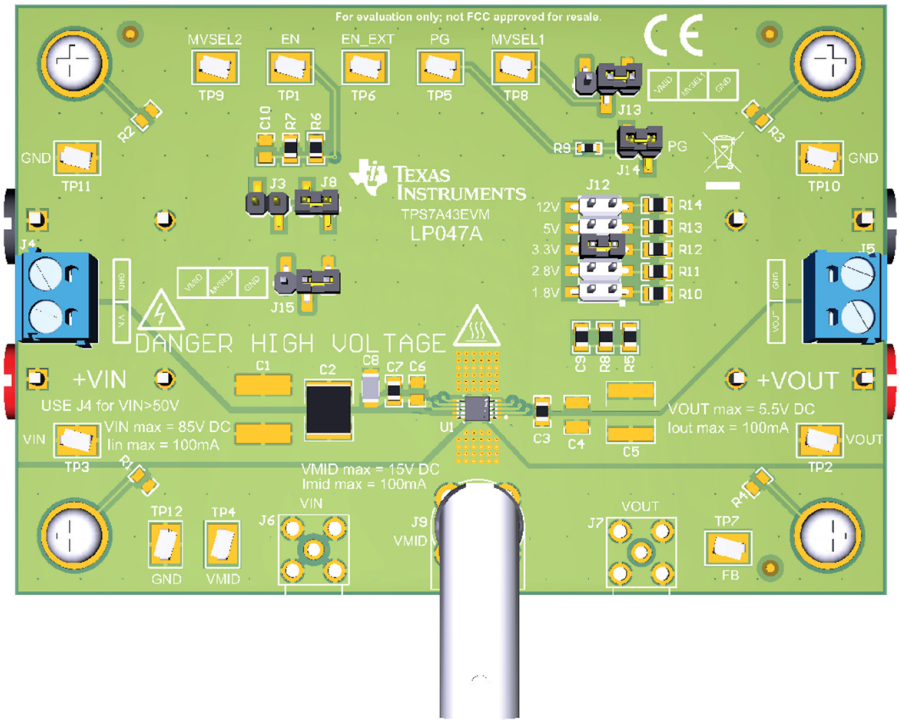
User's Guide

TPS7A43EVM-047 Evaluation Module

ABSTRACT



This user's guide describes the operational use of the TPS7A43EVM-047 evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS7A4301DGQ, low-dropout linear regulator (LDO). Included in this user's guide are setup and operating instructions, layout guidelines, a printed circuit board (PCB) layout, a schematic diagram, and a bill of materials (BOM). Throughout this document, the terms demonstration kit, evaluation board, and evaluation module are synonymous with the TPS7A43EVM-047.

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1 Introduction

Texas Instruments' TPS7A43EVM-047 EVM helps design engineers evaluate the operation and performance of the TPS7A4301DGQ linear regulator for possible use in their own circuit application. This particular EVM configuration contains a single 50-mA, high-voltage, low-IQ, dual output low-dropout regulator for general applications. The regulator is capable of delivering up to 50 mA split between the 2 outputs and has a wide VIN range of up to 85V. For stability for the TPS7A4301DGQ, use a 1µF (or larger) output capacitor Cout and at least 3*Cout for the middle output.

1.1 Before You Begin

This evaluation module is not encapsulated and has exposed terminals with voltages that are connected to the main power supply; the following warnings are noted for the safety of anyone using or working close to the TPS7A43EVM-047. Observe all safety precautions.

WARNING

Failure to adhere to these steps or to not heed the safety requirements at each step may lead to shock, injury, and damage to the hardware. Texas Instruments is not responsible or liable in any way for shock, injury, or damage caused by negligence or failure to heed advice. If you are not trained in the proper safety of handling and testing power electronics please do not test this evaluation module.

WARNING

Danger: HIGH VOLTAGE! This evaluation board is intended for professional use only. This board has exposed high voltages. Do not operate this board without proper high-voltage/high-current safety practices. Read this user guide carefully before testing with TPS7A43EVM-047. Use floating measurement equipment such as high-voltage differential scope probes and see Section 3 and Section 4 for proper EVM setup and test equipment connection.

CAUTION:

Caution! Do not leave EVM powered when unattended.

HOT SURFACE:

Caution Hot Surface! Contact may cause burns. Do not touch. Please take the proper precautions when operating.

HIGH VOLTAGE:

Danger High Voltage! Electric shock is possible when connecting the board to live wire. The board should be handled with care by a professional. For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

2 Schematic

Figure 2-1 shows the schematic for the TPS7A43EVM-047.

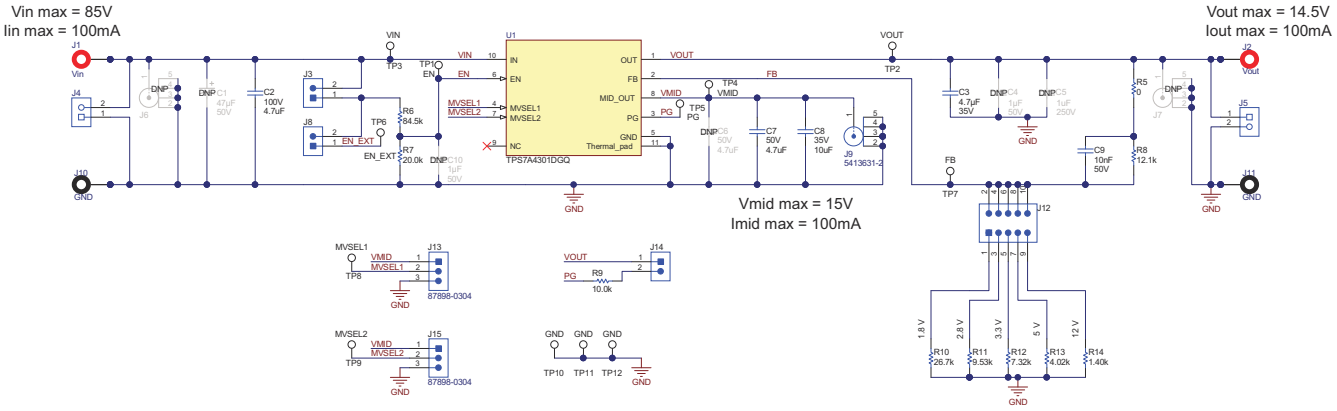

Figure 2-1. TPS7A43EVM-047 Schematic

3 EVM Setup

This section describes how to properly connect and setup the TPS7A43EVM-047, including the jumpers and connectors on the EVM board. See Section 4 for the proper connections of test equipment.

3.1 Jumper Connections

3.1.1 J3

Connect shunt across J3 and disconnect shunt across J8 if a divided down VIN will be used to trigger the precision EN.

3.1.2 J8

Connect shunt across J8 and disconnect shunt across J3 if a divided down voltage rail other than VIN will be used to trigger the precision EN. Use TP6 (EN_EXT) to connect the external voltage rail.

3.1.3 J12: Adjustable Output Voltage Selection

Connect a single shunt to select the output voltage. See Table 3-1 for help selecting VOUT.

Table 3-1. Selecting VOUT

VOUT	Pins
1.8V	1-2
2.8V	3-4
3.3V	5-6
5V	7-8
12V	9-10

3.1.4 J13: MVSEL1

Connect shunt across pins 1-2 to set MVSEL1 to logic high or across pins 2-3 for logic low. Refer to Table 3-2 for help setting VMID.

Table 3-2. Selecting VMID

VMID	MVSEL1	MVSEL2
10V	High	Low
12V	Low or High	High
15V	Low	Low

Note

Logic high and logic low for MVSEL1 and MVSEL2 are as defined in the PDS.

3.1.5 J14: Power-Good (PG)

Connect shunt if PG functionality will be used. If PG is not used, shunt can be connected or disconnected.

3.1.6 J15: MVSEL2

Connect shunt across pins 1-2 to set MVSEL2 to logic high or across pins 2-3 for logic low. Refer to Table 3-2 for help setting VMID.

Note

Logic high and logic low for MVSEL1 and MVSEL2 are as defined in the PDS.

3.2 Test Points

Table 3-3 lists the test points for the TPS7A43EVM-047.

Table 3-3. Test Point Functions

TEST POINTS	NAME	DESCRIPTION
TP1	EN	Connects directly to EN pin of TPS7A43. Use this test point if precision EN will be driven directly with an external voltage rail other than VIN.
TP2	VOUT	Regulated DC output.
TP3	VIN	Unregulated DC input.
TP4	VMID	Regulated MID output.
TP5	PG	Power-good pin. Connect shunt across jumper J14 if PG will be used.
TP6	EN_EXT	External enable. Use this test point with shunt connected across J8 and shunt disconnected from J3 to use a divided down, external voltage other than VIN to drive the precision EN.
TP7	FB	Feeback pin of TPS7A43.
TP8	MVSEL1	MID output voltage select pin. See Table 3-2 for help selecting VMID.
TP9	MVSEL2	MID output voltage select pin. See Table 3-2 for help selecting VMID.
TP10	GND	Device GND.
TP11	GND	
TP12	GND	

3.3 Soldering Guidelines

To avoid damaging the LDO, use a hot-air system for any solder rework to modify the EVM for the purpose of repair or other application reasons.

4 Equipment Connection and Operation

Connect test equipment as described in this section and follow the listed steps to properly take measurements.

1. Configure the on-board shunts to set the main output voltage VOUT, the mid-output voltage VMID, EN, and PG. See Section 3 for help configuring the shunts.
2. Verify that the input voltage power supply is set from 4V to 85V.
3. Connect the anode of the power supply to J1 (VIN) and the cathode to J10 (GND).

Note

Using a dual banana connector presents an arc hazard for high voltages. DO NOT USE J1 AND J10 IF VIN > 50V. Instead, use J4.

4. Connect the load for the middle output to J9 (VMID).
5. Connect the anode of the load for the main output to J2 and the cathode to J11. Alternatively, J5 can be used here.
6. Turn on the power supply.
7. Vary VIN, EN, and the loads as necessary for testing purposes.

5 PCB Layout

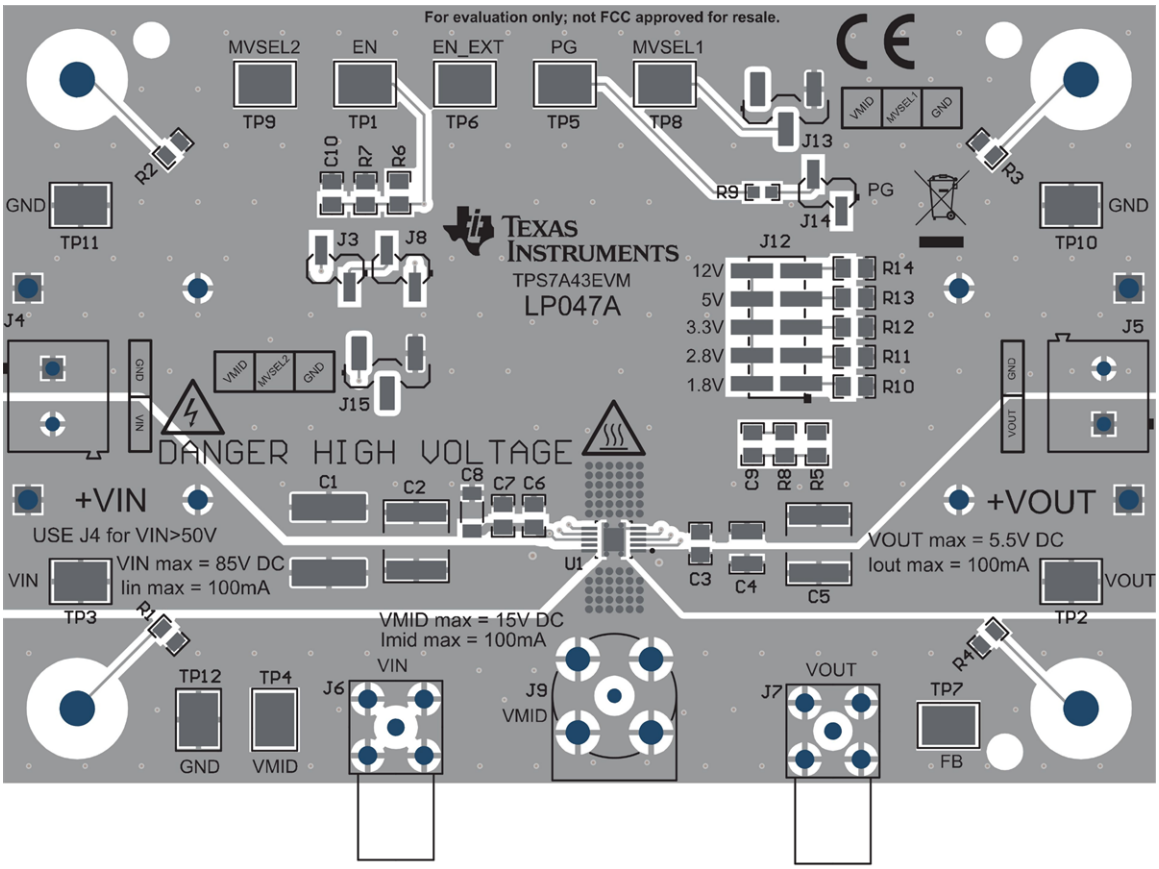

Figure 5-1. TPS7A43EVM-047 Top Layer Routing

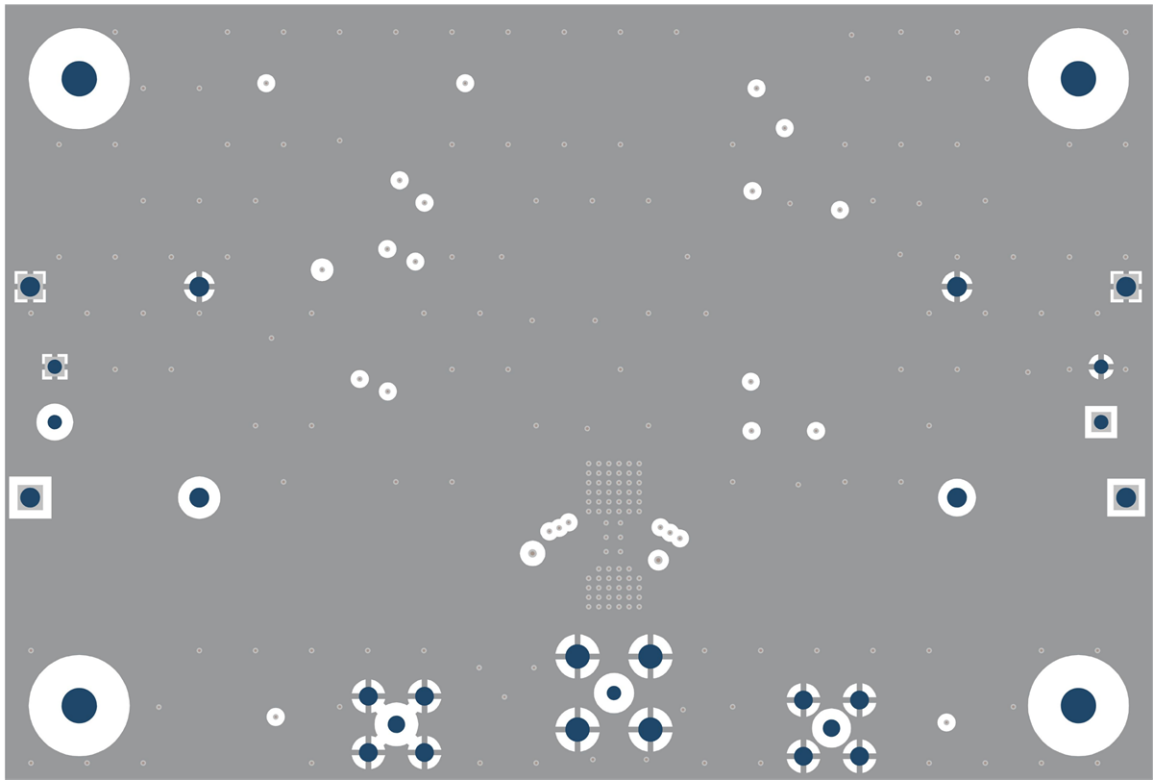

Figure 5-2. TPS7A43EVM-047 Internal Layer 1 Routing

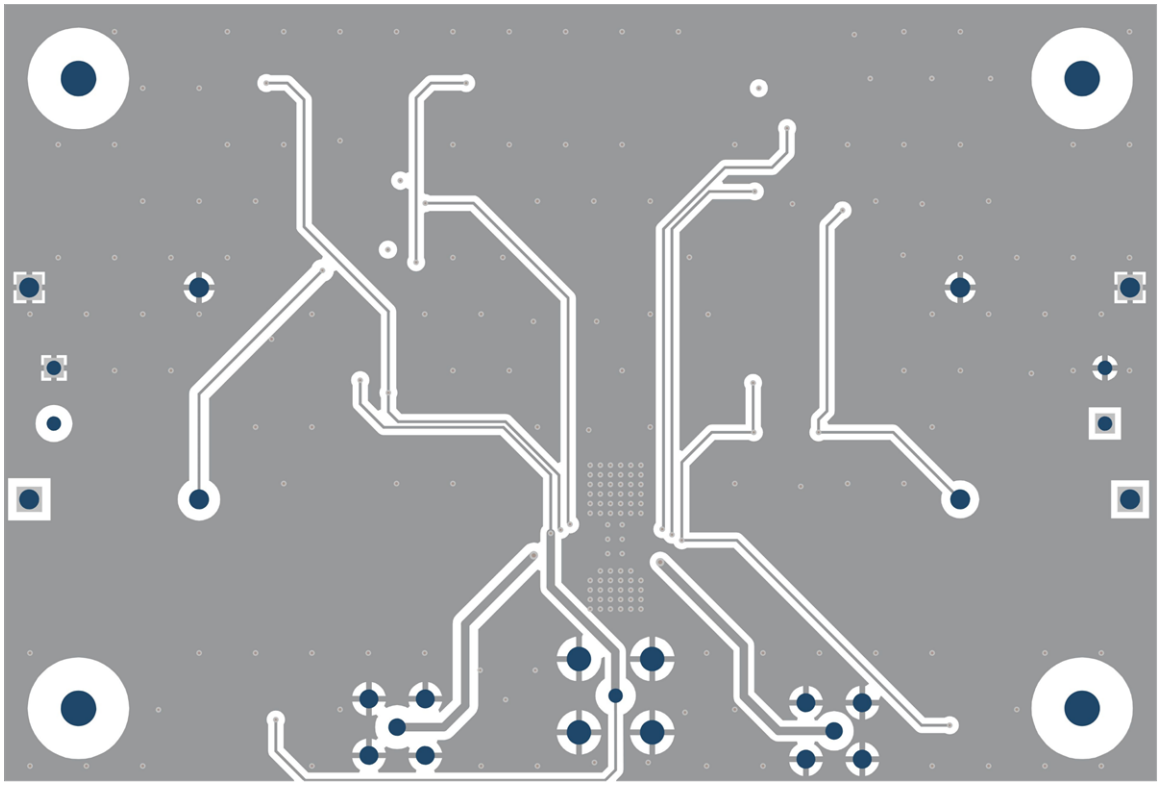

Figure 5-3. TPS7A43EVM-047 Internal Layer 2 Routing

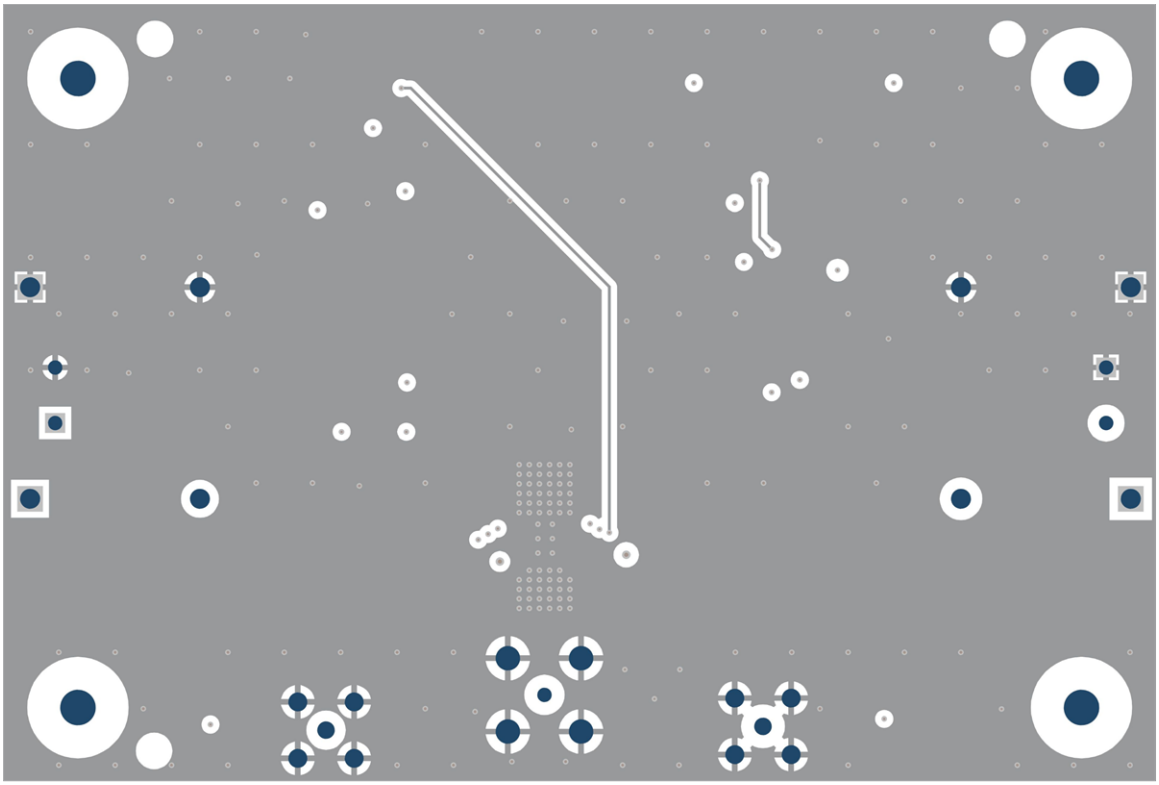

Figure 5-4. TPS7A43EVM-047 Bottom Layer Routing

6 Bill of Materials (BOM)

Table 6-1 shows the BOM for this EVM.

Table 6-1. TPS7A43EVM-047 BOM

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		LP047	Any		
C2	1	4.7uF	CAP, CERM, 4.7 uF, 100 V, +/- 20%, X7R, 2220	2220	C5750X7R2A475M230KA	TDK		
C3	1	4.7uF	CAP, CERM, 4.7 uF, 35 V, +/- 10%, X7R, 0805	0805	C2012X7R1V475K125AC	TDK		
C7	1	4.7uF	CAP, CERM, 4.7 uF, 50 V, +/- 10%, X7S, 0805	0805	GRM21BC71H475KE11K	MuRata		
C8	1	10uF	CAP, CERM, 10 uF, 35 V, +/- 20%, X7R, 1206_190	1206_190	C3216X7R1V106M160AC	TDK		
C9	1	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, 0805	0805	C0805C103K5RACTU	Kemet		
FID4, FID5, FID6	3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
H1, H3, H5, H7	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply		
H2, H4, H6, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone		
J1, J2	2		Standard Banana Jack, insulated, 10A, red	571-0500	571-0500	DEM Manufacturing		
J3, J8, J14	3		Header, 2.54mm, 2x1, Tin, SMT	Header, 2.54mm, 2x1, SMT	M20-8770246	Harwin		
J4, J5	2		Terminal Block, 5 mm, 2x1, Tin, TH	Terminal Block, 5 mm, 2x1, TH	691 101 710 002	Wurth Elektronik		
J9	1		Connector, TH, BNC Right angle, 50 ohm gold	5413631-2	5413631-2	AMP		
J10, J11	2		Standard Banana Jack, insulated, 10A, black	571-0100	571-0100	DEM Manufacturing		
J12	1		Header, 100mil, 5x2, SMT	Header, 100mil, 5x2, SMT	15910100	Molex		
J13, J15	2		Header, 2.54mm, 3x1, Gold, SMT	Header, 2.54mm, 3x1, SMT	87898-0304	Molex		
R5	1	0	RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6GEY0R00V	Panasonic		
R6	1	84.5k	RES, 84.5 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW080584K5FKEA	Vishay-Dale		
R7	1	20.0k	RES, 20.0 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW080520K0FKEA	Vishay-Dale		
R8	1	12.1k	RES, 12.1 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF1212V	Panasonic		
R9	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale		
R10	1	26.7k	RES, 26.7 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF2672V	Panasonic		
R11	1	9.53k	RES, 9.53 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW08059K53FKEA	Vishay-Dale		
R12	1	7.32k	RES, 7.32 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF7321V	Panasonic		
R13	1	4.02k	RES, 4.02 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW08054K02FKEA	Vishay-Dale		
R14	1	1.40k	RES, 1.40 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF1401V	Panasonic		

Table 6-1. TPS7A43EVM-047 BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5	5	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12	12		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone		
U1	1		LDO, Adjustable, Dual Output, 1.24~14.5V, 10/12/15V, 50mA, Precision Enable, Power-Good, HVSSOP10	HVSSOP10	TPS7A4301DGQ	Texas Instruments		
C4	0	1uF	CAP, CERM, 1 µF, 50 V,+/- 10%, X8L, AEC-Q200 Grade 0, 1210	1210	C1210C105K5NACTU	Kemet		
C5	0	1uF	CAP, CERM, 1 uF, 250 V, +/- 10%, X7R, 2220	2220	GRM55DR72E105KW01L	MuRata		
C6	0	4.7uF	CAP, CERM, 4.7 uF, 50 V, +/- 10%, X7S, 0805	0805	GRM21BC71H475KE11K	MuRata		
C10	0	1uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0805	0805	885012207103	Wurth Elektronik		
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J6, J7	0		Connector, Right Angle SMA 50 ohm, TH	SMA	901-143	Amphenol RF		
R1, R2, R3, R4	0	0	RES, 0, 1%, 0.5 W, 0805	0805	5106	Keystone		

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
Month Year	*	Initial Release

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