Application Report
SCAA099–February 2009

Fibre Channel and SAN Clock Generation Using the CDCM6100x

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ABSTRACT

This application report is a guide for using Texas Instruments CDCM6100x in a Fibre Channel application as a clock distributor and clock synthesizer along with measured jitter performance results.

1 Background

Today's networking boxes require clock generation and buffering. Traditional methods involved a clock oscillator and a clock buffer. For Fibre Channel and Storage Area Network (SAN) applications, a typical 106.25-MHz, 187.5-MHz, 212.5-MHz, or 250-MHz clock is needed. Due to the low jitter and accuracy needed for these clock oscillators, their cost are high. So how does a designer lower cost but maintain low jitter, high accuracy, and clock buffering in a single solution? The CDCM6100x answers this question.

2 Functional Description

The CDCM6100x is a highly versatile, low-jitter frequency synthesizer which can generate low jitter clock outputs, selectable among LVPECL, LVDS, or LVCMOS, from a low-frequency crystal or LVCMOS input for a variety of wireline and data communication applications. The CDCM6100x features an on-chip PLL that can be easily configured solely through control pins. The overall output jitter performance is less than 1 ps, rms or 35 ps, pk-pk, thus making these devices a perfect choice to use in demanding applications like Fibre Channel, Ethernet, and SAN. The CDCM6100x is packaged in a small 32-pin, 5-mm × 5-mm QFN package. The CDCM6100x is available in one-, two-, and four-output versions.

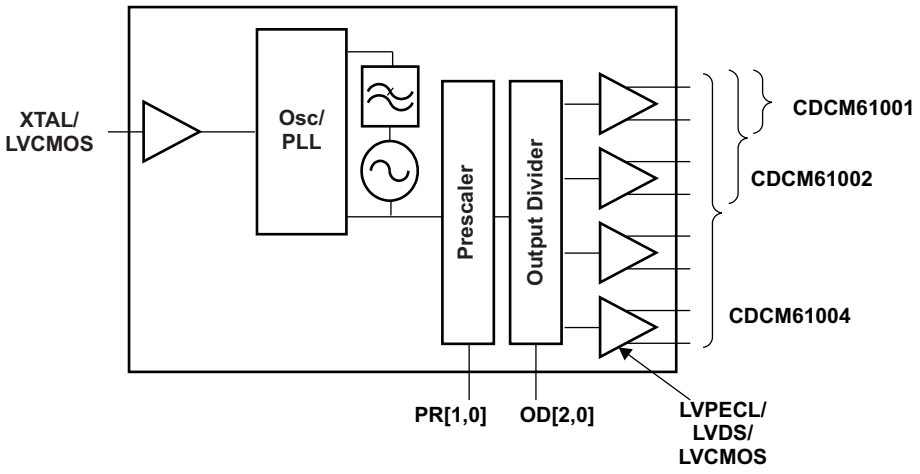


Figure 1. CDCM6100x Functional Block Diagram

3 Application

Today's Fibre Channel and SAN clocking require low jitter (typ < 1 ps rms or lower). Typical Fibre Channel and SAN clock speeds are 106.25 MHz, 187.5 MHz, 212.5 MHz, or 250 MHz. For these systems, the output signal type needed can be differential (LVPECL or LVDS) or single-ended 3.3-V LVCMOS. This application report demonstrates solutions that can meet these needs while also offering a lower cost solution to today's high-priced oscillators and clock buffers.

4 Test Equipment and Setup

All the measurements discussed in this application report were taken under normal operating conditions using a 3.3-V power supply and at room temperature.

Equipment used:

- Agilent E5052A Signal Source Analyzer
- Power supply
- CDCM6100x EVM

5 Block Diagram and Jitter Test Results of Fibre Channel Solutions

The two following solutions show how to generate clocks from the CDCM6100x devices and a low-cost, standard 26.5625-MHz crystal. The 26.5625 MHz is fed into the CDCM6100x VCO core to generate a 106.25-MHz or 212.5-MHz frequency available to the output buffer. The output signal type can be native LVPECL, LVDS, or LVCMOS. These examples select LVPECL for the output buffers but also included are some LVDS and LVCMOS measurements at the end of this application report.

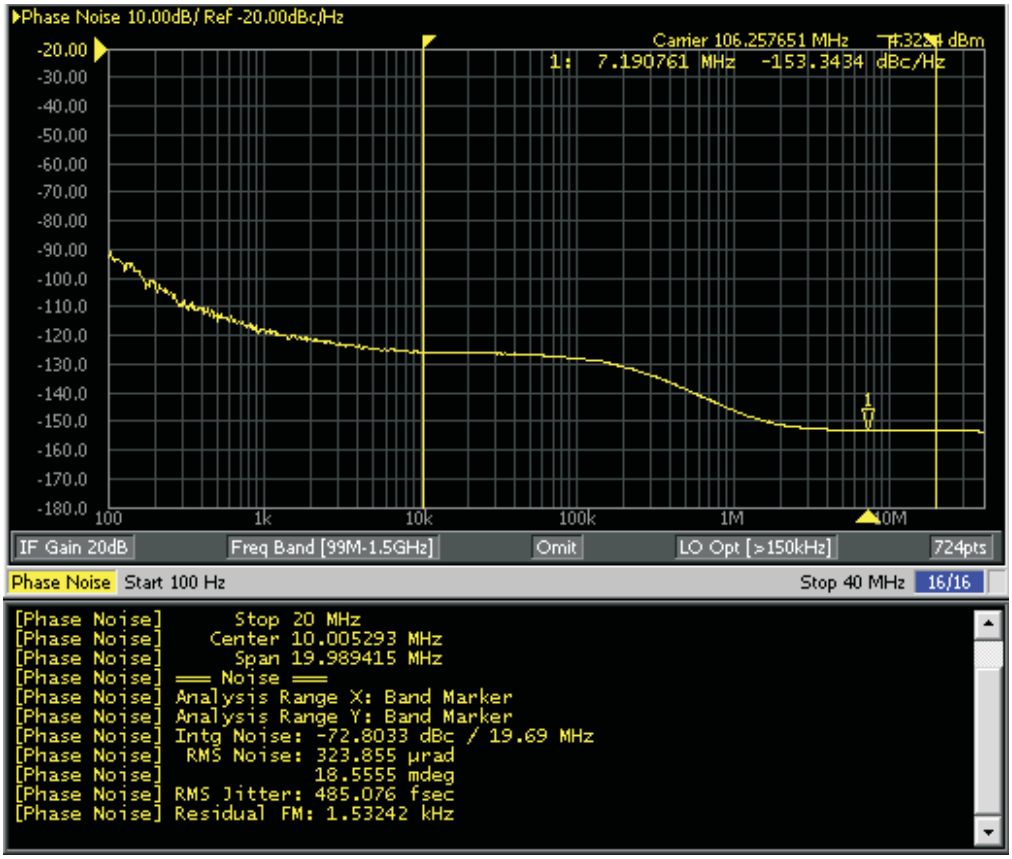
5.1 Fibre Channel Solution 1 Block Diagram:

Solution 1 uses the four-output version CDCM61004 to generate 106.25 MHz. If less outputs are needed, the CDCM61001 or CDCM61002 can supply one or two outputs, respectively.

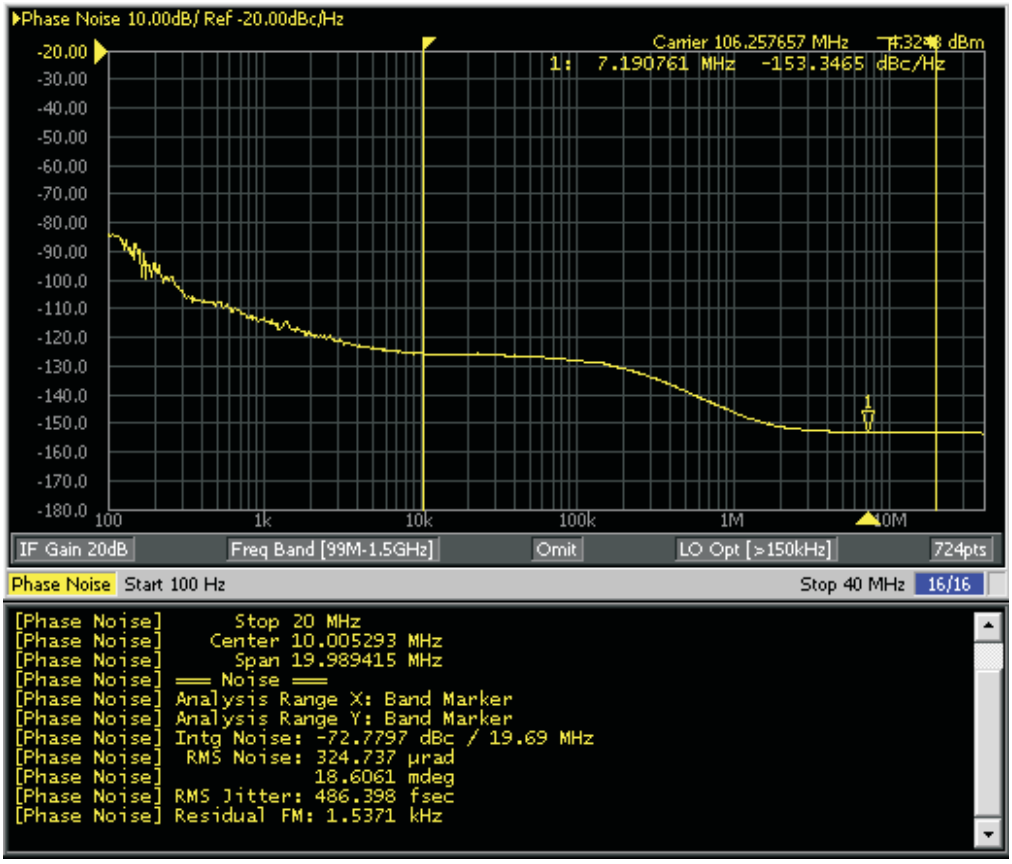
Figure 2. FC Block Diagram 1

5.2 Fibre Channel Solution 1 Jitter Test Results:

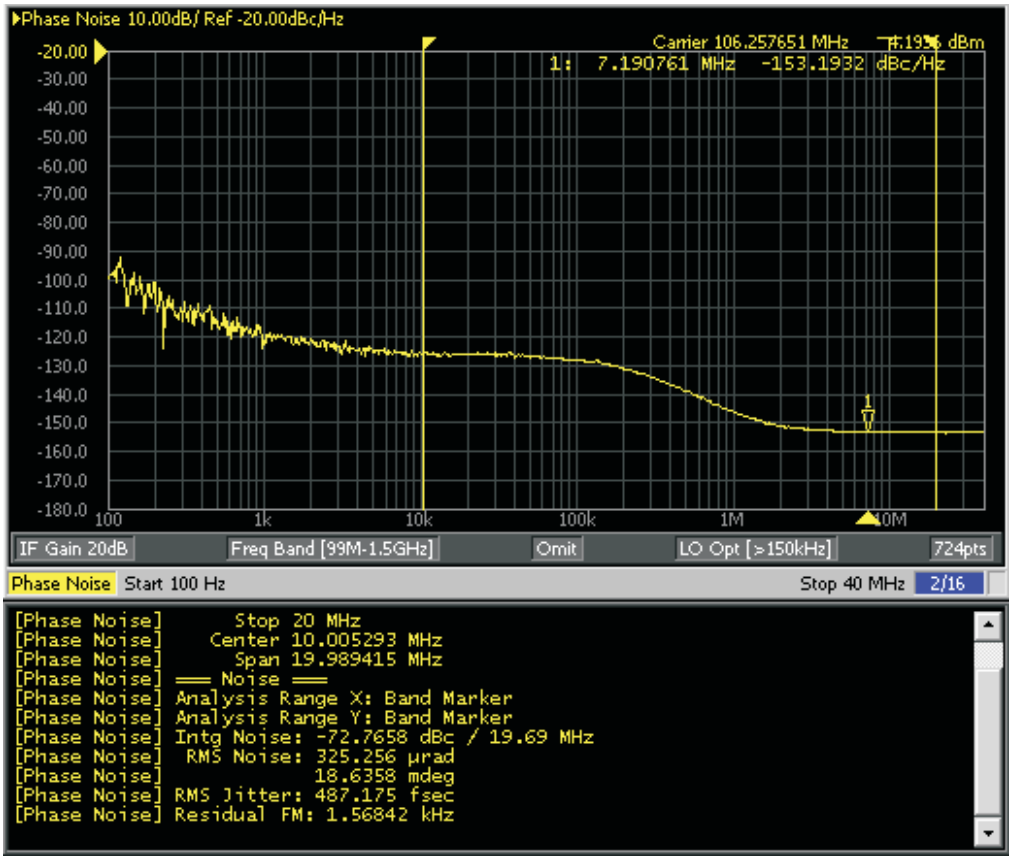
OUT_0 = 106.25-MHz LVPECL – RMS Jitter is 485 fsec (10 kHz–20 MHz)



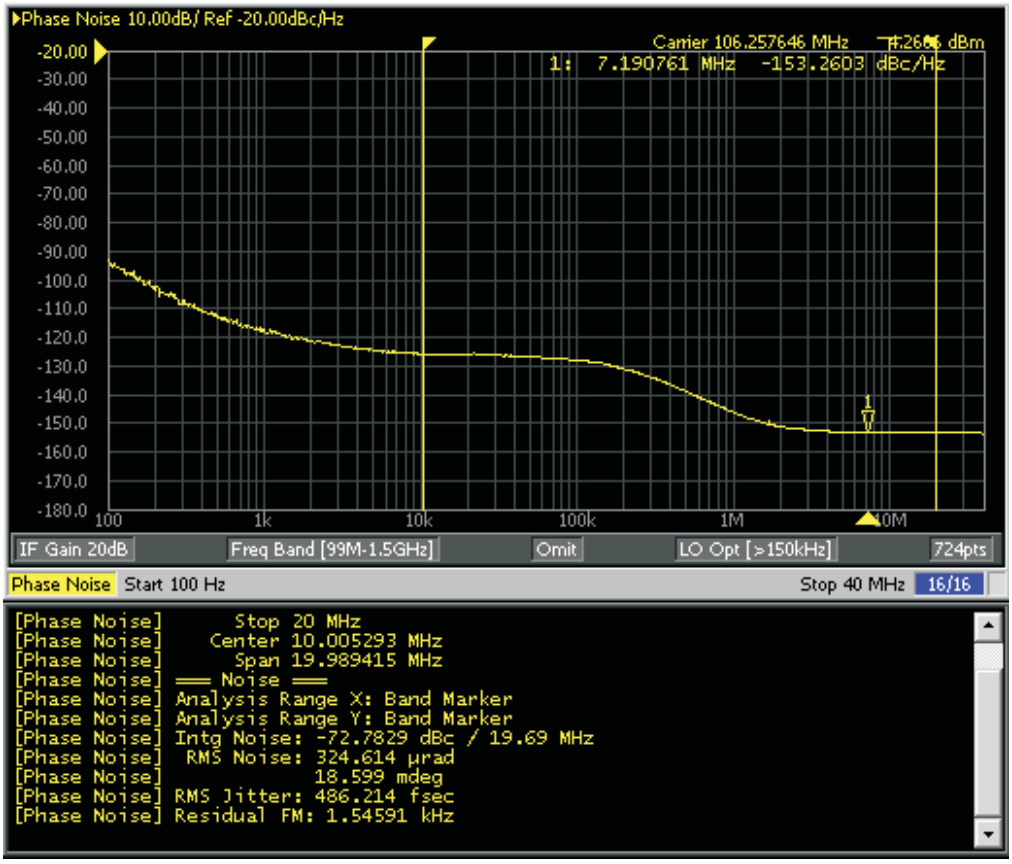
OUT_1 = 106.25-MHz LVPECL – RMS Jitter is 486 fsec (10 kHz–20 MHz)



OUT_2 = 106.25-MHz LVPECL – RMS Jitter is 487 fsec (10 kHz–20 MHz)



OUT_3 = 106.25-MHz LVPECL – RMS Jitter is 486 fsec (10 kHz–20 MHz)



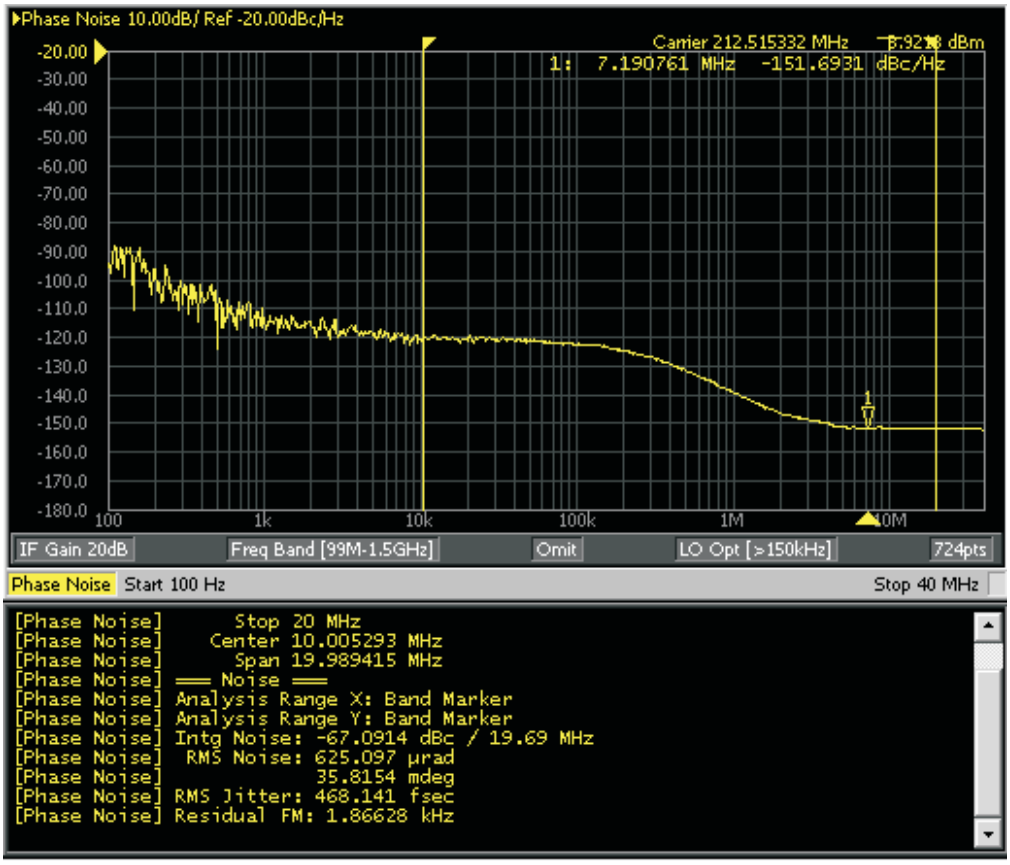
5.3 Fibre Channel Solution 2 Block Diagram:

Solution 2 uses the two-outputs version CDCM61002 to generate two copies of 212.5 MHz. If more or less outputs are needed, the CDCM61001 or CDCM61004 supplies one or four outputs, respectively.

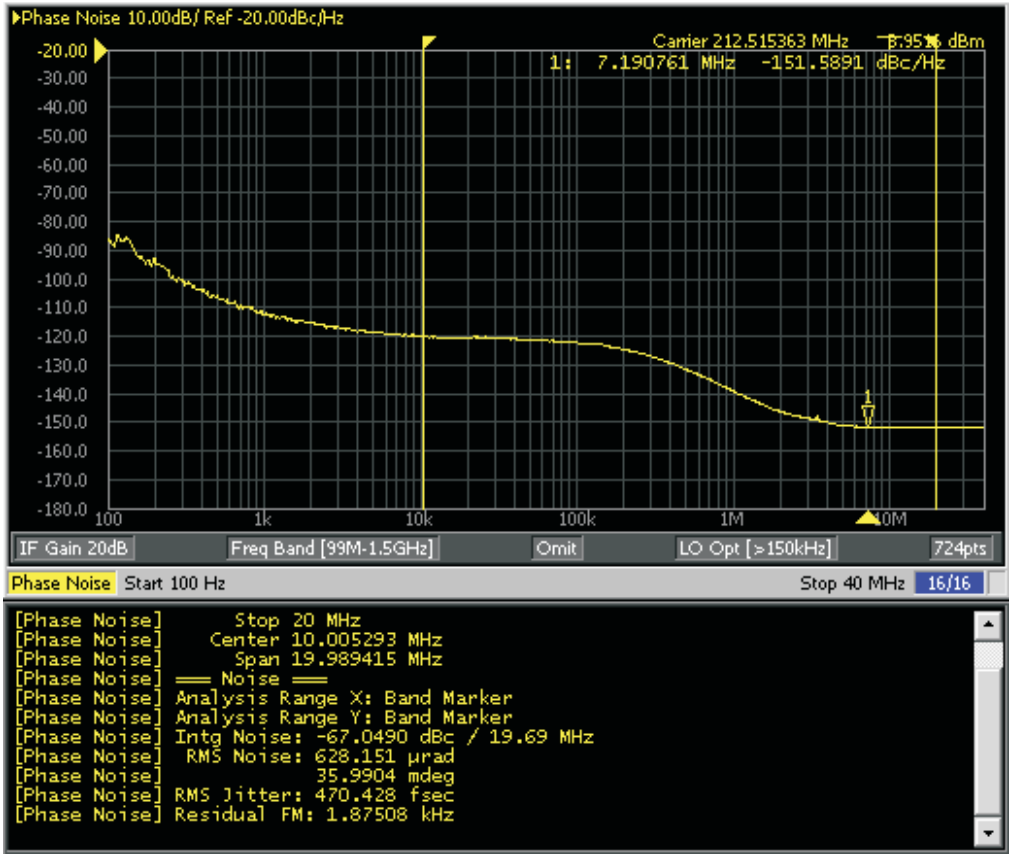
Figure 3. FC Block Diagram # 2

5.4 Fibre Channel Solution 2 Jitter Test Results:

OUT_0 = 212.5-MHz LVPECL – RMS Jitter is 468 fsec (10 kHz–20 MHz)



OUT_1 = 212.5-MHz LVPECL – RMS Jitter is 470 fsec (10 kHz–20 MHz)



6 Block Diagram and Jitter Test Results of SAN Solutions

The following two solutions show how to generate SAN clocks from the CDCM6100x devices and a low-cost, standard, 25-MHz crystal. The 25 MHz is fed into the CDCM6100x VCO core to generate a 187.5-MHz or 250-MHz frequency available to the output buffer. The output signal type can be native LVPECL, LVDS, or LVCMOS. These examples select LVPECL for the output buffers.

6.1 SAN Solution 1 Block Diagram:

SAN Solution 1 uses the one-output version CDCM61001 to generate 187.5 MHz. If more outputs are needed the CDCM61002 and CDCM61004 can supply two or four outputs, respectively.

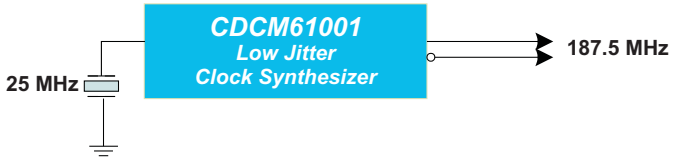
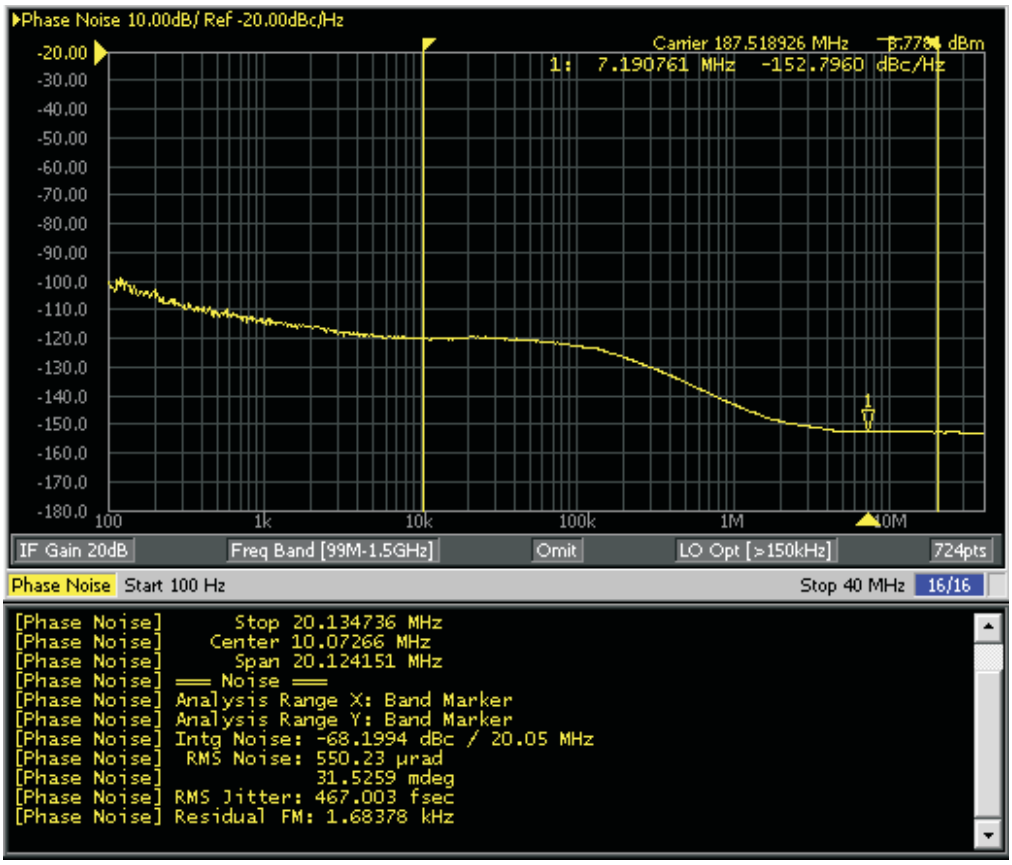


Figure 4. SAN Block Diagram 1

6.2 SAN Solution 1 Jitter Test Results:

OUT_0 = 187.5-MHz LVPECL – RMS Jitter is 467 fsec (10 kHz – 20 MHz)



6.3 SAN Solution 2 Block Diagram:

Solution 2 uses the four-output version CDCM61004 to generate four copies of 250 MHz. If less outputs are needed, the CDCM61001 or CDCM61002 supplies one or two outputs, respectively.

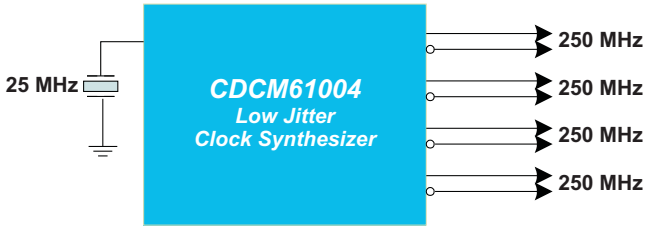
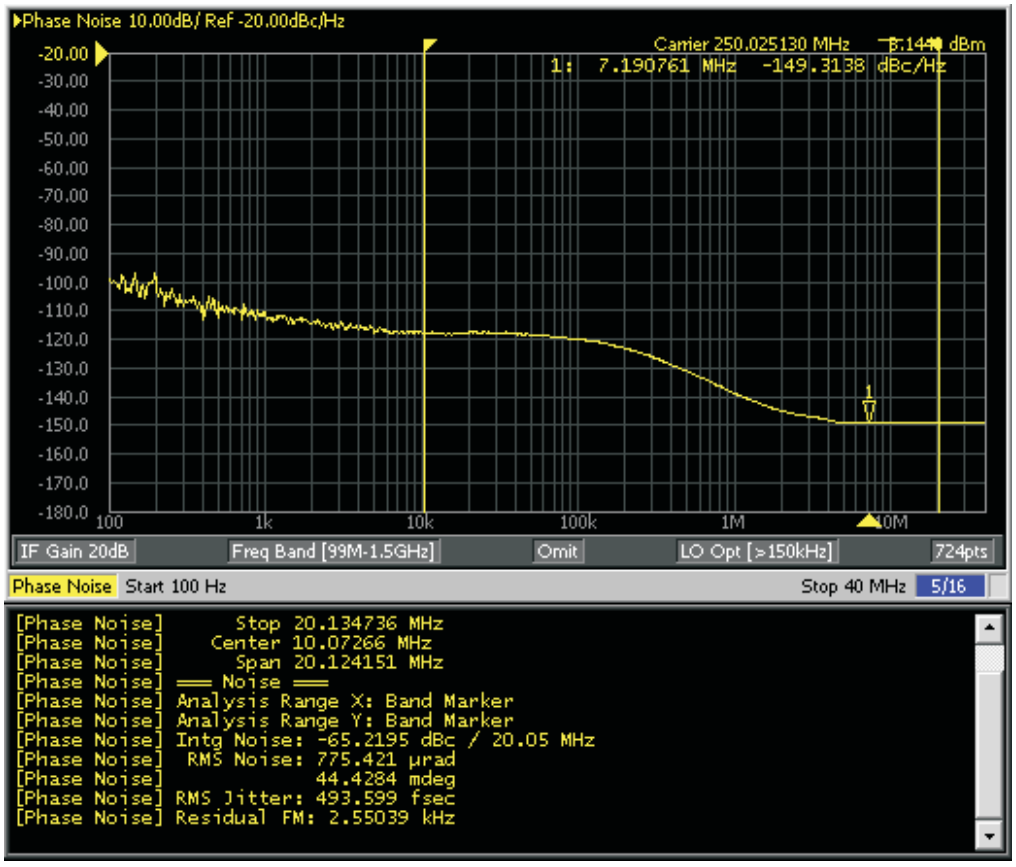


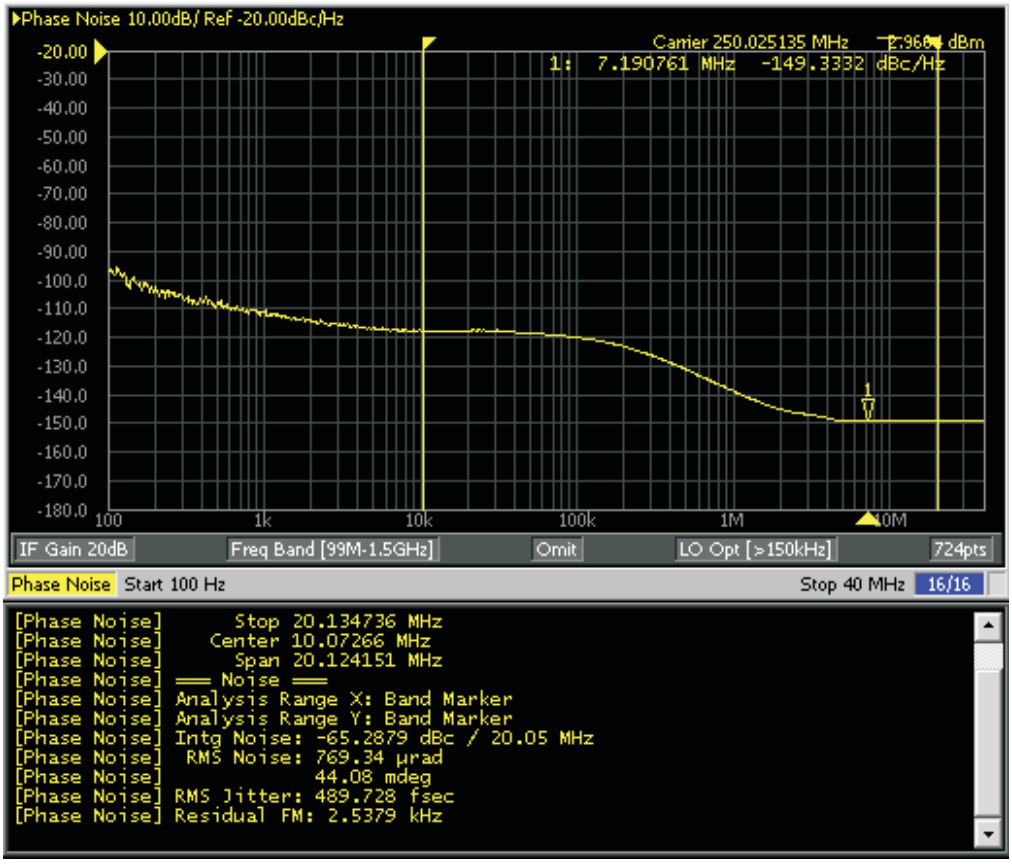
Figure 5. SAN Block Diagram 2

6.4 SAN Solution 2 Jitter Test Results:

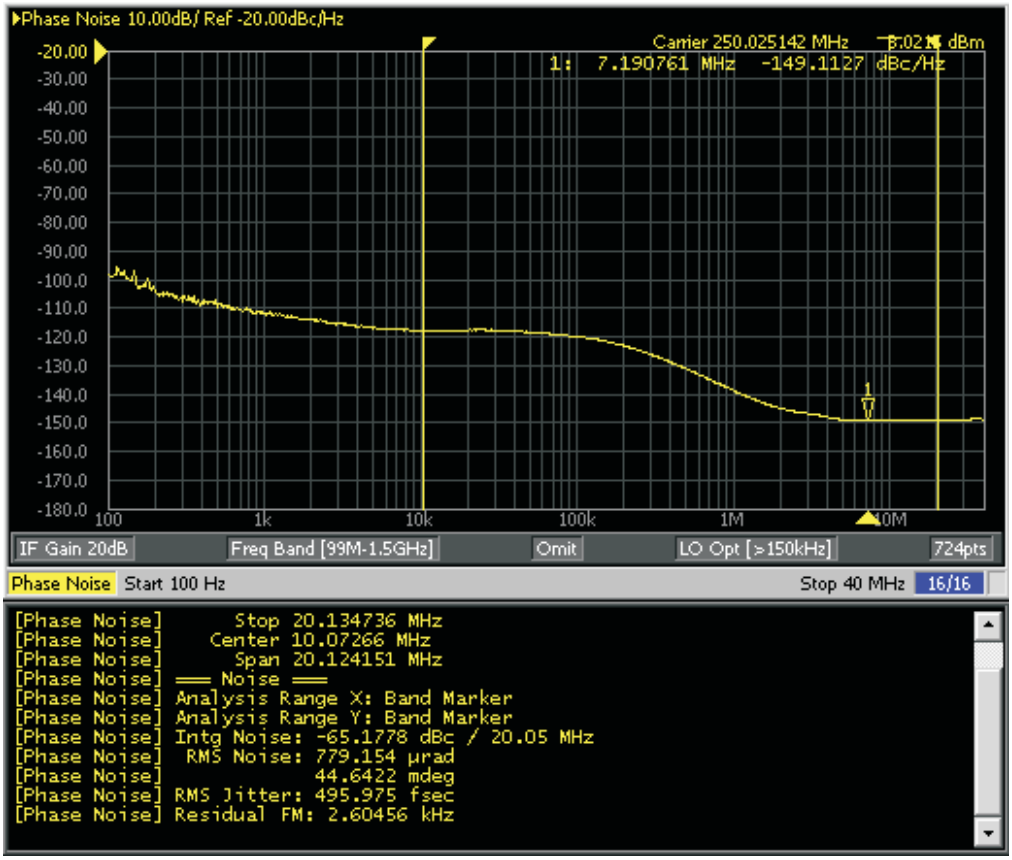
OUT_0 = 250-MHz LVPECL – RMS Jitter is 494 fsec (10 kHz – 20 MHz)



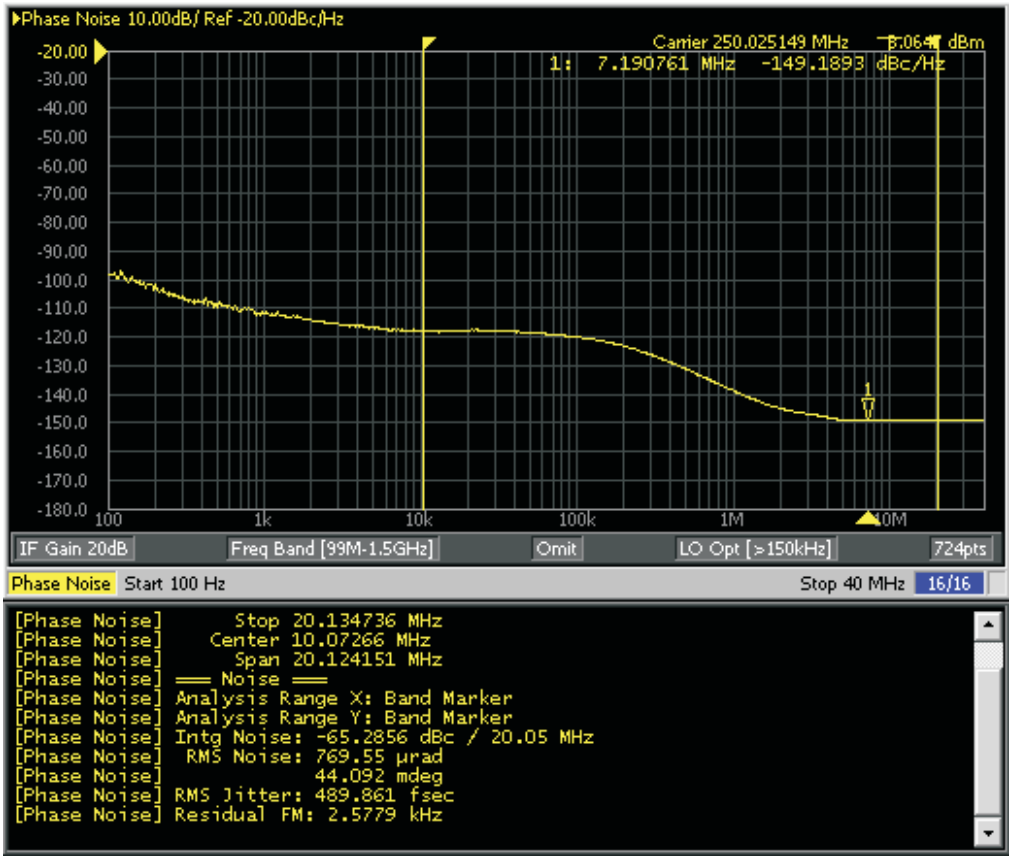
OUT_1 = 250-MHz LVPECL – RMS Jitter is 490 fsec (10 kHz – 20 MHz)



OUT_2 = 250-MHz LVPECL – RMS Jitter is 496 fsec (10 kHz – 20 MHz)



OUT_3 = 250-MHz LVPECL – RMS Jitter is 490 fsec (10 kHz – 20 MHz)



7 Performance Summary

7.1 Fibre Channel Configurations

Performance results of these Fibre Channel configurations are:

1. **CDCM61004 = 106.25 MHz**
   OUT_0 = 106.25-MHz LVPECL – ***RMS Jitter is 485 fsec*** (10 kHz–20 MHz)
   OUT_1 = 106.25-MHz LVPECL – ***RMS Jitter is 486 fsec*** (10 kHz–20 MHz)
   OUT_2 = 106.25-MHz LVPECL – ***RMS Jitter is 487 fsec*** (10 kHz–20 MHz)
   OUT_3 = 106.25-MHz LVPECL – ***RMS Jitter is 486 fsec*** (10 kHz–20 MHz)
2. **CDCM61002 = 212.5 MHz**
   OUT_0 = 212.5-MHz LVPECL – ***RMS Jitter is 468 fsec*** (10 kHz–20 MHz)
   OUT_1 = 212.5-MHz LVPECL – ***RMS Jitter is 470 fsec*** (10 kHz–20 MHz)

7.2 SAN Configurations

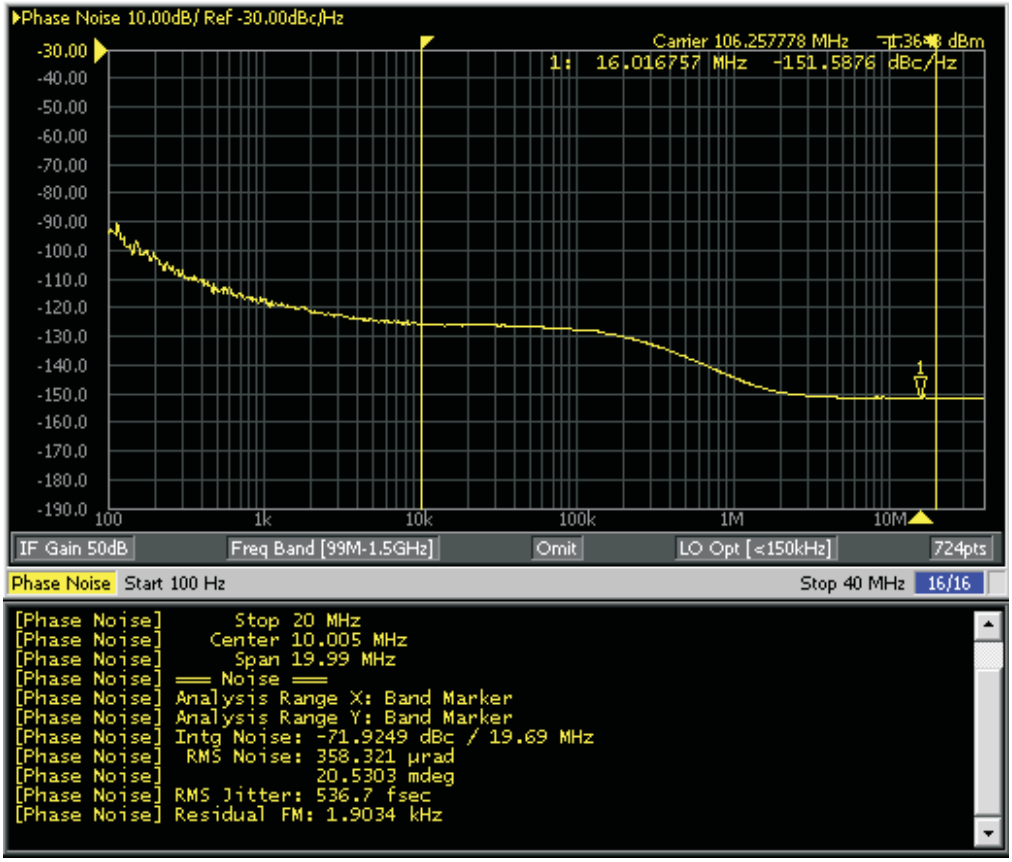
Performance results of these SAN configuration are:

1. **CDCM61001 = 187.5 MHz**
   OUT_0 = 187.5-MHz LVPECL – ***RMS Jitter is 467 fsec*** (10 kHz–20 MHz)
2. **CDCM61004 = 250 MHz**
   OUT_0 = 250-MHz LVPECL – ***RMS Jitter is 494 fsec*** (10 kHz–20 MHz)
   OUT_1 = 250-MHz LVPECL – ***RMS Jitter is 490 fsec*** (10 kHz–20 MHz)
   OUT_2 = 250-MHz LVPECL – ***RMS Jitter is 496 fsec*** (10 kHz–20 MHz)
   OUT_3 = 250-MHz LVPECL – ***RMS Jitter is 490 fsec*** (10 kHz–20 MHz)

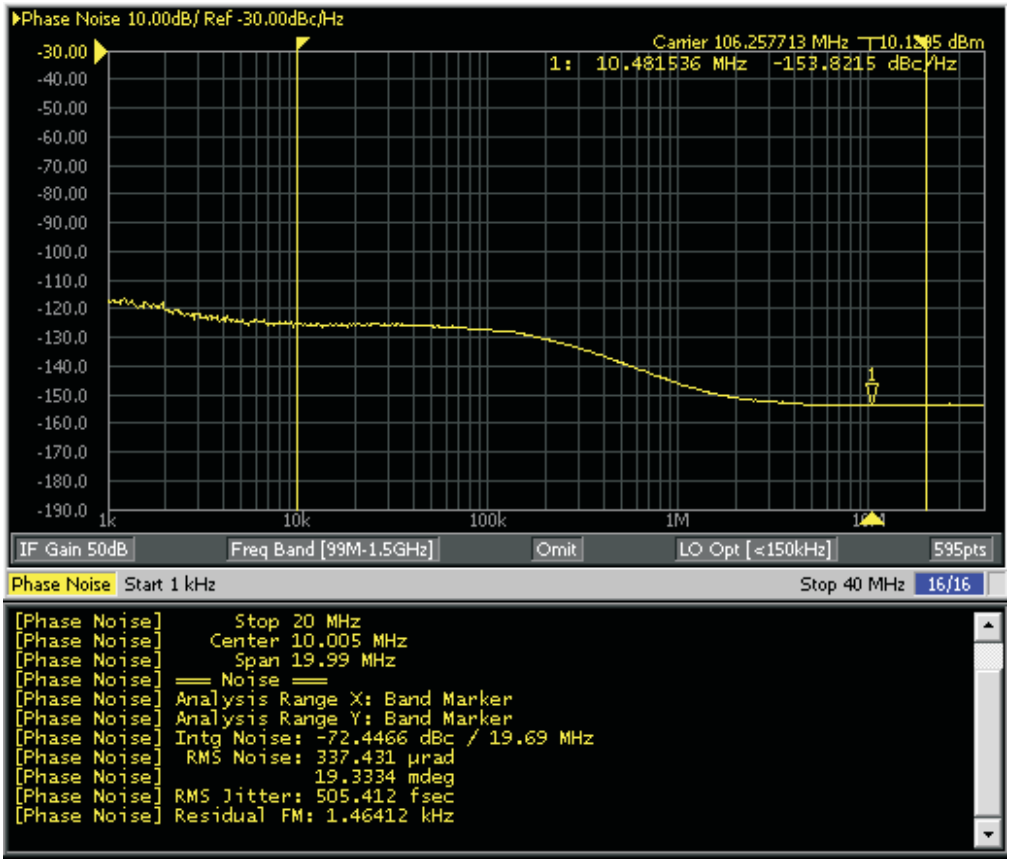
8 Additional Data

As previously mentioned, the CDCM6100x output type can be configured to LVPECL, LVDS, or LVCMOS. The following are some additional jitter measurements with LVDS and LVCMOS outputs

106.25-MHz LVDS – RMS Jitter is 537 $f$sec (10 kHz–20 MHz)



106.25-MHz LVCMOS – RMS Jitter is 505 $f$sec (10 kHz–20 MHz)



Conclusion

The CDCM6100x performance meets today's Fibre Channel and SAN frequencies with low-jitter requirements, <1 ps RMS. It is a simple, hardware-configurable device that requires no preprogramming. The CDCM6100x is offered in a 32-pin, 5-mm × 5-mm QFN package. This single, 3.3-V device can replace the functionality of expensive oscillators and buffers. In addition to lowering cost, the CDCM6100x offers additional advanced features like a buffered crystal output for measuring the actual frequency of the input crystal.

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