Application Note

Utilizing Timing Components in TI Programmable Logic Devices (TPLD)

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ABSTRACT

Systems often require timers ranging from hundreds of microseconds to several seconds and typically designed with multiple timing components and discrete logic to achieve this. TI Programmable Logic Devices (TPLD) can be configured to generate multiple timers and additional glue logic within a single device, vastly decreasing the overall design size, BOM, and time to market. This application note will discuss how to generate various timers and what is achievable with the oscillator and counters/delay generator macro-cells within the TPLD.

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Trademarks

1 Introduction

Systems often require timers ranging from hundreds of microseconds to several seconds and typically require multiple timing components and discrete logic to achieve this. TI Programmable Logic Devices (TPLD) can be configured to generate multiple timers and additional glue logic within a single device, vastly decreasing the overall design size and design time. This application note will discuss what is achievable with the oscillator and counters/delay generator macro-cells within the TPLD to generate various timers.

2 Configuring Oscillators in TPLD

Oscillators within a TPLD are configurable where the operating frequency can be selected between two options, as shown in Figure 2-1, or fixed to a specific frequency. The operating frequency is fed into a pre-divider and a secondary divider stage to provide a wide range of frequencies that can be used in a TPLD design. The pre-divider stage output is also routed to the clock input of the counter/delay generator macro-cells, where a separate second stage divider is available. For the options available within each device, see the device-specific TPLD data sheets.

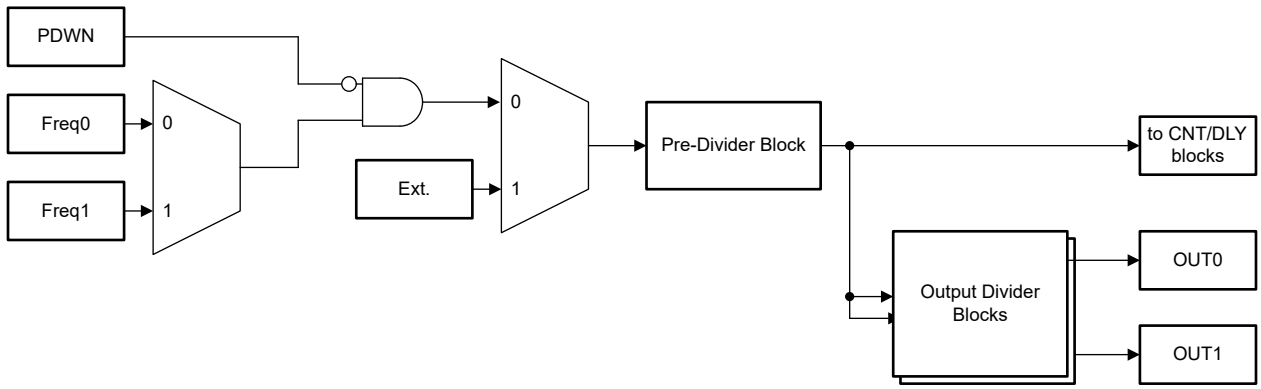

Figure 2-1. Oscillator Macro-cell Block Diagram

The TPLD1201, for example, has one internal oscillator, selectable to operate at 25kHz or at 2MHz. The selected clock then feeds into a pre-divider stage that divides the operating frequency by 1, 2, 4, or 8. The output divider stage provides an additional divide by 1, 2, 3, 4, 8, 12, 24, or 64 option per output. From the output of the pre-divider, the counters have an additional divisor of 1, 4, 12, 24, 64, or 4096 for each counter.

Table 2-1 shows the minimum and maximum frequencies that can be realized at the output of the oscillator and the clocks to drive the counters and/or delay generators in the TPLD1201.

Table 2-1. Minimum and Maximum Clocks Realizable With Internal Dividers in TPLD1201

Frequency	25kHz						2MHz					
Pre-Divider	1			8			1			8		
2nd divider	1	64	4096	1	64	4096	1	64	4096	1	64	4096
CLK freq.	25kHz	390Hz	6.1Hz	3.1kHz	48.8Hz	0.7Hz	2.0MHz	31.2kHz	488Hz	250kHz	3.9 kHz	61Hz
CLK period	40µs	2.56ms	163ms	320µs	20.4ms	1.31s	500ns	32µs	2.04ms	4µs	256µs	16.3ms

3 Configuring Timing Macro-Cells in InterConnect Studio (ICS)

The oscillator dividers as well as the counter macro-cells can be utilized to generate a wide variety of frequencies. The frequency of a counter output can be calculated by: $f_{out} = f_{clk}/(DATA + 1)$. After a reset occurs, an additional 2 clock cycles are needed for clock synchronization.

The circuit shown below in Figure 3-1, configured in InterConnect Studio (ICS), shows an example of using the 25kHz oscillator in the TPLD1201 to generate a 625Hz square wave with 50% duty cycle. To achieve this, the oscillator pre-divider is set to divide by 2, changing the base frequency to 12.5kHz. This is input to the counter macro-cell's clock port to generate a 1.25kHz signal, which can be calculated by using the aforementioned equation: $f_{out} = 12.5kHz/10$, where $f_{clk} = 12.5kHz$ and $DATA = 9$. To achieve a 50% duty cycle, the output of the counter is then fed into a D flip-flop, which further divides the input frequency by 2, resulting in a 625Hz signal.

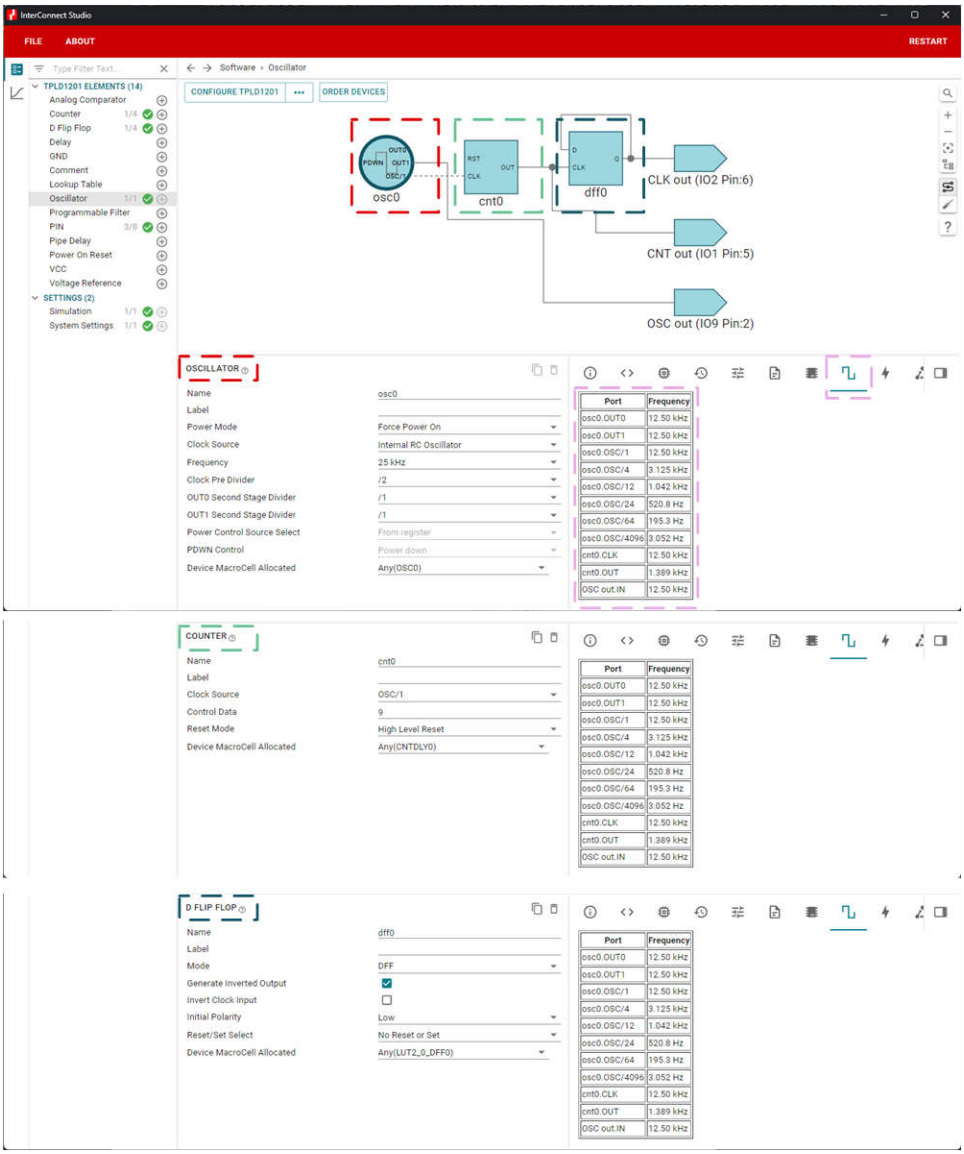

Figure 3-1. Timing Components Configuration in InterConnect Studio (ICS)

Figure 3-2 and Figure 3-3 show simulation results of the circuit within ICS and logic analyzer captures of the circuit in the TPLD1201, respectively.

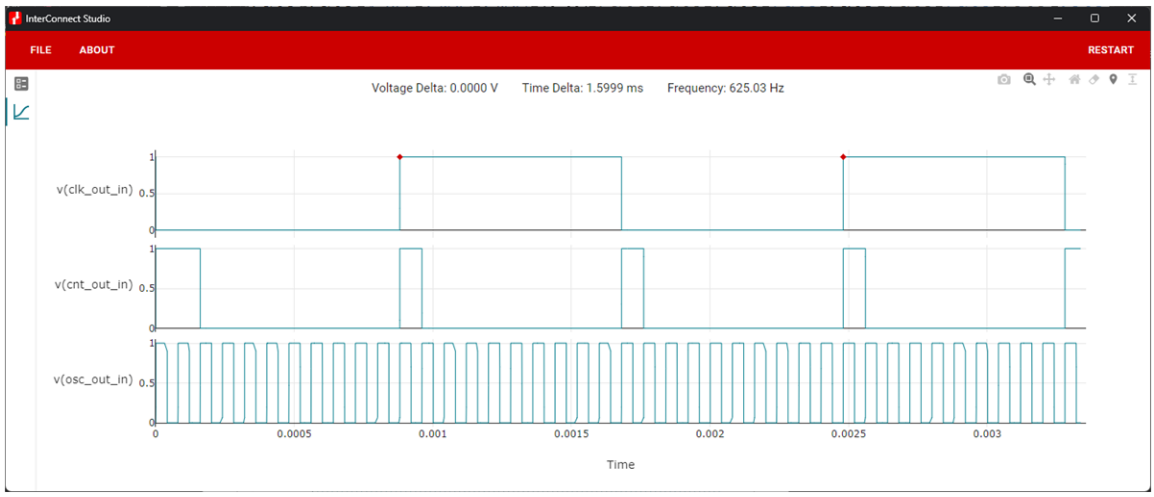

Figure 3-2. ICS Simulation Output

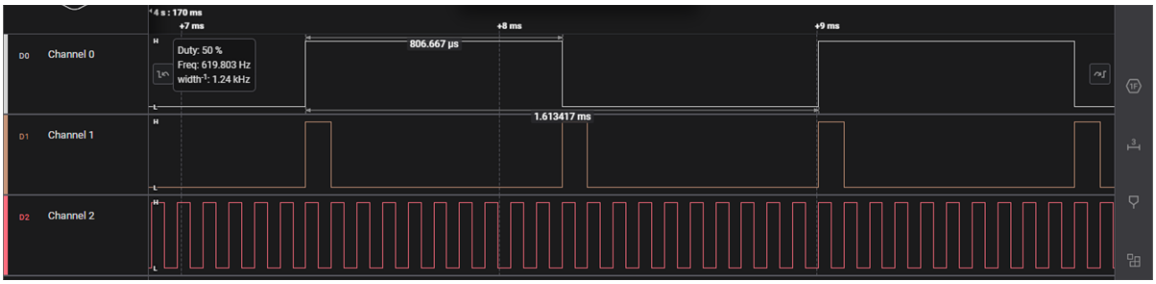

Figure 3-3. Logic Analyzer Capture of TPLD1201 Output

4 Synchronizing Signals Example

The delay generator macro-cell can be utilized to synchronize two signals. The delay generator will delay an input signal by $t_d = (DATA + t_{d\_err} + 2)/f_{clk}$, where t_{d_err} is error due to phase shifts between the input and the clock and f_{clk} is the frequency of the signal passed into the clock input of the delay generator. One caveat to properly use the delay generator is the input signal's pulse width (high and low) must be greater than three times the period of the clock input.

The circuit shown in Figure 4-1 generates two signals, one outputting at ~357Hz and the other at ~4.17kHz. The slower signal should be routed into the IN port of the delay generator, and using the External Clock option, the faster signal should be routed into the CLK port.

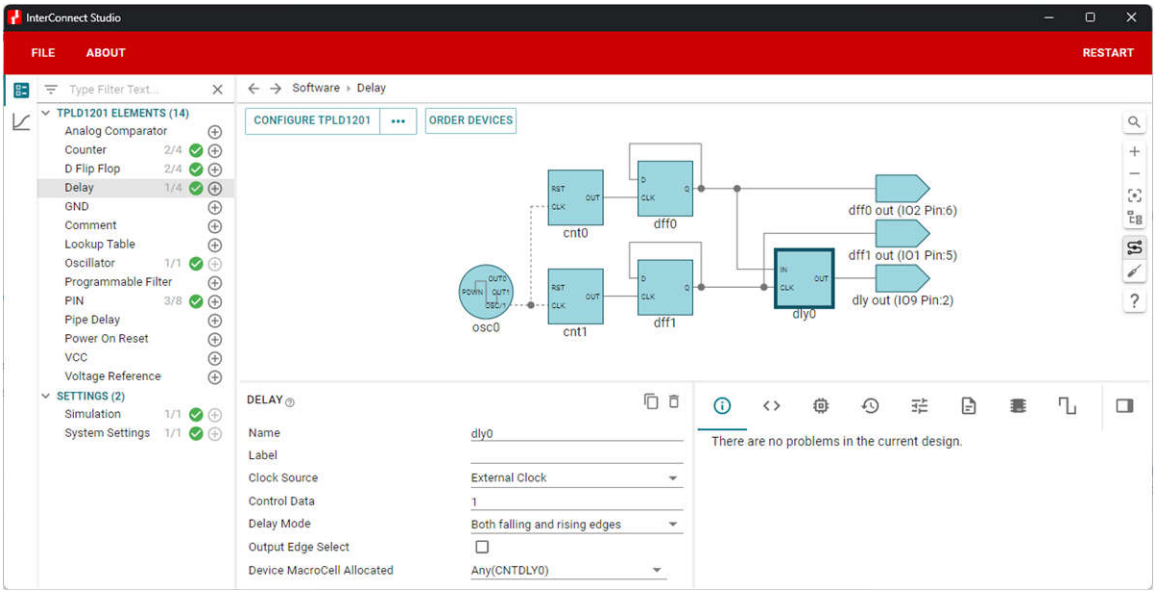

Figure 4-1. Synchronizing Signals Example Circuit

Simulation results in ICS and measured logic analyzer captures on the TPLD1201 can be found in Figure 4-2 and Figure 4-3, respectively. As evident in the images, the *dff0_out* and *dff1_out* signals were initially asynchronous and *dly0* was utilized to synchronize *dff0_out* to *dff1_out*. Note: if the frequency of the two signals are not factors, the delay will result in a slight distortion of the input signal.

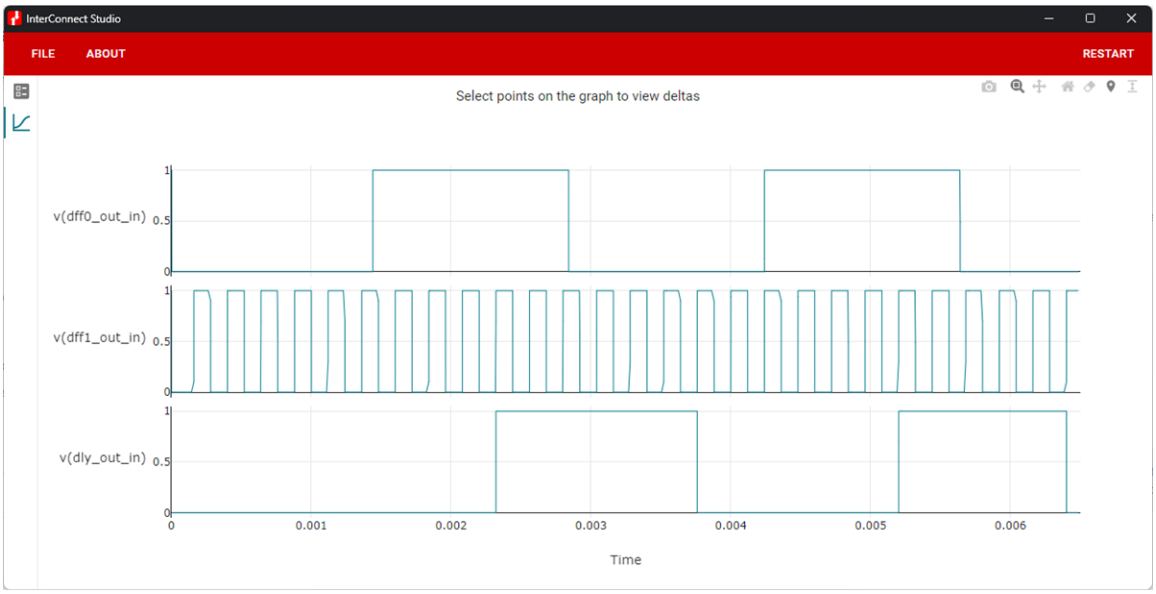

Figure 4-2. ICS Simulation of Synchronizing Signals Circuit

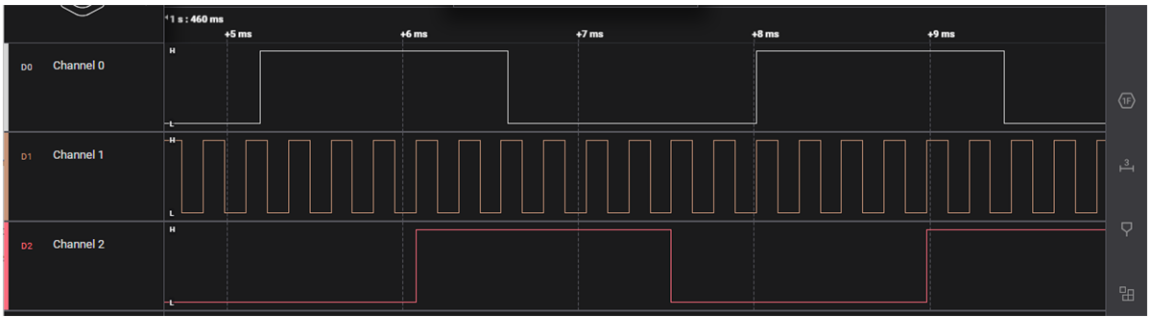

Figure 4-3. Logic Analyzer Capture of Synchronizing Signals Circuit

5 Summary

Designs can be easily simplified and the complexity can be reduced by considering TPLDs in place of discrete implementations. By offering numerous solutions with varying number of general-purpose I/Os (GPIO), look-up tables, D-type flip-flops and latches, counters, delay generators, and integrated oscillator(s), TPLD will help elevate designs to levels that may not have ever been considered. Whether developing low-power handheld devices or interfacing sensors, the flexibility and ease of programming the TPLD provides makes it a solution that is hard to ignore.

6 References

- Texas Instruments, TI Programmable Logic Devices
- Texas Instruments, TPLD1201 Product Folder

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