PCIe 1.0a Device Prevent Resume from S1

DIBU

ABSTRACT

There are times when attempting to resume from S1 in a Microsoft Windows environment (Windows XP or Vista) that the system does not wake up if a PCIe 1.0a-compliant device such as the XIO2000A or XIO2200A is in the system. This problem is not caused by the Texas Instruments devices, but is instead due to a problem with the PCI Express Base 1.0a specification with regards to exiting L1 state. The PCI Express Base 1.1 specification resolved the problem; however, because the Texas Instrument devices comply with the PCIe Base 1.0a specification, they adhere to the PCIe Base1.0a rules for exiting L1.

Contents

Issue: Failure to Resume from S1

As a system is entering a low-power system state (specifically S1), the operating system places the XIO2000A/XIO2200A into a low power device state (D1, D2, or D3 hold). Once in the low-power device state, the XIO2000A/XIO2200A requests to enter L1 by transmitting PM_Enter_L1. Once it receives a PM_Request_Ack from the upstream port, the XIO2000A/XIO2200A is in the L1 state. At this point, the system can complete its transition to a suspended state (S1).

When trying to resume from S1, the upstream device (chipset) initiates the recovery phase and the link transitions back to the L0 state. The upstream device sends a TLP to the downstream device. The downstream device acknowledges the received TLP, and then it may return to the L1 state. At this point a problem may occur. The received TLP may cause the downstream component to internally generate a completion TLP that gets held up inside the device. The PCIe 1.0a base specification does not permit a downstream device to send a TLP while in the L1 state. This causes the operating system to get into a condition in which it waits on a TLP that never arrives, and the computer does not resume from S1.

PCI Express Base 1.0a L1 Exit Requirements

Without explaining the D-state functionality described in the PCI Express Base 1.0a specification, only the key requirements mentioned in the specification are mentioned in this document. The three sections in the following list in the PCI Express Base 1.0a specification describe how a 1.0a-compliant device must function.

- Section 5.3.1.2 (line 20): While in the D1 state, a function must not initiate any TLPs on the link with the exception of a PME message, as defined in Section 5.3.3.
- Section 5.3.1.3 (line 2): While in the D2 state, a function must not initiate any TLPs on the link with the exception of a PME message, as defined in Section 5.3.3.
- Section 5.3.2.2 (line 21): A downstream component would initiate an L1 exit transition to bring the link to L0 such that it may then inject a PME message.

As these sections indicate, the XIO2000A/XIO2200A can exit L1 only if it has a PME message to send.

PCI Express Base 1.1 L1 Exit Requirements

The functionality described in the 1.0a specification definitely has a problem if the upstream device does not send a TLP that puts the downstream device into D0 before sending any other TLPs after the link is placed in the L1 state. The PCI Express Base 1.1 specification resolves the issue by allowing a downstream device to send a TLP even if the link is in L1. The three sections in the following list describe some of the keys changes made to the PCI Express Base 1.0a specification.

- Section 5.3.1.2 (Line 19): While in the D1 state, a function must not initiate any Request TLPs on the link with the exception of a PME message, as defined in Section 5.3.3.
- Section 5.3.1.3 (Line 3): While in the D2 state, a function must not initiate any Request TLPs on the link with the exception of a PME message, as defined in Section 5.3.3.
- Section 5.3.2.2 (line 27): L1 exit must be initiated by a component if that component must transmit a TLP on the link.

Resolution

The issue can be resolved by preventing the Windows operating system from placing the XIO2000A/XIO2200A into a low-power device state (D1, D2, or D3 hot) when suspending the system into S1. The following instructions tell the operating system to leave the XIO2000A/XIO2200A in D0 when suspending the system.

Copy the lines below starting with “Windows Registry Editor…” into a text file ending in .reg (NoPmCaps.reg, for example). You can right-click on this file in the Explorer Shell and merge its contents into the registry. This sets PCI_HACK_NO_PM_CAPS (0x0000000020000000) for VID 104C and DID 8231.

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 Windows Registry Editor Version 5.00

[HKEY_LOCAL_MACHINE\SYSTEM\CurrentControlSet\Services\pci\Parameters]

"104C8231"=hex:00,00,00,20,00,00,00,00
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