Functional Safety Information

SN74LVC1G3157-Q1
Functional Safety, FIT Rate, FMD, and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for SN74LVC1G3157-Q1 (DBV and DCK package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

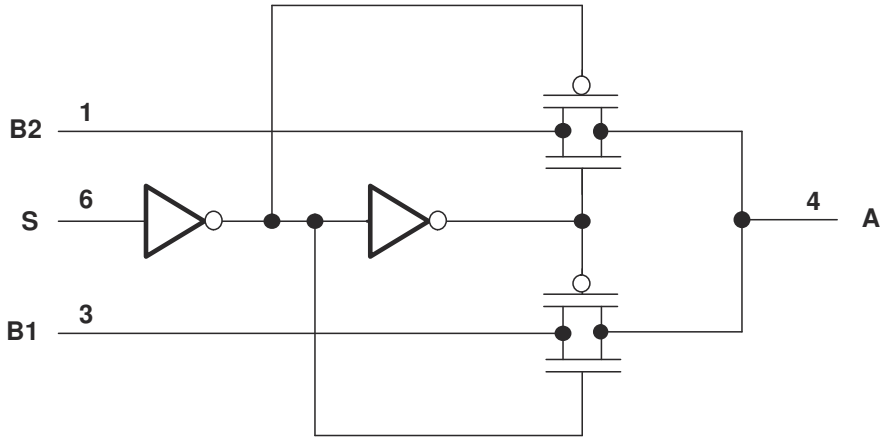

Figure 1-1. Functional Block Diagram

SN74LVC1G3157-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 DBV Package

This section provides functional dafety failure in time (FIT) rates for DBV package of SN74LVC1G3157-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5
Die FIT Rate	3
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
3	CMOS Analog switch, Bus Interface FCT, HC, LV, LVC, ALVC, VHC, and so forth.	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 DCK Package

This section provides functional safety failure in time (FIT) rates for the DCK package of the SN74LVC1G3157-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	4
Package FIT rate	2

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
3	CMOS Analog switch, Bus Interface FCT, HC, LV, LVC, ALVC, VHC, and so forth.	8 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN74LVC1G3157-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
NO or NC no output (Hi-Z)	20%
NO or NC channel stuck on	10%
NO or NC channel stuck off	10%
NO or NC functional out of specification voltage or timing	60%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the SN74LVC1G3157-Q1 (DBV and DCK package). The failure modes covered in this document include the following typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VDD (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 SN74LVC1G3157-Q1 DBV and DCK Package

Figure 4-1 and Figure 4-2 shows the SN74LVC1G3157-Q1 pin diagram for the DBV and DCK package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the SN74LVC1G3157-Q1 data sheet.

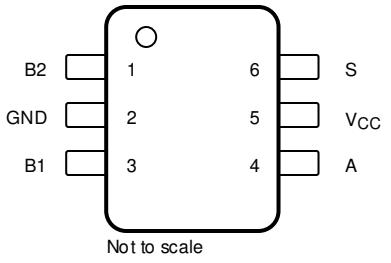

Figure 4-1. Pin Diagram (DBV) Package

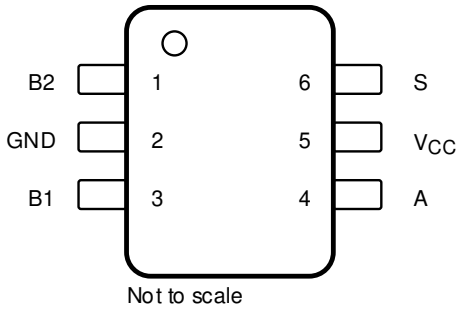

Figure 4-2. Pin Diagram (DCK) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
B2	1	Corruption of analog signal on B2 pin. If there is no limiting resistor in the switch path device damage is possible.	A
GND	2	No effect, normal operation.	D
B1	3	Corruption of analog signal on B1 pin. If there is no limiting resistor in the switch path device damage is possible.	A
A	4	Corruption of analog signal on A pin. If there is no limiting resistor in the switch path device damage is possible.	A
VCC	5	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
S	6	S pin stuck to GND. Cannot control switch states.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
B2	1	Corruption of analog signal on B2 pin.	B
GND	2	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
B1	3	Corruption of analog signal on B1 pin.	B
A	4	Corruption of analog signal on A pin.	B
VCC	5	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
S	6	Loss of control on Select pin. Switch in undefined state.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
B2	1	GND	Corruption of analog signal on B2 pin. If there is no limiting resistor in the switch path device damage is possible.	A
GND	2	B1	Corruption of analog signal on B1 pin. If there is no limiting resistor in the switch path device damage is possible.	A
B1	3	A	Not considered corner pin.	D
A	4	VCC	Corruption of analog signal on A pin. If there is no limiting resistor in the switch path device damage is possible.	A
VCC	5	S	Select pin stuck high. Cannot control switch states.	B
S	6	B2	Not considered corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VCC

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
B2	1	Corruption of analog signal on B2. If there is no limiting resistor in the switch path device damage is possible.	A
GND	2	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
B1	3	Corruption of analog signal on B1. If there is no limiting resistor in the switch path device damage is possible.	A
A	4	Corruption of analog signal on A. If there is no limiting resistor in the switch path device damage is possible.	A
VCC	5	No effect, normal operation	D
S	6	S pin stuck to VCC. Cannot control switch states.	B

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