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1 Overview

This document contains information for the TPS723-Q1 (SOT-23 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

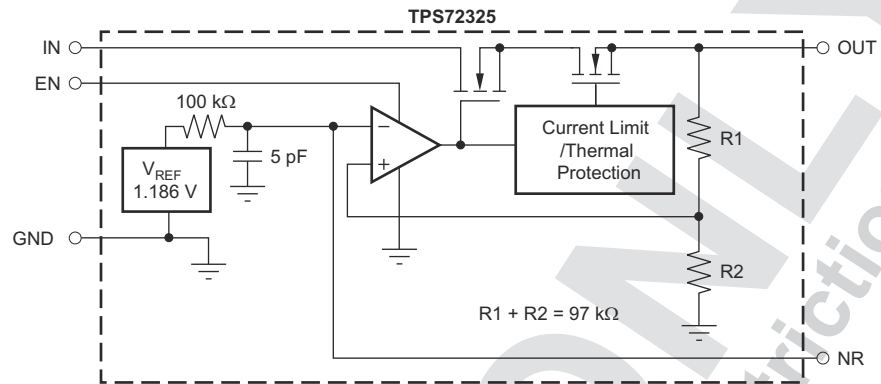


Figure 1-1. Functional Block Diagram

The TPS723-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS723-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	8
Die FIT rate	6
Package FIT rate	2

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 250mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS723-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT high (following VIN)	40
VOUT not in specification (voltage or timing)	10
VOUT low (no output)	40
Short circuit any two pins	10

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS723-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-1](#) shows the TPS723-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS723-Q1 data sheet.

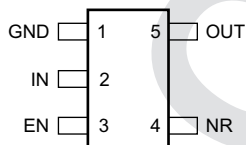


Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device contains DBV pin configuration. Device operates at free-air temperatures between -40°C and 125°C.
- Device operates at an input voltage less than -2.7V and more than -10V.
- Device operates according to all recommended operating conditions and does not exceed the absolute maximum ratings.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	No effect. Normal operation.	D
IN	2	Output voltage is at or near ground.	B
EN	3	LDO is always off due to EN being grounded.	B
NR	4	Output voltage is at or near ground.	B
OUT	5	Output voltage is at or near ground. Device is in current limit. The device can cycle in and out of thermal shutdown depending on power dissipation.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	There is no current loop for internal biasing; device cannot operate.	B
IN	2	No input to LDO. Output is at or near ground.	B
EN	3	EN pin voltage floats as the LDO contains no internal pullup or pull-down. LDO is in unknown state.	B
NR	4	Normal operation. Reference voltage does not have reduced noise.	C
OUT	5	Device output is unregulated and the load is not powered.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GND	1	IN	Output voltage is near or at ground.	B
IN	2	EN	If EN is positive voltage above the IN absolute maximum rating, IN can be damaged.	A
			If EN is negative voltage within recommended operating conditions there is no damage to the LDO, but device is always on when IN is powered.	B
NR	4	OUT	Output voltage is at or near ground.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	Output voltage is at or near ground.	B
IN	2	No effect. Normal operation.	D
EN	3	If EN is positive voltage above the IN absolute maximum rating, IN can be damaged.	A
		If EN is negative voltage within recommended operating conditions there is no damage to the LDO, but device is always on when IN is powered.	B
NR	4	Output voltage follows input voltage (overrides the voltage reference).	B
OUT	5	Regulation is not possible. The output voltage equals input voltage.	B

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