Functional Safety Information

REF35-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the REF35-Q1 (SOT-23 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

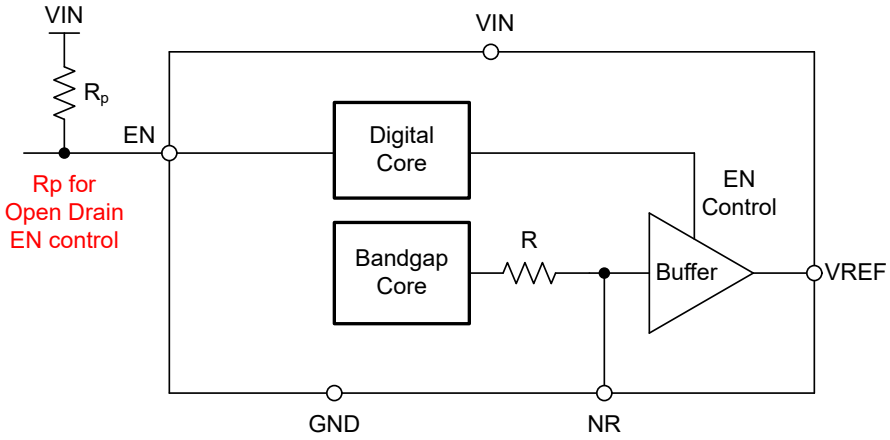

Figure 1-1. Functional Block Diagram

The REF35-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the REF35-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	4
Die FIT rate	2
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 20mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the REF35-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
V_{REF} output open or HIZ	30
V_{REF} output to ground	10
V_{REF} output out of voltage or timing specs	50
V_{REF} output stuck on	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the REF35-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the REF35-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the REF35-Q1 data sheet.

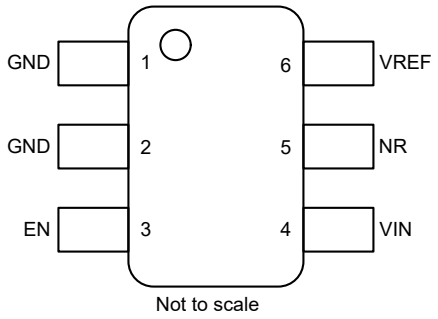

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- V_{IN} = 2.2V, V_{REF} = 1.8V
- NR and EN pins are open.
- C_{IN} = 0.1uF and C_{REF} = 1uF

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	Normal Operation.	D
GND	2	Normal Operation.	D
EN	3	The device is in shutdown mode.	B
VIN	4	The device has no power for normal operation	B
NR	5	No damage to device. The output does not regulate and is held low.	B
VREF	6	Potential device damage due to short circuit current. Not recommended condition.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	No damage to device. The output does not regulate and is held low.	B
GND	2	No damage to device. The output does not regulate and is held low.	B
EN	3	Normal operation. This pin can be left floating.	D
VIN	4	Device is unpowered.	B
NR	5	No damage to device. No impact to functionality.	D
VREF	6	No damage to device. No impact to functionality.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GND	1	GND	Normal Operation.	D
GND	2	EN	Loss of enable and disable functionslity. The device is in shutdown mode.	B
EN	3	VIN	Loss of enable and disable functionality. The device is in active mode.	B
VIN	4	NR	No damage to device. The output does not regulate and follows Vin	B
NR	5	VREF	No damage to device. NR pin pull more current than expected. Performance degration.	C
VREF	6	GND	Potential device damage while powering up. Not recommended condition.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	The device has no power for normal operation	B
GND	2	The device has no power for normal operation	B
EN	3	Loss of enable and disable functionality.	B
VIN	4	Normal operation.	D
NR	5	No damage to device. The output does not regulate and follows Vin	B
VREF	6	Large current can flow into V_{REF} , which can cause permanent damage	A

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