Application Report
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Using the ADS7841 and ADS7844 With 15-Clock Cycles

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ABSTRACT

This application report presents an analysis on the use of the 15-clock cycle method of operation for the ADS7841 and ADS7844 described in their respective data sheets. The advent of commercially available processors such as the TMS470 no longer restricts users from implementing the 15-clock cycle method with simple microprocessors. This method, however, does present some challenges to the software interface which is explored in this application report.

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1 Introduction

The serial peripheral interface (SPI) from Motorola began as a simple, fixed 8-bit transfer between master and slave devices on a common databus. Over the years, the interface has expanded with new processor development to allow the user to increase the number of clock cycles the master device could transmit. This typically added clock cycles in 4- or 8-bit increments allowing the master to issue 8, 12, 16, 20, etc. clocks per communication cycle.

The data sheets for both the ADS7841 and ADS7844 (12 bit, 4 and 8 channels with SPI control) describe *the fastest way to clock* data by using only 15 clocks per conversion cycle. The data sheets also suggest that this method is not possible with most microprocessors and is limited to field programmable gate arrays (FPGA) or application specific integrated circuits (ASIC).

2 TMS470 and TMS320x28xx Processors

The TMS470 series of microprocessors as well as the TMS320 28xx series of DSPs have implemented an SPI interface that allows the user to choose from 1 to 16 clocks per communication cycle. With such flexibility in the SPI interface, it is no longer appropriate to say that users must implement an FPGA or ASIC in order to use the ADS7841 or ADS7844 devices in the 15-clock cycle mode.

2.1 15 Clocks per Conversion

The 15-clocks-per-conversion method of interfacing the ADS784x devices does increase the effective throughput rate as mentioned in the data sheets. Running the devices at the 3.2-MHz serial clock speed shown in the specification tables boosts the throughput from [(1/3.2 MHz) $\times$ 16 clocks = 5 μS = 200 KSPS] to [(1/3.2 MHz) $\times$ 15 clocks = 4.68 μS = 213.6 KSPS].

The actual throughput, however, also depends on the time between data transfers initiated by the master SPI controller which typically runs in a burst clock fashion. The DSP can somewhat control the latency between data transfers by using programmable delay time, FIFO transfers, etc., but the user should still expect to see something slightly under 200 KSPS in the final application using a microprocessor.

2.2 Software Manipulation With an SPI Interface

The software associated with running an SPI interface often requires some manner of data manipulation in the processor. The sequence is started when the master transmits a *START* bit in the MSB position of the input data byte as shown in Figure 1.

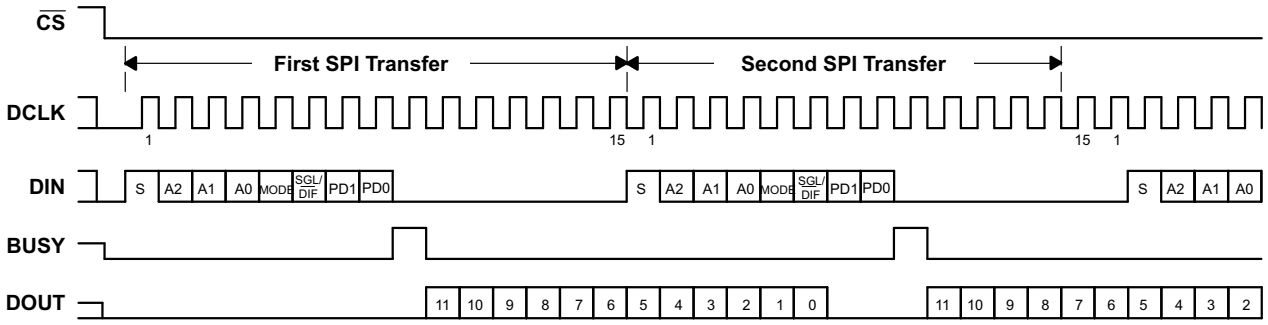

Figure 1. Typical 15-Cycle Interface

Because the data transfer to and from the data converter happens simultaneously, the host begins looking for the MSB of the conversion results on the same edges associated with the START bit. As shown in Figure 1, the MSB of the first set of conversion results is available on the 10th rising clock edge. To further complicate things, the second SPI cycle which begins conversion sequence 2 starts off reading bit 5 of the previous conversion cycle results. To effectively use the conversion data, the host must be able to shift and re-assemble the received data.

2.3 Accuracy versus Resolution

The 15-clocks-per-conversion method presents an additional caveat in regards to the 12-bit ADS7841 and ADS7844 devices.

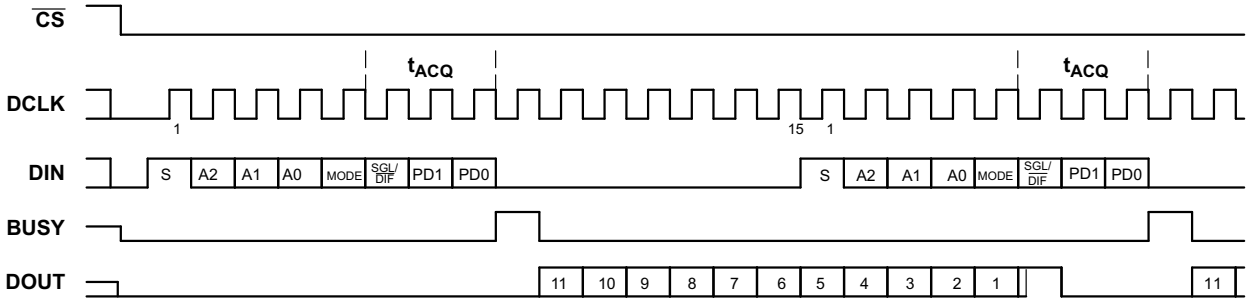

Figure 2. Short Cycled LSB

Both the ADS7841 and ADS7844 devices begin converting the acquired data during the period where the BUSY indicator goes high (see Figure 2). During the clock cycle when BUSY is active, the MSB is being converted with each subsequent bit converted during the next clock period. The actual data output shift, however, is one cycle delayed. In other words, the MSB is converted on cycle 9 and presented on cycle 10.

The data acquisition phase (opening of the sample/hold switches) begins after the reception of the MODE bit. On the falling edge of clock 5, the device internally forces the D0 output bit to a high state after a delay of approximately 200 ns. The result is the appearance of a *runt* bit which typically is missed by the host processor, because its duration is significantly less than ½ clock cycle. The received data is therefore 12 bits accurate, but with only 11 bits of resolution. The LSB is essentially lost to the host processor.

2.4 Conclusion

The 15-clocks-per-conversion method of using the ADS7841 and ADS7844 devices is a viable option when used with the SPI ports of TMS470 or TMS320x280x or 281x processors without the need to add expensive ASICs or complicated FPGAs. The drawbacks with this method include the loss of the LSB data, which ultimately reduces the overall accuracy of the system.

3 References

1. *TMS470R1x Serial Peripheral Interface (SPI) Reference Guide* (SPNU195)
2. *TMS320x281x, 280x DSP Serial Peripheral Interface (SPI) Reference Guide* (SPRU059)
3. *ADS7841, 12-Bit, 4-Channel Serial Output Sampling Analog-to-Digital Converter* data sheet (SBAS084)
4. *ADS7844, 12-Bit, 8-Channel Serial Output Sampling Analog-To-Digital Converter* data sheet (SBAS100)

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