LDO PSRR Measurement Simplified

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ABSTRACT

This application report explains different methods of measuring the Power Supply Rejection Ratio (PSRR) of a Low-Dropout (LDO) regulator and includes the pros and cons of these measuring methods.

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1 What is PSRR?

Power Supply Rejection Ratio or Power Supply Ripple Rejection (PSRR) is a measure of a circuit's power supply's rejection expressed as a log ratio of output noise to input noise. PSRR provides a measure of how well a circuit rejects ripple, of various frequencies, injected at its input. The ripple can be either from the input supply such as a 50Hz/60Hz supply ripple, switching ripple from a DC/DC converter, or ripple due to the sharing of an input supply between different circuit blocks on the board. In the case of LDOs, PSRR is a measure of the regulated output voltage ripple compared to the input voltage ripple over a wide frequency range (10Hz to 1MHz is common) and is expressed in decibels (dB). The PSRR is very critical parameter in many audio and RF applications.

The basic equation for PSRR is:

$$\text{PSRR} = 20\log\frac{\text{Ripple}_{\text{Input}}}{\text{Ripple}_{\text{Output}}} \quad (1)$$

Historically LDOs have poor high frequency PSRR performance, but currently TI has LDOs with PSRR > 40dB at 5MHz. One important point regarding the PSRR graphs in TI LDO datasheet is that the PSRR axis is inverted (See Figure 1). The PSRR is calculated as rejection so it should be a negative number; however, the graph shows it as positive number so that a higher number denotes higher noise rejection.

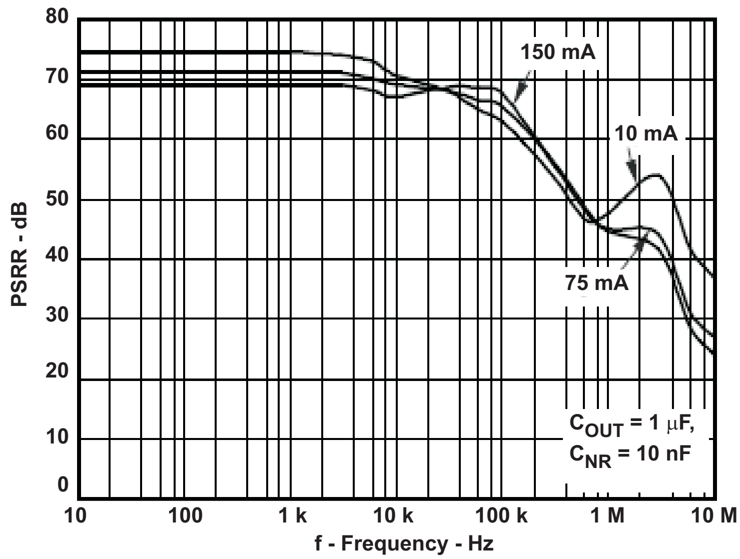

Figure 1. PSRR Graph of TPS717xx LDOs

2 Measuring PSRR of LDO

The following sections explain different methods of measuring the PSRR of an LDO.

1. Measuring PSRR using LC summing node method:

   The basic method of measuring PSRR is shown in Figure 2. In this method, DC voltage and AC voltages are summed together and applied at the input of the LDO. VDC is the operating point bias voltage and VAC is the noise source used in the test. Capacitor C prevents VAC from shoring VDC and inductor L prevents VDC from shorting VAC. So L and C are used for isolating both the sources, VDC and VAC, from each other.

   The L and C will create a high pass filter for VAC which will limit how low in frequency we can measure the PSRR. The 3dB point of this filter is determined by Equation 2. Frequencies below the 3dB point will start to be attenuated which will make measurements more difficult. The highest frequency that can be measured is determined by the self resonant frequencies of the L and C components.

   $$F_{min} = 1/\ 2\Pi\ \sqrt{LC} \quad (2)$$

   A drawback to this method is that it works well only for mid-range frequencies (approximately 1 kHz to 500 kHz).

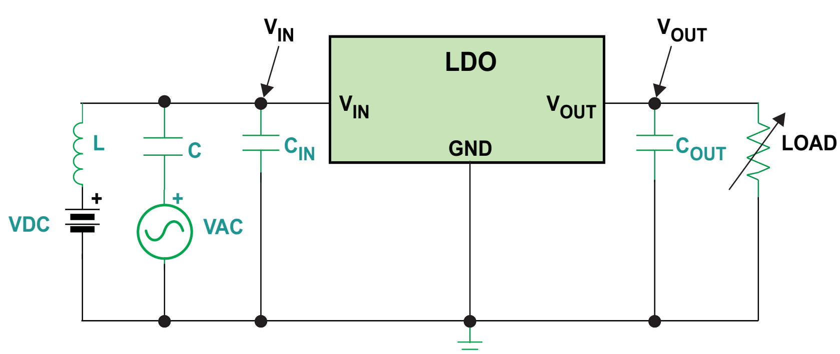

Figure 2. Basic Method of Measuring PSRR of LDO

2. Measuring PSRR using summing amplifier

   To improve the measurement of PSRR, a recommended method is described using a high-bandwidth amplifier as summing node to inject the signals and provides the isolation between VAC and VDC. This method is tested and verified using TPS72715 LDO and THS3120 high-speed amplifier from Texas

Instruments. The basic set-up is shown in Figure 3. The PSRR is measured with a no-load condition and the resulting measured PSRR graph corresponds with the datasheet graph of PSRR.

Keep in mind the following while measuring the PSRR using this method:

a. The input capacitor of LDO should be removed before the measurement because this capacitor could cause the high-speed amplifier to go unstable.

b. Vin and Vout should be measured with high-impedance probes (either scope or network analyzer) immediately at the Vin or Vout pins to minimize the set-up inductance effects.

c. There test set-up should not have any long wires since this will add inductance and impact the results.

d. While selecting the values of AC and DC inputs, the following conditions should be considered:

   VAC (max) + VDC < V_{ABS} (max) of LDO

   VDC – VAC > V_{UVLO} of LDO

   Also, the best results will be obtained if:

   VDC–VAC>Vout + Vdo + 0.5 where Vout is the output voltage of the LDO and Vdo is the specified drop out voltage at the operating point.

e. At very high frequencies, the response of the amplifier will start to attenuate the VAC signal that is applied to the LDO. At some point, the attenuated VAC will be too small to measure on the output of the LDO.

f. As load current increases, the open-loop output impedance of LDO decreases (Since a MOSFET output impedance is inversely proportional to the drain current), thus lowering the gain. Increasing the load current also pushes the output pole to higher frequencies, which increases the feedback loop bandwidth. The net effect of increasing the load is therefore reduced PSRR at lower frequencies (because of reduced gain) along with increased PSRR at higher frequencies.

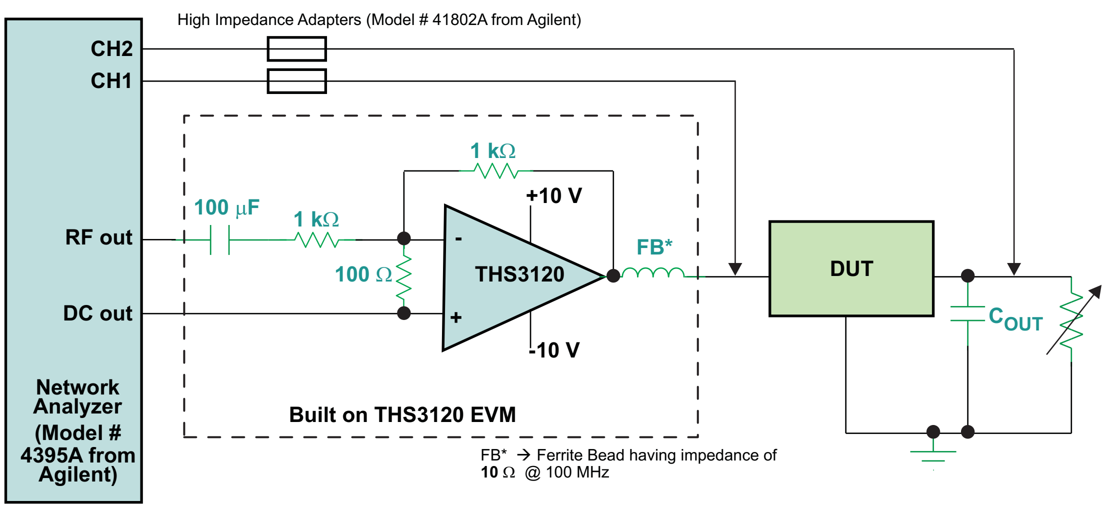

Figure 3. Recommended Method of Measuring PSRR of LDO

Figure 4 shows the PSRR graph measured with this method.

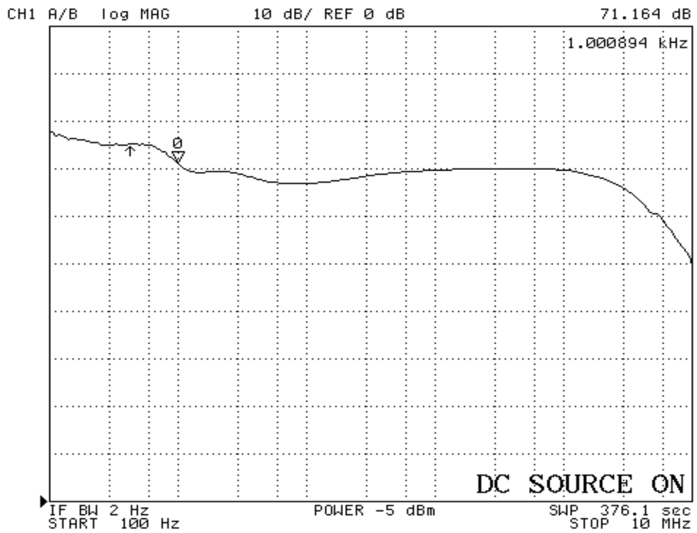

Figure 4. PSRR Measured With Recommended Method

The THS3120 is suitable for measuring PSRR up to VDC = 5V, Frequency = 10MHz and I_{load} = 400mA.

3 Measuring PSRR Using Oscilloscope

If the user does not have a network analyzer then there is a simpler but more cumbersome method which uses a signal generator, DC source and oscilloscope to measure the PSRR. An AC signal from signal generator is applied along with DC signal at the input of the LDO, as shown in either of the afore mentioned methods, and the output of the LDO is measured on an oscilloscope at different VAC frequencies. The PSRR is calculated using the Equation 1 where $Ripple_{(input)}$ is the amplitude of the input AC signal and $Ripple_{(output)}$ is the amplitude of output signal. This is then repeated at different frequencies of VAC to generate a piecemeal graph of PSRR.

This method can be used along with the set-ups described in the previous section. But this method is only good for LDOs with lower PSRR values due to resolution and sensitivity of oscilloscopes. Since most oscilloscopes can measure down to the millivolt range, the maximum range of PSRR that could realistically be measured using an oscilloscope is about 40dB–50dB.

Using the TPS78101EVM from Texas Instruments, the PSRR is measured using signal generator and oscilloscope. The input and output waveforms are as shown in Figure 5:

Test conditions are:

a. Vout = 3V
b. I_{load} = 150mA
c. VAC = 1V (p-p) at 1kHz
d. VDC = 4.3V dc

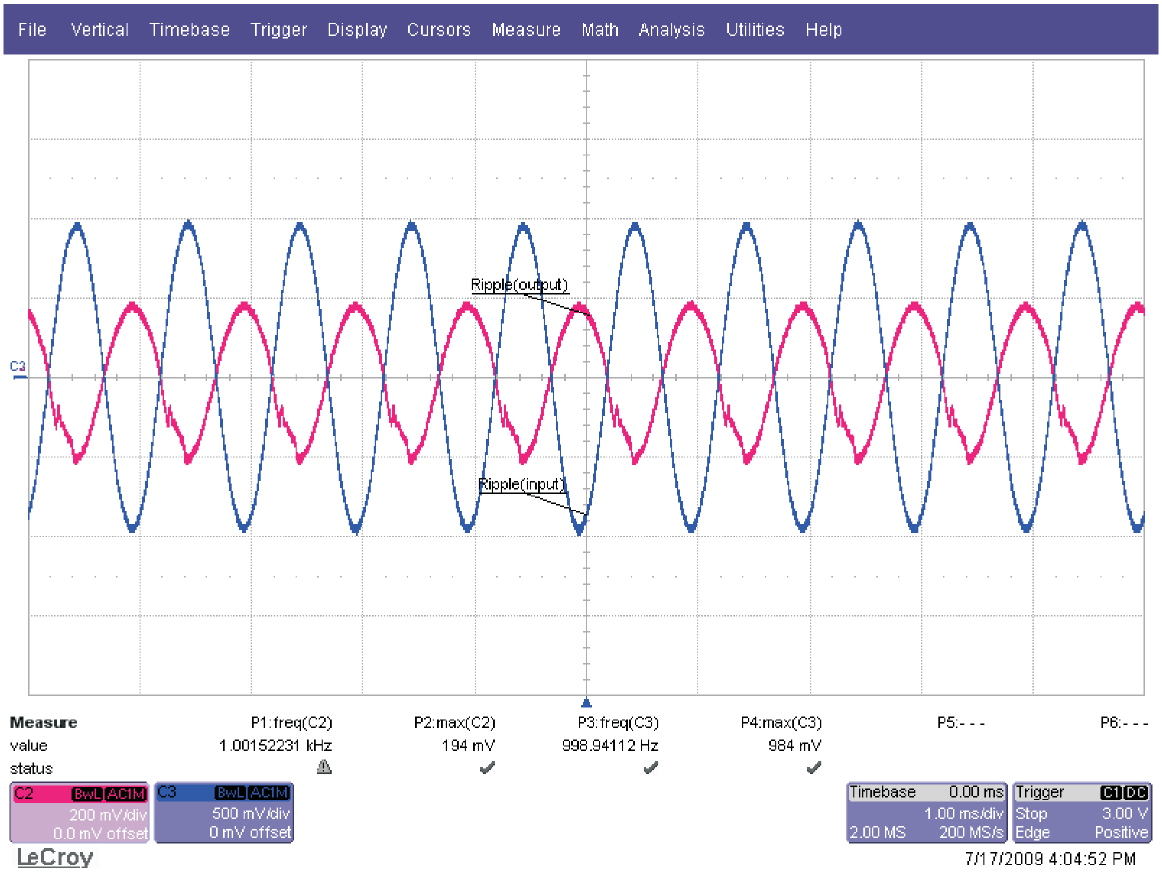

Figure 5. Input and Output Waveforms for Measuring PSRR Using Oscilloscope

And the PSRR is calculated from waveforms in Figure 5 is:

$Ripple_{(input)}$ = 984 mV
$Ripple_{(output)}$ = 194 mV
PSRR = 20 log10($Ripple_{(input)}$/ $Ripple_{(output)}$) = 20 log10(0.984/0.194) = 14.10dB which closely matches the PSRR specified in the datasheet of TPS78101.

This application report shows various methods to measure the PSRR of an LDO and also explains different aspects which need to be considered while measuring PSRR.

4 Implications of the LDO Noise

Let us take an example of a DC-DC Converter with integrated LDOs (such as TPS57140-Q1).

The bandgap noise that is internal to the LDO regulator becomes a limiting factor in the rejection of high frequency components. One of the example where its bad affect can be seen is when a a fast-falling input transient is applied at the input of the DC/DC converter. During the fast input falling edge, if the slew rate of the input is higher than a particular value, the internal LDO regulator of the device resets because of the power-supply rejection-ratio (PSRR) limitation. The fast transition corresponds to higher frequencies. The bandgap noise that is internal to the LDO regulator becomes a limiting factor in the rejection of high frequency components. For example, using the TPS57140- Q1 design simulation and bench test measurement, the resulting slew-rate value measured is 1.2 V/µs. If the slew rate is higher than this value, the device gets disabled and regenerates a soft start. Higher ESR of the input capacitor negatively affects the slew rate of the input voltage and the duration of this rate because of high current transient across the ESR according to ESR × C × dV/dt. Therefore, the use of a low-ESR ceramic capacitor is recommended.

Refer to *Design Considerations for DC-DC Converters in Fast-Input Slew Rate Applications* (SLVA693) for more information

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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