Application Note

Error Calculation for Unbuffered R2R DAC – Example Using DAC11001A

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ABSTRACT

The 20-bit DAC11001A is a highly accurate, low-noise, voltage-output, single-channel, digital-to-analog converters (DACs). The DAC11001 are specified monotonic by design, and offer excellent linearity of less than 4 LSB (max) across all ranges. The unbuffered voltage output offers low noise performance (7 nV/√Hz) in combination with a fast settling time (1µs), making this device an excellent choice for low-noise, fast control-loop, and waveform generation applications. When designing for these applications, its is necessary to calculate the total error contributed by the DAC and the associated circuit components. This report helps in understanding various DAC errors and how to calculate the total error in the system.

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1 Introduction

This application report describes how to calculate the total error in a DAC11001 system from various components like reference, reference buffer, output buffer, and the DAC itself. Figure 1-1 shows an example circuit topology using DAC11001 to get a 20 bit linear output. In this example, REF6025 used as reference and OPA828 as output and reference buffer respectively.

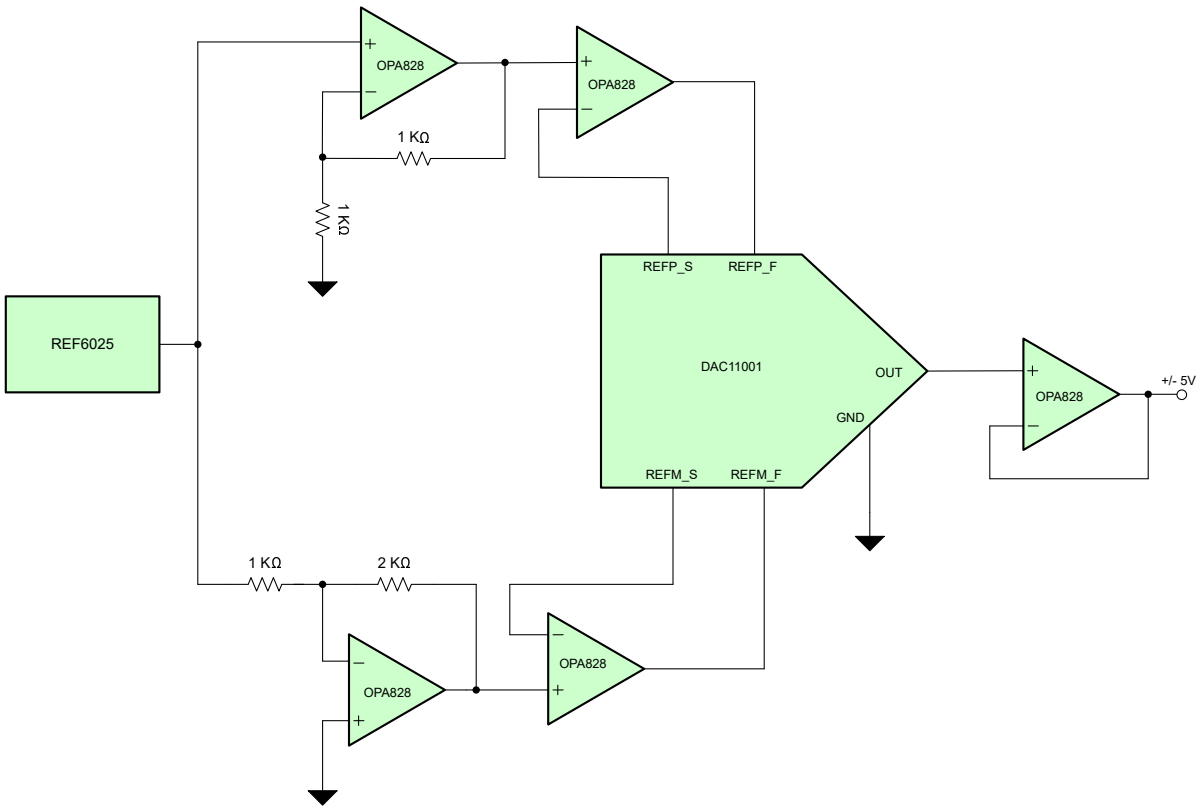

Figure 1-1. Circuit Topology

Table 1-1. Design Inputs

Parameters	Specifications
Output Voltage	±5 V
Reference source	2.5 V
Output Type	Buffered
Resolution	20-bit
Operating Temperature Range	-40 to 125°C

2 DAC Error Sources

Static errors, errors that affect the accuracy of the converter when it is converting static (dc) signals, can be described using four terms. These terms are offset error, gain error, integral nonlinearity and differential nonlinearity. Each term can be expressed in least significant bit (LSB) units or as a percentage of the full-scale range (FSR). For example, an error of ½ LSB for an 8-bit converter corresponds to 0.2% FSR. Figure 2-1 shows DAC ideal and actual transfer function. All the error sources and calculations in this document is expressed in parts-per-million (ppm).

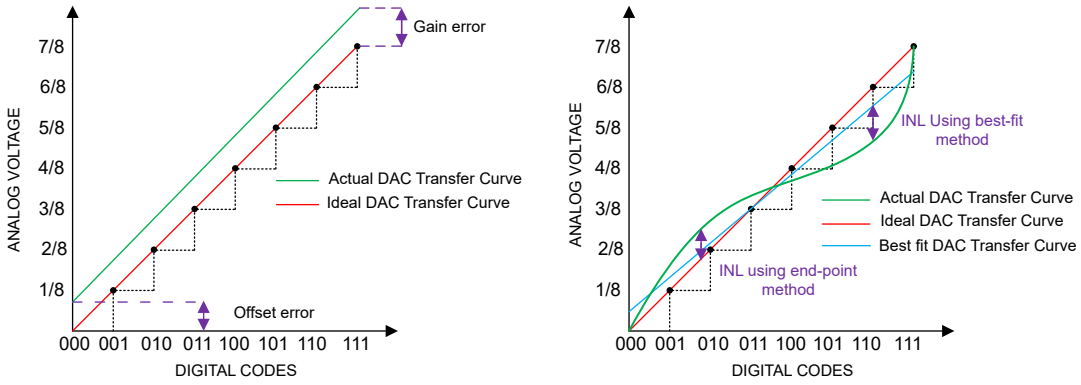

Figure 2-1. DAC Ideal and Actual Transfer Function

2.1 Offset Error

Offset error is the difference between the ideal output and the measured output in the linear region of the DAC transfer function. This error affects all codes by the same amount and usually can be compensated for by a trimming process.

$$Offset\ Error\ (ppm) = Offset\ Error(\%\ FSR) \times 10^4 \quad (1)$$

2.2 Gain Error

The gain error is the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero. Basically, this error represents a difference in the slope of the actual and ideal transfer functions and as such corresponds to the same percentage error in each step.

$$Gain\ Error\ (ppm) = Gain\ Error(\%\ FSR) \times 10^4 \quad (2)$$

2.3 Integral Non Linearity (INL)

The integral nonlinearity error (sometimes referred to as simply linearity error) is the deviation of the values on the actual transfer function from a straight line. This straight line can be either a best-fit straight line which is drawn so as to minimize these deviations or it can be a line drawn between the end points of the transfer function once the gain and offset errors have been compensated. The second method is called end-point linearity and is the usual definition adopted in data sheets.

$$Integral\ Non\ Linearity\ Error\ (ppm) = \left(\frac{INL\ Error\ (LSB)}{2^{Resolution} - 1}\right) \times 10^6 \quad (3)$$

2.4 Noise Sources

At any given code, the DAC, reference buffer, and output buffer noise sources error due to the noise sources comprises of DAC, reference buffers and output buffer contribute to the total noise error. These errors comprises of both voltage and current noises from reference buffers and ouput buffer. Current noises from the operational amplifiers in the inverting and non-inverting stages manifests as voltage noise due to the presence of the resistors in the amplifier stages.

At code D_n, noise at the output of the buffer will be:

$$V_n\left(nV/\sqrt{Hz}\right) = \sqrt{{V_{n0}}^2 + \left(\frac{D_n}{2^{20}}\right) \times {V_{n1}}^2 + \left(1 - \frac{D_n}{2^{20}}\right) \times {V_{n2}}^2 + \ + {V_{n3}}^2} \quad (4)$$

Where,

V_n = Total Noise at the output of the DAC

D_n = DAC Code

V_{n0} = Noise from DAC

V_{n1} = Output Noise from the non-inverting reference buffer

V_{n2} = Output Noise from the inverting reference buffer

V_{n3} = Noise from the output buffer

In Equation 4, V_{n1}, V_{n2} and V_{n3} includes both voltage and current noise.

3 Error Sources from Reference

Reference error consists of initial accuracy, temperature drift, noise, load regulation, and line regulation.

3.1 Initial Accuracy

The initial accuracy of voltage reference (VREF) indicates how close to the stated nominal voltage the reference voltage is guaranteed to be at room temperature under stated bias conditions.

$$Initial\ accuracy(ppm) = Initial\ accuracy(\%) \times 10^4 \quad (5)$$

3.2 Temperature Drift

The variation in V_{REF} over temperature is defined by its temperature coefficient (TC, also referred to as temperature drift) which has units of ppm per degree Celsius (ppm/ºC). The temperature coefficient can be specified over several different temperature ranges, including the commercial temperature range (0 to 70ºC), the industrial temperature range (-40 to 85ºC), and the extended temperature range (-40 to 125ºC). Error due to temperature drift can be calculated by the following equation. Please note that the below equation assumes uses the box method for calculating the error. The box method calculates TC using the difference in the maximum and minimum V_{REF} measurements over the entire temperature range . For more information about this method, please refer to the article Voltage Reference Selection Basics

$$Temperature\ Coefficient\ Error\ (ppm) = Output\ Voltage\ TempCo\left(ppm/^oC\right) \times Max\ Operating\ temperature\ Range \quad (6)$$

3.3 Load Regulation Error

Load regulation is the measure of the variation in V_{REF} as a function of load current and is specified either as a percentage or in parts-per-million (ppm) per milliampere (ppm/mA). It is calculated by dividing the relative change in V_{REF} at minimum and maximum load currents by the range of the load current. Load regulation depends on both the design of the reference and the parasitic resistance separating it from the load, so the reference should be placed as close to the load as the PCB layout will allow.

$$Load\ Regulation\ Error(ppm) = Load\ Regulation(ppm/mA) \times Reference\ Current(mA) \quad (7)$$

3.4 Line Regulation Error

Line regulation applies only to series voltage references and is the measure of the change in the reference voltage as a function of the input voltage. The importance significance of line regulation error depends on the tolerance of the input supply. In situations where the input voltage tolerance is within 10% or less, it may not significantly contribute to the total error. The extension of line regulation over frequency is the Power Supply Rejection Ratio (PSRR). PSRR is rarely specified, but typical curves are usually provided in the data sheet. As with line regulation, the importance significance of PSRR depends on specifics the characteristics of the input

supply. If V_{IN} is noisy (generated with a switching regulator, sensitive to EMI, or subject to large load transients), PSRR may be critical.

3.5 0.1 - 10 Hz Peak-to-Peak Noise

The internally-generated noise of a voltage reference causes a dynamic error that degrades the signal to- noise ratio (SNR) of a data converter. Low frequency V_{REF} noise is specified over the 0.1 Hz to 10 Hz bandwidth as a peak-to-peak value (in µV or ppm). Filtering below 10 Hz is impractical, so the low-frequency noise contributes directly to the total reference error.

$$0.1\ to\ 10Hz\ noise(ppm) = \left({}^{0.1\ to\ 10Hz\ noise(\mu V_{PP})}\Big/_{Output\ Voltage}\right) \times 10^6 \tag{8}$$

When calculating the total error in V_{REF} it is best to separate error specifications where a maximum value is guaranteed (TC, initial accuracy, load regulation, line regulation) and those where only a typical value is provided (0.1 Hz to 10 Hz noise, thermal hysteresis, and long-term stability). Other than initial accuracy, the guaranteed specifications are all linear coefficients and their contribution to the total error can be calculated based on the operating ranges of the reference (temperature range, load current, and input voltage).

3.6 Example Using REF7025

Table 3-1 shows an example calculation using REF7025 as voltage reference.

Table 3-1. REF7025 Example Calculation

Error Components	Error in ppm
Initial Error	250
Temperature Coefficient Error	200
Load Regulation	75
Noise Error	0.25
Total Error	**525.25 (All error sources are added)**

4 Error Sources from Inverting and Non-Inverting Gain Stage

4.1 Input Offset Voltage Error

Input offset voltage, V_{IO}, is defined as the DC voltage that must be applied between the input terminals to force the quiescent DC output voltage to zero or some other level, if specified. If the input stage was perfectly symmetrical and the transistors were perfectly matched, V_{IO} = 0 V.

$$Input\ offset\ Volatge\ Error(ppm) = {}^{V_{os}(max)(V) \times Offset\ Voltage\ Gain}\Big/_{|\ (Opamp's\ Output\ Volatge)(V)\ |} \tag{9}$$

where,

$$Offset\ Voltage\ Gain\ =\ 1 + {}^{Rf}\Big/_{R_g} \tag{10}$$

Where R_f and R_g are the feedback and the gain setting registers respectively. Above equation is valid for both inverting and non-inverting amplifier stages.

4.2 Input Offset Voltage Drift Error

Input offset voltage drift error is defined as the expected change in input offset voltage due to change in temperature. To calculate the offset voltage drift error in ppm see Equation 11.

$$Input\ offset\ Voltage\ Drift\ Error\left(\ ppm\ \right) \tag{11}$$

$$= \frac{\frac{dV_{OS}}{dT}\left(max\right)\left(\mu V/^{o}C\right) \times\ Max\ Operating\ temperature\ Range\left(^{o}C\right) \times\ \ Offset\ Voltage\ Gain\ \times 10^6}{|\ Op\ amp's\ Output\ Volatge(V)\ |}$$

4.3 Power Supply Rejection Ratio (PSRR) Error

Power supply rejection ratio describes how well an amplifier rejects variations in the power supply voltage. PSRR is defined as the shift in offset per volt of shift in power supply, and generally is given in units of micro-volts per volt (µV/V). The OPA828 used in this design note has a maximum PSRR of 7 µV/V. Thus, for the OPA828, the power supply can change 1 V with only 7 µV of shift in the offset. Note that this is DC PSRR, where as PSRR in general is frequency dependent. As frequency increases, PSRR decreases. Equation 12 can be used to calculate the offset error due to PSRR for a given power supply ripple voltage.

$$Offset\ Voltage\ Error\ due\ to\ PSRR\ = \left(\frac{Ripple\ Voltage(V)}{10^{PSRR(min)dB/20}}\right) \times 10^6 \times \left(Offset\ Voltage\ Gain/_{Output\ Voltage(V)}\right) \quad (12)$$

4.4 Open Loop Gain Error

This error describes the deviation of gain from the set value due to the finite nature of the open loop gain of the operational amplifier. This error can be minimized by selecting a high open loop gain amplifier.

$$Open\ Loop\ Gain\ Error(ppm) = Gain \times \left[\frac{1}{1+\left(10^{AOL(dB)/20}\right)\times\left(\frac{R_g}{R_g+R_f}\right)}\right] \quad (13)$$

4.5 Resistor Tolerance Error

This error refers to the gain error caused by the tolerance of the gain setting resistors. This is one of the major contributors of error in any amplifier design. \ and Equation 15 can be used to calculate the error due to resistor tolerances for both the non-inverting and inverting gain stages.

Equation for non-inverting stage:

$$Resistor\ Tolerance\ Error(ppm) = \frac{\left\{\left[1+\frac{R_f(\Omega)\times\left(1+\frac{Tolerance(\%)}{100}\right)}{R_g(\Omega)\times\left(1-\frac{Tolerance(\%)}{100}\right)}\right] - Abs\left(1+\frac{R_f}{R_g}\right)\right\}}{Abs\left(1+\frac{R_f}{R_g}\right)} \times 10^6 \quad (14)$$

Equation for inverting stage:

$$Resistor\ Tolerance\ Error(ppm) = \frac{\left\{\left[1+\frac{R_f(\Omega)\times\left(1+\frac{Tolerance(\%)}{100}\right)}{R_g(\Omega)\times\left(1-\frac{Tolerance(\%)}{100}\right)}\right] - Abs\left(-\frac{R_f}{R_g}\right)\right\}}{Abs\left(-\frac{R_f}{R_g}\right)} \times 10^6 \quad (15)$$

5 Example Calculation using DAC11001A

Referring to Figure 1-1 for the circuit example, we can calculate the error from all sources which are mentioned below.

Table 5-1. Reference Non-inverting Amplifier (OPA828)

Error Source	Error in ppm
Input Offset Voltage	140
Offset voltage drift	60
Bias Current	0.6
Offset Current	0.3
Resistor Tolerance	100.01
Resistor Tolerance Drift	499.88
Total	**532.05**

Table 5-2. Reference Buffer (OPA828)

Error Source	Error in ppm
Input Offset Voltage	140
Offset voltage drift	60
Total	**152.32**

Table 5-3. Reference Inverting Amplifier (OPA828)

Error Source	Error in ppm
Input Offset Voltage	210
Offset voltage drift	90
Bias Current	1.2
Offset Current	0.6
Resistor Tolerance	200.02
Resistor Tolerance Drift	0.25
Total	**303.66**

Table 5-4. R2R DAC (DAC11001A)

Error Source	Error in ppm
Integral Non Linearity	1.9
Zero Code Error	3.81
Zero Code Drift	40
Gain Error	10
Gain Error Drift	40
Total	**57.95**

Table 5-5. Voltage Reference (REF6025)

Error Source	Error in ppm
Initial Error	250
Temperature Coefficient Error	200
Load Regulation	75
Total	**525**

Table 5-6. DAC Output Buffer (OPA828)

Error Source	Error in ppm
Input Offset Voltage	70
Offset Voltage Drift	30
Total	**76.2**

6 Error Summary

Total error for this DAC circuit topology can be calculated using root-sum-square method or worst-case error method. Assuming all the error sources are not correlated to each other, we can calculate the total error as follows.

$$Total\ Error\ = \sqrt{Vref\ Error^2 + DAC\ Error^2\ +\ Non\ Inverting\ Amp\ Error^2 + Inverting\ Amp\ Error^2\ + \ldots\ldots\ldots} \quad (16)$$

Table 6-1. Total Error Calculations

Error Contribution	Error in ppm
DAC11001A	57.95
Voltage Reference (REF6025)	525
Non Inverting Amplifier (OPA828)	532.05
Inverting Amplifier (OPA828)	303.66
Reference Buffer (Both inverting and non inverting stages)	215.38
DAC output buffer (OPA828)	76.2
Total	**840.65**

As shown in Table 6-1, it is clear that the total error in the 20-bit DAC system is dominated by the reference amplifier and the buffer section. DAC11001A contributes approximately 4% of the total error in the system.

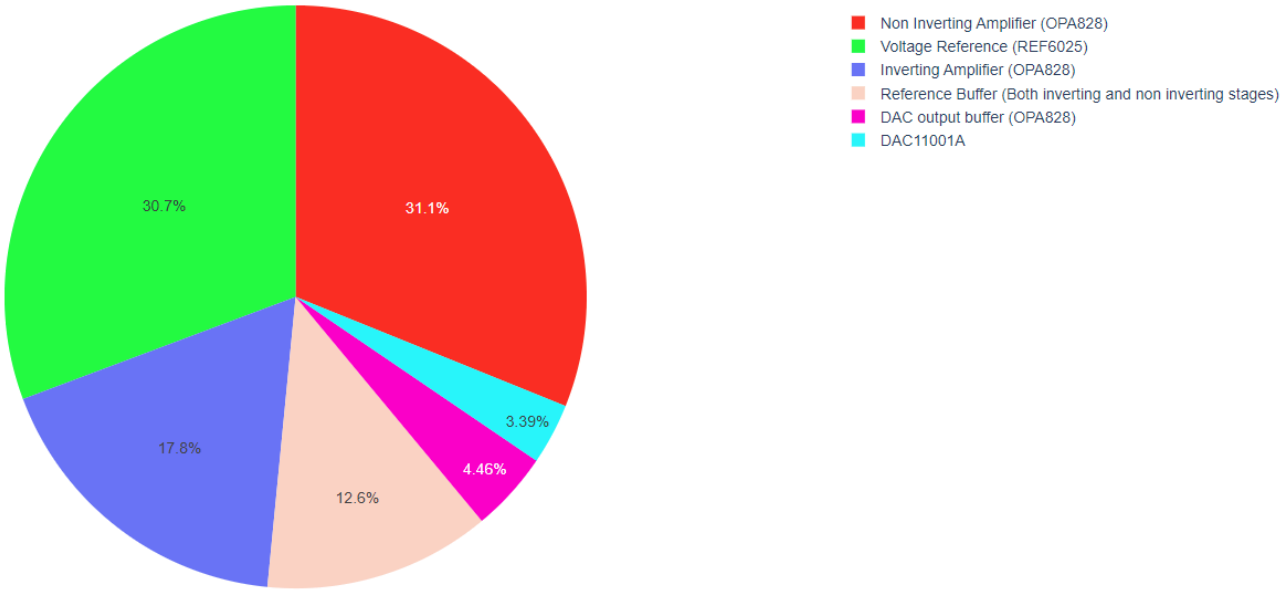

Figure 6-1. Error Distribution Pie Chart

Table 6-2. Design Featured Devices

Device	Key features	Link
DAC11001A	DACx1001 20-Bit, 18-Bit, and 16-Bit, Low-Noise, Ultra-Low Harmonic Distortion, Fast Settling, High-Voltage Output, Digital-to-Analog Converters (DA	DAC11001A
OPA828	OPA828 Low-Offset, Low-Drift, Low-Noise, 45-MHz, 36-V JFET-Input, RRO Operational Amplifier	OPA828
REF6025	REF60xx High-Precision Voltage Reference With Integrated ADC Drive Buffer	REF6025

7 References

- Texas Instruments, *Tips and Tricks for Designing with Voltage References* voltage reference design
- Texas Instruments, *Introduction to Digital to Analog Converters* training
- Texas Instruments, *TI Precision Labs- Key AC & DC Specifications* training

8 Revision History

Changes from Revision * (May 2022) to Revision A (August 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated equation	6

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