Application Note

Design and Test of a HART-Enabled Field Transmitter for 4-20mA Loops

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ABSTRACT

This application note describes integrating the AFE881H1 into a HART®-enabled field transmitter for 4-20mA loop instrumentation. HART (Highway Addressable Remote Transducer) allows for two-way digital communication across the current loop at the same time as transmitting the value of a primary process variable. First, a basic introduction to 4-20mA loops and the HART protocol is presented. The AFE881H1 is then introduced as an ultra-low-power, 16-bit digital-to-analog converter (DAC) combined with a HART modem. This device also has an on-board analog-to-digital converter (ADC) and integrated diagnostic sensors for system monitoring. Testing for this transmitter for HART registration is also presented. Physical layer tests and test setups for the waveform are described as well as the data link layer (DLL) tests for the HART signaling and timing. Application layer tests for HART universal commands (UAL) and commonly-implemented commands (CAL) are also described. Finally, other TI devices with HART connections are showcased. TI offers several HART modems that convert HART signals into either UART or SPI communication. All these devices all integrate HART into many industrial products.

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Trademarks

1 Introduction

1.1 The 4-20mA Loop

Understanding the 4-20mA loop is essential to explaining how HART is implemented in a field transmitter. The 4-20mA loop is a standard signaling method often used in factory automation and control to transmit information on a current loop. A sensor at a remote location measures a process variable and sets the current through the loop to indicate the measurement value. Figure 1-1 shows basic diagram of the loop.

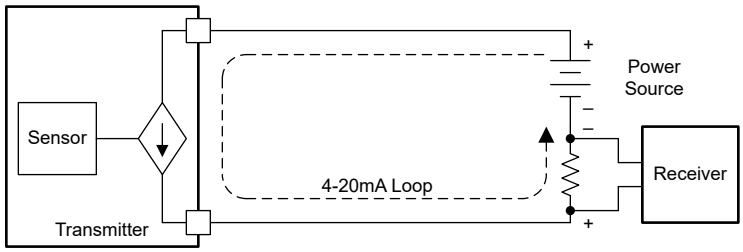

Figure 1-1. Components of the 4-20mA loop

The 4-20mA loop has four basic components. The first component is the loop. Each transmitter operates on a separate loop and a receiver measures the current in the loop across a resistor. The loop is simple, durable, and easy to debug. The loop is robust against electrical noise, making the loop reliable for long-distance transmissions. The 4-20mA loop can be extended to 500 meters or longer. The loop is also cost-effective and already commonly exists in many factory automation and control systems.

Second, the loop has a transmitter with a sensor used in process control. This sensor measures a parameter such as pressure, temperature, flow, or any other input for an industrial process or factory floor. The transmitter converts the measurement into the current value in the loop. For example, a transmitter measures the temperature of an oven from between 100°C to 500°C. In the 4-20mA loop, 4mA is used as the minimum value of the measurement and 20mA is used as the maximum value of the measurement. In that case, 4mA translates to 100°C and 20mA translates to 500°C. All measurements are linearly converted to this current value. In some systems, loop currents under 4mA and currents over 20mA can be used to indicate some error from the transmitter. For transmitters compliant to the NAMUR NE 43 standard, currents below 3.6mA or above 21mA are interpreted as a sensor fault. For designers of these systems, noise, resolution, and linearity are all important parameters for transmitter design.

Next, the loop has a power supply capable of sourcing at least 20mA. If NAMUR fault levels are supported by the transmitter, then higher levels of current are needed to indicate an error. The power supply is often a standard voltage of 24V. However, voltages of 36V, 15V, 12V or other voltage can be seen depending on the system. This power supply sends current through the loop and often also powers the transmitter.

Finally, there is a receiver that measures the current on the loop. The receiver measures the voltage across a series resistance. The current is calculated and converted to the *primary variable*. A load resistance of typically 250Ω is measured with an ADC to convert the primary variable back to the measured result from the transmitter.

1.2 The HART Protocol

HART is a backwards-compatible enhancement to 4-20mA instrumentation that allows two-way communication with smart, microprocessor-based field devices.

The HART signal is superimposed onto a 4-20mA loop current and modulated for two-way digital communications. This is important because 4-20mA loops are already a well-adopted standard in factory automation and control. The fact that this technology is backwards compatible and can be used with already-existing infrastructure means that this is easy to adopt and cost effective.

HART is a standardized communication protocol, where the controller sends commands, and a remote transmitter returns standardized responses. The application layer data received by the commands communicates device status and diagnostics. Process data can be sent to include the data's floating-point digital values, the engineering units of the primary variable, and other information about the data the device is measuring.

There are several different versions of the HART protocol. This application note discusses only the basic HART frequency shift keyed (FSK) signal in a remote transmitter on a 4-20mA loop. For more in-depth information about the HART protocol see *A Basic Guide to the HART Protocol*.

1.2.1 Adding HART to the 4-20mA Loop

Starting with the original diagram for the 4-20mA loop in Figure 1-1, HART can be added to the transmitter and receiver. HART communication uses the original 4-20mA loop and adds a two-way digital signal to the loop using HART modems. Again, this backwards compatibility makes HART any easy add-on to existing infrastructure. Figure 1-2 shows how HART is added to the basic 4-20mA loop.

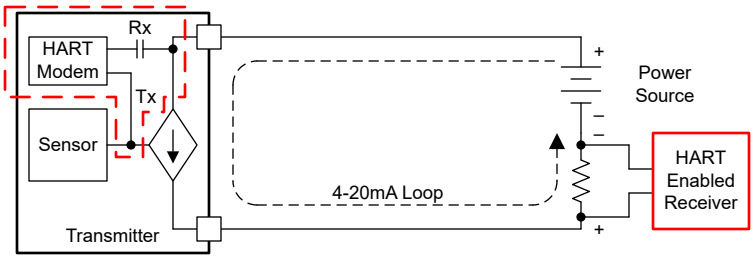

Figure 1-2. Adding HART to the 4-20mA loop

The HART FSK is added to the signal controlling the current in the loop. In the transmitter, the HART modem receives the signal from the loop. The modem capacitively couples the input voltage to receive the HART signal. The modem also modulates the current to send the HART signal. This transmitted signal is superimposed onto the current representing the primary variable as measured by the sensor.

At the same time, the receiver measures the voltage across the resistor to measure the primary variable. In the HART-enabled receiver, a HART modem is used to both transmit commands and receive HART communication from the transmitter. However, the primary variable measurement requires a low pass filter to filter out the HART signal. A resistor is used to measure the current in the loop which represents the primary variable. The minimum resistance for HART communication is 230Ω, and 250Ω is often used.

1.2.2 HART FSK

HART communication uses an FSK signal to create digital bits in the communication. The modem sends two different frequencies for bits that become the 0 or 1 in the digital communications. This digital communication is similar to UART in byte structure using 8 data bits, odd parity, and 1 stop bit. Figure 1-3 shows a representation of the instantaneous current in the loop with a HART modulated signal. This HART signal is superimposed onto the 4-20mA current that represents the primary variable.

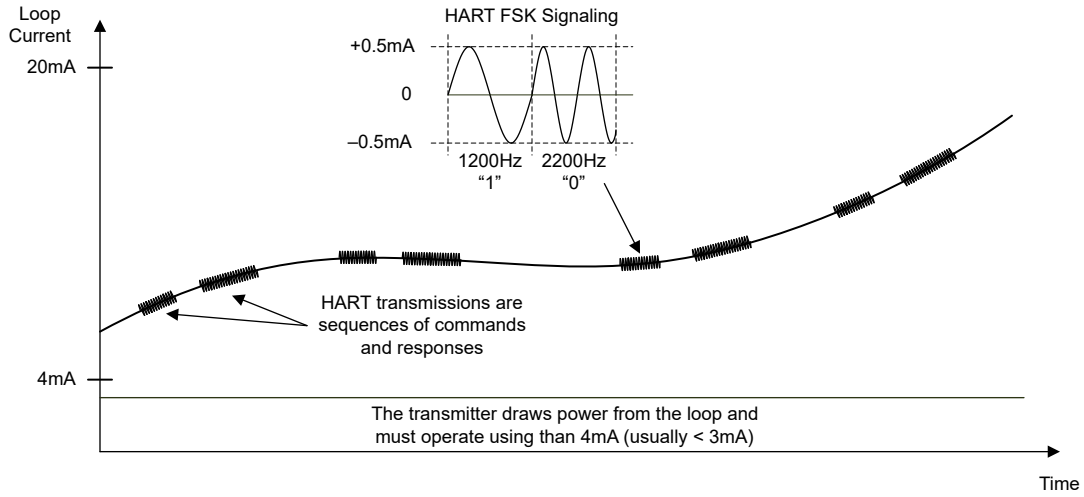

Figure 1-3. The HART FSK Modulated Onto the 4-20mA Current Loop

Transmitters often operate on the loop power. The power applied to the loop is also used to power the transmitter. Because there is no other source of power and the loop's zero scale is 4mA, the transmitter must operate with a current budget of under this amount of current. With currents below 3.6mA representing errors, the transmitter must effectively operate with a maximum budget of 3mA. This is shown in the shaded section at the bottom of the previous figure.

Bits for HART transmissions are represented as two FSK signals. Different frequencies represent 1s and 0s. A 1200Hz signal is a digital 1 and a 2200Hz signal is a digital 0. The data is sent at 1200 baud so each bit is 833µs. The primary variable is sent as the current in the loop. This current operates at a low frequency below 20Hz. Figure 1-4 shows the frequency bands used for the primary variable and the HART FSK frequencies.

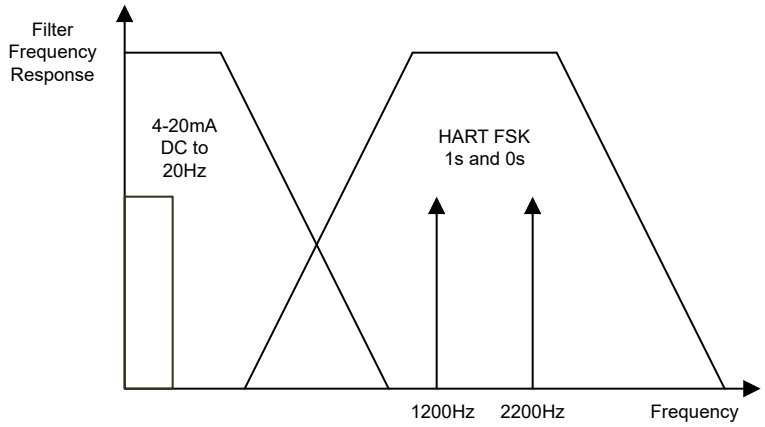

Figure 1-4. The Primary Variable and HART Frequency Bands the 4-20mA Current Loop

Because the primary variable and the HART signal share the same transmission, the signals must be filtered to be received. This diagram shows the frequency content of the primary variable and the HART signal.

In the HART enabled receiver, the primary variable is read using a low-pass filter to measure the voltage across a resistor. This signal, represented as the shaded area of the figure, is generally under 20Hz so the low-pass filter has a cutoff frequency of about 25Hz. The HART transmits at a higher frequency, with the FSK bits at 1200Hz and 2200Hz. This HART signal is received using a band-pass filter that typically operates from 500Hz to 10kHz.

2 AFE881H1 HART Modem

Here, the AFE881H1 HART modem IC is introduced. This device is used as the centerpiece for a HART-enabled transmitter. Figure 2-1 shows the AFE881H1 block diagram.

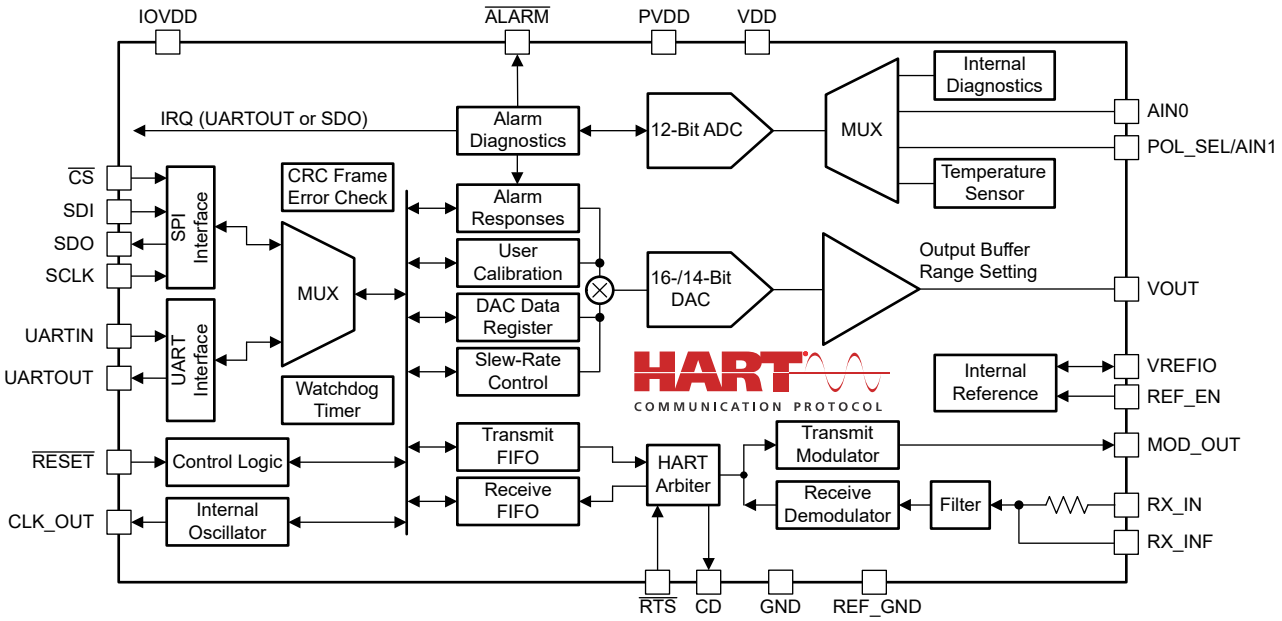

Figure 2-1. AFE881H1 Block Diagram

The block diagram shows many of the features of the device. The AFE881H1 has a 16-bit voltage output DAC used to set the loop current and has an integrated HART modem. The DAC has user calibration that can adjust for offset and gain error. The DAC also has slew rate control that can slow DAC output transitions. The slew rate control can be used to help shape the output signal for HART testing.

The device also has an internal, 12-bit, multiplexed ADC. ADC measurements of internal nodes of the device can be monitored for programmable alarms for functional safety. An internal precision reference can be used for both the DAC and ADC.

SPI or UART communication can be used to program the device, or a combination of the two can be used for the HART protocol. The device has optional cyclic redundancy check (CRC) for error checking communications and a watchdog timer verify communication connections.

The integration of the DAC, HART modem, ADC, and other system monitor functions make the AFE881H1 a good choice as the centerpiece for a remote transmitter.

2.1 AFE881H1 HART Transmitter

To test HART functionality of the device, a board was constructed for registration as a HART transmitter. Figure 2-2 shows the AFE881H1 HART block diagram transmitter design.

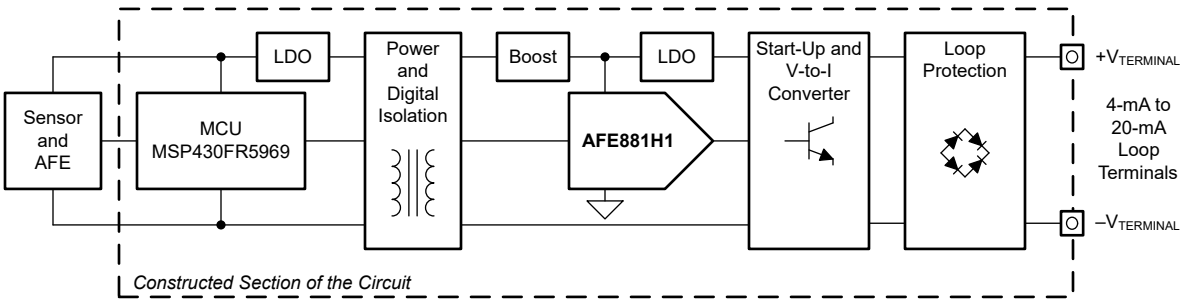

Figure 2-2. 2-wire Transmitter Design Using an AFE881H1 Block Diagram

The terminals connected to the loop are shown on the right side of the block diagram. This connection to the loop powers the entire transmitter. A bridge rectifier at the input protects against reverse connection to the loop. The rectified loop voltage powers a start-up circuit that provides power to a low-dropout regulator (LDO), that in turn powers the AFE881H1. The LDO powers a fly-back converter acting as a boost and supplies power across an isolation barrier. On the other side of the isolation barrier, another LDO powers the MCU and any sensor connected to the transmitter. The LDOs also power the digital signal isolation on each side of the barrier.

HART communications are translated with the AFE881H1 HART modem. The device receives the HART signal through a capacitive coupled connection to the positive terminal side after the loop protection to the board. The HART signal is transmitted to the loop through the voltage-to-current (V-to-I) stage of the board.

Note that this transmitter board does not have a sensor to transmit data. The loop current is nominally set to 4mA as an output, except for specific HART tests. The main purpose of this board is to test the HART communication functionality of the AFE881H1.

2.2 Detailed Schematic

Figure 2-3 shows the AFE881H1 HART detailed schematic transmitter design. The figure shows the loop power connection on the right side of the figure. Input protection is placed between the input terminals and the transmitter circuit. The positive loop connection then goes to a startup circuit for the board and powers an LDO. This LDO powers the AFE device, op-amps, and V-to-I control.

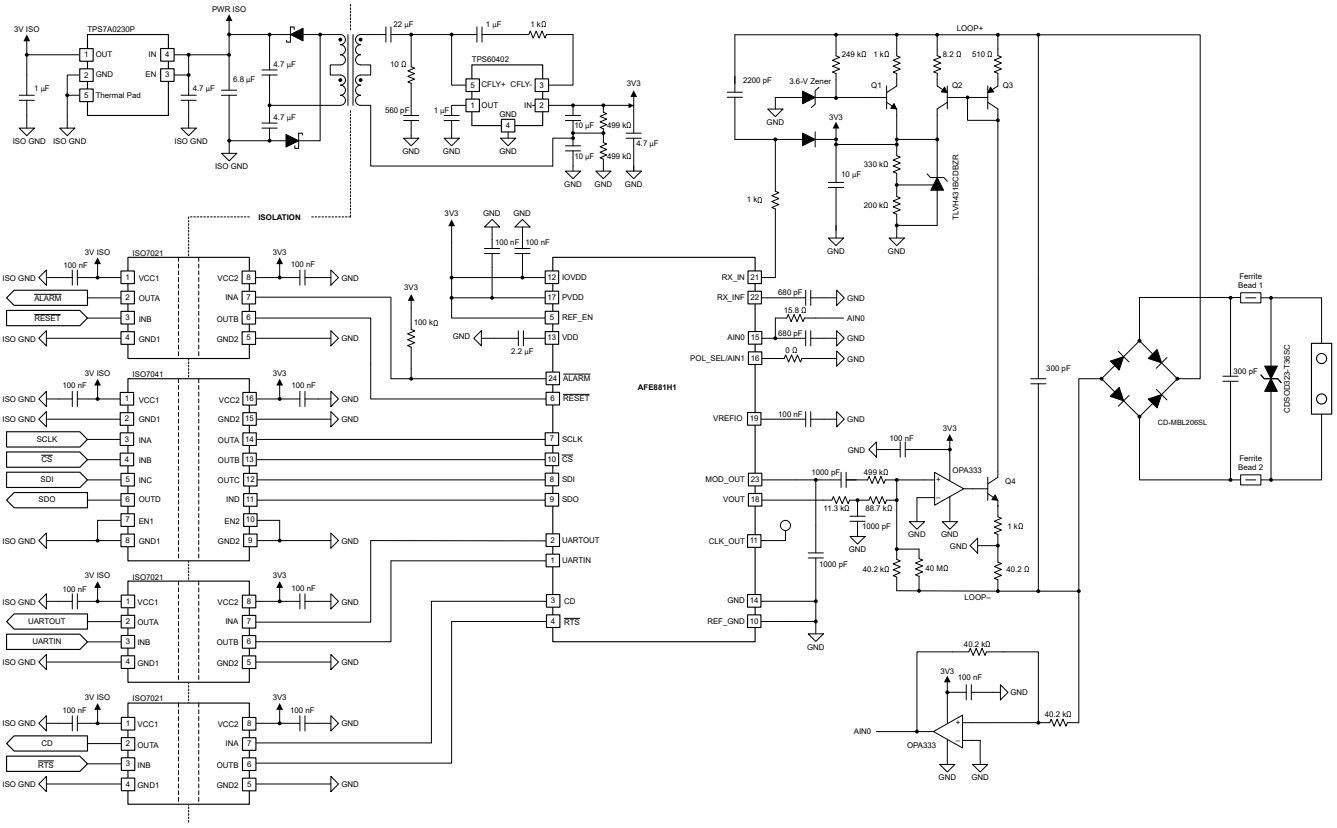

Figure 2-3. 2-wire Transmitter Design Using an AFE881H1 Circuit Schematic

The LDO also drives a flyback converter acting as a boost to drive power across an isolation barrier. A set of digital isolators send communication across the isolation barrier. On the opposite side of the isolation is another LDO that powers the microprocessor.

The AFE881H1 controls the loop current through the V-to-I section. The DAC voltage sets the output from 0.3V to 2.5V. The output is sent through a V-to-I converter block using an OPA333 and an NPN bipolar junction transistor (BJT) that controls the loop current. In the constructed circuit, a MSP430FR5969 is used as the microprocessor, but is not shown in the figure.

2.2.1 Input Protection

The input of the board is the loop connection on the right side of the schematic shown in Figure 2-3. Figure 2-4 shows input protection for the board starting with a TVS diode to prevent damage from over-voltage events. Ferrite beads and input capacitance also help reduce any high-frequency transients seen at the inputs. An input rectifier protect the transmitter from swapping the positive and negative inputs from mis-wiring.

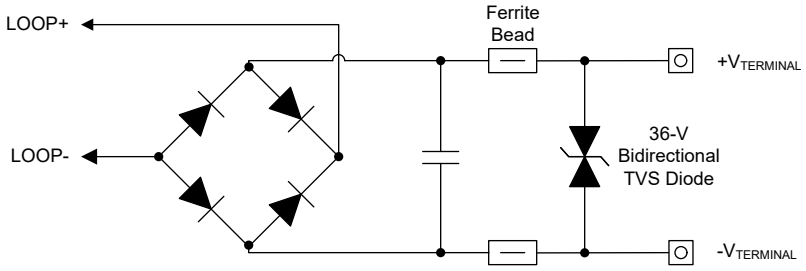

Figure 2-4. Input Protection Circuit at the Input Terminals of the Board

When voltage is applied to the input terminals, the power is delivered to the circuit through LOOP+ and LOOP- setting the current in the 4-20mA loop.

2.2.2 Startup Circuit

The schematic in Figure 2-5 shows the startup circuit of the HART transmitter. When power is applied, voltage pulls up on LOOP+ to start up the TLV431B LDO to power the board.

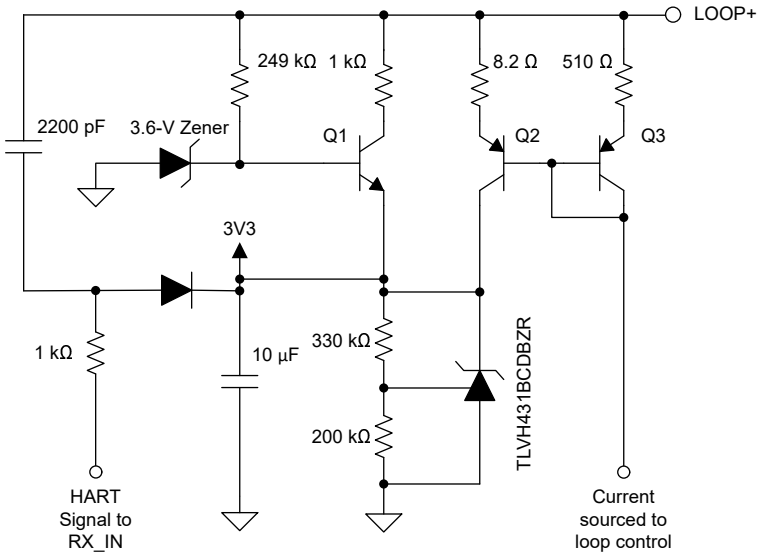

Figure 2-5. Transmitter Board Startup Circuit

The 249kΩ resistor allows current to flow through the 3.6V Zener diode, the voltage pulls up on the base of Q1. The Zener voltage starts the current through Q1 to turn on the LDO. The TLV431B LDO sets up the 3.3V supply.

As the 3.3V supply comes up, the control circuitry pulls current from Q3. This turns on Q2, which then takes over supplying current to the LDO.

When the 3.3V LDO output reaches the final value, the voltage at the emitter of Q1 rises. With the 3.6V driving the base of Q1 and 3.3V at the emitter, this voltage difference reduces the base-emitter voltage of Q1 to 0.3V. With a low base emitter voltage, Q1 shuts off. Q2 the maintains the current needed to drive LDO output and shunt the extra loop current. Because Q2 is the primary path of current through the transmitter, the transistor must be a PNP capable of high-power dissipation.

Take care when selecting the Zener diode. The voltage across the Zener diode varies with the loop voltage and the temperature of the circuit. This variance can change the V_{BE} across Q1 and change the total current going

through the start-up circuit. If the voltage is too high, the Zener diode sets Q1 to continue to source current after the circuit starts up. If the voltage is too low, the Zener diode prevents the TLVH431B from turning on. Verify proper start up by checking that the 3.3V supply starts up, and that Q1 turns off when in operation

2.2.3 Voltage-to-Current Stage

Figure 2-6 shows a simplified schematic of the V-to-I stage of the transmitter. This stage sets the current of the loop based on the voltage output of the DAC.

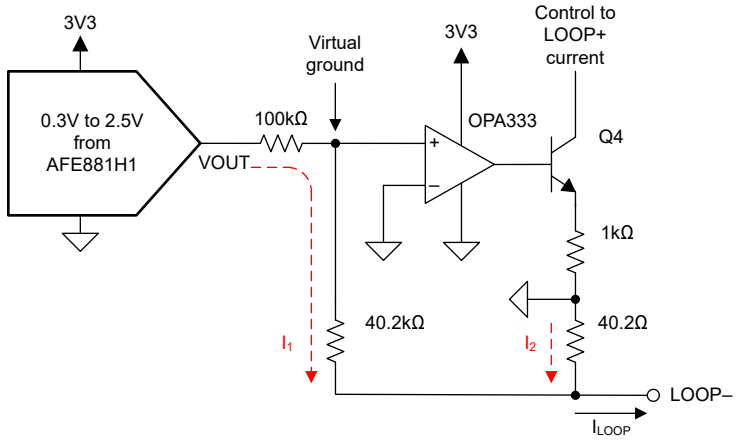

Figure 2-6. Voltage-to-Current Converter Stage for the Transmitter Board

In this circuit, the DAC voltage is set across 100kΩ of equivalent resistance. The voltage at the opposite end of the 100kΩ is a virtual ground set by the feedback of the OPA333. The output of the OPA333 drives Q4 which sets the controls the loop current.

The current I_1 flows through the 40.2kΩ resistor to set the LOOP– to a voltage below ground.

$$I_1 = VOUT / 100k\Omega \quad (1)$$

$$V_{LOOP-} = I_1 \times 40.2k\Omega \quad (2)$$

Current through the 40.2kΩ resistor is amplified 1000:1 with the 40.2Ω resistor and I_2 is pulled from ground to LOOP–.

$$I_2 = V_{LOOP-} / 40.2\Omega = I_1 \times 40.2k\Omega / 40.2\Omega = I_1 \times 1000 \quad (3)$$

$$I_{LOOP-} = I_1 + I_2 = 1001 \times I_1 = 1001 \times VOUT / 100k\Omega \quad (4)$$

2.2.4 Voltage-to-Current Calculation

The OPA333 drives control to the LOOP+ current and sets I_2 to maintain the LOOP– voltage. Because of the ratio of the resistors, I_2 is 1000 times larger than I_1. I_{LOOP-} equals I_1 plus I_2, I_{LOOP-} is 1001 times I_1.

Note that the original schematic has a large resistance in parallel with the 40.2kΩ resistor. The parallel resistance slightly reduces the current gain to 999 to 1 and I_{LOOP-} equals VOUT / 100.

The DAC code maps directly to the current through the loop. Because the DAC has an output voltage range of 0.3V to 2.5V, the voltage is mapped to loop current of 3mA to 25mA. Because the loop current is based on the DAC voltage, the current can be set as a function of the DAC_CODE.

$$I_{LOOP-} = VOUT / 100 \quad (5)$$

$$I_{LOOP-} = [(DAC\_CODE / 2^{16}) \times 2.2V + 0.3V] / 100 \quad (6)$$

Table 2-1 shows different DAC code values and how the values map to the loop current in milliamps. Loop currents 3.375mA and 21.75mA are chosen as the sensor error indicator levels.

Table 2-1. DAC Code Values Converted to Voltage Output and Loop Current Setting

OUTPUT CONDITION	DAC CODE	DAC OUTPUT (V)	LOOP CURRENT (mA)
DAC minimum	0x0000	0.3	3
Error low	0x045D	0.3375	3.375
In-range minimum	0x0BA2	0.4	4
In-range mid-scale	0x68BA	1.2	12
In-range maximum	0xC5D1	2.0	20
Error high	0xDA2E	2.175	21.75
DAC maximum	0xFFFF	2.5	25

2.2.5 HART Signal Transmission

The HART signal is added to the loop current through superposition of a summing junction from the OPA333 shown in Figure 2-7.

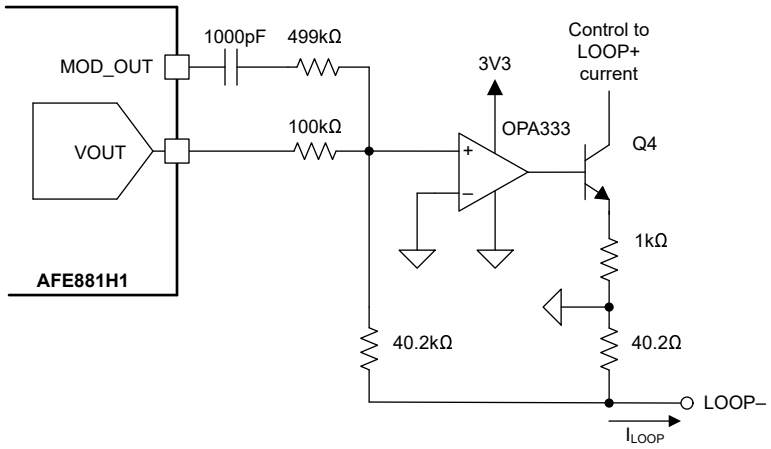

Figure 2-7. Addition of the HART Signal From MOD_OUT to the V-to-I Stage

The MOD_OUT signal is nominally 500mV$_{PP}$. This voltage is summed into the loop current through a DC blocking 1000pF capacitor and a 499kΩ resistor. 499kΩ is a standard 1% resistor value.

Similar to the VOUT calculation of the V-to-I stage, the HART current is calculated to be 1.002mA$_{PP}$, where the HART signal amplitude is 1mA$_{PP}$.

2.2.6 HART Input Protection

The HART input to the AFE881H1 is capacitive coupled to LOOP+ which operates at a voltage near to the positive supply. With higher voltages of operation, the HART RX_IN pin requires protection from these voltages at startup. Figure 2-8 shows a clamp used in the circuit to prevent the pin from being exposed to high loop voltages.

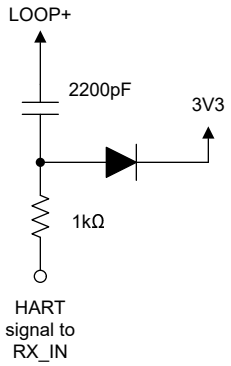

Figure 2-8. RX_IN Clamp Circuit for Over-Voltage Protection

To sense the HART signal, the RX_IN pin is connected to LOOP+ through a DC blocking capacitor, which keeps the RX_IN pin at a low voltage. However at startup, LOOP+ goes to a high voltage and the capacitor starts at 0V. This pulls the RX_IN pin up to a high voltage which quickly drops from the low capacitance.

The clamp protects the HART input pin. A series 1kΩ resistor limits any current going into the pin while a diode clamps the resistor to 3.3V.

2.2.7 Current Consumption

Table 2-2 shows the current consumption of the various components on the board. The AFE881H1 in particular operates on very low power and can also be operated with a supply as low as 1.8V. The power savings is particularly important because the transmitter must be able to operate with less than 3mA of current, and power savings for this portion can be applied to use in the sensor.

Table 2-2. Design Components Current Consumption

DEVICE	DESCRIPTION	TYPICAL CURRENT (µA)
TPS7A0533	LDO	4
AFE881H1	16-bit DAC	180
OPA333 (2)	Operational amplifier	17 (each)
TLVH431B	Shunt regulator	60
MSP430	Microcontroller	Dependent on firmware
ISO7021D (2), ISO7041F	Digital isolation	Dependent on communications

2.2.8 HART Transmitter Board

Figure 2-9 shows picture of the AFE881H1 HART transmitter design. Loop power is applied to the board through a terminal at the right side of the board. In series with this connection is a 499Ω resistor. The black clip leads across the resistor are for two HART modems attached to a HART test system. The wires then connect to a power supply that typically runs at 24V.

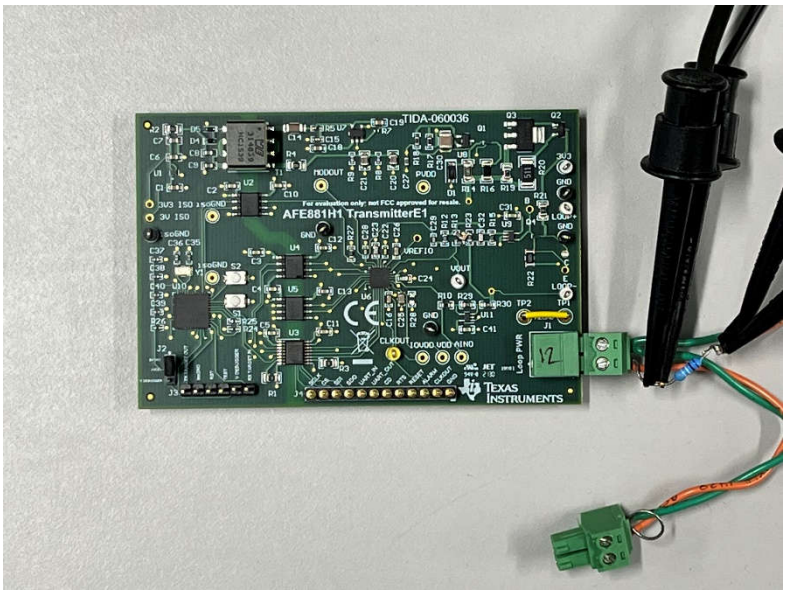

Figure 2-9. Transmitter Circuit With Modem Clip Leads Around Test Resistor

A second terminal connector is placed in parallel to this system, shown in the figure as unconnected. This connector is used to test two transmitters together in HART multi-drop mode, and is not used for the standard 4-20mA loop.

2.2.9 HART Protocol Stack

As a HART modem, AFE881H1 organizes the physical layer of the transmissions. The physical layer refers to the HART FSK signal superimposed on the 4-20mA loop. The AFE881H1 translates this signal for the microprocessor to UART or SPI. However, the firmware programmed into the microprocessor sets the framing for communication or interprets the HART commands. This firmware is the known as HART protocol stack.

The HART stack manages the communication between devices in the of the protocol. The firmware checks that messages are delivered correctly and handles error checking and correction. The stack also is responsible for the correct responses to application commands in the HART protocol.

For this design, the HART stack was written for the MSP430FR5969. This firmware for this transmitter was developed by Smart Embedded Systems (SES) of Pleasanton, CA. For more information about SES services, see www.smartembeddedsystems.com.

3 HART Testing and Registration

3.1 HART History and the FieldComm Group

HART was established by Rosemount Incorporated in the mid-1980s. This protocol is based on the Bell 202 modem communication standard. Rosemount is now a subsidiary of Emerson Electric Company.

Rosemount developed HART as a proprietary communication standard to add smart capability to field instruments. As this communication standard became popular, the standard developed into HART and became an open protocol. Since 2015, the HART protocol has been governed by the FieldComm Group. FieldComm maintains the protocol and oversees any changes or modifications. HART is currently on Revision 7.

HART compliant devices are also registered by the FieldComm Group. Registration is completed after testing the device for compliance to the protocol and a paid registration fee.

3.2 HART Testing Overview

Previously, Figure 2-1 showed the block diagram of the AFE881H1 device. In the middle of the figure is the HART communication protocol logo. To use this logo, the device was designed into a transmitter in a HART registered device.

To be HART registered, the device is first tested by the company that created the device. Test results are used to generate a report sent to the FieldComm Group with an application for registration. Test results include physical layer tests that verify the waveform, check the timing of the HART FSK carrier signal, and verify timing with some HART specific digital lines built into the HART modem. Additionally, there are many tests that verify the HART protocol to check that the device has the proper response to commands from a HART controller.

3.2.1 HART Protocol Specifications

Below is a list of HART protocol specifications. These specifications outline how HART devices respond to commands as well as describe how the physical layer of the protocol.

- HART Communication Protocol Specification (HCF_SPEC-13 FCG TS20013)
- Token-Passing Data Link Layer Specification (HCF_SPEC-81 FCG TS20081)
- Command Summary Specification (HCF_SPEC-99 FCG TS20099)
- Universal Command Specification (HCF_SPEC-127 FCG TS20127)
- Common Practice Command Specification (HCF_SPEC-151 FCG TS20151)

These specifications can be viewed online at the FieldComm Group website. These specifications cannot be downloaded by non-member companies, but can be purchased as a bound book. Member companies can download electronic copies of the protocol specifications in a PDF. Companies purchase membership from the FieldComm Group.

3.2.2 HART Protocol Test Specifications

This is a list of HART protocol *test* specifications. The following documents describe the details of HART testing. The documents describe how the tests are constructed and what different test failures look like.

- FSK Physical Layer Test Specification (HCF_TEST-2 FCG TT20002)
- Token-Passing Data Link Layer Test Specification (HCF_TEST-1 FCG TT20001)
- Universal Command Test Specification (HCF_TEST-3 FCG TT20003)
- Common Practice Command Test Specification (HCF_TEST-4 FCG TT20004)

While the entire HART protocol specifications can be viewed online, only the *table of contents* of these test specifications can be viewed online at the FieldComm Group website. Non-member companies must purchase the bound books. Member companies can download electronic copies of the specifications in a PDF.

3.2.3 Remote Transmitter Device Testing

There are several different physical device types compatible with HART communication. Devices are categorized by impedance level. These devices can be high impedance devices such as current output, voltage inputs, or remote, two-wire transmitter devices attached to 4-20mA loops. Other devices can be low impedance devices such as current inputs, voltage outputs, or actuators that must have an impedance of 230Ω to 600Ω within the HART frequency band of operation.

Each of these different physical device types require different tests and different test setups. This application note discusses the testing for a remote transmitter device.

3.3 HART Test Equipment

Below are some of the equipment needed to run HART testing for your field transmitter.

- A test load resistor used in the loop. This is typically 500Ω depending on the particular test.
- An oscilloscope is required to observe the HART signals. The physical layer tests require the FSK to have a certain waveshape and magnitude, that have specific rise and fall times.
- A frequency counter is needed to observe the frequency of the FSK bits. In these tests, an oscilloscope is used to verify the frequency.
- A DC power source of about 40V maximum powers the loop.
- A signal generator is used for generate interference noise of different frequencies and amplitude to verify HART communications in presence of noise.

There are also a few specialized pieces of equipment required to run the HART physical layer tests. These devices are shown in Figure 3-1.

Figure 3-1. HART Test System Shown With an HCF_TOOL-31, HCF_TOOL-32, and an FSK Physical Test Interface

A HART test system is required for the HART protocol testing. While this system is mostly required for the data link layer and command tests, the test system can be used to generate the HART responses from the transmitter to view the specific FSK bits and responses. The HART test system is Linux® based, and runs tests with a set of commands designed by FieldComm. The HART test system requires two HART registered RS-232 modems.

The HCF_TOOL-31 filter is needed for the physical layer tests. This filter is a passband Butterworth filter that passes the HART FSK digital signal. The filter has a 2nd order roll-off below 500Hz, 1st order roll-off above 10kHz, and a passband gain of 10. This filter passes the HART FSK signal but removes the lower frequencies of the primary variable and any noise from higher frequencies.

The HCF_TOOL-32 filter is also required. This filter is a low-pass Butterworth filter with a 2nd order roll-off above 25Hz and a passband gain of 10. This low-pass filter passes the analog primary variable from a field transmitter and rejects the HART FSK signal and higher frequencies.

Finally, the FSK Physical Layer Test interface is used to increase and decrease the HART sinusoids from the HART test system in the transmission. This device is used to determine the sensitivity of the field transmitter for detecting the HART signal.

The HART test system, the HCF_TOOL-31 filter, the HCF_TOOL-32 filter, and the FSK Physical Layer Test interface can be purchased from FieldComm.

3.4 HART Physical Layer Testing

The HART physical layer tests are described in HCF TEST-2. This document defines the requirements for testing HART devices for compliance with the HART FSK Physical Layer Specification. These tests verify many different parameters of the HART communication.

- Verify the bit rate and signal frequencies for the HART transmission.
- Verify that a carrier detect signal is sent within a minimum time after the start or stop of a HART transmission.
- Measure the low-pass primary variable signal to check that a carrier detect start or stop does not disrupt the transmission of the primary variable.
- Check that the output noise is below a maximum level when the HART is not transmitting.
- Test the HART communications are still available when the current of the primary variable is cycling between the minimum of 4mA and maximum of 20mA (analog rate of change test).
- Measure the HART device to verify high receive impedance over the frequency of the primary variable and HART frequency band.
- Test HART transmission in the presence of in-band and out-of-band sinusoidal noise.
- Check the carrier detect level to make sure a HART signal is detected when the signal is at the minimum amplitude, and not detected below a lower amplitude, while maintaining carrier detect timing.

As part of the physical layer of the HART protocol, these tests cover the timing and amplitude of the HART signal as generated by the AFE881H1 and with the surrounding circuitry. The following sections describe the HART physical layer tests and test setups.

3.4.1 FSK Sinusoid Test

Figure 3-2 shows a block diagram of the HART FSK sinusoid test. Most HART tests require a similar setup with the transmitter as the device under test. The FSK sinusoid test verifies that the HART signal have the correct frequencies and wave shape for transmission.

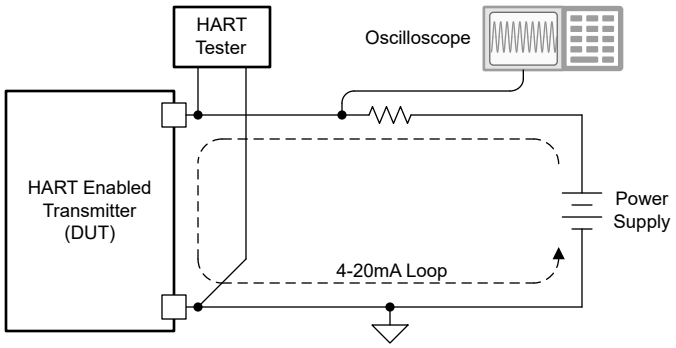

Figure 3-2. HART FSK Sinusoid Test Block Diagram

A Keysight E36313A is used as the 24V power supply. The power supply powers the loop and the transmitter sets the current through the loop. A series resistor is used to measure the current through the loop, but also attaches to the HART test system through a modem.

For the HART FSK sinusoid test, an oscilloscope measures the HART transmitted signals. The HART tester sends commands and the oscilloscope plots the responses to find a series of 1s and 0s to measure the HART bits. A frequency counter can be used to measure the frequency of the FSK bits, but an oscilloscope can also be used to verify the timing.

Figure 3-3 and Figure 3-4 define the tolerance of the HART FSK signals. As previously mentioned, the two FSK signals are 1200Hz and 2200Hz. However, there is some acceptable variation in the signal.

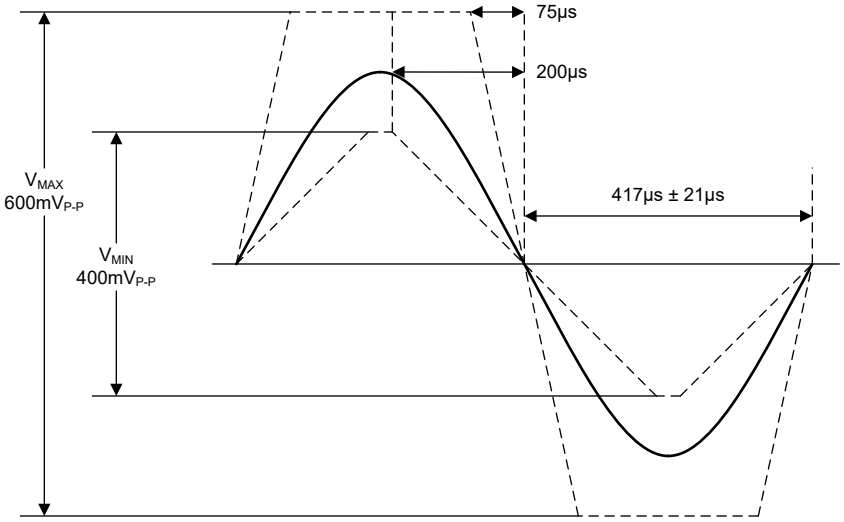

Figure 3-3. HART 1200Hz FSK Waveform Limits

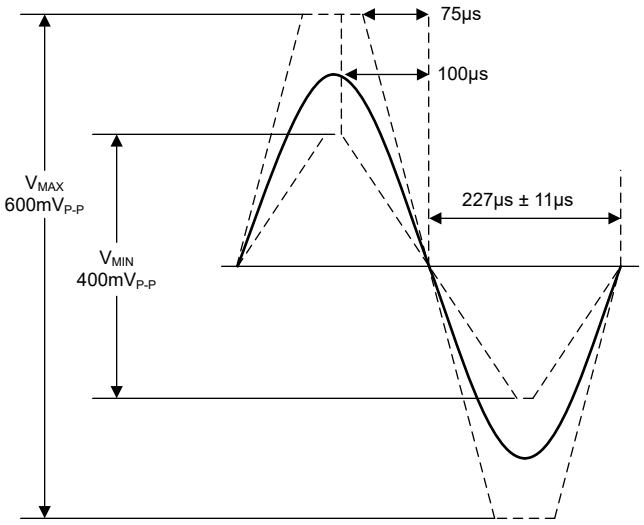

Figure 3-4. HART 2200Hz FSK Waveform Limits

These measurements define the FSK frequency variation allowed, the minimum and maximum voltages, and the rise times needed for the HART signal. In addition to the waveform requirements the two FSK frequencies, there is a transition requirement for the waveform shown in Figure 3-5.

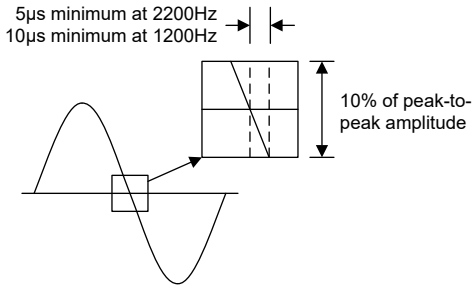

Figure 3-5. HART Sinusoidal Signaling Transition

These diagrams show the tolerance for amplitude of the HART signal, the frequency variation, and the rise time of the signals. To pass the tests, the HART sinusoid must fit within these trapezoidal windows shown in the figures.

The waveforms are taken from the AFE881H1 transmitter test setup using an oscilloscope. Figure 3-6 shows the oscilloscope photos taken for the two HART FSK sinusoids and Table 3-1 shows the test data taken from the measurements.

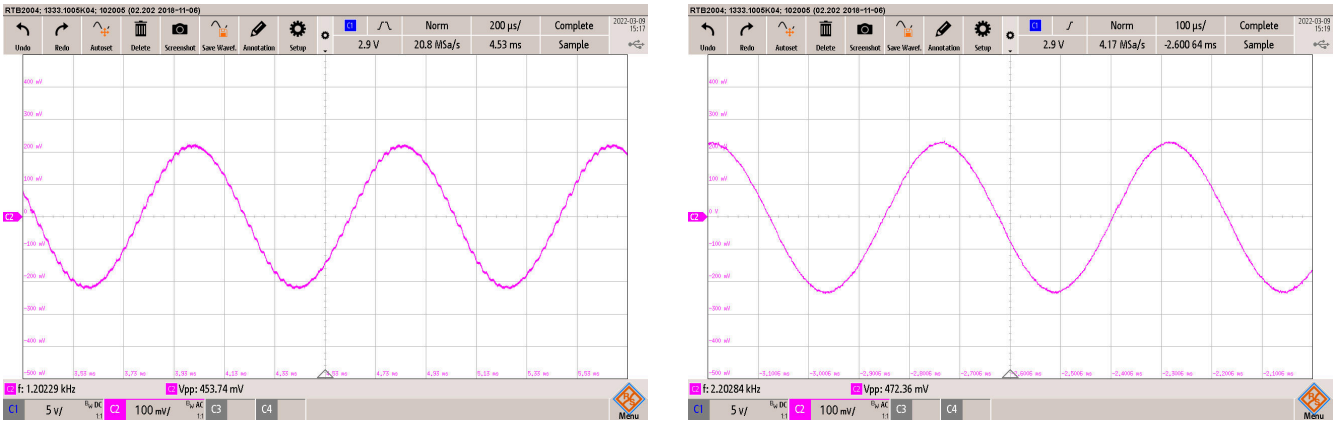

Figure 3-6. FSK Sinusoid Test Oscilloscope Results

Table 3-1. FSK Sinusoid Waveform Test Data

FSK FREQUENCY	TEST	MEASURED	MINIMUM	MAXIMUM	RESULT
1200Hz	Frequency	1202Hz	1188Hz	1212Hz	Pass
	Amplitude	454mV$_{PP}$	400mV$_{PP}$	600mV$_{PP}$	Pass
	Waveform rise time	130µs	80µs	200µs	Pass
	Waveform fall time	130µs	80µs	200µs	Pass
2200Hz	Frequency	1202Hz	1188Hz	1212Hz	Pass
	Amplitude	472mV$_{PP}$	400mV$_{PP}$	600mV$_{PP}$	Pass
	Waveform rise time	80µs	75µs	200µs	Pass
	Waveform fall time	80µs	75µs	200µs	Pass

While a 250Ω resistor is commonly used in 4-20mA loops, a 500Ω current sense resistor is required for this and the other physical layer tests.

3.4.2 Carrier Start and Stop Time Tests

In addition to the FSK characteristics, the physical layer tests also measure the start and start times of the carrier from the transmitter. Figure 3-7 shows a figure of the carrier start and stop time test setup. When the microprocessor in the HART transmitter sends a transmission, the request-to-send ($\overline{RTS}$) pin on the AFE881H1 is set low as a trigger to enable the modulator for the FSK. The modulator generates the sine-wave signals for the HART communication.

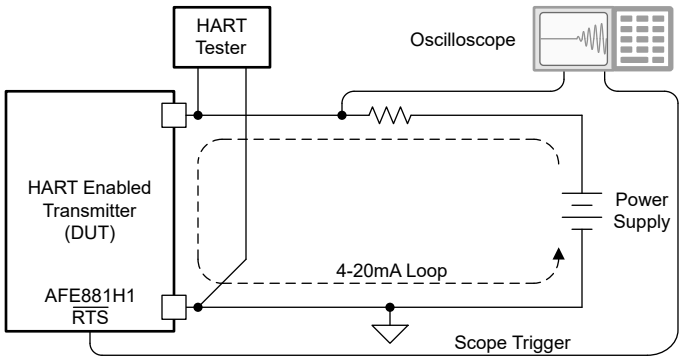

Figure 3-7. HART Carrier Start and Stop Time Tests Setup

When the active-low $\overline{RTS}$ pin on the AFE881H1 is set low, the modulator is enabled and the HART sinusoid appears on the MOD_OUT pin of the device. Part of the physical layer tests measure the time to enable the modulator when the $\overline{RTS}$ signal is set low, and the time to disable the modulator when the $\overline{RTS}$ signal is returned high.

In this setup, the $\overline{RTS}$ signal from the microprocessor triggers an oscilloscope to plot the enable and disable time for the HART signal. Figure 3-8 and Figure 3-9 show the required timing for the HART carrier start and stop tests.

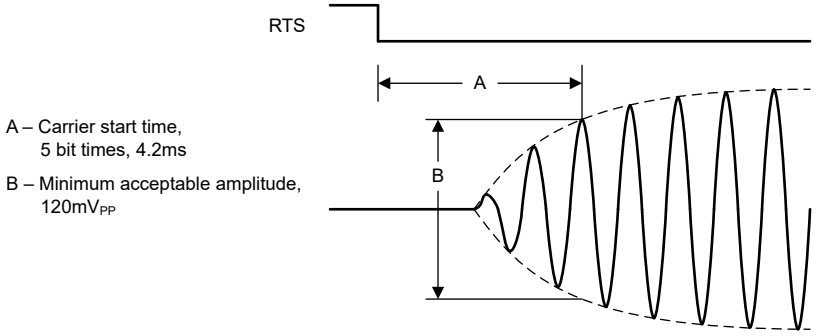

Figure 3-8. Carrier Start Timing

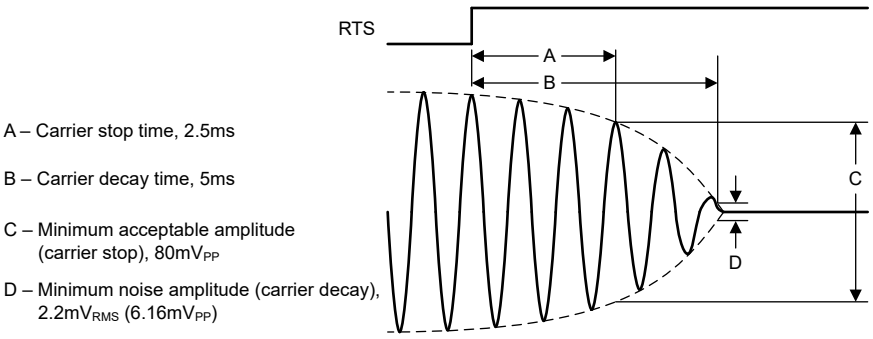

Figure 3-9. Carrier Stop Timing

For $\overline{RTS}$ enable, the maximum amount of time allowed to start the modulator is 5 HART bit times or 4.2ms. This is the time for the sinusoid to reach the minimum amplitude of $120mV_{PP}$. For $\overline{RTS}$ disable, the maximum carrier stop time is 2.5ms to verify that the carrier amplitude is below $80mV_{PP}$. There is a total of 5ms of allowable decay time. After this time period, the maximum noise amplitude from the HART signal is $2.2mV_{RMS}$ (or about $6.16mV_{PP}$). Figure 3-10 shows the oscilloscope plot for the HART carrier start and stop timing and Table 3-2 reports the measured data.

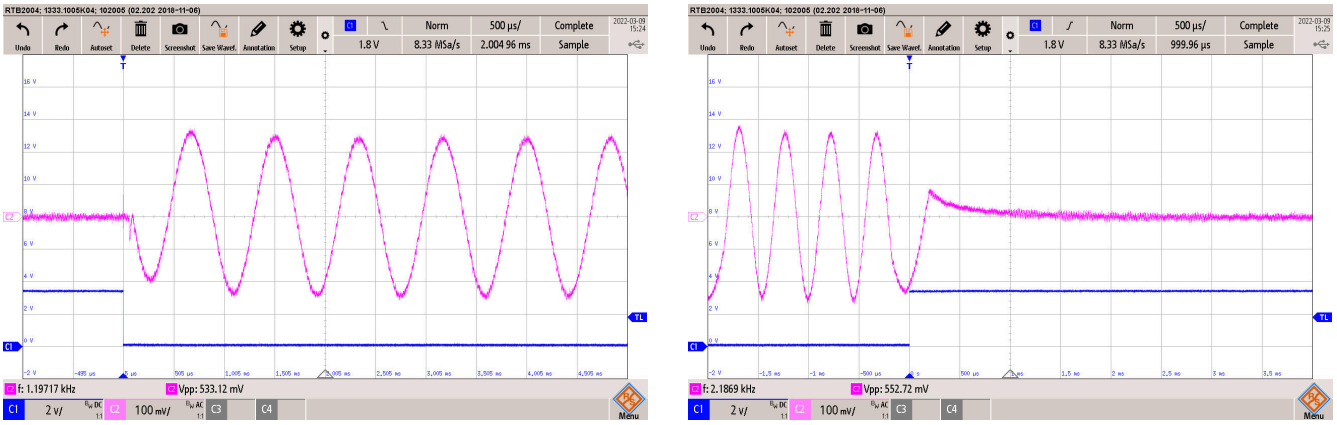

Figure 3-10. HART Carrier Start and Stop Time Test Oscilloscope Results

Table 3-2. FSK Sinusoid Start and Stop Time Test Results

TEST	MEASURED	MAXIMUM	RESULT
Carrier start time	120µs	4.2ms	Pass
Carrier stop time	0.4ms	2.5ms	Pass
Carrier decay time	1.8ms	5.0ms	Pass

3.4.3 Carrier Start and Stop Transient Tests

The next test is the carrier start and stop transient measurements. The test setup in Figure 3-11 is similar to the previous test where the carrier start and stop are measured. In this test setup, an HCF_TOOL-32 filter is measured by another channel of the oscilloscope. This low-pass filter removes the higher-frequency HART signal band and passes any signal below 25Hz. The filtered signal shows the current measurement of the primary variable. This test verifies that the HART transmission start and stop does not create any noise that interferes with the primary variable measurement.

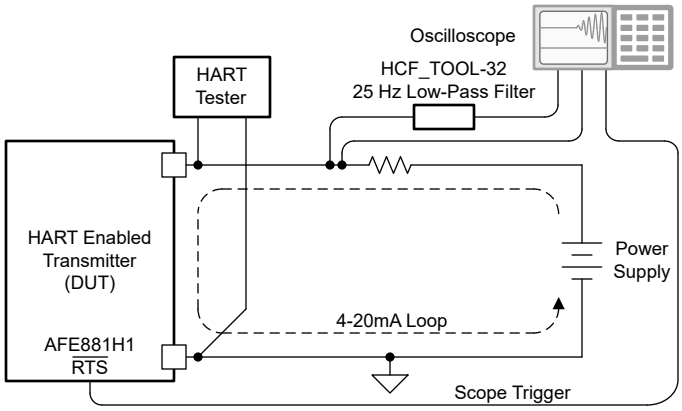

Figure 3-11. HART Carrier Start and Stop Time Test Setup

Figure 3-11 shows the oscilloscope plots of the HART signal while being enabled and disabled. Additionally, the oscilloscope measures the same signal filtered through the HCF_TOOL-32. The HCF_TOOL-32 is capacitively coupled to the resistive load. The low-pass filtered signal in blue shows the output noise amplitude of the transmitter. Here, the specification requires a peak amplitude of 100mV maximum. The transmitter maximum shows a 22.1mV$_{P-P}$ noise amplitude for the transition noise. Table 3-3 reports the results of the scope measurements.

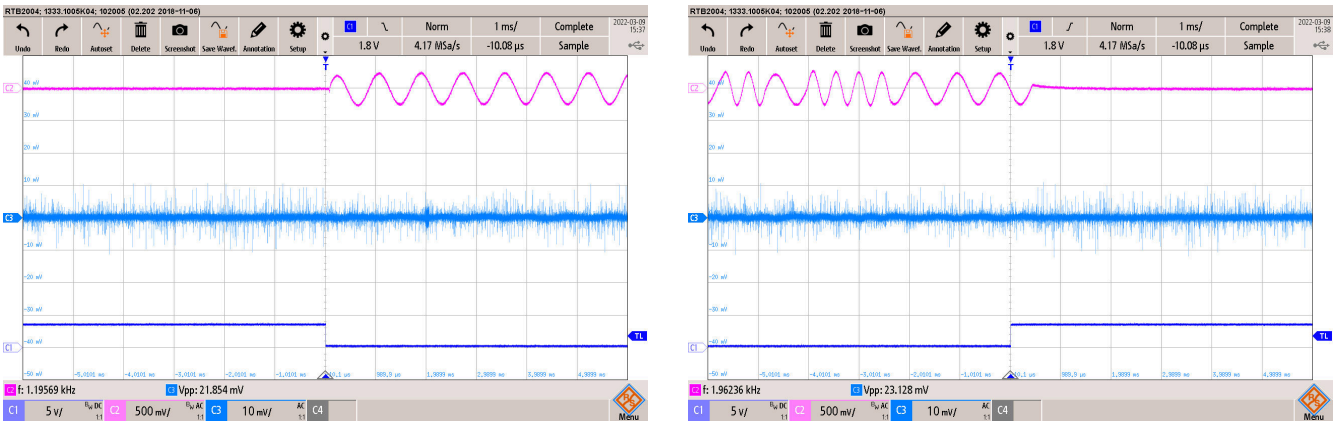

Figure 3-12. HART Carrier Start and Stop Time Transient Test Oscilloscope Results

Table 3-3. Carrier Start and Stop Measurement Results Filtered Through an HCF_TOOL-32

TEST	MEASUREMENT	MAXIMUM	RESULT
Carrier start peak analog filter output	21.8mV$_{PP}$	100mV$_{PP}$	Pass
Carrier stop peak analog filter output	22.1mV$_{PP}$	100mV$_{PP}$	Pass

3.4.4 Output Noise During Silence

Similar to the previous test, this test measures the HART signal band through a filter. Here, the HCF_TOOL-31 filter is used. This filter is a 500Hz to 10kHz bandpass filter that allows all of the in-band HART signal through. The test is devised to view the noise when the HART signal is inactive and verify there is no in-band noise that can be received as a HART signal in error. Figure 3-13 shows the test setup for the output noise during silence.

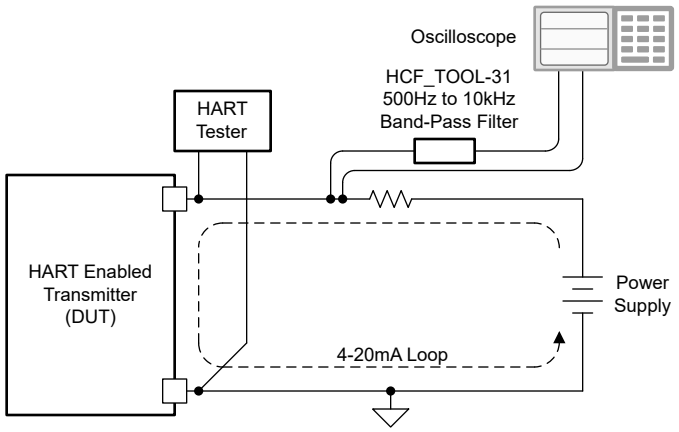

Figure 3-13. HART Output Noise During Silence Test Setup

Figure 3-14 shows the oscilloscope shot of the measurement of the output noise during silence. This shows the inactive HART signal at the top of the oscilloscope plot after the HART has been disabled. The middle trace in the plot shows the same signal filtered through the HCF_TOOL-31, showing the in-band noise for the primary variable. The bottom trace of the oscilloscope plot is the $\overline{RTS}$ which is high indicating the HART is inactive. Table 3-4 shows the results of the noise measured during silence.

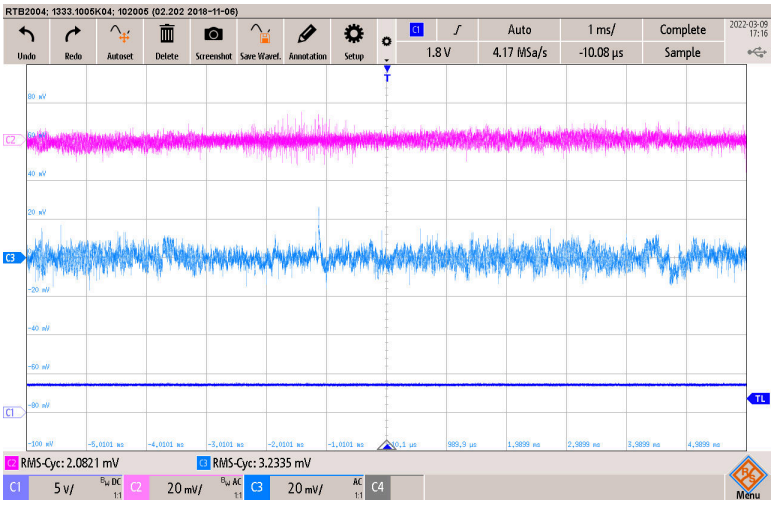

Figure 3-14. Output Noise During Silence Oscilloscope Test

Table 3-4. Output Noise During Silence Test Results

TEST	MEASUREMENT	MAXIMUM	RESULT
Broadband noise without filter	$2.08mV_{RMS}$	$138mV_{RMS}$	Pass
In-band noise using HCF_TOOL-31 bandpass filter	3.23_{RMS}	$22mV_{RMS}$	Pass

3.4.5 Analog Rate of Change Test

The analog rate of change test shows how fast the primary variable can be changed from minimum to maximum value and back again. For this test, a special test mode is encoded in the device to cycle the output from 4mA to 20mA at a rate of about 18Hz. This test mode is enabled through switches on the transmitter board. In the transmitter, the AFE881H1 is set to the sinusoidal slew-rate mode so that the transitions from minimum to maximum approximate a sine-wave shape. The sinusoidal slew-rate mode maximizes the signal in the low-pass primary-variable band.

This signal is then filtered through a HCF_TOOL-31 filter. This filter is a 500Hz to 10kHz bandpass filter that passes all of the in-band HART signal through. The test is devised to show that when the primary variable is changed, the transition does not cause any noise large enough to trigger a HART reception. Figure 3-15 shows the test setup for the analog rate of change test.

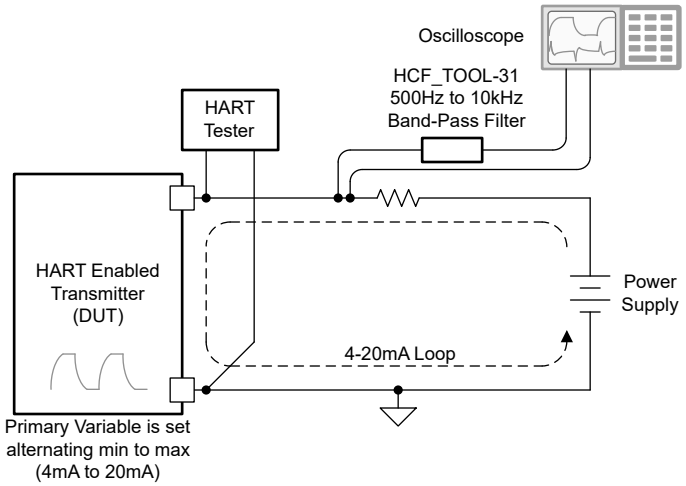

Figure 3-15. HART Analog Rate of Change Test Setup

Figure 3-16 shows a plot of the analog rate of change test. The top trace is the primary variable transitioning back and forth from minimum to maximum. This is a transition of 4mA to 20mA. Across a 500Ω resistor, this is an 8V transition. Table 3-5 reports the resulting measurements of the analog rate of change test.

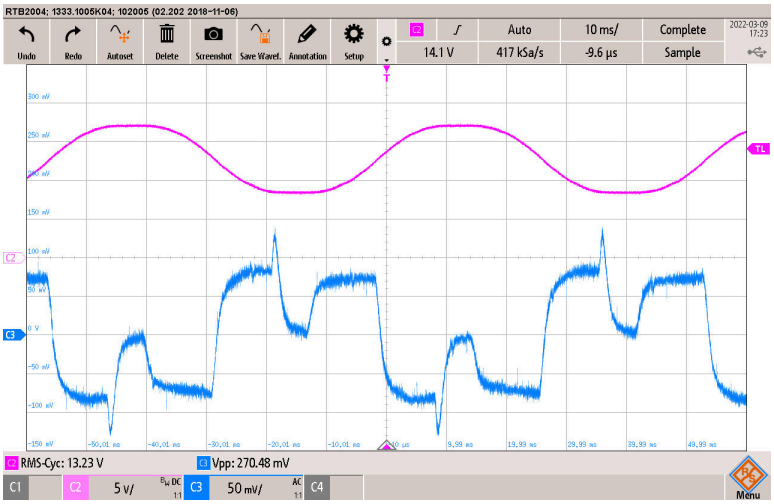

Figure 3-16. Analog Rate of Change Test Oscilloscope Results

The bottom trace shows the same signal filtered through an HCF_TOOL-31. This signal must be less than $150mV_{PEAK}$. For this test, the $270mV_{PP}$ result is the equivalent to $135mV_{PEAK}$, and the device passes this test.

Table 3-5. HART Analog Rate of Change Measurement Results

TEST	MEASUREMENT	MAXIMUM	RESULT
Analog signaling filtered signal amplitude	270mV$_{PP}$	150mV$_{PEAK}$	Pass
Communication errors during analog signaling	100 attempts	0 errors	Pass

During the test, the HART test system was also used to test active transmissions during this periodic output transition. Using the HART test system, the *comtest* command sends a set of consecutive commands. While the device is cycling through the minimum and maximum values, the HART test system sends 100 commands and the transmitter responds to these commands to verify there are no errors in transmission.

3.4.6 Receive Impedance Test

Another physical layer test is to measure the receive impedance of the transmitter. The AFE881H1 is built into a high-impedance transmitter and the receive impedance must be above a minimum level over both the primary variable and HART transmission frequencies. In this test, a 5kΩ series test resistance is used in the loop to measure the receive impedance of the transmitter. This test requires a significantly higher power supply voltage. The normal starting current of the transmitter is 4mA. This amount of current across 5kΩ is 20V and a supply of over 40V is required to operate this test. Figure 3-17 shows a block diagram of the test setup for measuring the receive impedance of the transmitter.

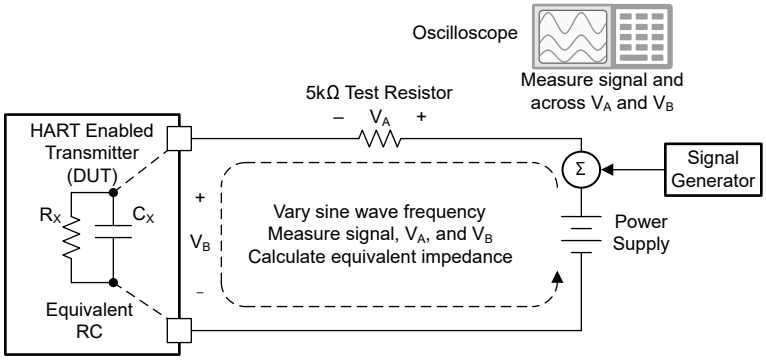

Figure 3-17. HART Receive Impedance Test Setup

A signal generator inputs a sine wave of different frequencies into the loop. The oscilloscope measures the voltage from the signal generator, the voltage across the test resistor, and the voltage dropped across the transmitter. From these three measured values on the oscilloscope, and using the known 5kΩ resistance of the test resistor, the equivalent impedance of the transmitter is calculated. Over frequency, an equivalent resistance and capacitance (Rx and Cx) can be calculated and plotted.

Table 3-6 tabulates the measured values for V_A and V_B and the calculated equivalent impedance for Z_M looking into the transmitter.

Table 3-6. Measured and Calculated Results from the Receive Impedance Test

FREQUENCY	V_A (V)	V_B (V)	Z_M (Ω, calculated)
200Hz	0.018	1	277778
500Hz	0.025	1	200000
950Hz	0.05	0.99	99000
1.6kHz	0.09	0.98	54444
2.5kHz	0.13	0.96	36923
5kHz	0.26	0.95	18289
10kHz	0.48	0.87	9063
20kHz	0.73	0.65	4452
50kHz	0.93	0.33	1774

The impedance is then plotted versus frequency in Figure 3-18.

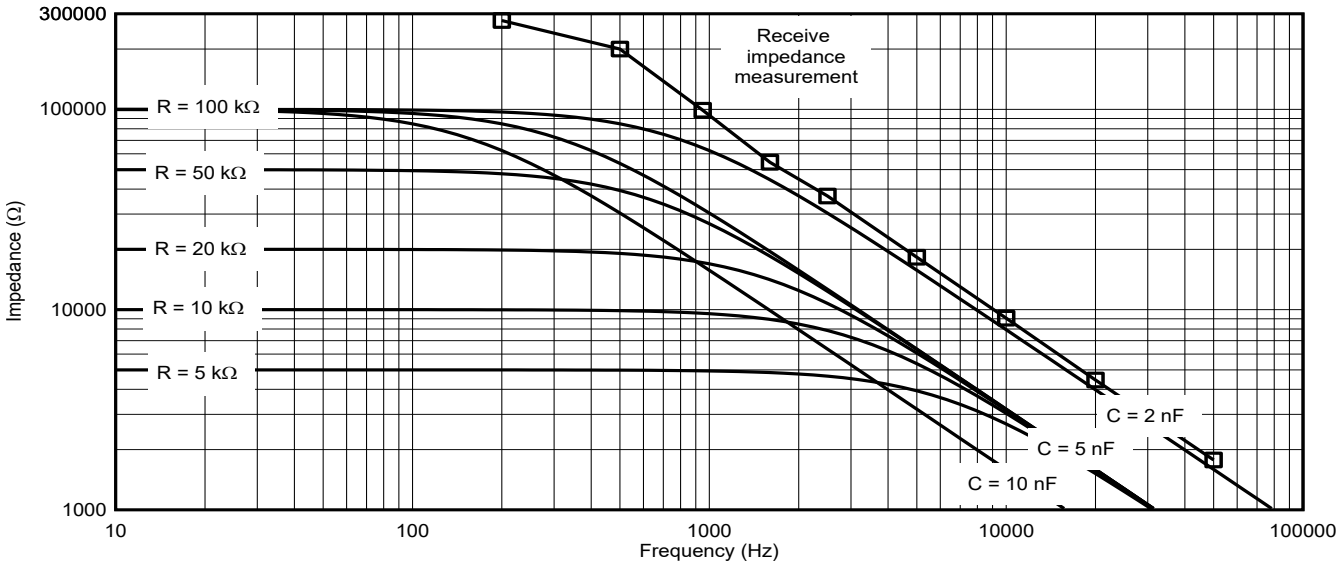

Figure 3-18. Receive Impedance Test Results Plotted Over Frequency

For this test, signals in a frequency range from 200Hz to 50kHz are measured and calculated. The equivalent resistance and capacitance for the transmitter receive impedance are 278kΩ and 1800pF. For high-impedance transmitters, the minimum equivalent resistance is 100kΩ and the maximum capacitance is 5nF.

3.4.7 Noise Sensitivity Test

The transmitter is also tested for the HART transmission in the presence of noise at different frequencies. For this test, a signal generator varies the supply voltage at different magnitudes and frequencies to simulate noise.

The noise sensitivity test verifies that the HART signal is received despite having out-of-band noise, and even some low-signal in-band noise. Figure 3-19 shows the test setup for the HART noise sensitivity test.

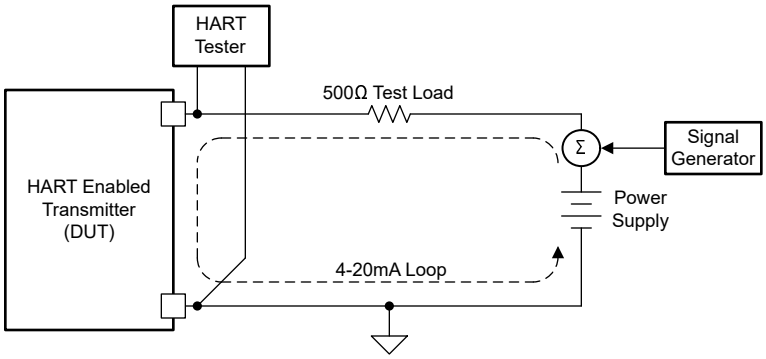

Figure 3-19. Noise Sensitivity Test

The signal generator is set to frequencies and amplitudes to mimic noise during a HART transmission. There are five frequency and amplitude combinations used for this test. Table 3-7 lists the different frequency and amplitude combinations used for the signal generator to simulate the noise.

Table 3-7. Measured Data from the Noise Sensitivity Test

TYPE OF INTERFERENCE	FREQUENCY	LEVEL	NUMBER OF MISSED COMMAND ERRORS	RESULT
In band	1700Hz	55mV$_{PP}$	0	Pass
Out of band	250Hz	220mV$_{PP}$	0	Pass
Out of band	125Hz	880mV$_{PP}$	0	Pass
Out of band	63Hz	3.52V$_{PP}$	0	Pass
Out of band	29Hz	16V$_{PP}$	0	Pass

While the signal generator is active, the HART test system sends 100 consecutive commands to the transmitter. The transmitter sends a response to the commands. Any missed command or interrupted transmission is considered an error.

3.4.8 Carrier Detect Test

The last of the physical layer tests are the carrier detect tests. During these tests, the modem is replaced with the HCF_TOOL-35 physical layer test interface. This tool is a HART modem interface with an adjustable output that can vary the amplitude of the tester HART signals. Figure 3-20 shows the HART carrier detect test setup.

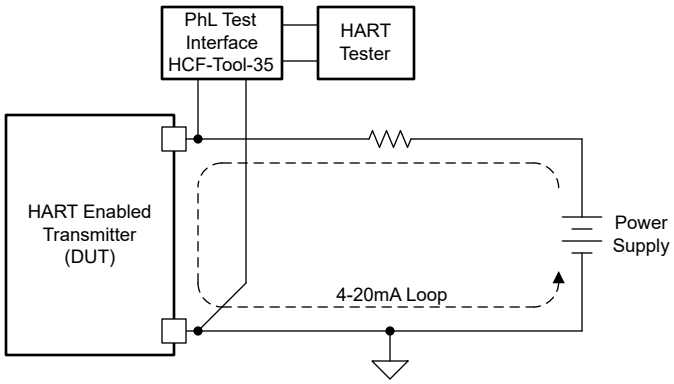

Figure 3-20. HART Carrier Detect Test Setup

The carrier detect tests verify what minimum amplitude of transmission is needed to identify the signal as a HART signal. The test also identifies the maximum in-band signal that is not identified as a HART signal. An oscilloscope is used to verify the amplitude of the signal. The test also verifies the time required for a start and stop with a HART minimum amplitude transmission.

For the carrier detect tests, the signal level is dropped from the typical 500mV_{PP} level to 120mV_{PP}. The HART modem communication must still be received by the transmitter. After completion, the signal level is dropped even further to 80mV_{PP}, where the transmitter must reject any commands. Finally, the signal level is raised back to 120mV_{PP}. The device must again receive HART communication from the test system. Each of these tests are performed while sending 100 HART commands to the transmitter.

After these tests are completed the start and stop time are re-tested with the 120mV_{PP} signal to verify transmission. Table 3-8 reports the results for the Carrier Detect tests

Table 3-8. Carrier Detect Test Results

TEST	SIGNALING AMPLITUDE	MEASUREMENT	MAXIMUM	RESULT
Successful error-free communications	120mV_{PP}	100 communication attempts	0 errors	Pass
Unsuccessful Communications	80mV_{PP}	100 communication attempts	0 successful communications	Pass
Successful error-free communications (return)	120mV_{PP}	100 communication attempts	0 errors	Pass

This test uses a 250Ω current sense resistor. Carrier start and stop times must be less than 5ms (less than 6 bit times).

3.5 Data Link Layer Tests

After the physical layer tests, the data link layer (DLL) tests verify the syntax of the commands and the structure of the HART communication frames. These tests check the construction of the frame including the preamble, delimiter, addressing, and byte counts. Tests also check the transmitter frame generation, constructing the response data into the proper format to be understood by a controller. DLL tests also verify different cases for bus arbitration, with specific time responses from the transmitter in request-response and in burst modes.

3.5.1 Data Link Layer Test Specifications

HCF_SPEC-081 defines the token-passing data link layer specification. The DLL is responsible for the reliable, error free communication of data between HART compatible devices. This document specifies the rules used by HART products to communicate digital information over a physical link.

To test the DLL, the test specifications are outlined by HCF_TEST-1. These tests cover:

- HART communication frame detection and recognition by the transmitter
- Frame generation from the transmitter for reception by the controller
- Bus arbitration to check that the transmitter responds promptly after receiving a command, and sending commands in burst mode
- Data link layer services that control bytes sent in the data frame for the application layer

The Linux-based HART test system has a set of pre-programmed tests to verify the data link layer. For all DLL tests, the HART test system runs the test and records a log of the test and results. In the HART test system, the *hartmenu* command gives a list of different tests available. These tests can be run consecutively, where the tests are run one after another until user intervention is required. Alternately, tests can be run individually, where the user can select a specific test.

Table 3-9 shows a list of data link layer tests.

Table 3-9. DLL Test List and Results

TEST NUMBER	DESCRIPTION	RESULT
DLL001	FSK preamble check	Pass
DLL002	Delimiter check	Pass
DLL003	Frame expansion check	Pass
DLL004	Short frame check	Pass
DLL005	HART controller address bit check	Pass
DLL006	Burst mode bit check	Pass
DLL007	Long frame address check	Pass
DLL009	Incorrect byte count check	Pass
DLL010	Vertical parity check	Pass
DLL011	Framing error check	Pass
DLL012	Check byte test	Pass
DLL013	FSK gap receive timeout test	Pass
DLL014	Long message test	Pass
DLL015	Start of message in data field check	Pass
DLL016	Preamble check for BACK frames	Pass
DLL017	Preamble check for ACK frames	Pass
DLL018	Gap errors in ACK frames check	Pass
DLL019	Gap check for BACK frames	Pass
DLL020	Dribble byte check for ACK frames	Pass
DLL021	Dribble byte check for BACK frames	Pass
DLL022	Test host address bit for BACK frames	Pass
DLL023	Test burst mode bit of burst-mode transmitter device frames	Pass
DLL024	Test transmitter device responds within STO	Pass
DLL025	Burst hold during HART controller preamble	Pass
DLL026	Test burst response time after a DUT ACK	Pass
DLL027	Test response time between consecutive bursts	Pass
DLL028	BACK timing with STXs errors	Pass
DLL029	Burst mode timeout on other transmitter device	Pass
DLL030	Burst after response from other transmitter device	Pass
DLL032	Read unique identifier	Pass
DLL033	Write polling address	Pass
DLL034	Read unique identifier with tag (Command 11)	Pass
DLL035	Write number of response preambles	Pass
DLL038	Read unique identifier with tag (Command 21)	Pass
DLL039	Transmitter device time-out stress test	Pass
DLL040	Unique address test	Pass
DLL041	Framing successive messages	Pass
DLL042	Command number expansion	Pass

The DLL tests with the exception of DLL039 take about 13 hours to complete. Near the end of the run, there are a few tests that require user intervention to cycle power on the devices.

DLL039 is the final DLL test to be run. In this time-out stress test, the tester sends 2 million consecutive commands and records the log with any errors in the response from the device. Because HART communication responds at about 1 command per second, this test takes about 19 days to complete. An uninterrupted power supply is highly recommended when running this test.

3.5.2 Data Link Layer Test Logs

When the data link layer tests are run, the HART test system opens up a HART sniffer window to view the commands and responses from the tester to the transmitter device. Figure 3-21 shows this HART utility window and gives a active reading of the HART communication as the signal occurs. The “Msg sent from queue 1” indicates that there is a preamble sent as a communication to the device. The preamble is followed by a delimiter, address, command, and error correction bytes from the HART test system.

Figure 3-21. HART Sniffer Display From the HART Tester

While each of the data link layer tests are run, the HART test system generates a log that is used to show the communication and can be reviewed by FieldComm Group. Figure 3-22 shows a small segment of one of these logs.

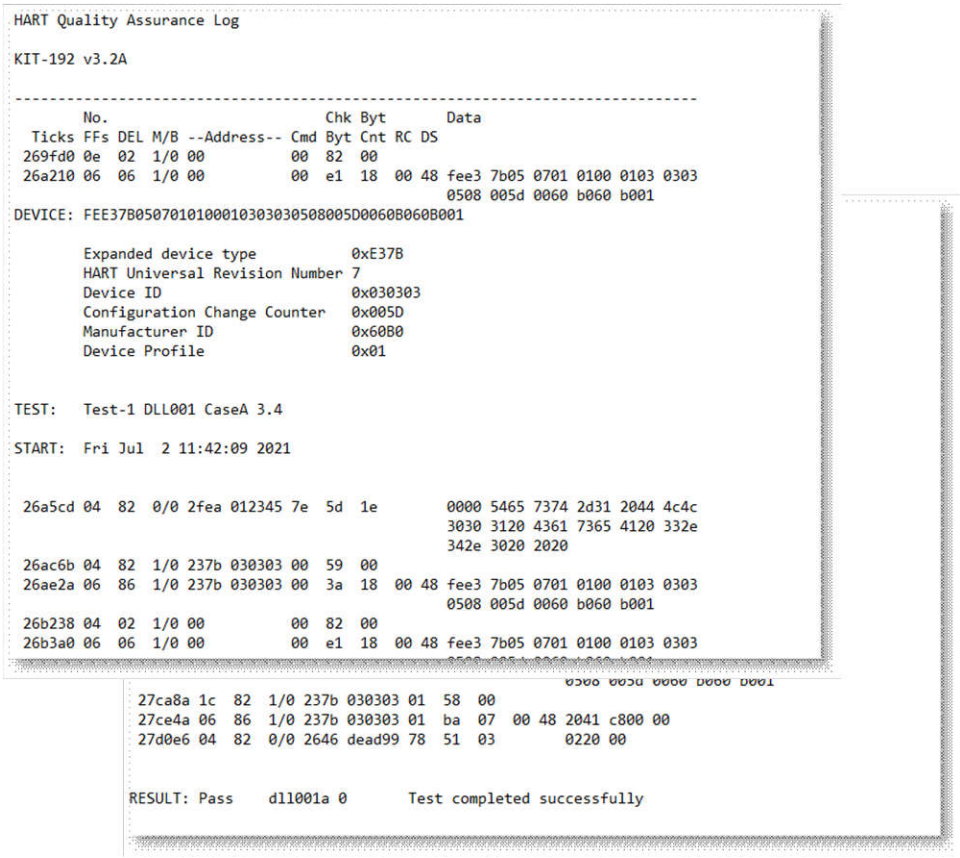

Figure 3-22. DLL Test System Logs

These test logs record which test is run, device information, the communication transaction with a time stamp, verifies the communication, and flags any failures. After all tests are complete, the HART test system generates a full set log files. These log files are zipped together and sent to FieldComm with the device registration request.

3.6 Universal Command Tests

The HART test system also runs the universal command tests of the application layer (UAL) starting from the *hartmenu* application. The universal command specification is defined under HCF_SPEC-127. These tests verify the application layer of the protocol and check the universal HART commands supported by the transmitter. The UAL test specification is defined by HCF_TEST_3. The test setup is the same as the DLL test setup, and also uses the HART test system to send commands to the transmitter. These tests verify the following functions of the applications layer:

- Verify Support for All Universal Commands. These tests scan for the range of universal commands from 0 to 31 and look for a proper response.
- Read Dynamic Variables. These tests check the responses to commands 1, 2, 3, and 9 for dynamic variable.
- Verify Write Commands. The write tests check initial values, and subsequent write values. This tests the results of different data fields.
- Verify Configuration Read Commands.
- Confirm Write Protect. This is a test of the write protect into the transmitter (if this function is supported).
- Test Cold Start Bit. The controller must be able to detect a cold start (i.e. a power failure).
- Read Device Variables. This test verifies the proper operation of command 9.
- Test the Configuration Changed Bit. This test verifies support for and proper operation of command 38 and checks a configuration changed counter to reset the status bit.
- Support for Command 48, Read Additional Device Status. This test verifies support for command 48 and checks the ability to reset the More Status Available bit.

The end of the tests available require some user intervention for setting the cold start bit and checking the more status available bit.

Table 3-10 lists the tests run by the HART test system to verify support for universal commands and the results of the test.

Table 3-10. UAL Command Test List and Results

TEST NUMBER	DESCRIPTION	RESULT
UAL000	Confirm all universal commands are supported	Pass
UAL001	Read dynamic variables (commands 1, 2, and 3)	Pass
UAL005	Write message	Pass
UAL006	Write tag descriptor and date	Pass
UAL007	Verify command 14 and 15 response	Pass
UAL008	Verify final assembly number	Pass
UAL009	Verify write protect	Not applicable
UAL010	Verify cold start bit	Pass
UAL011	Read device variables (command 9)	Pass
UAL012	Read dynamic variable classification	Pass
UAL013	Write long tag	Pass
UAL038	Reset configuration changed flag	Pass
UAL048	Read additional device status	Pass

The HART stack programmed into the transmitter passes these tests, except that the write protect was not programmed into the functionality. For this verify write protect test (UAL009), the test is checked as *Not applicable*. The complete set of UAL tests take about 30 minutes to complete. As with the DLL tests, running the UAL tests enables a HART sniffer window and generates a set of test logs for these tests for the application submission.

3.7 Common-Practice Command Tests

The last of the HART tests verify that common-practice commands of the application layer (CAL) are implemented in the transmitter. The CAL test specification is described by HCF_TEST_4. These tests check for highly-recommended commands that are implemented in many HART devices. Here is a basic list of common-practice commands that can be implemented in HART devices and tested as part of the CAL tests:

- Read selection of up to four dynamic variables
- Write damping time constant
- Write device range values
- Calibrate (set zero, set span)
- Set fixed output current
- Perform self-test
- Perform host reset
- Trim primary variable zero
- Write primary variable unit
- Trim DAC zero and gain
- Write transfer function (square root/linear)
- Write sensor serial number
- Read or write dynamic variable assignments

Table 3-11 shows the set of common-practice command tests run by the HART tester. While the transmitter designed in this application note uses a HART stack that shows functionality of the device, this design is not a full-functioned device used as a real transmitter in an application. Many commands have been implemented, but not all are supported from this list of tests. This complete set of CAL tests take about 4 hours to complete.

Table 3-11. CAL Command Test Results

TEST NUMBER	DESCRIPTION	RESULT
CAL000	Checks for common practice commands	Pass
CAL001	Write protect test	Not implemented
CAL033	Read device variables	Pass
CAL034	Write primary variable damping value	Pass
CAL035	Write primary variable range values	Pass
	Primary variable units code unaffected by command 35	Pass
CAL036	Set primary variable upper range value	Not applicable
CAL037	Set primary variable lower range value	Not applicable
CAL040	Enter/exit fixed current mode	Pass
CAL041	Perform self test	Pass
CAL042	Perform device reset	Pass
CAL043	Set primary variable zero	Not applicable
CAL044	Write primary variable units	Pass
CAL045	Trim loop current zero	Pass
CAL046	Trim loop current gain	Pass
CAL047	Write primary variable transfer function	Not applicable
CAL049	Write primary variable transducer serial number	Not applicable
CAL050	Read dynamic variable assignments	Not applicable
CAL051	Write dynamic variable assignments	Not applicable
CAL052	Set device variable zero	Not applicable
CAL053	Write device variable units	Not applicable
CAL054	Read device variable information	Pass
CAL055	Write device variable damping value	Not applicable
CAL056	Write device variable transducer serial number	Not applicable
CAL060	Read analog channel and percent of range	Not applicable
CAL062	Read analog channels	Not applicable

Table 3-11. CAL Command Test Results (continued)

TEST NUMBER	DESCRIPTION	RESULT
CAL063	Read analog channel information	Not applicable
CAL064	Write analog channel additional damping value	Not applicable
CAL065	Write analog channel range values	Not applicable
CAL066	Enter/exit fixed analog channel mode	Not applicable
CAL067	Trim analog channel zero	Not applicable
CAL068	Trim analog channel gain	Not applicable
CAL069	Write analog channel transfer function	Not applicable
CAL070	Read analog channel endpoint values	Not applicable
CAL071	Lock device	Not applicable
CAL072	Squawk	Pass
CAL073	Find device	Not applicable
CAL074	Verify I/O system commands	Not applicable
CAL078	Command aggregation	Not applicable
CAL079	Write device variable	Not applicable
CAL080	Verify device variable trim commands	Not applicable
CAL091	Trending	Not applicable
CAL101	Subsystem burst mode	Not applicable
CAL103	Support for multiple burst messages	Pass
CAL104	Smart data publishing	Pass
CAL107	Write burst device variables	Pass
CAL108	Write burst mode command number	Pass
CAL109	Burst mode control	Pass
CAL115	Event notification	Not applicable
CAL512	Country code	Not applicable
CAL518	Location description	Not applicable
CAL520	Process unit tag	Not applicable
CAL523	Read condensed status mapping array	Not applicable
CAL524	Manipulating condensed status map	Not applicable
CAL526	Status simulation	Not applicable

As with the DLL and UAL tests, running the CAL tests from *hartmenu* generates a set of logs for the registration submission.

3.8 Device Specific Command Tests

In addition to the universal commands and the common-practice commands, manufacturers can implement device specific commands into devices. The following list shows some device specific commands that can be implemented.

- Read or write low-flow cut-off
- Start, stop, or clear totalizer
- Read or write density calibration factor
- Choose PV (mass, flow, or density)
- Read or write materials or construction information
- Trim sensor calibration
- PID enable
- Write PID set point
- Valve characterization
- Valve set point
- Travel limits
- User units
- Local display information

Again, these commands can be implemented by device manufacturers but are not required. Device specific commands are not tested through the HART specification and are not implemented as tests in the HART test system.

3.9 HART Protocol Test Submission

After all the physical layer tests and DLL, UAL, and CAL tests are completed, the device is ready to submit for registration. Fieldcomm HART registration applications require the following documentation:

- Complete a HART Field Device Test Report
- Compose a test document describing the setup and test procedure for the device
- Complete marketing forms for FieldComm on how this device is to be used and marketed
- Physical layer test results are compiled in the Field Device Test Report
- Results from DLL, UAL, and CAL tests are zipped up from the test logs and submitted

3.10 HART Registration

After the submission, FieldComm reviews the test results and log files. After reviewing the submission and checking the results, FieldComm requests a couple of transmitters to verify testing.

Testing and registration requires about six weeks to complete as long as there are no problems discovered in the tests. Any problems discovered in the tests require a re-submission of the device. If the design has been reviewed to satisfaction, FieldComm informs you that the device has been registered.

After completion, FieldComm sends a letter recognizing that the design is now HART registered. The response is accompanied by a certificate of registration for the design and the HART registered logo can be used on the data sheet. Figure 3-23 shows the certificate of registration for the AFE881H1 transmitter device.

HART® REGISTERED

Certificate of Registration
FieldComm Group Verified

Texas Instruments Manufacturer	AFE881H1-TI-Design (TIDA-060036) Product Name
60B0 Manufacturer ID (Hex)	E54B Expanded Device Type (Hex)
7 HART Protocol Revision	01 Device Revision (Hex)
00 Hardware Revision (Hex)	01 Software Revision (Hex)
03/18/2022 Test Date	FieldComm Group Verification Method

The above product has successfully completed the validation process and meets the requirements to be "HART REGISTERED".

"HART REGISTERED" products conform to GB/T 29910.1-6-2013 and IEC 61158 standards.

Registration Number: L2-06-1000-987.3 Registration Issue Date: May 31, 2022 Approval:

FIELDCOMM GROUP™
Connecting the World of Process Automation

HART® is a registered trademark of FieldComm Group

Figure 3-23. HART Registration for an AFE881H1-Based Transmitter Design

4 Other TI HART Modem Designs

There are a few TI designs that have been created to demonstrate HART communications. First, the DAC8740H device was the first of TI's HART modem devices used in factory automation and control. The DAC8740H is one device of a family of HART modems detailed in Table 4-1.

Table 4-1. DAC874xH HART Modem Devices

DEVICE	Communication
DAC8740H	UART
DAC8741H	SPI
DAC8742H	UART/SPI

The DAC8740H has two associated designs that have HART implementations. First is the *Highly-Accurate, Loop-Powered, 4mA to 20mA Field Transmitter With HART Modem Reference Design*. This design was registered with FieldComm as a HART device. Figure 4-1 shows the board that was used for the TI design.

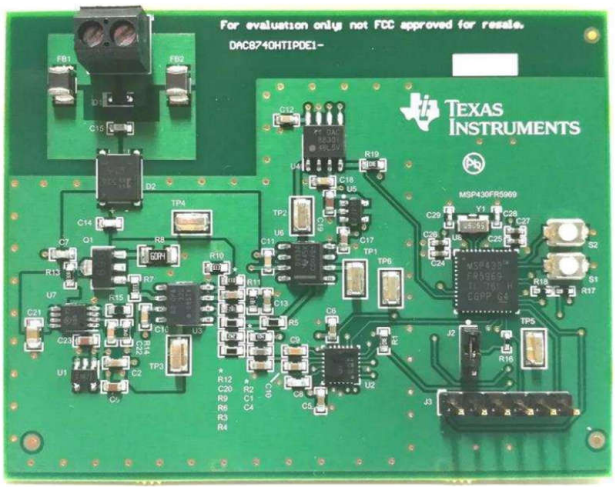

Figure 4-1. Board used for Highly-Accurate, Loop-Powered, 4mA to 20mA Field Transmitter With HART Modem Reference Design

The second design is *HART-Enabled PLC Analog Input Module Reference Design*. This design was not registered with FieldComm, but the design guide does have measurements and test procedures to show that the design passes the various HART tests.

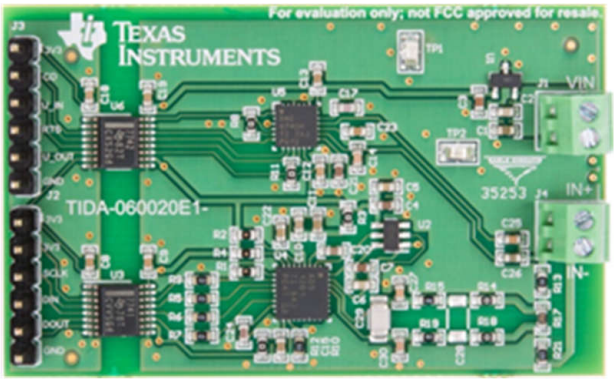

Figure 4-2. Board used for HART-Enabled PLC Analog Input Module Reference Design

As shown previously in the transmitter design, the AFE881H1 is a HART modem with an integrated DAC. The AFE881H1 is part of a family of HART modem devices detailed in Table 4-2.

Table 4-2. AFE881H1 Family of HART Modem Devices

DEVICE	DAC RESOLUTION	DAC OUTPUT RANGE
AFE881H1	16-Bit	0.3V to 2.5V
AFE781H1	14-Bit	0.3V to 2.5V
AFE882H1	16-Bit	0V to 2.5V
AFE782H1	14-Bit	0V to 2.5V

Evaluation modules (EVMs) are available for the AFE881H1 and the AFE882H1. For the AFE881H1EVM, the board outputs the DAC voltage for evaluation. For the AFE882H1EVM which is a similar device but with a DAC output of 0V to 2.5V), the EVM uses an XTR305 to create a voltage or current output.

A front-end board EVM incorporating a V-to-I conversion stage can be released. These front-end boards operate as transmitter on a 4-20mA loop when a supply voltage is applied. Figure 4-3 shows an AFE881H1 modular front-end board.

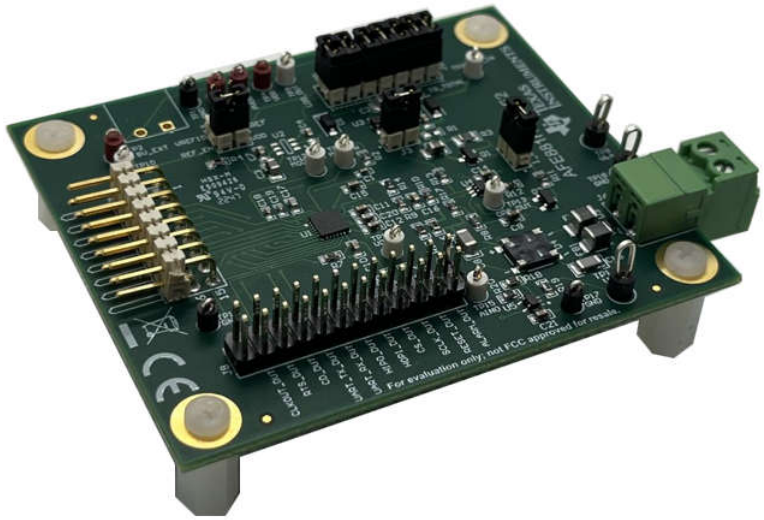

Figure 4-3. AFE881H1 modular front-end board

The connector on the right side of the board connects to the loop power, and a load resistor can be added to either side of the loop connection. The left side of the EVM is connected to a digital back-end board. For GUI control from a PC, the digital back end board has a USB connection. An FTDI device sends SPI or UART signals back and forth from the device to the PC.

Digital back-end boards have also been created with a launchpad connector. TI launchpad kits can be used to write firmware and control the device.

As a test of the front-end/back-end board ecosystem, these boards were used as a vehicle to run HART tests for the AFE882H1. The modular EVM for the AFE882H1 is shown in Figure 4-4.

Figure 4-4. AFE882H1 Front-End Board With Digital Back-end Board and MSP430FR5969 Launchpad as a HART Transmitter

As before, the front-end board is connected to a power supply and acts as the controller for a 4-20mA loop. In this modular setup, an EXP-MSP430FR5969 launchpad board is programmed for the HART stack. The HART stack from the AFE881H1 transmitter design was reused for the AFE882H1. This launchpad is connected to a digital back-end (LP-DBE) interface board and connected to a front-end board which contains the AFE882H1 device. Similar to the AFE881H1 transmitter board, the loop power is supplied by a connector that connects to the right side of the board. HART tests were successfully run on this board, and FieldComm has also completed testing of this board. Using this setup, a AFE882H1 design was registered as a HART transmitter.

5 Summary

This application note describes the use of the AFE881H1 HART modem as the basis of a HART-enabled transmitter design. Details of construction are presented showing the operation, input protection, voltage-to-current conversion, and HART signal transmission. This application note also describes the basics of HART protocol testing and registration. Physical layer tests are first shown, describing different tests for FSK shape, frequency, and in-band and out-of-band noise. The HART test system is used to check the data link layer, universal command, and commonly-implemented commands in the device. For any developer, these tests are run on the HART-enabled device, compiled, and sent to FieldComm for HART device registration.

Finally, other TI HART modem devices and design collateral are presented. The DAC8740H and AFE881H1 are parts in two families of TI HART modem products with EVM boards available to validate these devices.

6 Acknowledgments

TI acknowledges Smart Embedded Systems (SES) in Pleasanton, California for the development of the HART stack used in this design. SES was instrumental in achieving device registration with the FieldComm Group. To reach out to SES, go to SES.

7 References

- Texas Instruments, *AFEx81H1 16-Bit and 14-Bit, Low-Power DACs With Internal HART® Modem, Voltage Reference, and Diagnostic ADC for 4-mA to 20-mA Loop-Powered Applications*, data sheet.
- Texas Instruments, *AFEx82H1 16-Bit and 14-Bit, Low-Power DACs With Internal HART® Modem, Voltage Reference, and Diagnostic ADC for 4-mA to 20-mA Loop-Powered Applications*, data sheet.
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- Texas Instruments, *AFE881H1EVM User's Guide*, user's guide.
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- Texas Instruments, *A Basic Guide to the HART Protocol*, application note.
- Texas Instruments, *Highly-Accurate, Loop-Powered, 4mA to 20mA Field Transmitter With HART Modem Reference Design*, reference design.
- Texas Instruments, *HART-enabled PLC analog input module reference design*, reference design.

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