Application Note

AM68x Processor Power Solutions Using LP87334E PMIC for Industrial Applications

ABSTRACT

This application note describes a low cost, small size, non-safety power design recommended for AM68x processor line as used on *SK-AM68 Processor Starter Kit*. A selection guide that reviews system tradeoffs and design benefits is included. The guide can assist in power design selection and feature set comparisons. Example power and control map diagrams are provided to accelerate the design process.

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Trademarks

1 Introduction

The *AM68x* processor line provides highly flexible, real-time, and low latency processing for a broad range of industrial applications. These processors come in an array of variants with up to two Arm® Cortex® -A72 cores and up to six Arm® Cortex® -R5F cores each. TI has multiple power designs using different power management ICs (PMIC) to support an end product's desired feature set.

The *LP8733x* power design described below provides four Power Distribution Network (PDN) variants to supply AM68x processors according to a system's desired features. A selection guide has been created that outlines PDN features, optional functions, flexibility and design advantages for each PDN-6x variant. The power design highlights the value and flexibility of using a PMIC centric power design.

2 PDN Selection Guide

Selecting a AM68x power design begins with answering a few end product questions:

1. What is the desired market segment (automotive, industrial)?
2. What is the desired operational temperature range?
3. What is the desired MCU processing mode (MCU Island or Extended MCU)?
4. What are the desired optional features?
    a. Low-power modes: MCU Only, DDR Retention, GPIO Retention
    b. Key functions: UHS-1 SD card, USB2.0 signaling, HS SoC eFuse programming

When a system’s desired features are determined, the PDN selection guide enables identification of a recommended power design. All recommended PDN designs provide:

1. Processor peak power demands for full entitlement operation
2. Base power resources to supply all voltages and controls needed for the SoC platform (SoC, LPDDR, Flash, power devices)
3. Flexibility to trade off BOM cost and PCB area vs. optional features

A PDN design that groups MCU and Main supplies into common power rails can reduce a total number of power resources, BOM cost, PDN routing and PCB area. A grouped PDN supports Extended MCU processor operations that combines SoC Main and MCU processing resources. A grouped PDN will not provide a board design with FFI across power rails or MCU Island processing. One example of a grouped MCU and Main power solution is the J721S2 PDN-6x scheme that uses a *LP87334E* PMIC. Table 2-1 shows the PDN-6x base feature set supported by the base power resources and common across all variants. Table 2-2 shows all optional features available across the four PDN-6x (x = G, H, J, K) variants.

A PDN design that isolates MCU and Main supplies into independent power rails is needed to enable MCU Island processing and MCU Only low power mode. Independent MCU and Main power rails provides a board design with Freedom From Interference (FFI) across power rails for more robust systems. An isolated PDN typically requires more power resources that increases BOM cost, PDN routing and PCB area. For comparison, the J721S2 EVM SOM board (*J721S2XSOMG01EVM*) uses a J721S2 Dual *TPS6594-Q1* and *LP8764-Q1* PDN-0A scheme with isolated MCU and Main supplies. This J721S2 PDN-0A also supports up to ASIL-D functional safety capability, automotive qualified devices and a full feature set (base + all optional). A list of all optional features supported by J721S2 PDN-0A follows:

- Three low power modes (MCU Only, DDR Retention, GPIO Retention),
- Three key functions (UHS-I SD card, USB2.0 signaling, HS SoC eFuse programming

Table 2-1. PDN-6x Base Feature Set for Non-Safe, Grouped Design

Base Features	PDN-6x (all variants)
Safety	None
MCU and Main supplies	Grouped
MCU operations	Extended MCU
Power Resource PNs	LP87334E, TPS6287xZ0, TPS62850x
SoC / Pwr Devices T_J ranges [C]	-40 to +105 / -40 to +125
SoC Clk [GHz]	< 2
SDRAM Memory EMIF / Bank Qty: SDRAM Memory Type (size, max rate):	2 EMIFs / Dual Banks LPDDR4 (64 Gb/each, 4266 MTs)
Boot (size) Flash Memory: Storage (size) Flash Memory:	OSPI (512Mb) or HyperFlash (1 Gb and 128 MB) eMMC (16GB)
MCU I/O Signal Levels: Main I/O Signal Levels:	Dual 1.8/3.3 V Dual 1.8/3.3 V

Table 2-2. PDN-6x Optional Features per Variant for Non-Safe, Grouped Design

Optional Features	PDN-6G	PDN-6H *SK-AM68 Processor Starter Kit*	PDN-6J	PDN-6K
Low Power Modes	None	None	None	None
Key Functions	HS SoC Efuse Prgm, UHS-I SD Card, USB2.0 interface	HS SoC Efuse Prgm, UHS-I SD Card	HS SoC Efuse Prgm	None
Power Resource PNs	2x TLV73318P, TPS61240, TLV7103318	TLV73318P, TPS61240, TLV7103318	TLV73318P	
Pwr IC Cost Ratio	1.0	0.99	0.85	0.83
Pwr IC Area Ratio Actual Area [mm^2]	1.0 68.2	0.87 59.0	0.82 55.7	0.68 46.5

3 LP87334E PMIC Settings

The *LP87334E* is an integrated power management IC (PMIC) device optimized for *AM68x* processors. LP87334E simplifies the design process, reduces time to market and enables direct implementation of recommended power solutions. Table 3-1 provides an overview of the basic features.

Table 3-1. LP87334E Basic Features

Features	LP8733x
Operational Ambient Temperature Range	-40 to +125 C
Input Voltage Range	2.8 V to 5.5 V
Total Number of Regulators	4
DC-DC step-down converters	qty = 2, max current = 3 A, output voltage = 0.7 - 3.36 V, remote voltage sense
LDOs	qty = 2, max current = 0.3 A, output voltage = 0.8 - 3.3V
Additional Features	• Programmable sequencer for start-up & shut down delays of power resources & GPO signals • 2 configurable GPO signals for controlling discrete power resources • I2C serial interface control • Interrupt function with programmable masking • Programmable power-good signal (PGOOD) • Output short-circuit and overload protection • Overtemperature warning and protection • Overvoltage protection (OVP) • Undervoltage lockout (UVLO)

Table 3-2 shows the regulator output voltage with both startup and shutdown sequencing delays for LP87334E. For more information on operation and specifications of this device, please see the *LP8733x* data sheet.

Table 3-2. LP87334E Voltage and Sequencing Table

PMIC	LP87334E	
Regulator Settings	**Output Voltage**	**Startup / Shutdown Delay**
Buck0	0.85 V	3 ms / 0.5 ms
Buck1	1.1 V	3 ms / 0.5 ms
LDO0	0.8 V	1 ms / 1 ms
LDO1	1.8 V	0 ms / 3 ms
GPO0	PP ref to VANA (1)	1 ms / 1 ms
GPO2	OD with Rpu(1)	11 ms / 0 ms

(1) GPO and GPO2 control signals have OTP settings that select either Push-Pull (PP) buffer type referenced to PMIC's VANA input supply or Open-Drain buffer type with external pull-up resistor (Rpu) to desired voltage.

4 Example Power Maps

Power resource and control signal mapping diagrams for the four PDN-6G/H/J/K variants with different optional features using the *LP87334E* PMIC to support the *AM68x* platform (SoC, LPDDR4 and Flash memories, power resources) are shown and described below. All PDN-6x variants use the same base power components: LP87334E PMIC, two *TPS6287xZ0* high current buck converters and one *TPS62850x* buck converter. All PDN-6x schemes group MCU and Main supplies into common power rails and do not include safety features.

4.1 AM68x Single LP87334E PDN-6K, Base Features Only

PDN-6K uses only the base power components to provide the lowest cost and smallest PCB area needed for all essential AM68x platform operations without any optional features as shown in Figure 4-1. The PDN-6x base power components include:

- *LP87334E* PMIC
- Two *TPS6287x* high current buck converters
- One *TPS62850x* buck converter

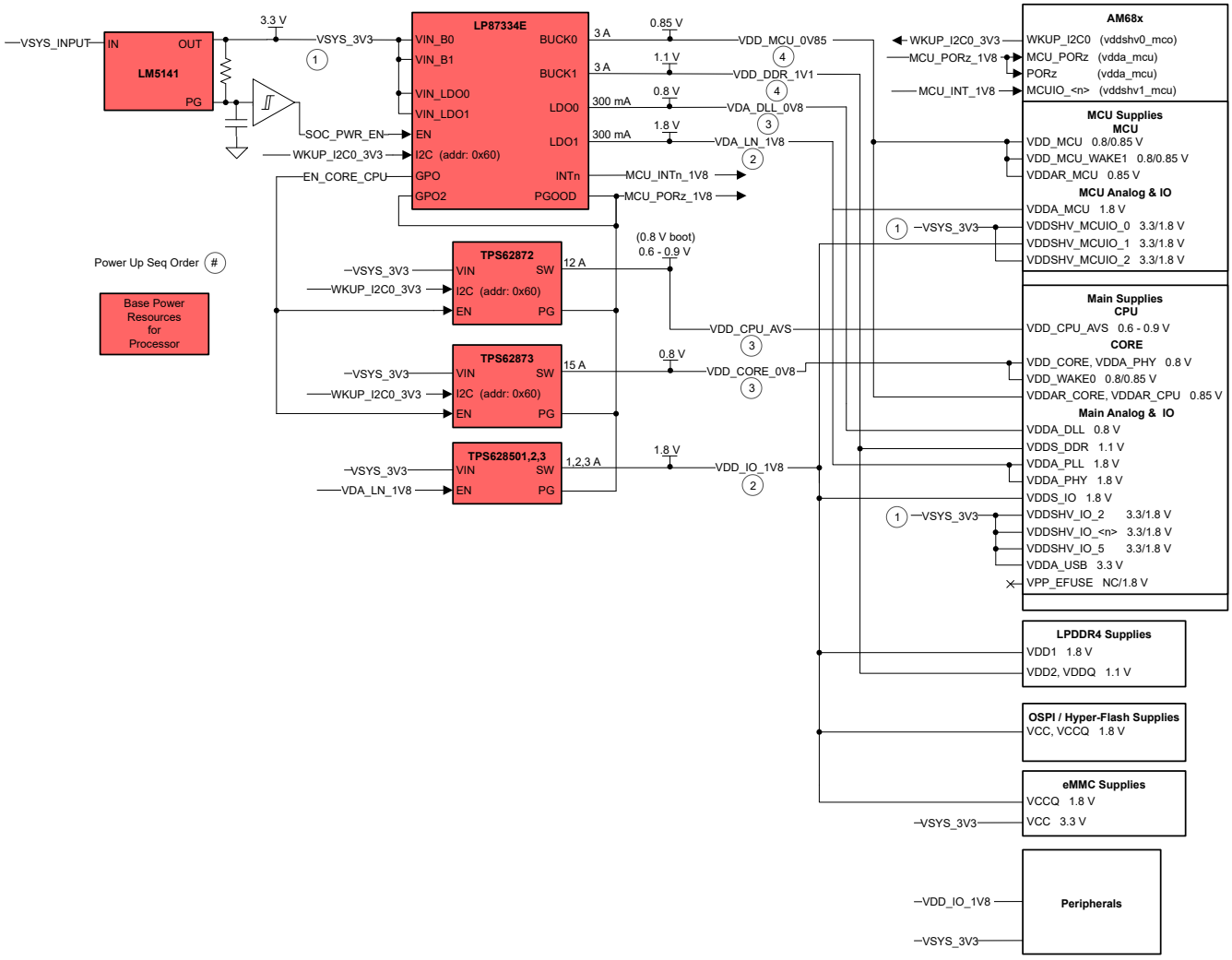

Figure 4-1. AM68x Single LP87334E PDN-6K, Base Features Only

4.2 AM68x Single LP87334E PDN-6J, Base and eFuse Programming

The PDN-6J scheme adds one *TLV3318P* LDO to the base power components as shown Figure 4-2 to enable *on-board* eFuse programming of the high security AM68x processor for in-field security key updates.

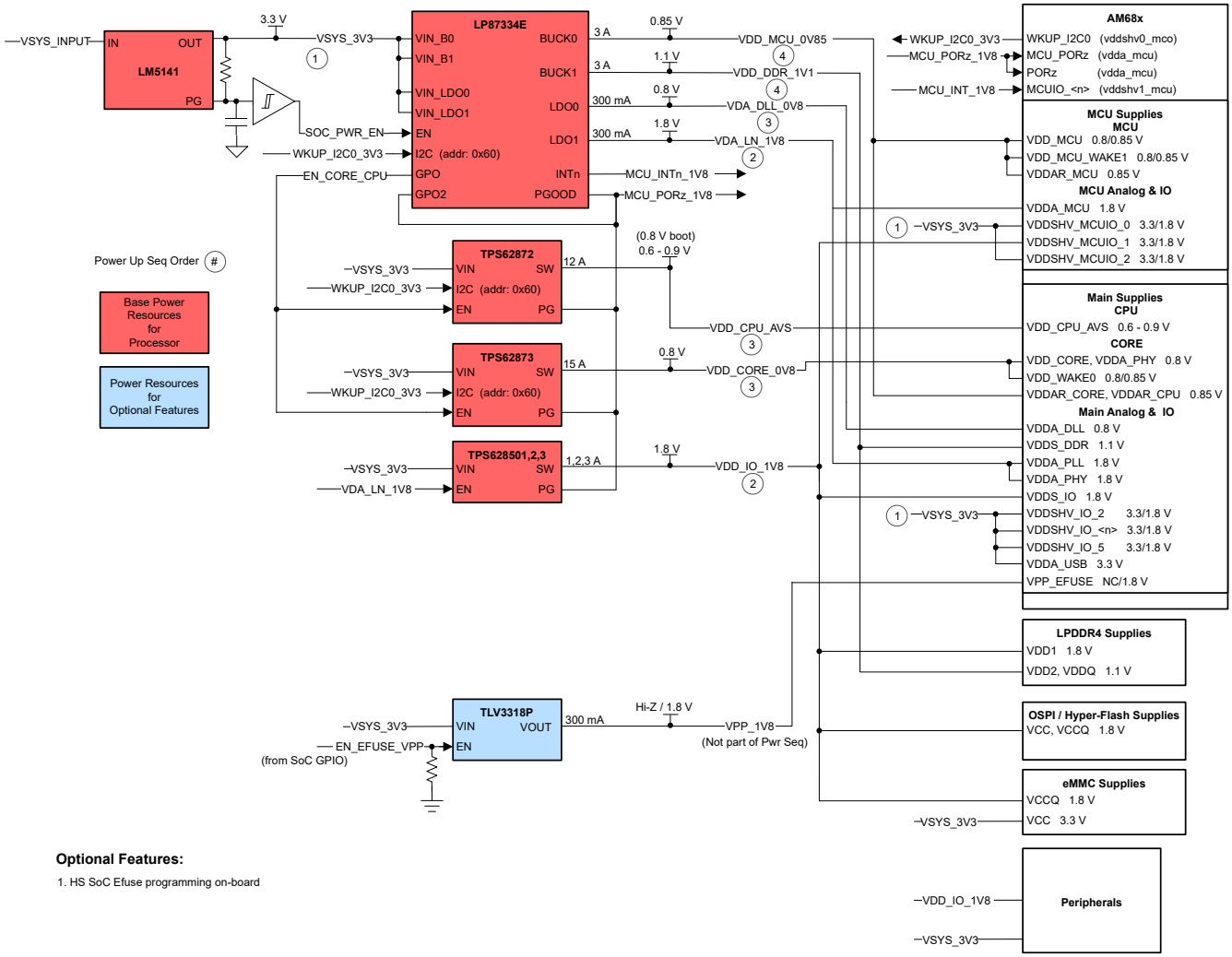

Figure 4-2. AM68x Single LP87334E PDN-6J, Base and eFuse Programming

4.3 AM68x Single LP87334E PDN-6H, Base, eFuse and SD Card

The PDN-6H scheme adds two components: one *TPS61240* boost converter to supply 5.0 V and one *TLV103318* dual voltage LDO as shown Figure 4-3. These additional power resources enable compliant UHS-I high-speed SD card storage. The *SK-AM68 Processor Starter Kit* uses PDN-6H scheme.

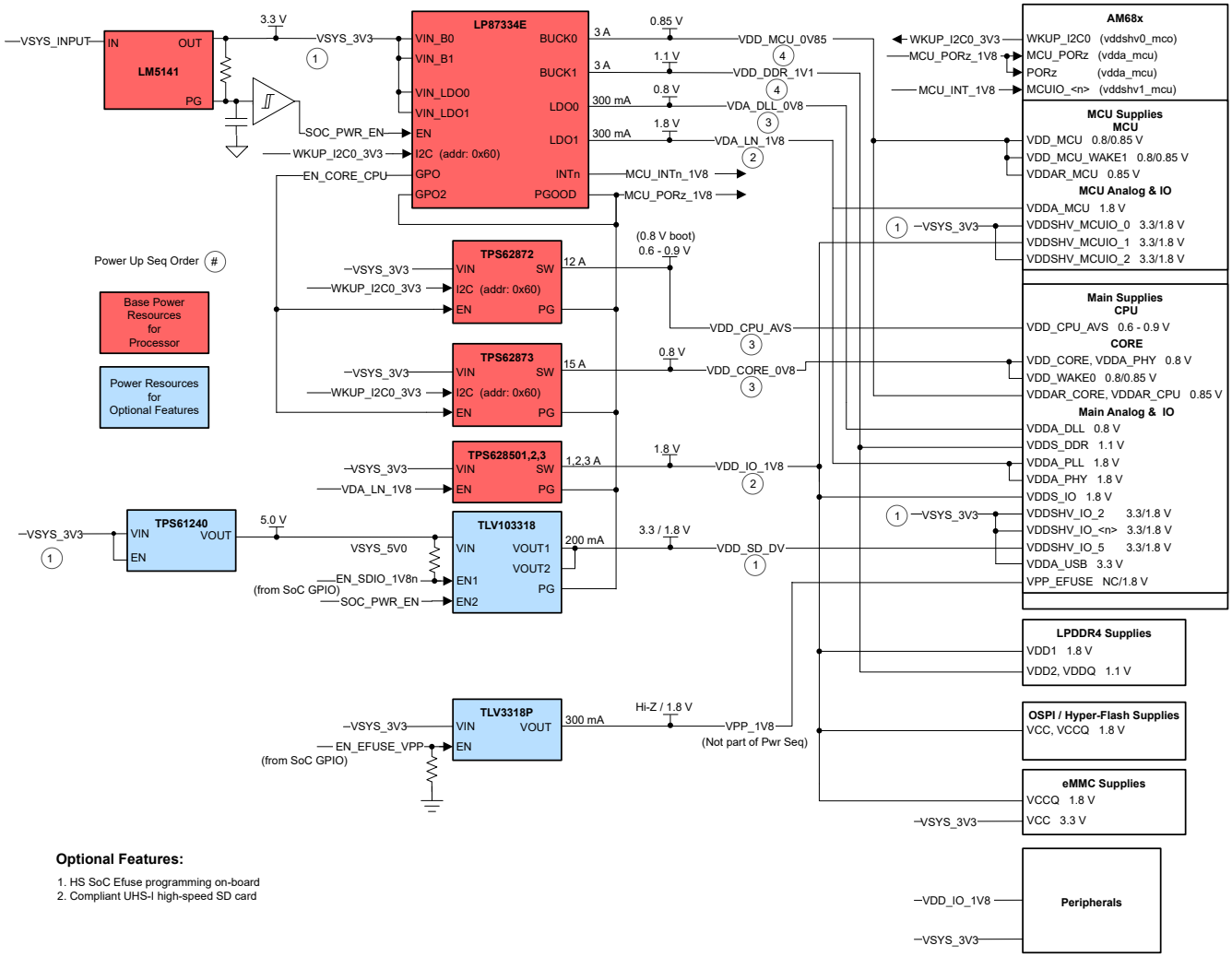

Figure 4-3. AM68x Single LP87334E PDN-6H, Base, eFuse and SD Card

4.4 AM68x Single LP87334E PDN-6G, Base, eFuse, SD Card, and USB2.0

The PDN-6G scheme adds one TLV3318P LDO to supply a low noise 3.3 V analog supply to AM68x as shown Figure 4-4. This design optimizes USB 2.0 data eye performance for reduced error rate communications.

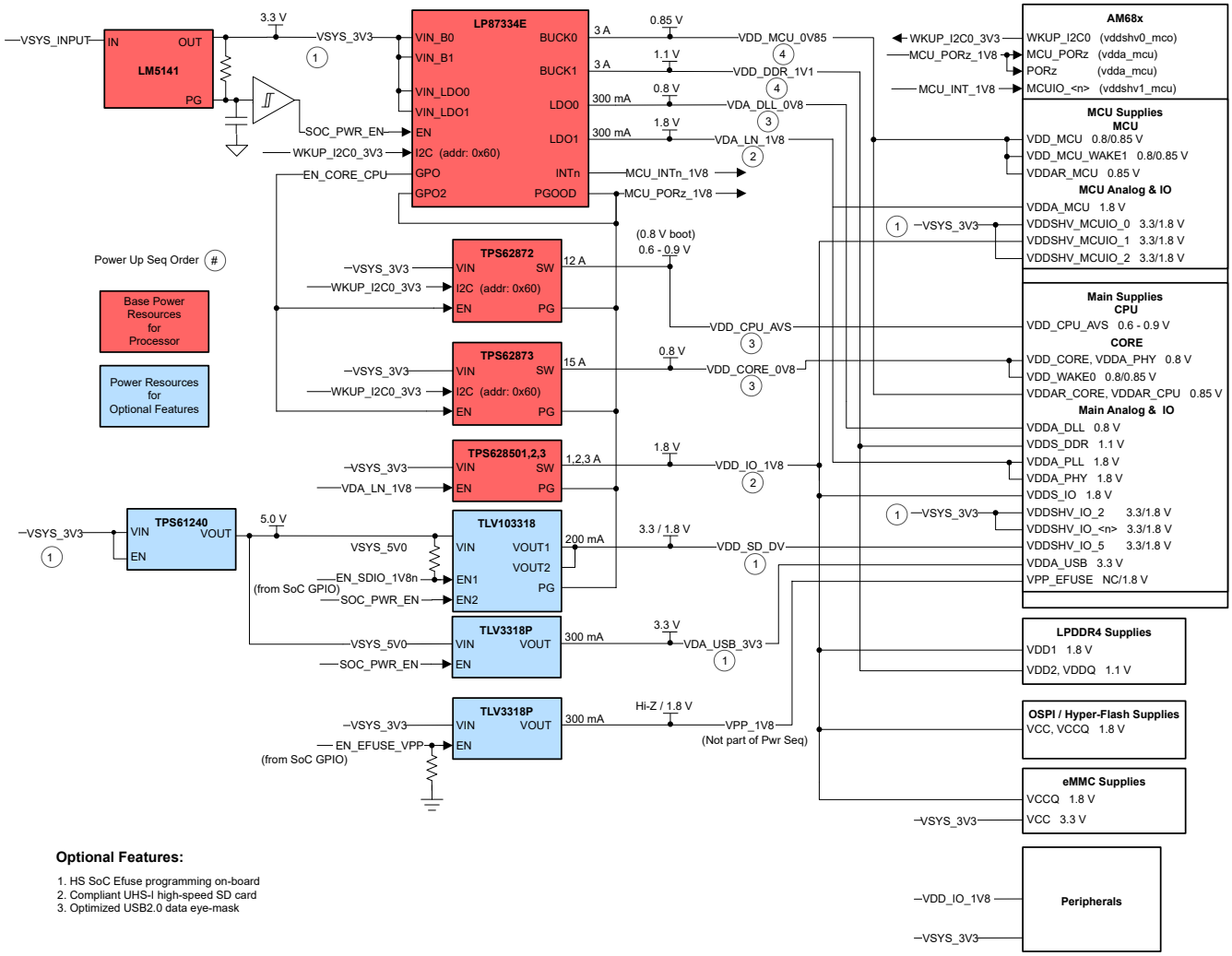

Figure 4-4. AM68x Single LP87334E PDN-6G, Base, eFuse, SD Card, and USB2.0

5 Conclusion

The PDN-6x power design is composed of four variants (G, H, J, and K) to provide peak power for the *AM68x* processor line and the *SK-AM68 Processor Starter Kit* uses PDN-6H scheme. The highly integrated *LP8733x* PMIC is the central power device that enables low cost, reduced area power designs for non-safety, industrial AM68x processor applications. A PDN selection guide outlined different AM68x use cases along with the PDN-6x base and optional features to assist selection of an AM68x power design. Example power maps for each PDN variant were provided to clarify different power designs and help accelerate the design process.

6 References

- Texas Instruments, *AM68x Processors, Silicon Revision 1.0*, data sheet.
- Texas Instruments, *SK-AM68 Processor Starter Kit*, user guide.
- Texas Instruments, *LP8733, Product Information and Support*, data sheet.
- Texas Instruments, *The Benefits of FlexPower PMIC Devices*, application brief.
- Texas Instruments, *TPS6287x 2.7-V to 6-V Input, 6-A, 9-A, 12-A, 15-A, Stackable, Synchronous Step*, data sheet.
- Texas Instruments, *TPS62850x 2.7-V to 6-V, 1-A / 2-A / 3-A Step-Down Converter in SOT583 Package*, data sheet.
- Texas Instruments, *TLV733P Capacitor-Free, 300-mA, Low-Dropout Regulator in 1-mm × 1-mm X2SON Package*, data sheet.
- Texas Instruments, *Dual, 200mA, Low-Iq, Low-Dropout Regulator for Portable Devices*, data sheet.
- Texas Instruments, *TPS6124x 3.5-MHz High Efficiency Step-Up Converter*, data sheet.

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