TVP5150AM1 Powerdown Mode

Digital Video and Imaging

1 Lowest Power Consumption in TVP5150AM1 Powerdown Mode

Mobile applications such as cell phones and PDAs have low power consumption as a key requirement. The TVP5150AM1 offers very low power consumption in normal operation. When the TVP5150AM1 is not in use, the power consumption must also be very low. This application report outlines how to correctly implement the powerdown mode to ensure the lowest power consumption. All of the following pins must either (1) be enabled as outputs, or (2) be disabled and externally driven low or high, or externally pulled low or high through a resistor. The pin numbers are for the 32-terminal TQFP (PBS) package.

Pin	Name
11-18	YOUT[7:0]
21	SCL
22	SDA
23	FID/GLCO
24	VSYNC/PALI
25	HSYNC
26	AVID
27	INTREQ/GPCL/VBLK

If these I/O pins on the TVP5150AM1 are left in a floating state (0.4 V < I/O voltage < 2.9 V) during powerdown mode, the I/O buffers leak current. If not enabled as outputs or driven externally, each pin should be either pulled up or down through a 10-kΩ (or similar) resistor. Pin YOUT7/I2CSEL is always pulled high or low for the I^2C address select, so the YCrCb output must always be disabled (bit 3 of register 0x03 set to 0) in powerdown mode and pins YOUT[6:0] driven or pulled high/low. The clock pin should always be enabled.

To prevent current leakage in powerdown mode, one of the following three options must be followed:

1. Do not use powerdown function (pin 28); instead, power off the TVP5150AM1 when not in use. If the system is using a RAM patch code, the system must redownload the patch code to the TVP5150AM1 each time the TVP5150AM1 is powered back on.
2. Use hardware powerdown function (pin 28) with the I/O control and clock pins enabled. Enabling the outputs prevents them from floating, forcing them to 0 V or 3.3 V. The data outputs must be disabled and driven or pulled high/low. See Section 2.
3. Use hardware powerdown function (pin 28) with the I/O data and control pins disabled. If the I/O pins are disabled in powerdown mode, then it is required to use external pulldown/pullup resistors for these floating pins, or to drive them high or low with another device in the customer system. The clock pin is enabled. The SDA and SCL pins should already be pulled high for I^2C. See Section 3.

NOTE: Pin 23 is always enabled as an output in GLCO mode (default) and cannot be disabled. Because this pin is enabled as an output, it should not be pulled down or driven externally as recommended for the other I/O pins.

2 Procedure 1: Using the Powerdown Mode with Control/Clock Outputs Enabled and Data Outputs Disabled

System Requirements for This Example

- The following procedure ensures that the PCLK/SCLK, HSYNC, VSYNC/PALI, AVID, FID/GLCO, and INTREQ/GPCL/VBLK pins are enabled as outputs, and that the Y[7:0] pins are disabled, by setting register 0x0F to 0x0A and register 0x03 to 0x25. Enabling the control outputs prevents them from floating, forcing them to 0 V or 3.3 V. The clock is enabled and forced to a low state. These pins should not be pulled low/high through a resistor or driven low/high by another device in the system. The YOUT[6:0] pins should be pulled low/high through a resistor or driven low/high by another device in the system. YOUT7 should already be pulled high or low for the I^2C address select.

If the requirements above are met, powerdown mode is correctly initiated by the following procedure.

To Enter Powerdown Mode

1. Write the following values to the TVP5150AM1 internal registers.
   This I^2C write has double the normal amount of wait time, which must be accounted for.

   1. Write 0x51 to I2C_0x21 // Unlock password for register write
   2. Write 0x50 to I2C_0x22 // Unlock password for register write
   3. Write 0xFF to I2C_0x23 // Unlock password for register write
   4. Write 0x04 to I2C_0x24 // Unlock password for register write
   5. Write 0xC8 to I2C_0x21 // Bypass PLL to set clock low
   6. Write 0xC8 to I2C_0x22 // Bypass PLL to set clock low
   7. Write 0x17 to I2C_0x23 // Bypass PLL to set clock low
   8. Write 0x06 to I2C_0x24 // Bypass PLL to set clock low
   9. Write 0x0A to I2C_0x0F // Enable GLCO and GPCL pins
   10. Write 0x25 to I2C_0x03 // Enable control pins and clock; disable data outputs

2. Wait at least 250µs. (See detailed timing requirements below.)
3. Assert powerdown pin by setting a low level to pin 28. The device powers down.

To Exit Powerdown Mode

1. De-assert the powerdown pin by setting a high level to pin 28. The device powers up.
2. Wait for the external crystal to be stable (~20 ms).
3. Assert the reset pin by setting a low level to pin 8.
4. Wait at least 2 ms.
5. Negate the reset pin by setting a high level to pin 8.
6. Write 0x05 to I2C_0x10 for activating patch code.
7. Write preferred settings to I^2C.

NOTE: If the patch code is downloaded before entering powerdown mode, it remains in the internal program memory, while all settings to I^2C registers are negated by reset operation. Therefore, downloading the patch code is not required after exiting the powerdown mode.

3 Procedure 2: Using the Powerdown Mode With Outputs Disabled

System Requirements for This Example

- The following procedure assumes that the YOUT[7:0], HSYNC, VSYNC/PALI, AVID, and INTREQ/GPCL/VBLK pins are disabled as outputs by setting register 0x03 to 0x01. It is required to use external pulldowns for these floating output control and YOUT[6:0] pins, or to drive them high or low with another device in the customer system.
- The clock, PCLK/SCLK, is enabled and forced to a low state, so it should not be pulled or driven high/low.
- The FID/GLCO pin (pin 23) is always enabled as an output in GLCO mode (default) and can not be disabled. Since this pin is enabled as an output, it should not be pulled down or driven externally as recommended for the other I/O pins.

If the requirements above are met, the powerdown mode is correctly initiated by the following procedure.

To Enter Powerdown Mode

1. Write the following values to the TVP5150AM1 internal registers.
   This I^2C write has double the normal amount of wait time, which needs to be accounted for.

   1. Write 0x51 to I2C_0x21 // Unlock password for register write
   2. Write 0x50 to I2C_0x22 // Unlock password for register write
   3. Write 0xFF to I2C_0x23 // Unlock password for register write
   4. Write 0x04 to I2C_0x24 // Unlock password for register write
   5. Write 0xC8 to I2C_0x21 // Bypass PLL to set clock low
   6. Write 0xC8 to I2C_0x22 // Bypass PLL to set clock low
   7. Write 0x17 to I2C_0x23 // Bypass PLL to set clock low
   8. Write 0x06 to I2C_0x24 // Bypass PLL to set clock low
   9. Write 0x01 to I2C_0x03 // Enable clock; disable data outputs and control pins

2. Wait at least 250µs. (See detailed timing requirements below.)
3. Assert powerdown pin by setting a low level to pin 28. The device powers down.

To Exit Powerdown Mode

1. De-assert the powerdown pin by setting a high level to pin 28. The device powers up.
2. Wait for the external crystal to be stable (~20 ms).
3. Assert the reset pin by setting a low level to pin 8.
4. Wait at least 2 ms.
5. Negate the reset pin by setting a high level to pin 8.
6. Write 0x05 to I2C_0x10 for activating patch code.
7. Write preferred settings to I^2C.

NOTE: If the patch code is downloaded before entering powerdown mode, it remains in the internal program memory, while all settings to I^2C registers are negated by reset operation. Therefore, downloading the patch code is not required after exiting the powerdown mode.

4 Timing Requirements

Timing Requirement to Enter Powerdown Mode

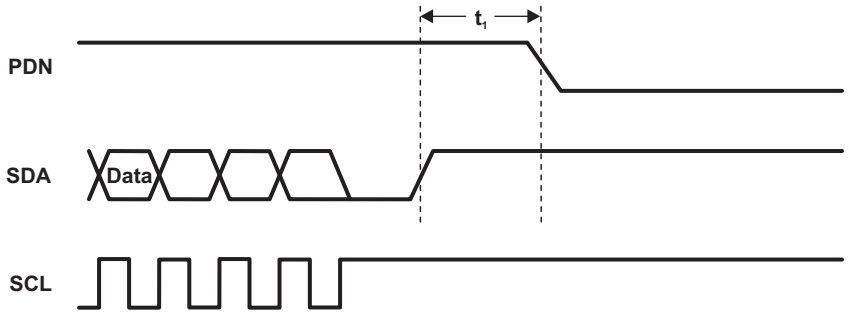

Figure 1. Powerdown Timing

Table 1. Powerdown Timing

PARAMETER		MIN	TYP	MAX	UNIT
t_1	Delay before entering powerdown mode	250			µs

Timing Requirements to Exit Powerdown Mode

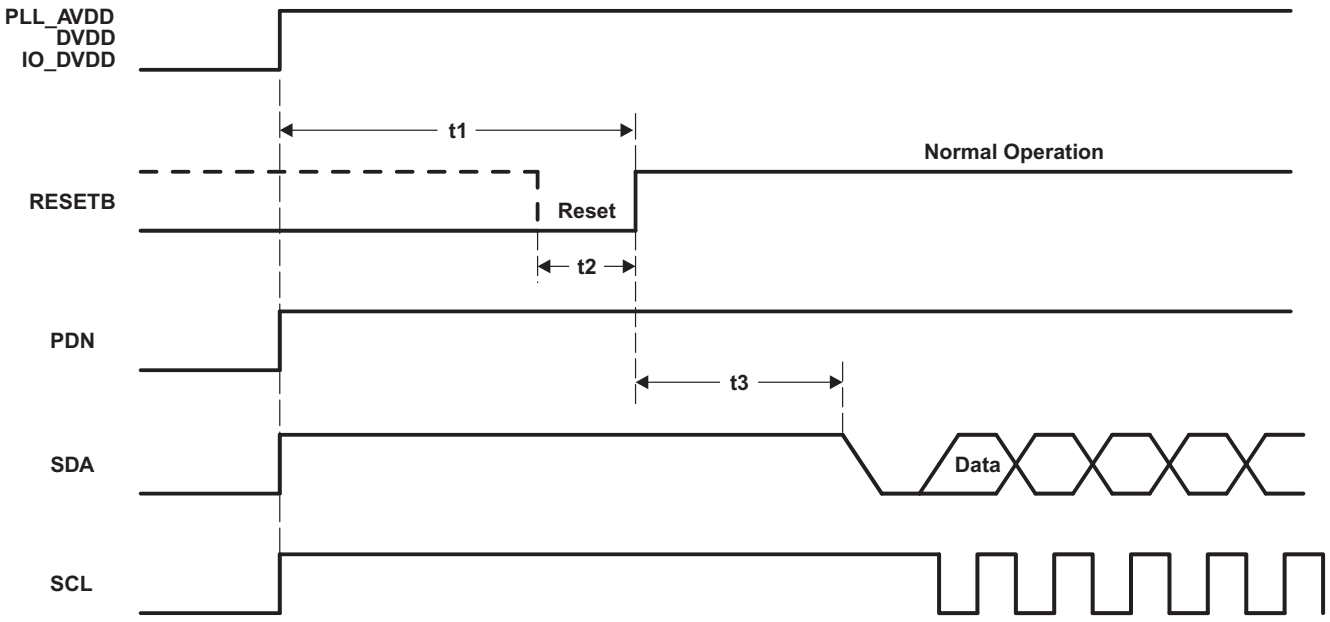

Figure 2. Power-On Reset Timing

Table 2. Power-On Reset Timing

PARAMETER		MIN	TYP	MAX	UNIT
t_1	Delay time between power supplies active and reset	20			ms
t_2	RESETB pulse duration	500			ns
t_3	Delay time between end of reset to I^2C active	200			µs

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