TAS5504A Errata

1 Volume/Mute Operation With Remapped Output Mixer

1.1 Problem Description

When the TAS5504A output mixer is used to mix several channels together or to route information from one DAP channel to a different PWM channel, then the TAS5504A can exhibit an unexpected response if one or more individual channels are set to mute. The mute can be performed with an individual channel mute or when the master volume plus individual volume is below –109 dB (0x1FC).

The issue is that the PWM channels corresponding to muted DAP channels are not restarted when coming out of an all-channel shutdown. All-channel shutdowns happen as a response to master mute, mute-pin assertion, I^2S clock error, or AM mode change. Using the pass-through output mixer configuration avoids this problem.

1.2 System Impact

If using the remapped output mixer configuration, then after resuming from an all-channel shutdown, the remapped output channels do not stream audio.

1.3 Workaround

Application software must ensure that combined master volume + channel volume does not go below –109 dB for all channels.

0xD0 Bit 30	Ouput Mixer Configuration	Mode	PWM (Speaker) Operation
1	Pass-through	4-channel mode	Normal operation
0 (default)	Remapped	4-channel mode	Constraints are placed in setting the combined volume below –109 dB and in using individual channel mute.

When remapping or mixing DAP channels to different PWM output channels (remapped output mixer configuration), consider the following limitations:

- Individual channel mute should not be used.
- The sum of the minimum channel volume and master volume must not be below –109 dB.
- 0xD0 bit 30 = 0

2 DRC Control Timing

2.1 Problem Description

Write operations to the DRC2 control register (0x97) can be missed if the values of the DRC1 control register (0x96) and DRC2 control register (0x97) are updated in successive I^2C operations. The issue is that a DRC2 control register update can be missed if it occurs immediately following a DRC1 control register update.

2.2 System Impact

The DRC2 control register configuration is changed, but due to an internal timing error in the DRC2 control register, the requested change is not recognized.

2.3 Workaround

Provide a 10-ms delay between I^2C writes to the DRC1 control register (0x96) and DRC2 control register (0x97).

3 PSVC Control When Using Subwoofer as Lineout

3.1 Problem Description

The problem occurs when the subwoofer is configured as lineout while PSVC is enabled.

One of the PSVC modes is called *subwoofer not part of PSVC calculation*. Normally, this mode is used when the subwoofer is configured as lineout. However, an audible problem occurs during volume changes. In this case, the subwoofer is always used for PSVC calculation even though it is configued not to do so (e.g., as lineout). So, during the volume ramp, the transient values are not correct, thereby creating audible artifacts.

3.2 System Impact

When the subwoofer is configured as lineout with PSVC enabled, audible artifacts can occur during volume changes.

3.3 Workaround

The subwoofer cannot be used as lineout if PSVC is enabled.

4 Use of 5-V CMOS I^2C Drivers

4.1 Problem Description

In systems using 5-V CMOS buffers for the I^2C interface, special pullup resistors are required.

The I^2C specification requires that V_{IH} is $0.7 \times V_{DD} = 3.5$ V when V_{DD} is 5 V. In some 5-V CMOS systems, the normal value for the I^2C pullup resistor is 4.7 kΩ. This could cause the voltage not to rise above 3.47 V, which violates the specification. The root cause has been identified as a TAS5504A 5-V tolerant buffer issue.

4.2 System Impact

1. No impact for 3.3-V operation
2. No impact for TTL operation
3. Impact only for 5-V CMOS operation where V_{IH} could be lower than the specification of 3.5 V.

4.3 Workaround

It is recommended that the I^2C pullup resistors, R_P, be 3.3 kΩ (see Figure 1). If a series resistor is in the circuit (see Figure 2), then the series resistors, R_S, should be less than or equal to 300 Ω.

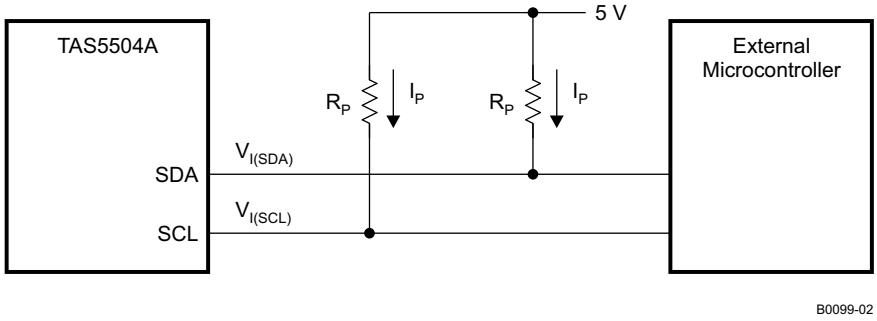
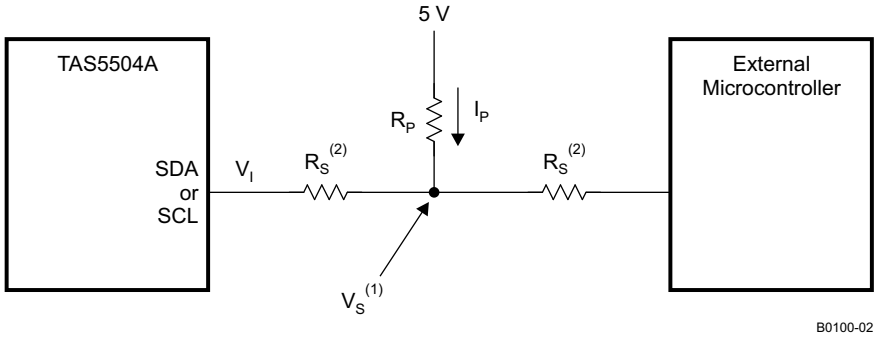


Figure 1. I^2C Pullup Circuit (With No Series Resistor)



(1) $V_S = 5 \times R_S/(R_S + R_P)$. When driven low, $V_S << V_{IL}$ requirements.

(2) $R_S \leq 300\ \Omega$

Figure 2. I^2C Pullup Circuit (With Series Resistor)

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5 One-Sample Delay in Channels 3 and 4

5.1 Problem Description

The TAS5504A exhibits a one-sample delay on channels 3 and 4 for sample rates of 32, 44.1, and 48 kHz. The delay occurs in the PWM section.

5.2 System Impact

This time misalignment can impact applications where the TAS5504A is used to provide crossover filtering and bi-amplification, as in powered loudspeakers. The problem that occurs in these cases is that a one-sample time delay in either the high-pass or low-pass path causes an error in the overall crossover frequency response.

The one-sample delay is not anticipated to cause any impact in other applications, because this corresponds to a relatively small position change, 7,19 mm or 0.28 in. for a 48-kHz sample rate.

5.3 Workaround

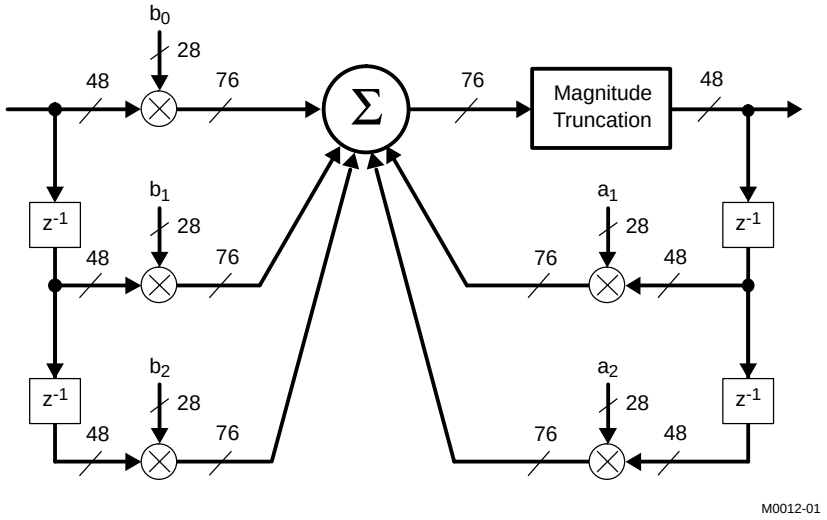
The time misalignment can be corrected by using a biquad to provide a one-sample delay for each of the nondelayed PWM channels for the 48-, 44.1-, and 32-kHz sample rates.

An example of this solution is the following:

When the input and output mixers provide a 1:1 input-to-output connection, a four-channel loudspeaker configuration uses one of the seven biquads in channels 1 and 2 to provide a one-sample delay. This added delay realigns all four channels.

To produce a one-sample delay with one of the TAS5504A biquads:

1. Set the b1 biquad coefficients to a gain of 1.
2. Set all of the other biquad coefficients (b0, b2, a1, and a2) to a gain of 0, as shown in the following diagram and table.



The one-sample delay setting is programmed using the following I²C register settings.

I²C SUBADDRESS	COEFFICIENT	HEX VALUE
Biquad I²C register Subaddress N	b_0—u(31:28), b0(27:24), b0(23:16), b0(15:8), b0(7:0)	0x00, 0x00, 0x00, 0x00
	b_1—u(31:28), b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x80, 0x00, 0x00
	b_2—u(31:28), b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
	a_1—u(31:28), a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
	a_2—u(31:28), a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00

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