Application Report
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FlatLink™ Data Transmission System Using SN75LVDS83B/SN75LVDS82/SN75LVDS86A

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ABSTRACT

This application report presents various system designs possible using the FlatLink™ transmitter: SN75LVDS83B, and the FlatLink™ receivers: SN75LVDS82 and SN75LVDS86A. These are low-voltage differential signaling (LVDS) serializer/deserializer (SerDes) devices commonly used to transmit video data to liquid crystal display (LCD) panels. The application report starts with an introduction of the FlatLink™ system, followed by the input and output data timing diagrams, and then finally shows different system designs with the help of system diagrams.

Contents

List of Figures

List of Tables

1 Introduction

FlatLink™ is an LVDS SerDes data transmission system. The serializer (transmitter) takes in three (or four) data words each containing seven single-ended data bits and converts this to an LVDS serial output. Each serial output runs at seven times that of the parallel data rate. The deserializer (receiver) device operates in the reverse manner. The three (or four) LVDS serial inputs are transformed back to the original seven-bit parallel single-ended data.

FlatLink™ devices are available in 21:3 or 28:4 SerDes ratios.

- The 21-bit devices are designed for 6-bit RGB video for a total of 18 bits in addition to three extra bits for horizontal synchronization, vertical synchronization, and data enable.
- The 28-bit devices are intended for 8-bit RGB video applications. Again, the extra four bits are for horizontal synchronization, vertical synchronization, data enable, and the remaining is the reserved bit. These 28-bit devices can also be used in 6-bit and 4-bit RGB applications as shown in the subsequent system diagrams.

The following report provides system diagrams for the successful implementation of a basic FlatLink™ system using the SN75LVDS83B *28-bit* serializer (transmitter) device.

2 TTL Input Data

The data inputs to the transmitter come from the graphics processor and consist of up to 24 bits of video information, a horizontal synchronization bit, a vertical synchronization bit, an enable bit, and a spare bit. The data can be loaded into the registers upon either the rising or falling edge of the input clock selectable by the CLKSEL pin. Data inputs are 1.8 V to 3.3 V tolerant for the SN75LVDS83B and can connect directly to low-power, low-voltage application and graphic processors.

The bit mapping is listed in Table 1.

Table 1. Bit Mapping

	Red	Green	Blue
LSB	R0	G0	B0
	R1	G1	B1
	R2	G2	B2
4-bit MSB	R3	G3	B3
	R4	G4	B4
6-bit MSB	R5	G5	B5
	R6	G6	B6
8-bit MSB	R7	G7	B7

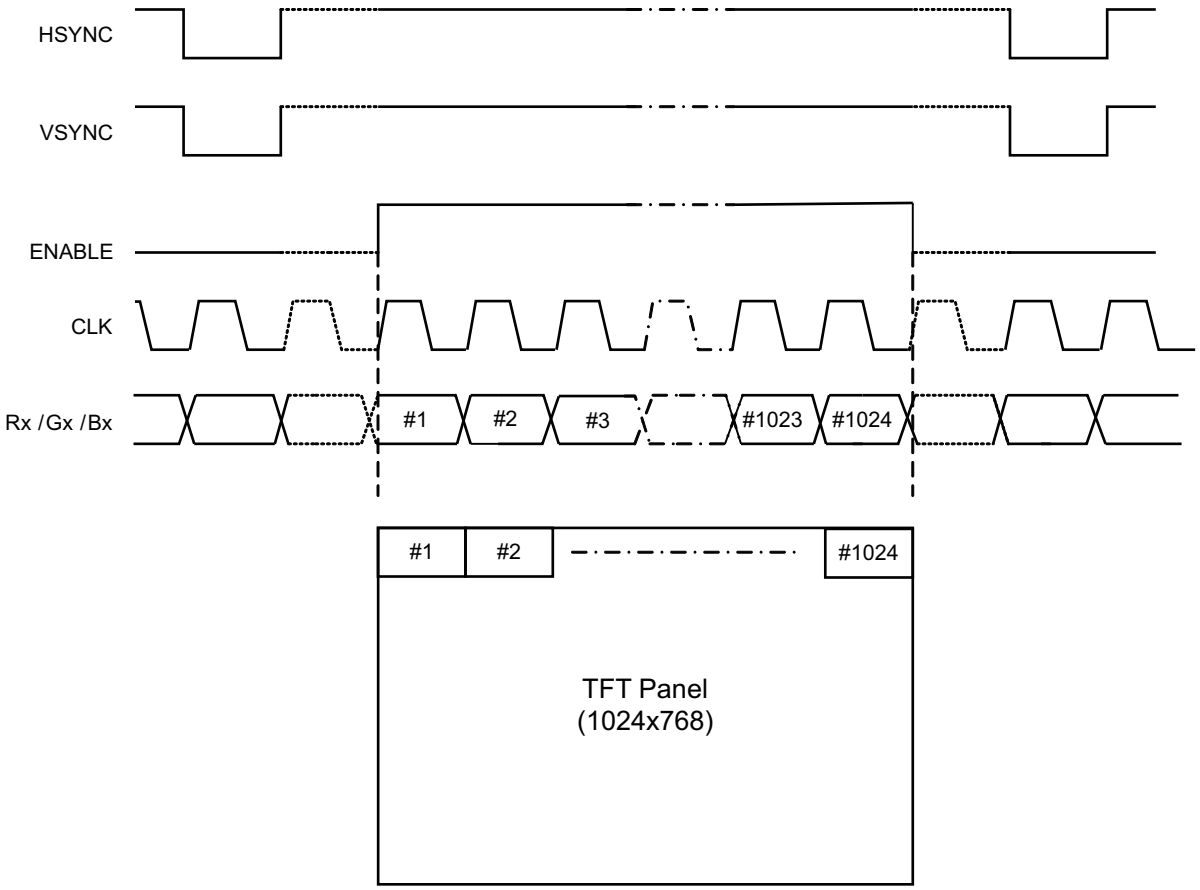


Figure 1. TTL Input Data Timing Diagram for XGA (1024 x 768)

3 LVDS Output Data

The pixel data assignment is listed in Table 2 for 24-bit, 18-bit, and 12-bit color hosts.

Table 2. Pixel Data Assignment

Serial Channel	Data Bits	8-Bit			6-Bit	4-Bit	
		Format-1 (1)	Format-2 (2)	Format-3 (3)		Non-Linear Step Size (4)	Linear Step Size (5)
Y0	D0	R0	R2	R2	R0	R2	VCC
	D1	R1	R3	R3	R1	R3	GND
	D2	R2	R4	R4	R2	R0	R0
	D3	R3	R5	R5	R3	R1	R1
	D4	R4	R6	R6	R4	R2	R2
	D6	R5	R7	R7	R5	R3	R3
	D7	G0	G2	G2	G0	G2	VCC

(1) *Format-1:* 2-MSBs of each color transmitted over 4th serial data channel (Y3). Dominant data format for LCD panel.
(2) *Format-2:* 2-LSBs of each color transmitted over 4th serial data channel. System designer needs to verify the data format by checking with the LCD display data sheet.
(3) *Format-3:* 24-bit color host to 18-bit color LCD panel display application.
(4) Increased dynamic range of the entire color space at the expense of non-linear step sizes between each step.
(5) Linear step size with less dynamic range.

Table 2. Pixel Data Assignment (continued)

Serial Channel	Data Bits	8-Bit			6-Bit	4-Bit	
		Format-1 (1)	Format-2 (2)	Format-3 (3)		Non-Linear Step Size (4)	Linear Step Size (5)
Y1	D8	G1	G3	G3	G1	G3	GND
	D9	G2	G4	G4	G2	G0	G0
	D12	G3	G5	G5	G3	G1	G1
	D13	G4	G6	G6	G4	G2	G2
	D14	G5	G7	G7	G5	G3	G3
	D15	B0	B2	B2	B0	B2	VCC
	D18	B1	B3	B3	B1	B3	GND
Y2	D19	B2	B4	B4	B2	B0	B0
	D20	B3	B5	B5	B3	B1	B1
	D21	B4	B6	B6	B4	B2	B2
	D22	B5	B7	B7	B5	B3	B3
	D24	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
	D25	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
	D26	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
Y3	D27	R6	R0	GND	GND	GND	GND
	D5	R7	R1	GND	GND	GND	GND
	D10	G6	G0	GND	GND	GND	GND
	D11	G7	G1	GND	GND	GND	GND
	D16	B6	B0	GND	GND	GND	GND
	D17	B7	B1	GND	GND	GND	GND
	D23	RSVD	RSVD	GND	GND	GND	GND
CLKOUT	CLKIN	CLK	CLK	CLK	CLK	CLK	CLK

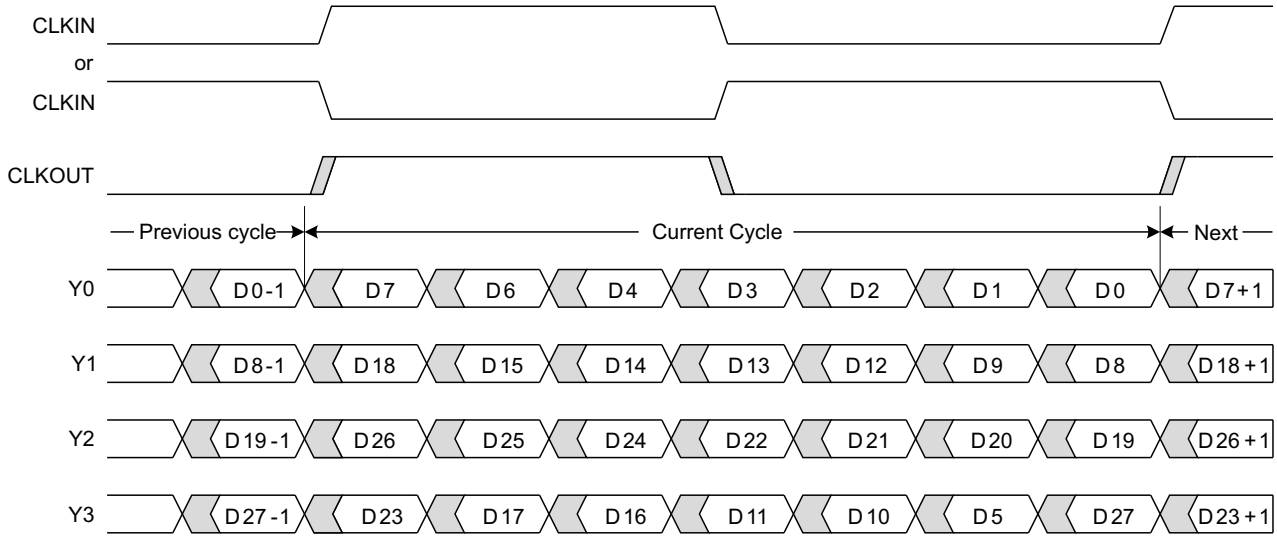
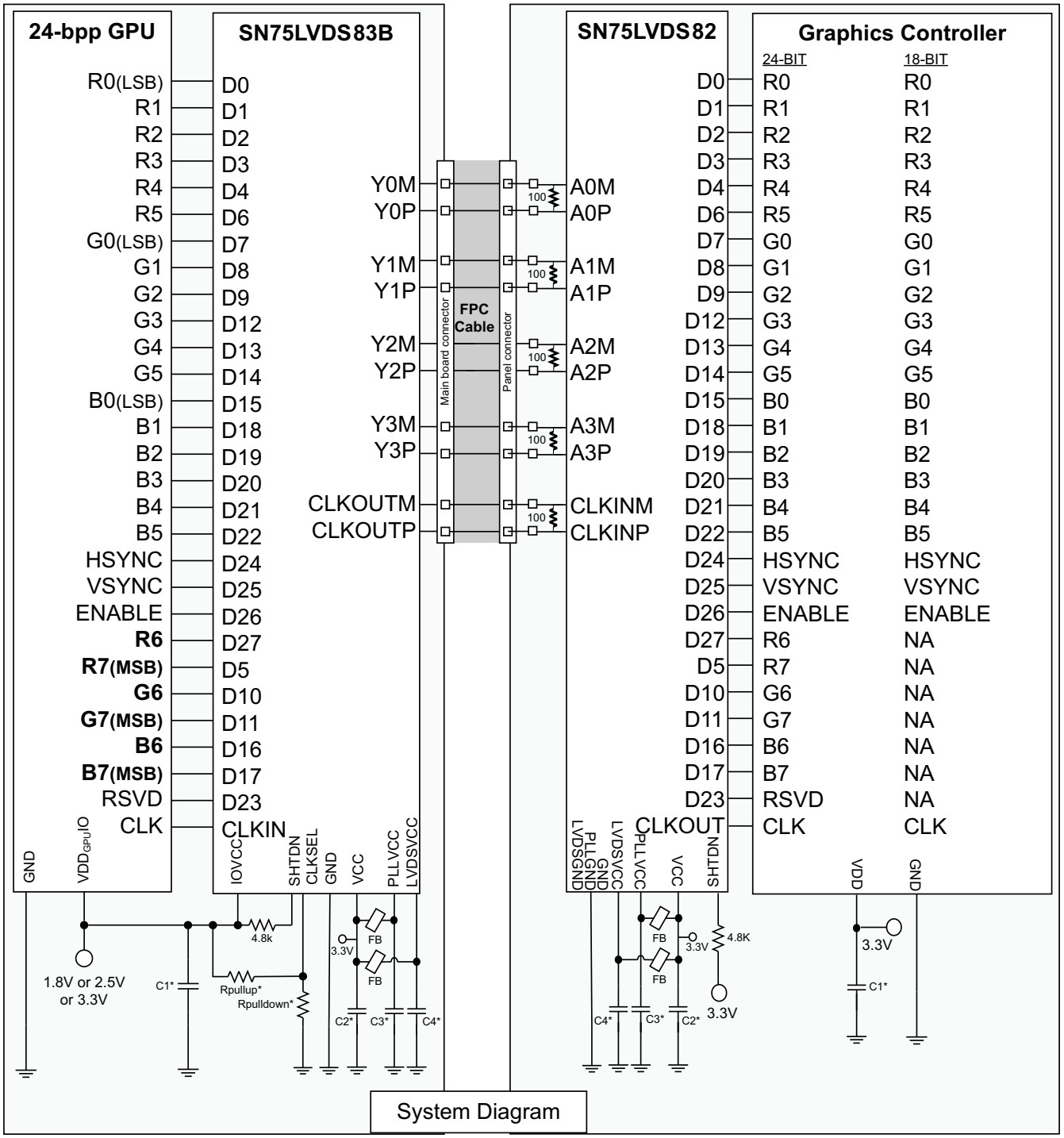


Figure 2. LVDS Output Data Timing Diagram

4 System Diagrams

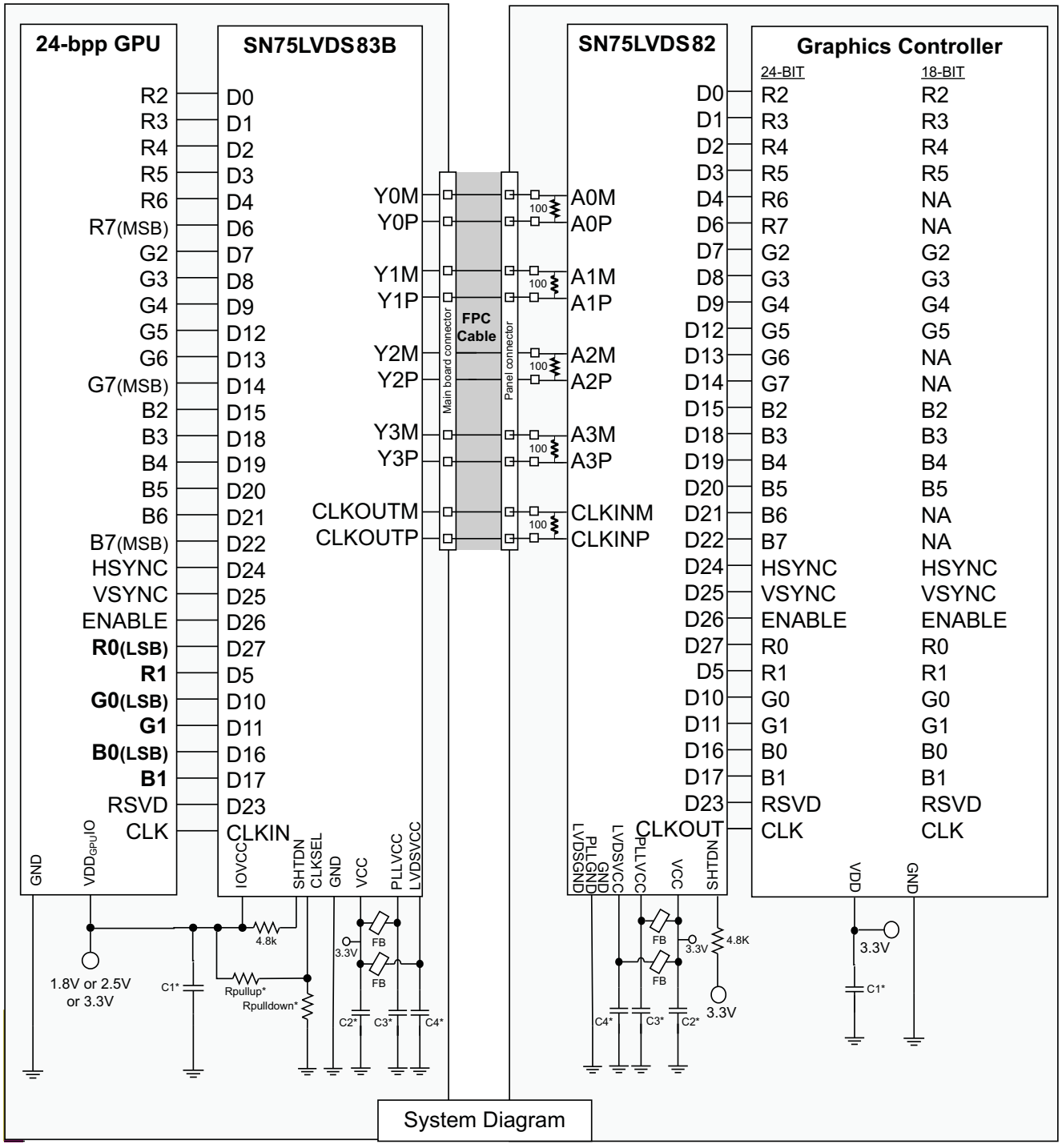
4.1 24-Bit Color Host to 24-Bit LCD Panel Application with 2 MSB Over 4th Channel



(Configuration most popular for 24-bit panels) — *Transmitter* SN75LVDS83B, *Receiver* SN75LVDS82

Figure 3. 24-Bit Color Host to 24-Bit LCD Panel Application with 2 MSB Over 4th Channel

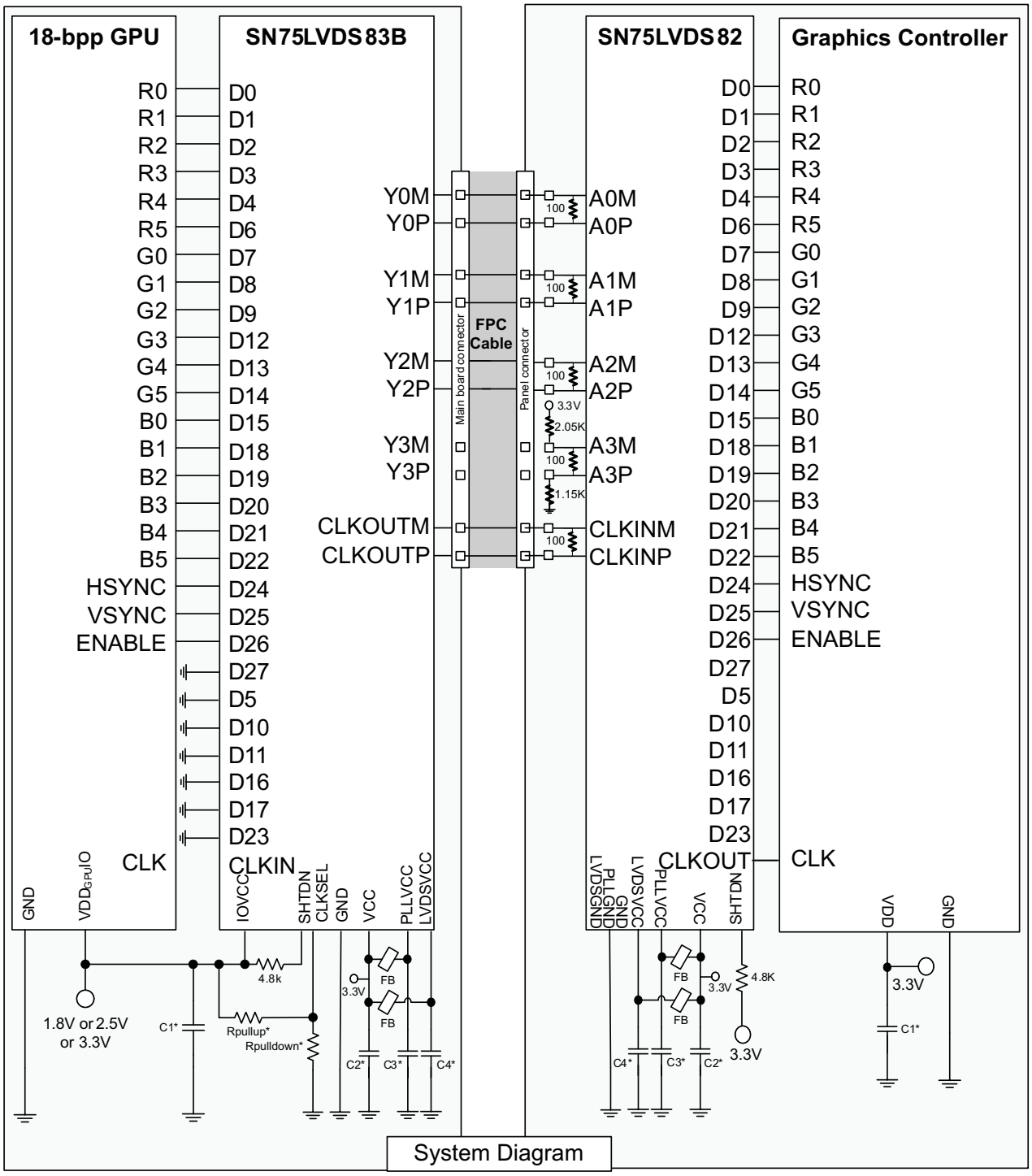
4.2 24-Bit Color Host to 24-Bit LCD Panel Application with 2 LSB Over 4th Channel



(Rare configuration for 24-bit panels) — *Transmitter* SN75LVDS83B, *Receiver* SN75LVDS82

Figure 4. 24-Bit Color Host to 24-Bit LCD Panel Application with 2 LSB Over 4th Channel

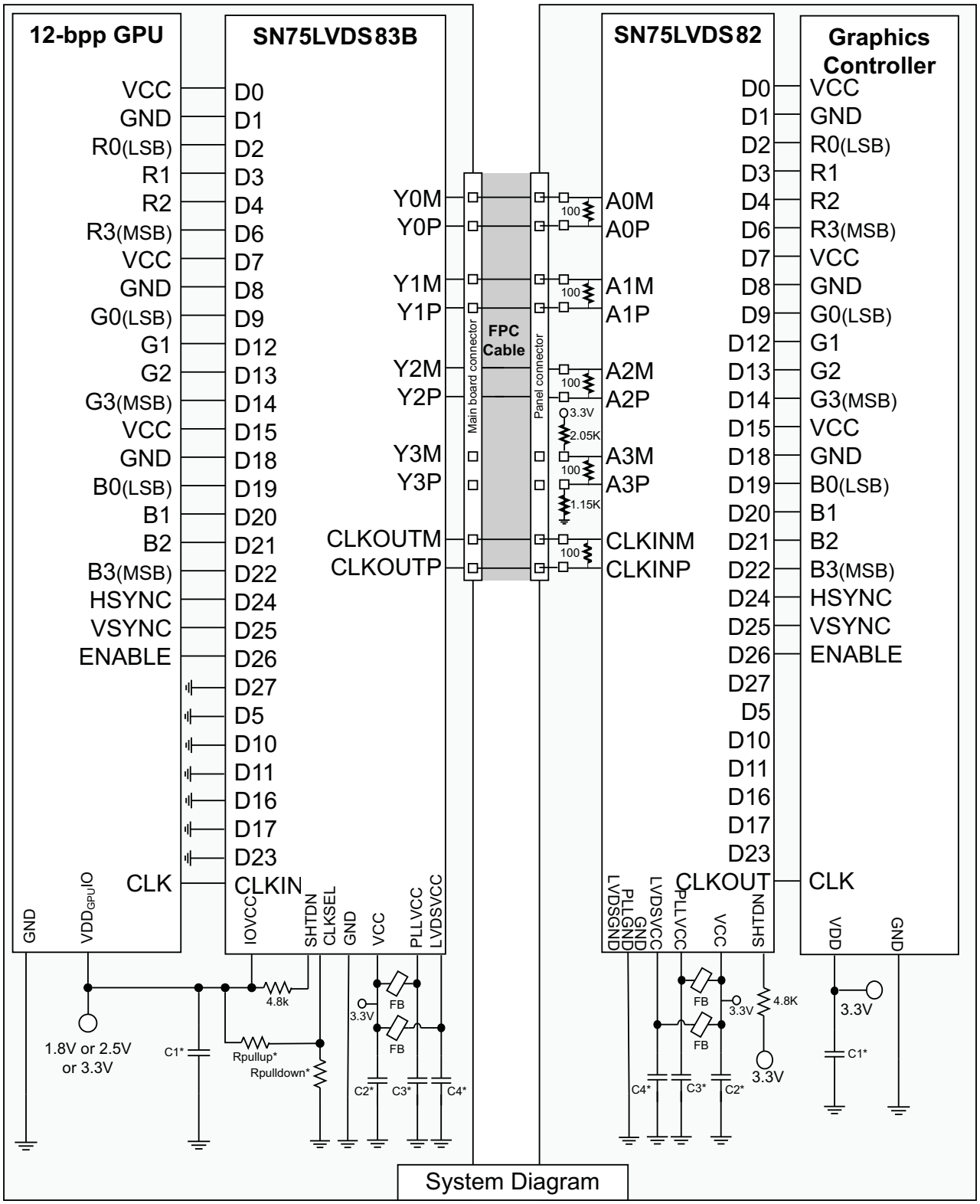
4.3 18-Bit Color Host to 18-Bit Color LCD Panel Display Application



Transmitter SN75LVDS83B, *Receiver* SN75LVDS82

Figure 5. 18-Bit Color Host to 18-Bit Color LCD Panel Display Application

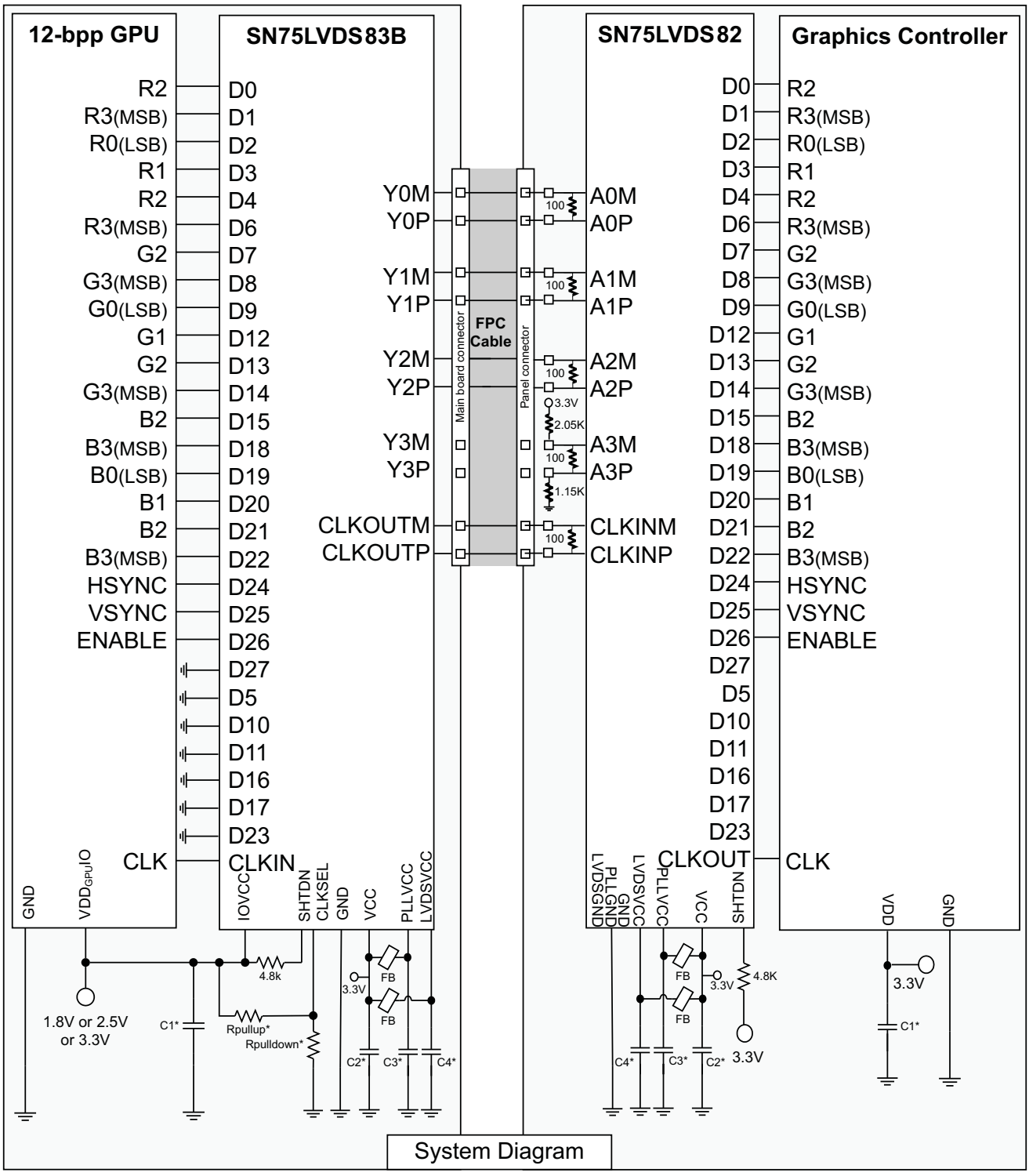
4.4 12-Bit Color Host to 18-Bit Color LCD Panel Display Application (Linear)



(A): Linear step size — *Transmitter* SN75LVDS83B, *Receiver* SN75LVDS82

Figure 6. 12-Bit Color Host to 18-Bit Color LCD Panel Display Application (Linear)

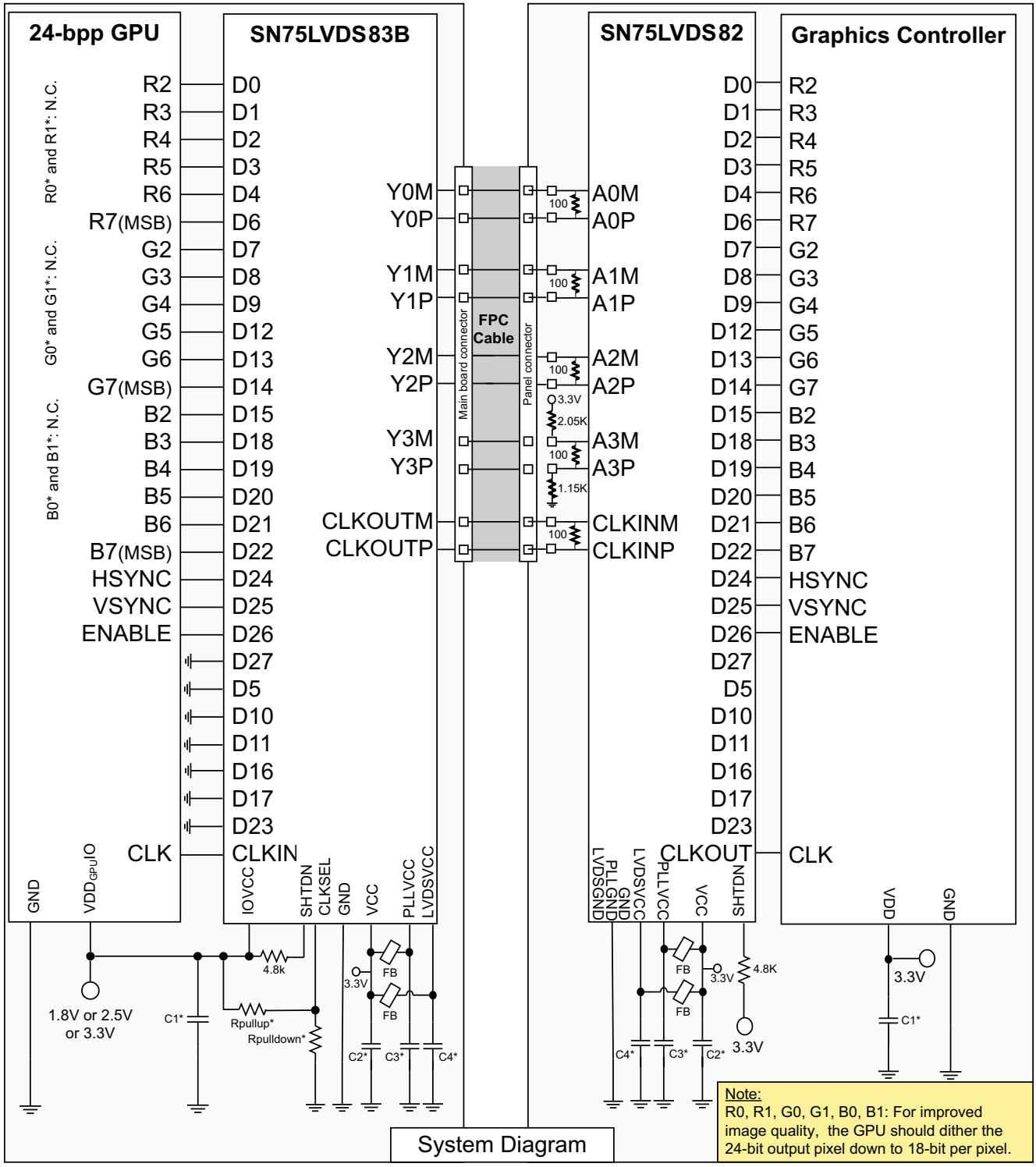
4.5 12-Bit Color Host to 18-Bit Color LCD Panel Display Application (Non-linear)



(B): Non-linear step size with increased dynamic range — *Transmitter* SN75LVDS83B, *Receiver* SN75LVDS82

Figure 7. 12-Bit Color Host to 18-Bit Color LCD Panel Display Application (Non-linear)

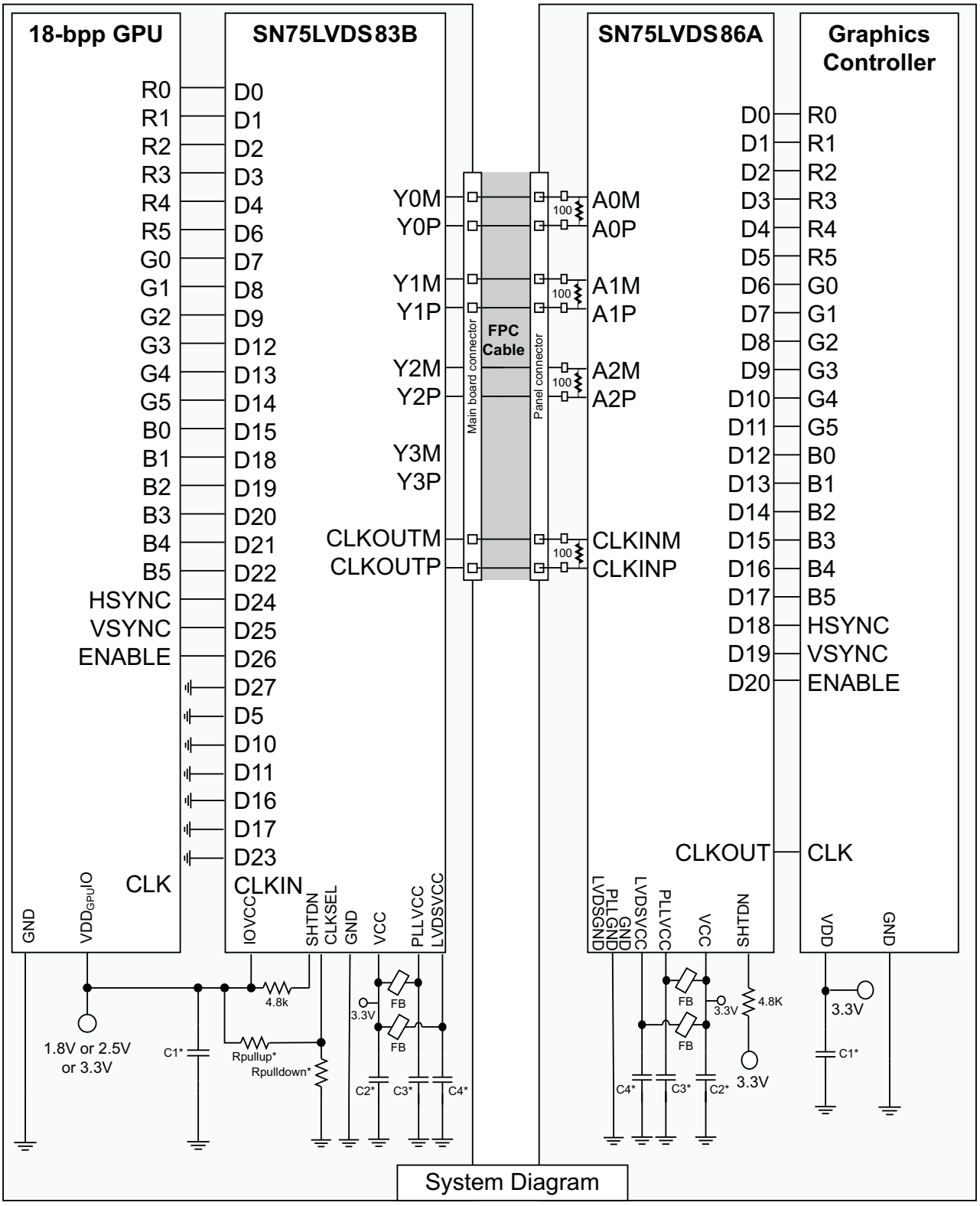
4.6 24-Bit Color Host to 18-Bit Color LCD Panel Display Application



Transmitter SN75LVDS83B, *Receiver* SN75LVDS82

Figure 8. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application

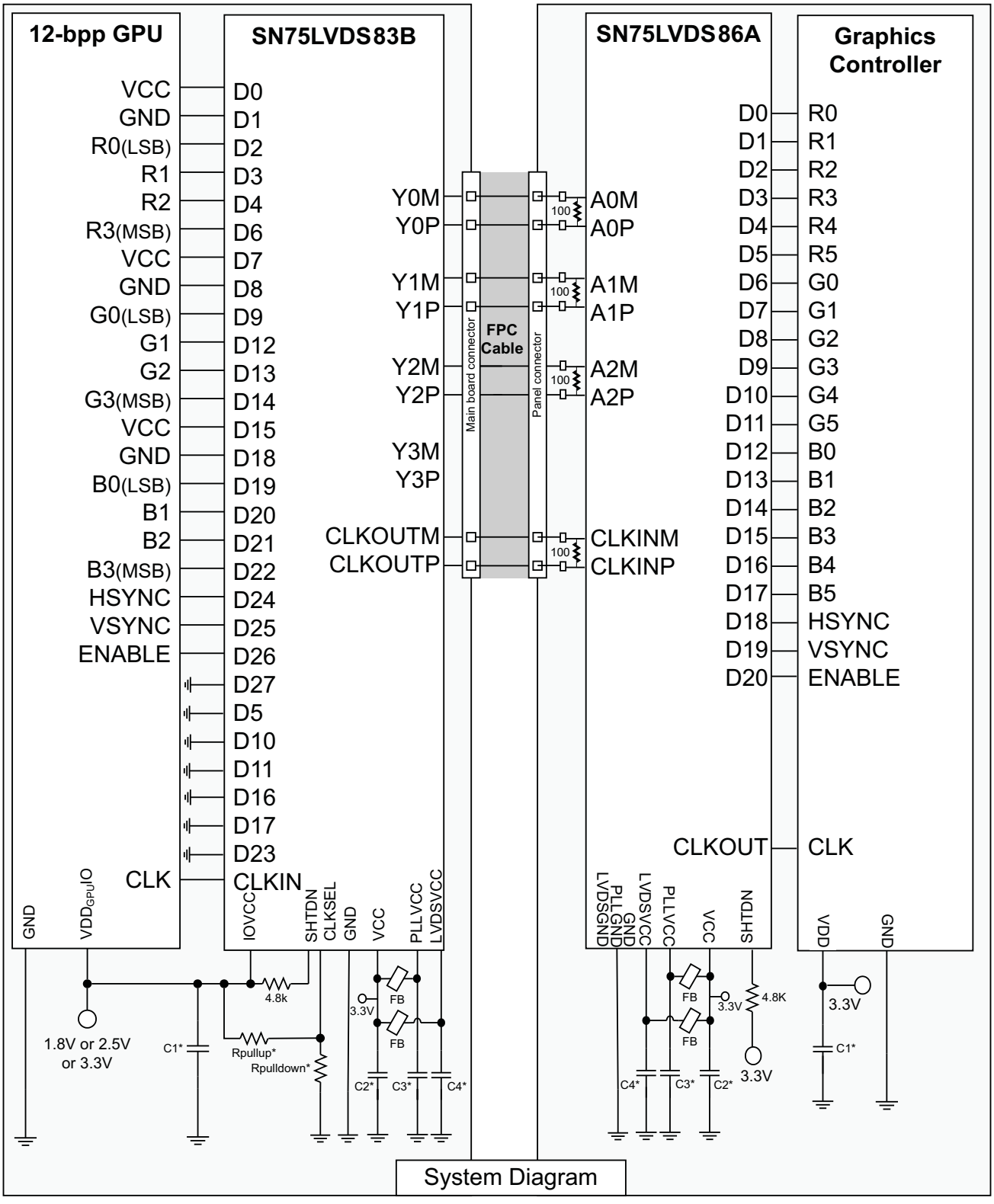
4.7 18-Bit Color Host to 18-Bit Color LCD Panel Display Application



Transmitter SN75LVDS83B, *Receiver* SN75LVDS86A

Figure 9. 18-Bit Color Host to 18-Bit Color LCD Panel Display Application

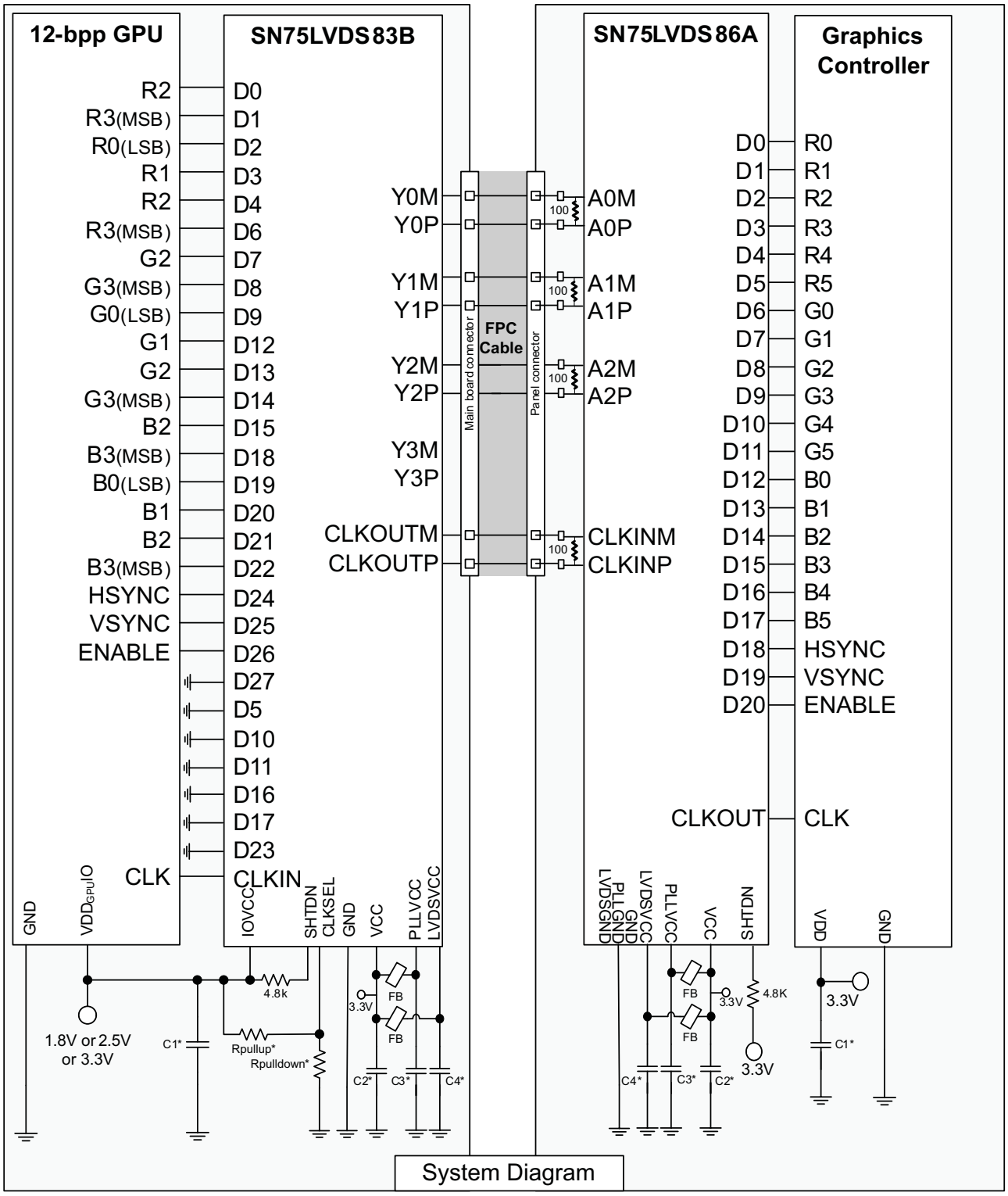
4.8 12-Bit Color Host to 18-Bit Color LCD Panel Display Application (Linear)



(A): Linear steps — *Transmitter* SN75LVDS83B, *Receiver* SN75LVDS86A

Figure 10. 12-Bit Color Host to 18-Bit Color LCD Panel Display Application (Linear)

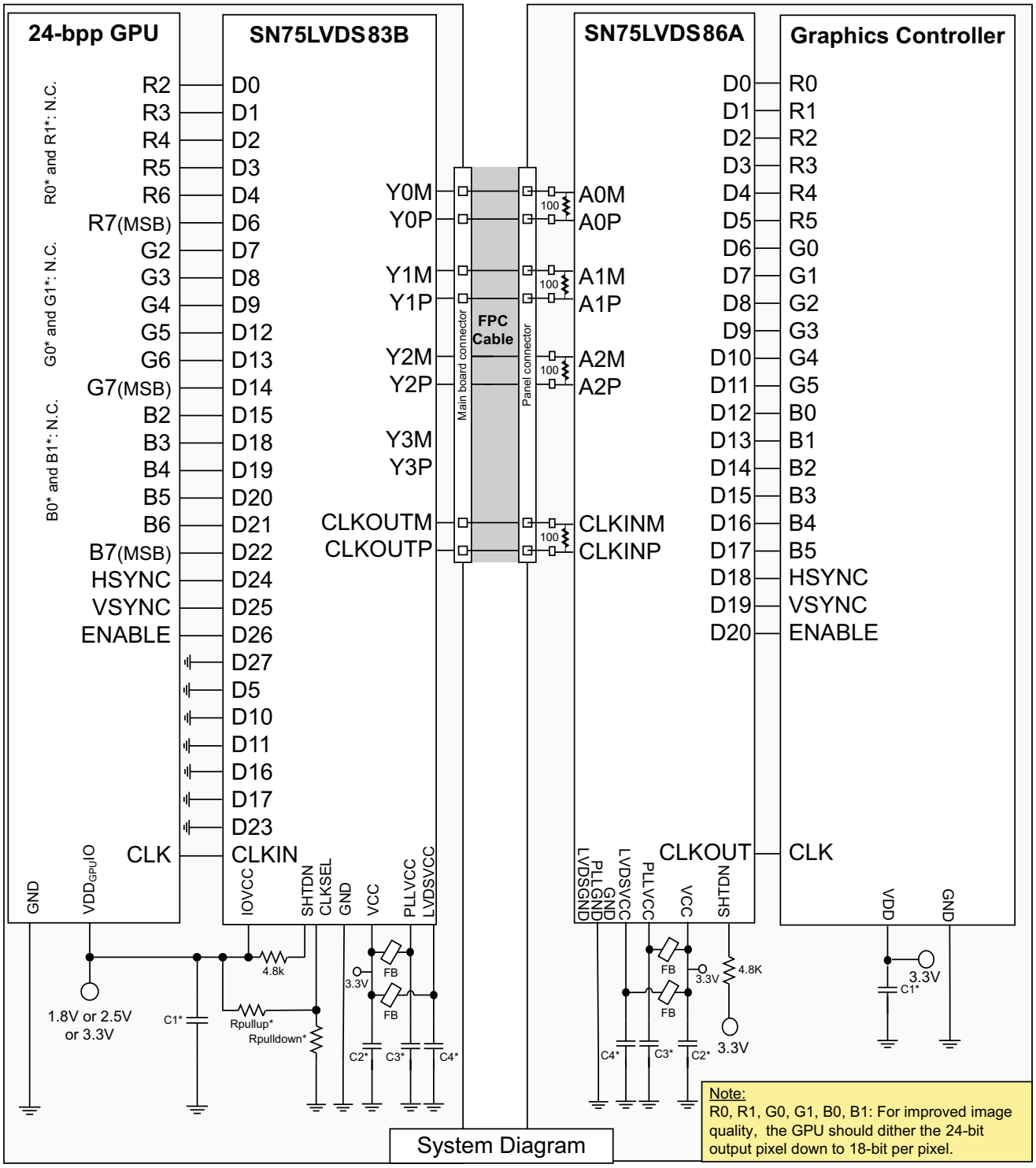
4.9 12-Bit Color Host to 18-Bit Color LCD Panel Display Application (Non-linear)



(B): Non-linear steps with increased dynamic range — *Transmitter* SN75LVDS83B, *Receiver* SN75LVDS86A

Figure 11. 12-Bit Color Host to 18-Bit Color LCD Panel Display Application (Non-linear)

4.10 24-Bit Color Host to 18-Bit Color LCD Panel Display Application



Transmitter SN75LVDS83B, *Receiver* SN75LVDS86A

Figure 12. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application

The points listed in Table 3 are valid for all of the previous system diagrams.

Table 3. Important Points to Note Regarding System Diagrams

R_{pullup}	Install only to use rising edge triggered clocking
$R_{pulldown}$	Install only to use falling edge triggered clocking
C1	Decoupling capacitor for the VDDIO supply; install at least 1 × 0.01 μF
C2	Decoupling capacitor for the VDD supply; install at least 1 × 0.1 μF and 1 × 0.01 μF
C3	Decoupling capacitor for the VDDPLL supply; install at least 1 × 0.1 μF and 1 × 0.01 μF
C4	Decoupling capacitor for the VDDLVDS supply; install at least 1 × 0.1 μF and 1 × 0.01 μF
Four 100-Ω terminating resistors are recommended (0603 or smaller package size)	

5 Power Up/Down Sequence

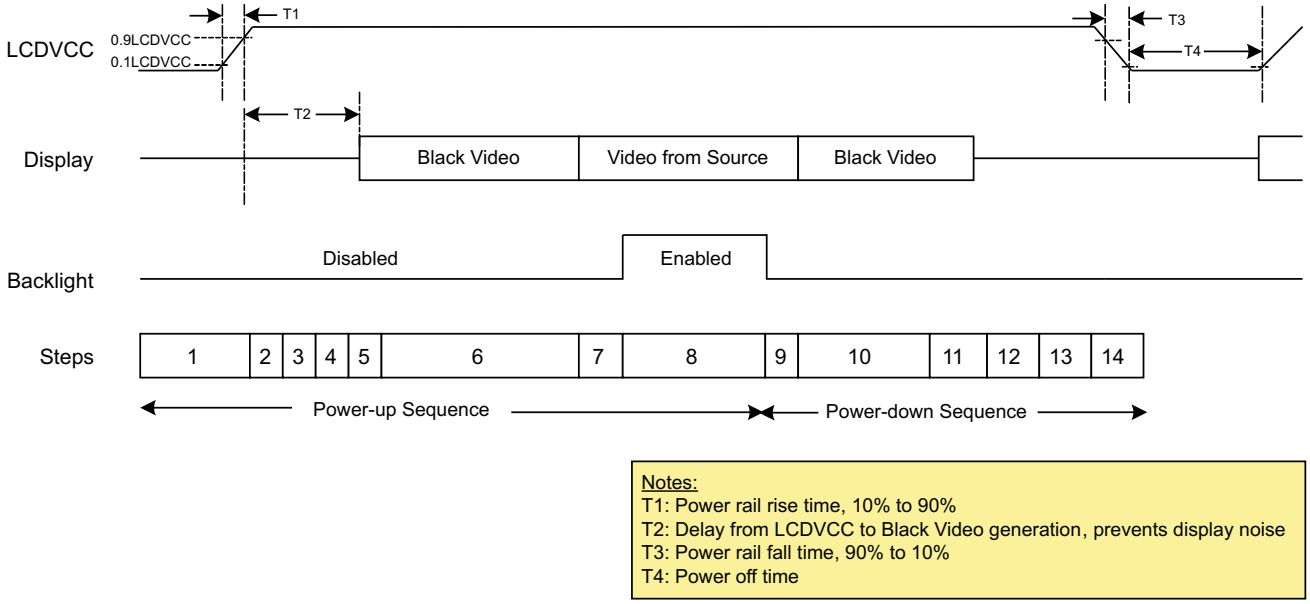


Figure 13. Power Up/Down Sequence

The user experience can be impacted by the way a system powers up and powers down an LCD screen. The following sequence is recommended:

- *Power up sequence (SN75LVDS83B SHTDN input initially low):*
  1. Ramp up LCD power (0.5 ms to 10 ms) but keep backlight turned off.
  2. Wait for additional 0 ms to 200 ms to ensure display noise does not occur.
  3. Enable video source output; start sending black video data.
  4. Toggle the transmitter (SN75LVDS83B) shutdown to high (SHTDN = HIGH). Power up the receiver (SN75LVDS82/SN75LVDS86A) and pull SHTDN to high (SHTDN = HIGH).
  5. Send at least 1 ms of black video data; this allows the SN75LVDS83B to be phase locked, and the display to show black data first.
  6. Start sending true image data.
  7. Enable backlight

  Note 1: In case an integrated receiver is used, step 5 is optional.

  Note 2: If SHTDN on the SN75LVDS83B is pulled high using pull-up, step 4 is also optional.
- *Power down sequence (SN75LVDS83B SHTDN input initially high):*
  1. Disable LCD backlight; wait for the minimum time specified in the LCD data sheet for the backlight to go low.
  2. Video source output data switch from active video data to black image data (all visible pixel turn

black); drive this for at least 2 frame times.

3. (11)Set SHTDN of receiver (SN75LVDS82/SN75LVDS86A) to low (SHTDN = LOW).
4. Set SN75LVDS83B input SHTDN = LOW; wait for 250 ns.
5. Disable the video output of the video source.
6. Remove power from the LCD panel for lowest system power.

Note 1: In case an integrated receiver is used, step 3 is optional.

Note 2: If SHTDN on the SN75LVDS83B is pulled high using pull-up, step 4 is also optional. In this case, keep the display power off until the SN75LVDS83B sends good, known data.

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