THS4001 SPICE Model Performance

James Karki

ABSTRACT

This document outlines the SPICE model of the THS4001 high-speed monolithic operational amplifier. General information about the model file structure, performance comparison, model listing, and a brief comment about symbols are included. The listing can be copied and pasted into an ASCII editor, or it can be down loaded by visiting the THS4001 product folder at http://www.ti.com/sc/docs/products/analog/ths4001.html.

Contents

1 Introduction

SPICE modeling has become commonplace today, especially with the advent of affordable PCs with computing power that surpasses the mainframes of yesteryear.

A major concern in SPICE modeling is the accuracy of the models. Without a good model, simulation results are not much more than verification of rudimentary circuit operation. The Boyle op amp model, introduced during the mid ‘70s, did not need a lot of computing resources and provided reasonable results for the μA741. Since its introduction the Boyle model has been enhanced to add more accuracy.

Today, full transistor models simulate with speed and accuracy on modest home systems. The goal, when creating the SPICE model of the THS4001 high-speed monolithic operational amplifier, is to provide a model that will accurately simulate the actual device in a circuit. The model is derived from the full transistor model used internally by TI design. Simplifications are made to speed simulation time and various performance parameters are adjusted to match the model to measured device performance.

2 File Structure

The THS4001 SPICE model file, THS4001.lib, is written in ASCII file format and is compatible with a wide variety of computing platforms. The model is written in subcircuit format and has been tested with MicroSim® PSpice® release 8 and OrCAD® PSpice® version 9. It should be compatible with most SPICE2 and SPICE3 based simulation programs.

The THS4001.lib file contains two subcircuit definitions for the THS4001 – THS4001 and THS4001_NN. Each model begins with a .SUBCKT statement and ends with a .ENDS statement. The THS4001 model defines the NULL pins for external connection. The THS4001_NN (No Null) does not. Aside from this, the models are identical.

3 Performance

Typical performance parameters are modeled, and normal part-to-part variations experienced in real life cannot be expected. At frequencies above a few hundred MHz, performance becomes more and more dependent on parasitic devices associated with the circuit, and modeling suffers. Even though the model is fairly accurate, circuit performance should be verified with lab testing. An EVM is available upon request.

The graphs shown in Figures 1 thru 21, listed below, compare simulation results to measured device data. The simulation results are dashed lines and the measured data are solid lines. Device performance is either measured using the THS4001 EVM or taken from the data sheet. SPICE simulation was done using MicroSim® PSpice® release 8. Most of the parameters are measured using Vcc = ±15 V, and performance follows at lower voltages.

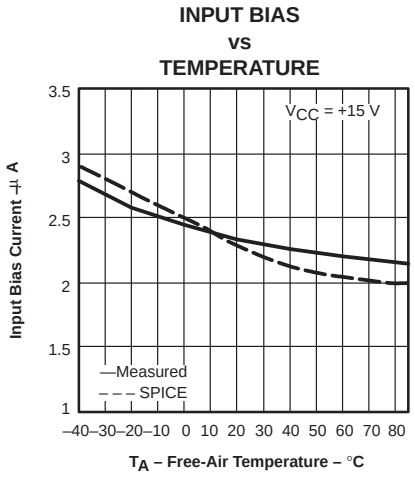


Figure 1

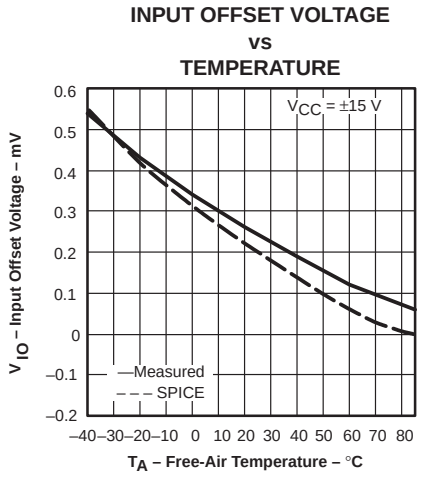


Figure 2

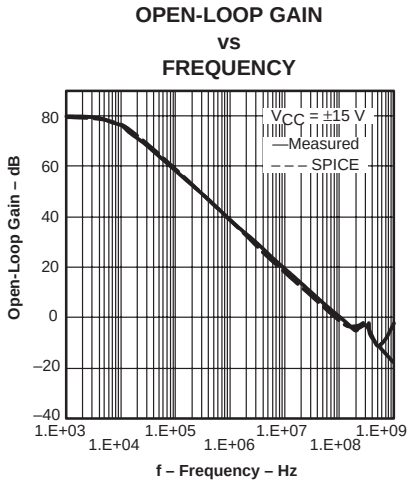


Figure 3

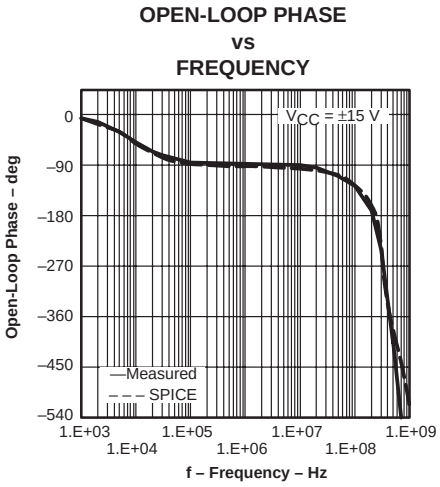


Figure 4

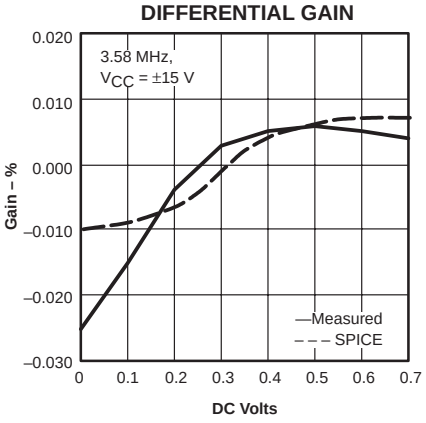
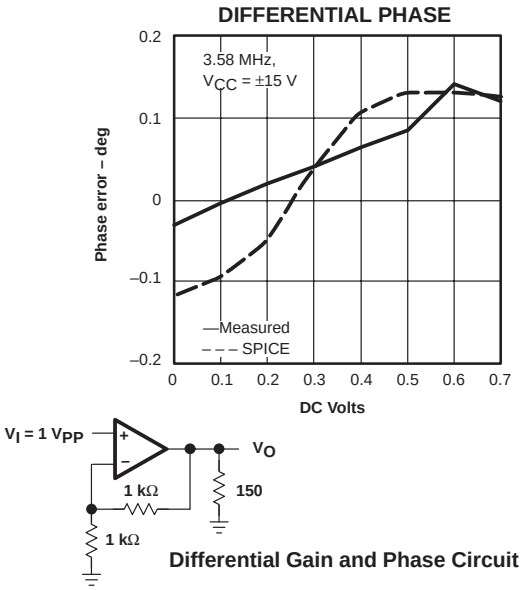
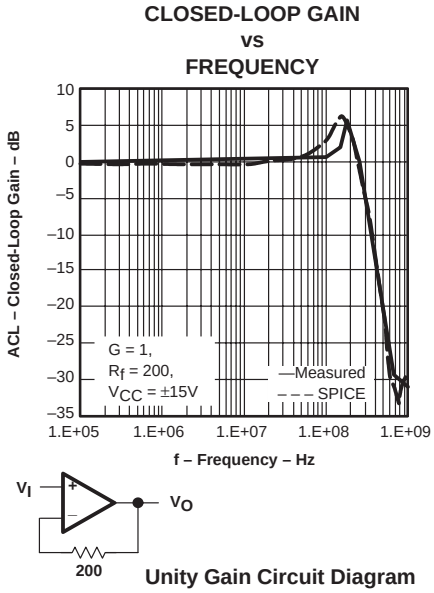


Figure 5



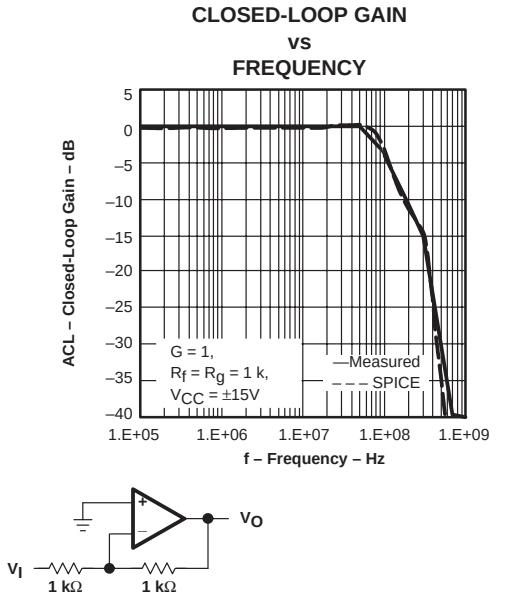
Differential Gain and Phase Circuit Diagram

Figure 6



Unity Gain Circuit Diagram

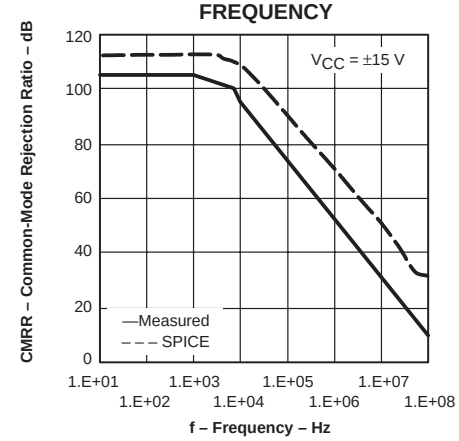
Figure 7

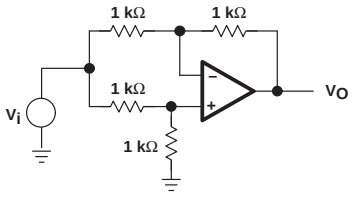


Inverting Gain-of-1 Circuit Diagram

Figure 8

COMMON-MODE REJECTION RATIO vs FREQUENCY



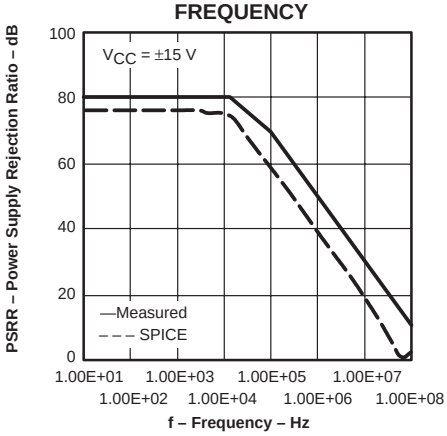


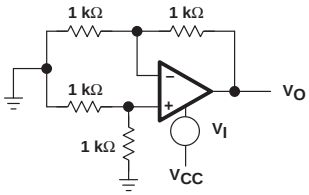
Common-Mode Rejection Ratio Circuit Diagram

NOTE: Offsetting one resistor by 0.02 Ω reduces the dc CMRR of the SPICE model to 102 dB

Figure 9

POWER SUPPLY REJECTION RATIO vs FREQUENCY

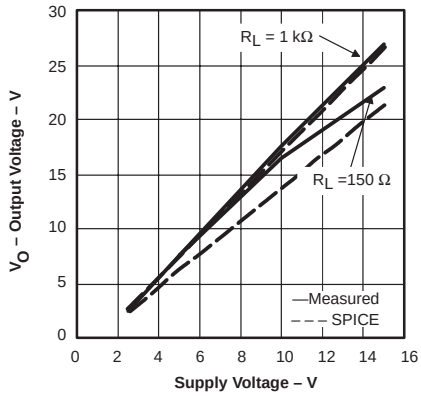


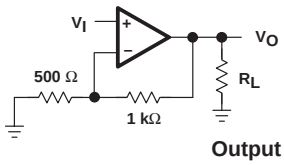


Power Supply Rejection Ratio Circuit Diagram

Figure 10

OUTPUT VOLTAGE vs SUPPLY VOLTAGE

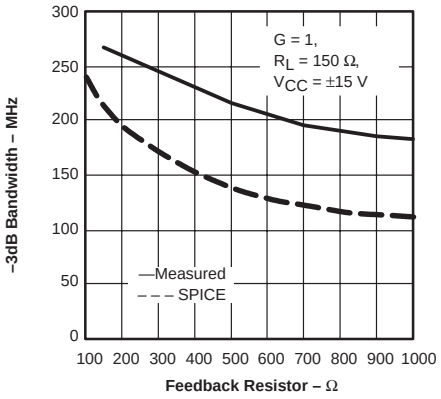


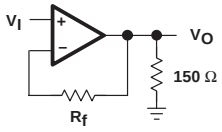


Output Voltage (pp) Circuit Diagram

Figure 11

–3dB BANDWIDTH vs FEEDBACK RESISTOR





–3dB Bandwidth vs Feedback Resistor Circuit Diagram

Figure 12

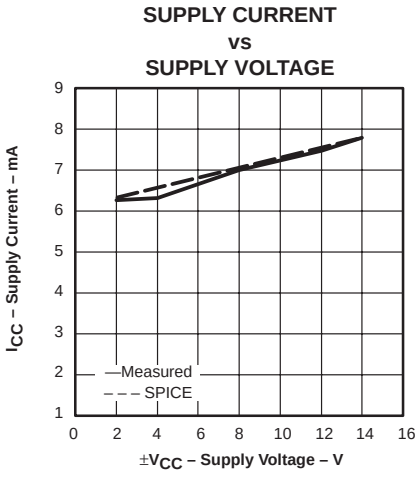


Figure 13

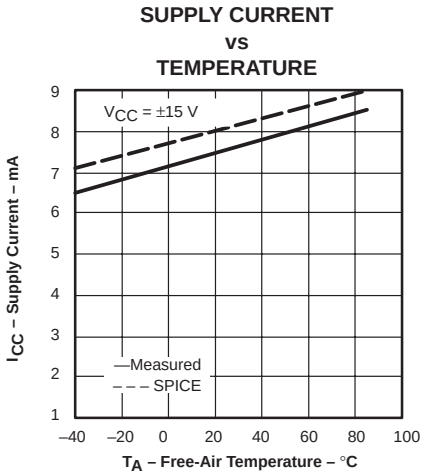


Figure 14

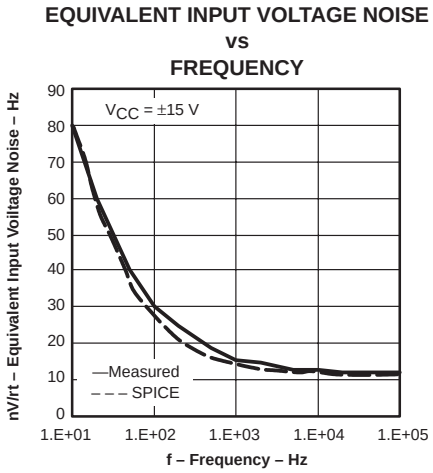


Figure 15

2nd HARMONIC vs FREQUENCY

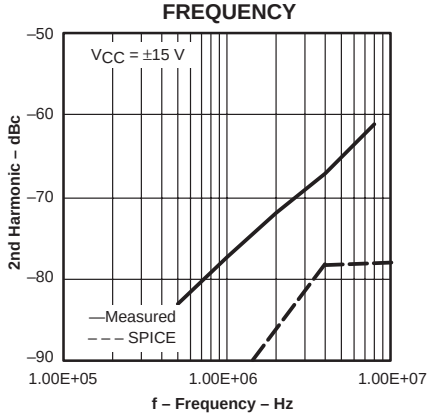
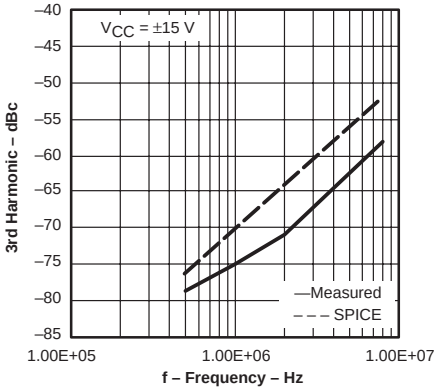
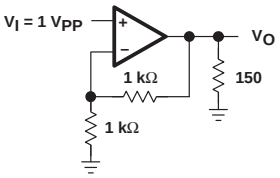


Figure 16

3rd HARMONIC vs FREQUENCY

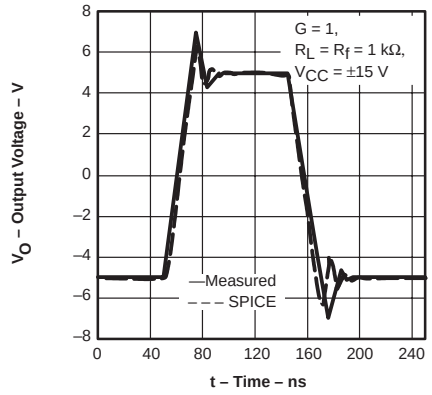


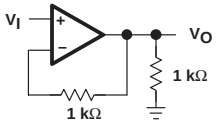


2nd and 3rd Harmonic vs Frequency Circuit Diagram

Figure 17

TRANSIENT RESPONSE vs TIME

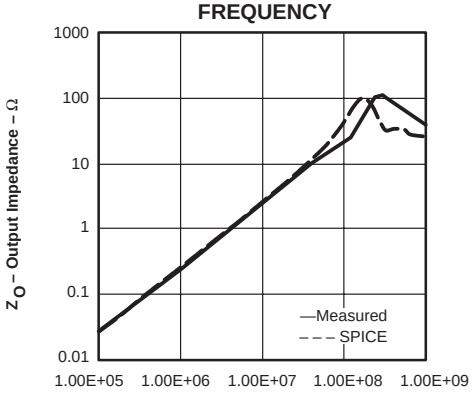


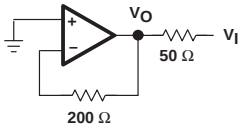


Transient Response Circuit Diagram

Figure 18

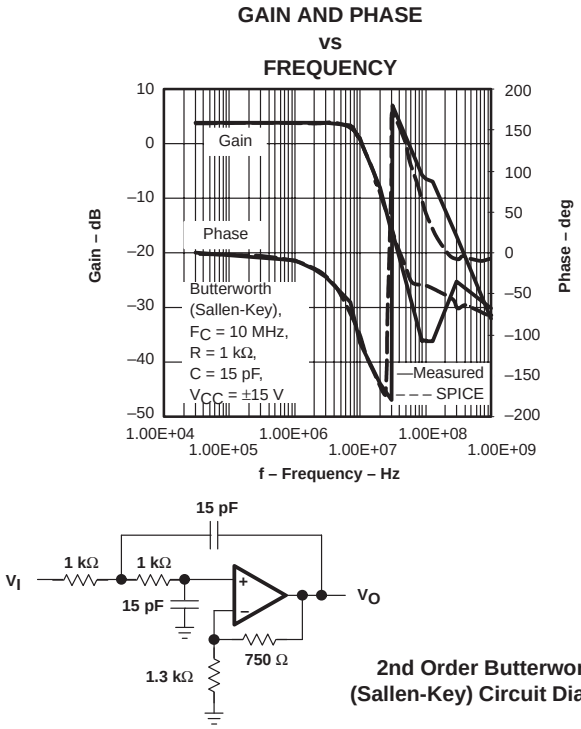
OUTPUT IMPEDANCE vs FREQUENCY





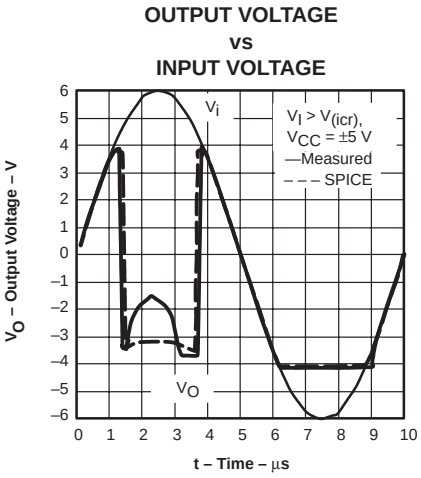
Z_O Output Impedance Circuit Diagram

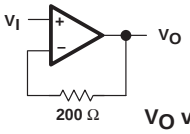
Figure 19



2nd Order Butterworth (Sallen-Key) Circuit Diagram

Figure 20





V_O vs V_I with V_I exceeding $V_{(icr)}$ Circuit Diagram

Figure 21

4 Schematic and Subcircuit Listing

The schematic representation of the model is shown in Figure 22 and the subcircuit listing follows. For brevity, the subcircuit listing has two .SUBCKT statements with the second one commented out:

```
.SUBCKT THS4001  1 2 3 4 5 6 7

*.SUBCKT THS4001_NN  1 2 3 4 5
```

This defines the model with external access to the null pins. To change to the model without access to the null pins, delete the * from the second line and add it to the front of the first line.

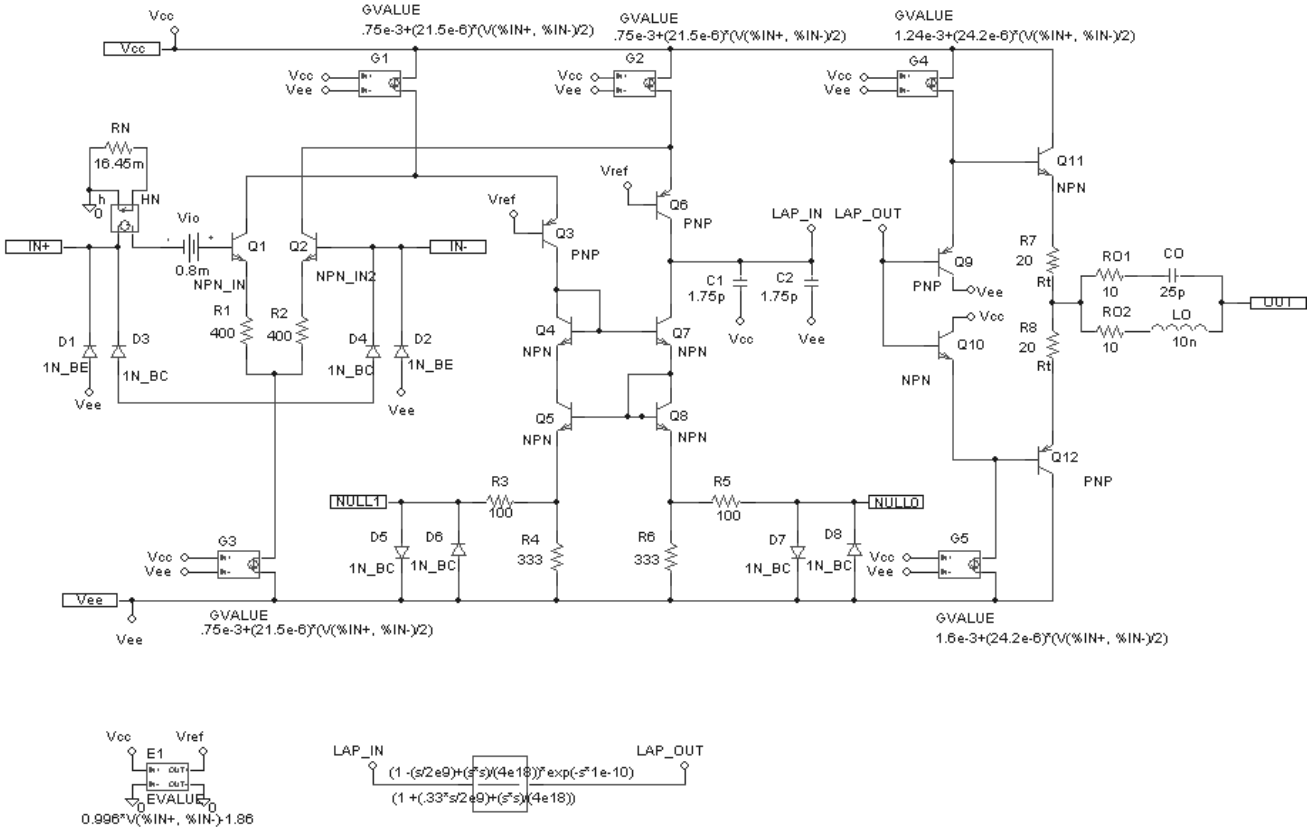


Figure 22. Model Schematic

4.1 Subcircuit Listing

```
* [Disclaimer] (C) Copyright Texas Instruments Incorporated 1999 All rights reserved
* non-exclusive, nontransferable license to use this SPICE Macro-model under the
* following terms. Before using this SPICE Macro–model, the user should read this
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* returned to Texas Instruments within 30 days. The user is granted this license only
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* applications but rights to derivative works and such modifications shall belong to
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* INCLUDING ANY LOST PROFITS OR OTHER INCIDENTAL, CONSEQUENTIAL, EXEMPLARY, OR PUNITIVE
* DAMAGES ARISING OUT OF THE USE OR APPLICATION OF THE SPICE Macro–model provided in
* this package. Further, Texas Instruments reserves the right to discontinue or make
* changes without notice to any product herein to improve reliability, function, or
* design. Texas Instruments does not convey any license under patent rights or any
* other intellectual property rights, including those of third parties.
*
* THS4001 SUBCIRCUIT
* HIGH SPEED MONLITHIC OPERATIONAL AMPLIFIER
* WRITTEN 10/6/99
* NULL PINS ARE ACTIVE IN THIS MODEL
* REFER TO THS4001_NN FOR MODEL WITH OUT NULL PINS
* TEMPLATE=X^@REFDES %IN+ %IN– %VCC+ %VCC– %OUT %NULL0 %NULL1 @MODEL
* CONNECTIONS:   NON–INVERTING INPUT
*                | INVERTING INPUT
*                | | POSITIVE POWER SUPPLY
*                | | | NEGATIVE POWER SUPPLY
*                | | | | OUTPUT
*                | | | | | NULL0
*                | | | | | | NULL1
*                | | | | | | |
.SUBCKT THS4001  1 2 3 4 5 6 7
*
* INPUT *
Q1          35 34 36 NPN_IN 1
Q2          12  2 32 NPN_IN2 1
R1          33 36  400
R2          33 32  400
* OFFSET *
Vio         34 14 1.1m
* NOISE *
RN           0 31  16.45m
HN          14  1 VHN 8
VHN         31  0 0V
* PROTECTION DIODES *
D1           4  1 D1N_BE
D2           4  2 D1N_BE
D3          13  1 D1N_BC
```

```
D4          13  2 D1N_BC
D5           7  4 D1N_BC
D6           4  7 D1N_BC
D7           6  4 D1N_BC
D8           4  6 D1N_BC
* SECOND STAGE *
Q3          11 41 35 PNP 1
Q4          11 11 10 NPN .5
Q5          10 38 37 NPN .5
Q6          40 41 12 PNP 1
Q7          40 11 38 NPN .5
Q8          38 38 09 NPN .5
C1           3 40  1.75p
C2           4 40  1.75p
R3          37  7  100
R4           4 37  333
R5           6 09  100
R6           4 09  333
* OUTPUT *
Q9           4 39 15 PNP 1
Q10          3 39 16 NPN 1
Q11          3 15 17 NPN 6
Q12          4 16 18 PNP 6
R7          19 17 Rt 20
R8          18 19 Rt 20
RO1         19 20  10
RO2         19 21  10
CO          20  5  25p
L_LO        21  5  10n
* BIAS SOURCES *
G1           3 35 VALUE= { .75e-3+(21.5e-6)*(V(3, 4)/2) }
G2           3 12 VALUE= { .75e-3+(21.5e-6)*(V(3, 4)/2) }
G3          33  4 VALUE= { .75e-3+(21.5e-6)*(V(3, 4)/2) }
G4           3 15 VALUE= { 1.24e-3+(24.2e-6)*(V(3, 4)/2) }
G5          16  4 VALUE= { 1.6e-3+(24.2e-6)*(V(3, 4)/2) }
E1          41  0 VALUE= { 0.996*V(3, 0)-1.86 }
* HIGH FREQUENCY SHAPING *
E_LAP  39  0 LAPLACE {V(40)}= {((1-(s/2e9)+(s*s)/(4e18))*exp(-s*1e-10))/((1
+(.33*s/2e9)+(s*s)/(4e18)))}

* MODELS *

.MODEL NPN_IN NPN
+ IS=170E-18 BF=400 NF=1 VAF=100 IKF=0.0389 ISE=7.6E-18
+ NE=1.13489 BR=1.11868 NR=1 VAR=4.46837 IKR=8 ISC=8E-15
+ NC=1.8 RB=251.6 RE=0.1220 RC=197 CJE=120.2E-15 VJE=1.0888 MJE=0.381406
+ VJC=0.589703 MJC=0.265838 FC=0.1 CJC=133.8E-15 XTF=272.204 TF=12.13E-12
+ VTF=10 ITF=0.294 TR=3E-09 XTB=1 XTI=5 KF=25E-15
.MODEL NPN_IN2 NPN
+ IS=170E-18 BF=390 NF=1 VAF=100 IKF=0.0389 ISE=7.6E-18
+ NE=1.13489 BR=1.11868 NR=1 VAR=4.46837 IKR=8 ISC=8E-15
+ NC=1.8 RB=251.6 RE=0.1220 RC=197 CJE=120.2E-15 VJE=1.0888 MJE=0.381406
+ VJC=0.589703 MJC=0.265838 FC=0.1 CJC=133.8E-15 XTF=272.204 TF=12.13E-12
+ VTF=10 ITF=0.294 TR=3E-09 XTB=1 XTI=5 KF=25E-15
.MODEL NPN NPN
```

```
+ IS=170E-18 BF=100 NF=1 VAF=100 IKF=0.0389 ISE=7.6E-18
+ NE=1.13489 BR=1.11868 NR=1 VAR=4.46837 IKR=8 ISC=8E-15
+ NC=1.8 RB=251.6 RE=0.1220 RC=197 CJE=120.2E-15 VJE=1.0888 MJE=0.381406
+ VJC=0.589703 MJC=0.265838 FC=0.1 CJC=133.8E-15 XTF=272.204 TF=12.13E-12
+ VTF=10 ITF=0.147 TR=3E-09 XTB=1 XTI=5
.MODEL PNP PNP
+ IS=296E-18 BF=100 NF=1 VAF=100 IKF=0.021 ISE=494E-18
+ NE=1.49168 BR=0.491925 NR=1 VAR=2.35634 IKR=8 ISC=8E-15
+ NC=1.8 RB=251.6 RE=0.1220 RC=197 CJE=120.2E-15 VJE=0.940007 MJE=0.55
+  VJC=0.588526 MJC=0.55 FC=0.1 CJC=133.8E-15 XTF=141.135 TF=12.13E-12
+ VTF=6.82756 ITF=0.267 TR=3E-09 XTB=1 XTI=5
.MODEL Rt RES TC1=-0.006
.MODEL D1N_BE D IS=10E-15 N=1.836 ISR=1.565e-9 IKF=.04417 BV=30 IBV=10E-6 RS=45
+ TT=11.54E-9 CJO=3E-12 VJ=.5 M=.3333
.MODEL D1N_BC D IS=10E-15 N=1.836 ISR=1.565e-9 IKF=.04417 BV=30 IBV=10E-6 RS=15
+ TT=11.54E-9 CJO=3E-12 VJ=.5 M=.3333
.ENDS
*
* THS4001 SUBCIRCUIT
* HIGH SPEED MONLITHIC OPERATIONAL AMPLIFIER
* WRITTEN 10/6/99
* NULL PINS ARE NOT MODELED
* REFER TO THS4001 FOR MODEL WITH NULL PINS
* TEMPLATE=X^@REFDES %IN+ %IN- %VCC+ %VCC- %OUT @MODEL
* CONNECTIONS:      NON-INVERTING INPUT
*                   | INVERTING INPUT
*                   | | POSITIVE POWER SUPPLY
*                   | | | NEGATIVE POWER SUPPLY
*                   | | | | OUTPUT
*                   | | | | |
*                   | | | | |
*                   | | | | |
.SUBCKT THS4001_NN  1 2 3 4 5
*
* INPUT *
Q1         35 34 36 NPN_IN 1
Q2         12  2 32 NPN_IN2 1
R1         33 36  400
R2         33 32  400
* OFFSET *
Vio        34 14 1.1m
* NOISE *
RN          0 31  16.45m
HN         14  1 VHN 8
VHN        31  0 0V
* PROTECTION DIODES *
D1          4  1 D1N_BE
D2          4  2 D1N_BE
D3         13  1 D1N_BC
D4         13  2 D1N_BC
D5          7  4 D1N_BC
D6          4  7 D1N_BC
D7          6  4 D1N_BC
D8          4  6 D1N_BC
```

```
* SECOND STAGE *
Q3          11 41 35 PNP 1
Q4          11 11 10 NPN .5
Q5          10 38 37 NPN .5
Q6          40 41 12 PNP 1
Q7          40 11 38 NPN .5
Q8          38 38 09 NPN .5
C1           3 40  1.75p
C2           4 40  1.75p
R3          37  7  100
R4           4 37  333
R5           6 09  100
R6           4 09  333
* OUTPUT *
Q9           4 39 15 PNP 1
Q10          3 39 16 NPN 1
Q11          3 15 17 NPN 6
Q12          4 16 18 PNP 6
R7          19 17 Rt 20
R8          18 19 Rt 20
RO1         19 20  10
RO2         19 21  10
CO          20  5  25p
L_LO        21  5  10n
* BIAS SOURCES *
G1           3 35 VALUE= { .75e-3+(21.5e-6)*(V(3, 4)/2) }
G2           3 12 VALUE= { .75e-3+(21.5e-6)*(V(3, 4)/2) }
G3          33  4 VALUE= { .75e-3+(21.5e-6)*(V(3, 4)/2) }
G4           3 15 VALUE= { 1.24e-3+(24.2e-6)*(V(3, 4)/2) }
G5          16  4 VALUE= { 1.6e-3+(24.2e-6)*(V(3, 4)/2) }
E1          41  0 VALUE= { 0.996*V(3, 0)-1.86 }
* HIGH FREQUENCY SHAPING *
E_LAP  39  0 LAPLACE {V(40)}= {((1-(s/2e9)+(s*s)/(4e18))*exp(-s*1e-10))/((1
+(.33*s/2e9)+(s*s)/(4e18)))}

* MODELS *

.MODEL NPN_IN NPN
+ IS=170E-18 BF=400 NF=1 VAF=100 IKF=0.0389 ISE=7.6E-18
+ NE=1.13489 BR=1.11868 NR=1 VAR=4.46837 IKR=8 ISC=8E-15
+ NC=1.8 RB=251.6 RE=0.1220 RC=197 CJE=120.2E-15 VJE=1.0888 MJE=0.381406
+ VJC=0.589703 MJC=0.265838 FC=0.1 CJC=133.8E-15 XTF=272.204 TF=12.13E-12
+ VTF=10 ITF=0.294 TR=3E-09 XTB=1 XTI=5 KF=25E-15
.MODEL NPN_IN2 NPN
+ IS=170E-18 BF=390 NF=1 VAF=100 IKF=0.0389 ISE=7.6E-18
+ NE=1.13489 BR=1.11868 NR=1 VAR=4.46837 IKR=8 ISC=8E-15
+ NC=1.8 RB=251.6 RE=0.1220 RC=197 CJE=120.2E-15 VJE=1.0888 MJE=0.381406
+ VJC=0.589703 MJC=0.265838 FC=0.1 CJC=133.8E-15 XTF=272.204 TF=12.13E-12
+ VTF=10 ITF=0.294 TR=3E-09 XTB=1 XTI=5 KF=25E-15
.MODEL NPN NPN
+ IS=170E-18 BF=100 NF=1 VAF=100 IKF=0.0389 ISE=7.6E-18
+ NE=1.13489 BR=1.11868 NR=1 VAR=4.46837 IKR=8 ISC=8E-15
+ NC=1.8 RB=251.6 RE=0.1220 RC=197 CJE=120.2E-15 VJE=1.0888 MJE=0.381406
+ VJC=0.589703 MJC=0.265838 FC=0.1 CJC=133.8E-15 XTF=272.204 TF=12.13E-12
+ VTF=10 ITF=0.147 TR=3E-09 XTB=1 XTI=5
```

```
.MODEL PNP PNP
+ IS=296E–18 BF=100 NF=1 VAF=100 IKF=0.021 ISE=494E–18
+ NE=1.49168 BR=0.491925 NR=1 VAR=2.35634 IKR=8 ISC=8E–15
+ NC=1.8 RB=251.6 RE=0.1220 RC=197 CJE=120.2E–15 VJE=0.940007 MJE=0.55
+  VJC=0.588526 MJC=0.55 FC=0.1 CJC=133.8E–15 XTF=141.135 TF=12.13E–12
+ VTF=6.82756 ITF=0.267 TR=3E–09 XTB=1 XTI=5
.MODEL Rt RES TC1=–0.006
.MODEL D1N_BE D IS=10E–15 N=1.836 ISR=1.565e–9 IKF=.04417 BV=30 IBV=10E–6 RS=45
+ TT=11.54E–9 CJO=3E–12 VJ=.5 M=.3333
.MODEL D1N_BC D IS=10E–15 N=1.836 ISR=1.565e–9 IKF=.04417 BV=30 IBV=10E–6 RS=15
+ TT=11.54E–9 CJO=3E–12 VJ=.5 M=.3333
.ENDS
*$
```

5 Note About Building a Symbol

The first line of the subcircuit definition – .SUBCKT THS4001 1 2 3 4 5 6 7 or – .SUBCKT THS4001_NN 1 2 3 4 5 – defines the name of the model and the subcircuit nodes available for external connection. When creating a symbol in PSpice®, the subcircuit node assignments need to match the TEMPLATE device property, and the MODEL value must equal the model name. The comment line in the file * TEMPLATE=X^@REFDES %IN+ %IN- %VCC+ %VCC- %OUT %NULL0 %NULL1 @MODEL or * TEMPLATE = X^@REFDES %IN+ %IN- %VCC+ %VCC- %OUT @MODEL gives the proper value for the TEMPLATE property. This associates the symbol pin names with subcircuit nodes available for external connections. The symbol pin numbers are used for packaging purposes and are not used for simulation. Using the forgoing, results in the associations shown in Table 1.

Table 1. Subcircuit Node to Symbol Pin Summary

SUBCIRCUIT NODE	THS4001 SYMBOL PIN NAME	THS4001_NN SYMBOL PIN NAME
1	IN+	IN+
2	IN–	IN–
3	Vcc+	Vcc+
4	Vcc-	Vcc-
5	OUT	OUT
6	NULL0	Not Used
7	NULL1	Not Used

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