TRF7960A Firmware Design Hints

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ABSTRACT

This application report is a reference for the firmware developer using TRF7960A in conjunction with microcontroller (for example, an MSP430™ or ARM™ device). This document supersedes *TRF796x Software Design Hints* (SLOA153).

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TRF796x and TRF7960A Firmware Hints Reference Table

Table 1. Firmware Hints Reference Table

	Item	TRF7960A	TRF7960	TRF7961
#1	ISO15693 only - Direct command (0x14) 'Transmit next slot'		✓	✓
#2	Missing IRQ	✓	✓	✓
#3	Lost IRQ	✓	✓	✓
#4	Wrong data due to overshoots	✓	✓	
#5	ISO14443A decoder		✓	
#6	Tags that do not follow the 14443A Layer 4 framing		✓	
#7	SPI with SS	✓	✓	✓

1   ISO15693 Only – Direct Command (0x14) EOF/TX Next Slot

Description

Sending of 'Transmit next slot' direct command (0x14) can happen only once (ISO15693).

Workaround

Before sending the 'Transmit next slot' direct command, the 'Reset' direct command has to be send. This is only used in ISO15693 Inventory command (with 16 time slots). ISO 15693 'Write Single Block' and 'Lock Block' commands are affected also if the 'Option' bit is set.

2   Missing IRQ

Description

The device does not send (on pin13) any interrupt requests on certain condition. The chip can go to a state where the sending of additional interrupts during RX or TX is stopped. This happens when the Stop Condition is exactly aligned with the byte boundary on TX data.

Workaround

The loading and reading of the FIFO should be coded in such a way, that the Stop Condition does not fall directly on the TX byte boundary.

3   Lost IRQ

Description

Lost IRQ if the end of RX IRQ is to come exactly at the same time the IRQ register is being read. See also #6.

Workaround

Add additional checks to retrieve the RX data in case the IRQ is suppressed by a coinciding read operation.

4   Wrong Data Due to Overshoots

Description

The ISO14443A 106-kbps decoder gives wrong data in certain condition. When the analog front end filter overshoots, the digitizer might produce a rising edge on the subcarrier data. If this occurs within a small time window, the decoder produces false data. This happens extremely rarely and is dependent on the antenna and filter characteristics.

Workaround

Switch to PM channel or adjust gain to avoid overshoots in the analog filter.

5 ISO14443A Decoder

Description

ISO14443A subcarrier decoded incorrectly – reading holes.

Workaround

Adjust gain setting of main RX channel; repeat reading until correct data results. (This might require additional time.)

6 Tags That Do Not Follow ISO14443A Layer 4 Framing

Description

When a transmit frame starts with the code 0x93, 0x95, or 0x97, the reply is not correctly framed. This happens because the TRF796x devices have an automatic anti-collision broken byte framing system that is activated with the 0x93, 0x95, or 0x97 code.

Workaround

Use TRF7960 Direct Mode.

7 Special SPI With SS Handling

7.1 SPI With SS Pin Only – No High Impedance

Description

Serial interface with SS pin only, the interface does not go to high impedance when SS is high. It is not possible to multiplex the serial port interface lines.

Workaround

An external three-state buffer must be used if the chip is connected to a serial bus and the interface lines are multiplexed.

7.2 SPI With SS Pin Only – Direct Commands

Description

Serial interface with SS pin only, the direct commands are not executed if they are the last operation in the SPI communication.In the SPI interface with SS pin the Stop condition clock pulse is missing (compared to the parallel interface and SPI without SS pin). Some operations are relying on this clock and they do not work as expected.

Workaround

If a direct command is the last operation in the SPI communication, the SS pin goes high. Afterward, an additional clock pulse has to be sent.

7.3 SPI With SS Pin Only – IRQ Status Bit

Description

Serial interface with SS pin only, IRQ status bits are not cleared after the IRQ Status register (0x0C) is read.

Workaround

A dummy read has to be made after reading the 'IRQ status' register (0x0C). This can be done in non-continuous or continuous mode. In continuous mode only 8 clock pulses are needed. In non continuous mode 16 clock pulses are needed: 8 for address and 8 for data.

7.4 *SPI With SS Pin Only − No TX If Single Bit in FIFO*

Description

Serial interface with SS pin only, the chip does not start with transmission if only one byte is loaded to the FIFO.

Workaround

The microcontroller must load an additional byte to the FIFO. The chip transmits only one byte on the TX if the "Number of complete bytes" in the registers 0x1D and 0x1E is 1.

7.5 *SPI With SS Pin Only − Clock Polarity Change*

Description

DATA_CLK clock polarity must be switched when FIFO read operation (single or continues) is executed. During SPI data transmission MOSI line is valid on rising edge, MISO line is valid on falling edge of Data CLK signal.

Workaround

Firmware need to switch clock polarity between FIFO writes and reads.

7.6 *SPI With SS Pin Only − IRQ Status Register Reset*

Description

The IRQ Status register (0x0C) is not automatically cleared after reading.

Workaround

Dummy register read is required to clear the content of the IRQ Status Register and drive the IRQ line to low.

7.7 *SPI With SS Pin Only − Single-Byte Direct Commands*

Description

All single byte direct commands need an additional CLK cycle to work.

Workaround

All direct command functions need to have an additional DATA_CLK cycle before Slave Select I line goes high.

7.8 SPI With SS Pin Only − Some Registers Do Not Take Default Values

Description

Some of the registers do not take the default values when the appropriate protocol is chosen in the ISO Control register.

Workaround

Manually program the default settings into the TRF796x during initialization.

Fourther information concerning the SPI can be found in *Using the SPI interface with the TRF7960* (SLOA140).

Table 2. Known Limitations With Specific Tags

No.	Tag Type	Problem	Workaround
T1	MIFARE™ ultralight	The 4-bit ACK and NAK reply can not be decoded with the integrated decoder/framer system. The 4-bit ACK is not according the standard ISO 14443A, so the internal data framing reports an error and must be by-passed.	Direct mode
T2	MIFARE classic (standard)	The parity check fails with the encrypted frames as the MIFARE standard encrypts also the parity bit.	Direct mode
T3	Tags that do not follow the ISO14443A Layer 4 framing	When a transmit frame starts with the code 0x93, 0x95, or 0x97, the reply is not correctly framed. This happens because the TRF796x devices have an automatic anticollision broken byte framer that is activated with the 0x93, 0x95 or 0x97 code.	Direct mode
T4	Cryptography cards such as JCOP or DESFire™	Using a cryptography card such as JCOP or DESFire at close proximity (<1 cm) can cause a wrong collision error detection.	The reason is the 'calculation noise' emitted by the card which can be suppressed if the gain is drastically reduced. We proposed to use addition gain reduction enabled by test register.
T5	ISO15693 cards requiring a slot delimiter (EOF)	There are ISO15693 cads on the market requiring a slot delimiter (EOF).	A dedicated MCU timer must be used to generate the 37.76-µs timing grid.

Table 3. TRF7960A Special Functions Register (0x10)

Bit	Bit Name	Function	Comment
B7		RFU	RFU
B6		RFU	RFU
B5		RFU	RFU
B4	next_slot_37us	Sets the time grid for next slot command in ISO15693	0 = 18.88us 1 = 37.77us
B3		RFU	RFU
B2	4_bit_RX	Enable 4-bit replay (for example, ACK or NCK used by some cards such as MIFARE Ultralight)	0 = normal receive 1 = 4-bit receive
B1	14_anticoll	Disable anti-collision frames for 14443A (this bit should be set to 1 after anti-collision is finished)	0 = anti-collision framing (0x93, 0x95, 0x97) 1 = normal framing (no broken bytes)
B0	col_7_6	Selects the number of subcarrier pulses that trigger collision error in ISO14443A 106 kbps	0 = 7 subcarrier pulses 1 = 6 subcarrier pulses

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