

THS4271EVM-UG

Unity Gain

User's Guide

DEVICE	EVM TITLE	USER'S GUIDE	DESCRIPTION	SHUTDOWN
THS4271	THS4271EVM-UG	THS4271 Unity Gain EVM	Noninverting unity gain configuration only	No
THS4271	THS4271EVM	THS4271/75EVM	Configurable for gains $\geq +2/-1$	No
THS4275	THS4275EVM	THS4271/75EVM	Configurable for gains $\geq +2/-1$	Yes

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It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide. The input supply voltage ($\pm V_S$) should be no greater than ± 7.5 V for dual supply (V_S should be no greater than 15 V for single supply operation). The differential input signal (V_{ID}) should be no greater than ± 3 V. The output current (I_O) should be no greater than 100 mA.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C . The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, refer to SSYA008.

Related Documentation From Texas Instruments

The URL's below are correct as of the date of publication of this manual. Texas Instruments applications apologizes if they change over time.

- THS4271/THS4275 data sheet (SLOS397)
- Application report (SLMA002), *PowerPAD Thermally Enhanced Package*, <http://www-s.ti.com/sc/psheets/slma004/slma002.pdf>
- Application report (SLMA004), *PowerPAD Made Easy*, <http://www-s.ti.com/sc/psheets/slma004/slma004.pdf>
- Application report (SSYA008), *Electrostatic Discharge (ESD)*, <http://www-s.ti.com/sc/psheets/ssya008/ssya008.pdf>
- Application report (SLOA102), *High Speed PCB Layout Tips*, <http://www-s.ti.com/sc/psheets/sloa102/sloa102.pdf>

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Introduction and Description

This EVM provides a platform for testing the THS4271 in 8-pin LLP (DRB) package in a noninverting, unity gain mode. It contains the high-speed op amp, a number of passive components, and various features and footprints that enable the user to experiment, test, and verify various operational amplifier circuit implementations.

The THS4271 unity gain EVM was developed to reduce peaking caused by lead inductance in the feedback path, which proved to be excessive in a more general layout. This EVM is designed to minimize peaking in the unity gain configuration. Each pad and trace on a PCB has an inductance associated with it, when in conjunction with the inductance associated with the package may cause peaking in the frequency response, hence, cause the device to become unstable.

Minimizing the inductance in the feedback path is critical for reducing the peaking of the frequency response in unity gain. The recommended maximum inductance allowed in the feedback path is 4 nH. This can be calculated by using the following equation:

$$L(\text{nH}) = K\ell \left[\ln \frac{2\ell}{W + T} + 0.223 \frac{W + T}{\ell} + 0.5 \right]$$

Where:

W = Width of trace

ℓ = Length of the trace

T = Thickness of the trace

K = 5.08 nH/inch

K = 0.2 nH/mm for Getek 4.2 epoxy polyphenylene oxide resin.

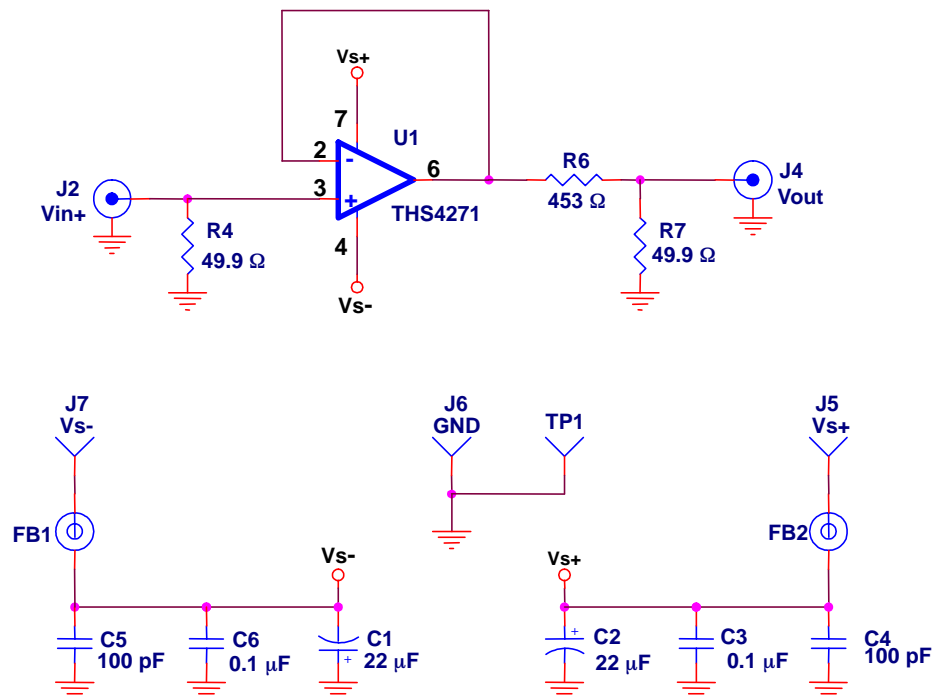
Dimensions are in inches unless otherwise specified.

1.1 Evaluation Schematic

As delivered, the EVM has a fully functional example circuit—just add power supplies, a signal source, and monitoring instrument. See Figure 1–1 for a complete schematic diagram. EVM features include:

- Wide operating supply voltage range: single supply 4.5 V to dual supply ± 7.5 V operation (see the device data sheet). Single supply operation is obtained by connecting both J6 (GND) and J7 (VS-) to ground.
- Nominal 50- Ω input impedance (R4). Termination can be configured according to the application requirement.
- 50- Ω impedance traces on Vin+, and the Vin- to Vout connection (see Figure 4-1—the vias provide the impedance)
- Convenient GND test point (TP1).
- 453- Ω series matching resistor (R6)—produces a 500- Ω load in combination with resistor R7. 500 Ω is the standard data sheet load impedance.
- Power supply ripple rejection capacitors (C1 and C2).
- Decoupling capacitors (C3, C4, C5, C6).
- Power PAD™ heatsinking capability.
- A good example of high-speed amplifier PCB design and layout.

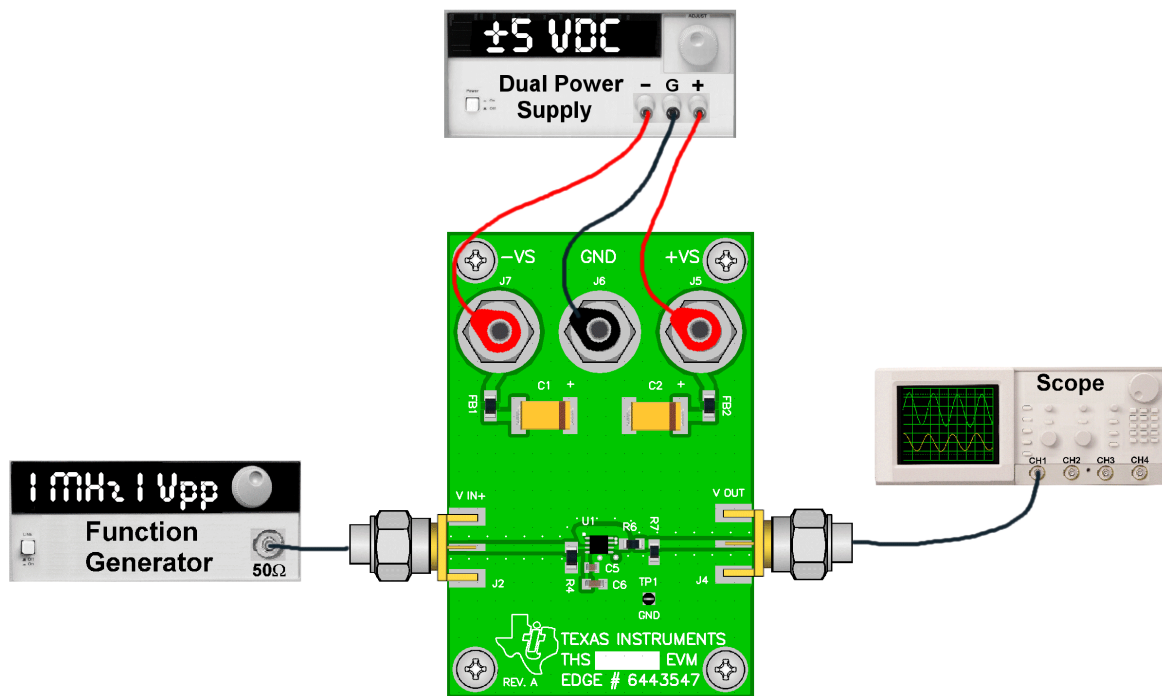
Figure 1-1. Schematic of the THS4271EVM-UG Unity Gain



Using the EVM

Figure 2-1 shows how to connect power supplies, signal source and monitoring instrument. It is recommended that the user connect the EVM as shown to avoid damage to the EVM or the op amp installed on the board.

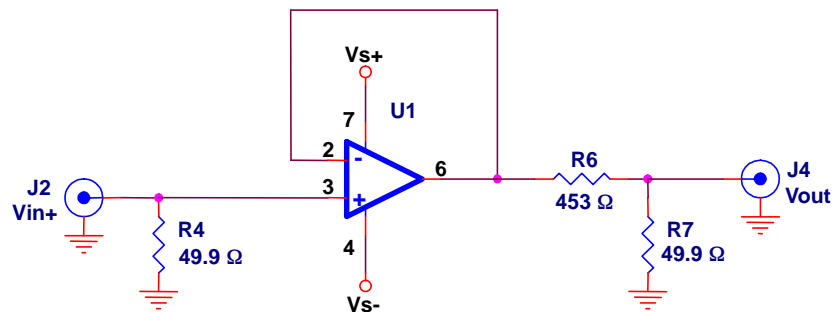
Figure 2-1. Test Equipment Connections



Example applications are presented in this chapter. These applications demonstrate the most popular circuits, but many other circuits can be constructed. The purpose of the EVM board is for the user to experiment with different circuits, exploring new and creative design techniques, which is the function of an evaluation board.

3.1 Default Configuration

Figure 3-1. Default Configuration



Note: This schematic reflects the default THS4271EVM-UG unity gain configuration. Power supply decoupling not shown.

The EVM output provides a 500- Ω load to the output of the EVM to provide optimum performance (per the data sheet). The load is implemented as a 453- Ω resistor (R6) in series with the output to J4 (V_{out}), and a 49.9- Ω output load resistor (R7) from J4 to ground.

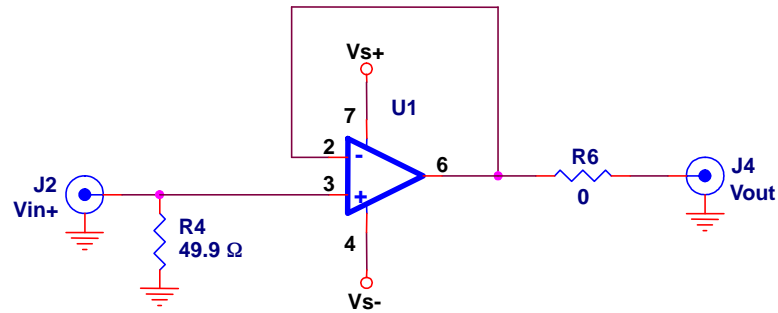
The gain measured from J2 to the output of the amplifier (pin 6) is 1. However, the interaction between R6 and R7 causes the output at J4 to be attenuated by 10:1.

When the EVM is monitored with a high input impedance instrument, R7 can remain on the board—however, when the EVM is monitored with an instrument that has an input impedance of 50 Ω , it is recommended that R7 be removed.

If the user provides an external load, R7 may be removed, and R6 replaced with a 0- Ω jumper as shown in Figure 3-2. The EVM then provides a voltage gain of 1 (0 dB) at the output connector J4.

Changing R6 to 49.9 Ω allows the EVM to connect to a 50- Ω load. This amplifier is designed to attain optimum performance driving 500- Ω loads, but 100- Ω loads can be driven. See the data sheet for device characteristics.

Figure 3-2. Noninverting Gain Stage



Note: Power supply decoupling not shown.

EVM Hardware Description

This chapter describes the EVM hardware. It includes the EVM parts list, and printed-circuit board layout.

Table 4-1. THS4271EVM-UG Unity Gain Bill of Materials

Item	Description	SMD Size	Reference Designator	PCB QTY	Manufacturer's Part Number	Distributor's Part Number
1	Bead, ferrite, 3A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R-00	(Digi-Key) 240-1010-1-ND
2	Capacitor, 22 μ F, tantalum, 25 V, 10%	D	C1, C2	2	(AVX) TAJD226K025R	(Garrett) TAJD226K025R
3	Capacitor, 100 pF, ceramic, 5%, 150 V	AQ12	C4, C5	2	(AVX) AQ12EM101JAJME	(TTI) AQ12EM101JAJME
4	Capacitor, 0.1 μ F, ceramic, X7R, 50 V	0805	C3, C6	2	(AVX) 08055C104KAT2A	(Garrett) 08055C104KAT2A
5	Resistor, 49.9 Ω , 1/8 W, 1%	0805	R7	1	(PHYCOMP) 9C08052A49R9FKHFT	(Garrett) 9C08052A49R9FKHFT
6	Resistor, 453 Ω , 1/8 W, 1%	0805	R6	1	(PHYCOMP) 9C08052A4530FKHFT	(Garrett) 9C08052A4530FKHFT
7	Resistor, 49.9 Ω , 1/4 W, 1%	1206	R4	1	(PHYCOMP) 9C12063A49R9FKRFT	(Garrett) 9C12063A49R9FKRFT
8	Test point, black		TP1	1	(Keystone) 5001	(Allied) 839-3601
9	Jack, banana receptacle, 0.25" diameter hole		J5, J6, J7	3	(HH Smith) 101	(Newark) 35F865
10	Connector, edge, SMA PCB jack		J2, J4	2	(Johnson) 142-0701-801	(Allied) 528-0238
11	Standoff, 4-40 hex, 0.625" length			4	(Keystone) 1808	(Newark) 89F1934
12	Screw, Phillips, 4-40, .250"			4	SHR-0440-016-SN	
13	IC, THS4271		U1	1	(TI) THS4271DRB	
14	Board, printed-circuit			1	(TI) Edge #6443547 Rev.A	

Figure 4-1. Board Layout Views

