TRF7970A Silicon Errata

This document describes the known exceptions to the functional specifications for the device.

Contents

1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all devices. Each commercial family member has one of two prefixes: XTRF or TRF (for example, TRF7970A).

These prefixes represent evolutionary stages of product development from engineering prototypes (XTRF) through fully qualified production devices or tools (TRF).

Device development evolutionary flow of the TRF7970A:

XTRF — Experimental device that is not necessarily representative of the final device's electrical specifications.

TRF — Fully qualified production device.

XTRF devices are shipped against the following disclaimer:

"Developmental products are intended for internal evaluation purposes.

TRF devices have been fully characterized, and the quality and reliability of the device have been fully demonstrated. TI's standard warranty applies.

Predictions show that prototype devices (XTRF) have a greater failure rate than the standard production devices. Texas Instruments recommends not to use these devices in any production system."

2 Revision Identification

Figure 1 provides an example of the device marking. The device revision can be determined by the symbols marked on the top of the device.

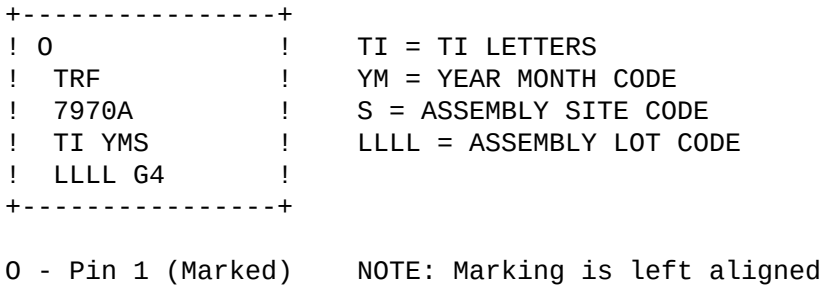

Figure 1. Package Markings

3 Known Design Exceptions to Functional Specifications

Device#B01 *In Reader/Writer communication mode at 106 kbps, 1-etu duration outside ISO 14443 specification.*

Expected Behavior The bit duration (1 etu) as defined by ISO14443A/NFC-A air interface is supposed to be 9.44 µs (±0.5%).

Issue The device fails this criterion. Measuring this value (for example, for EMVCO compliance testing), the 1 etu is approximately ≥9.587 µs and, hence, outside the given specification limits.

Condition The device operates as ISO14443A/NFC-A reader/writer and as NFC-A Peer to Peer (P2P) Initiator.

Implications The device fully supports ISO14443A communication. The device fail the EMVCO compliance testing as the 1-etu value is outside given range.

Workaround There is no workaround identified

Device#B02 *FIFO not accessible in SPI without SS mode.*

Expected Behavior FIFO is accessible in all SPI modes

Issue The TRF7970A was supposed to have three methods of communication with a microcontroller (MCU): Parallel Mode, Serial Peripheral Interface (SPI) with Slave Select (SS), and SPI without SS.

In the SPI operation mode without SS, the TRF7970A registers can be read from and written to; however, the FIFO is not accessible.

Condition SPI operation mode without SS

Implications FIFO is not accessible.

Workaround The following workarounds exist:

1. Use SPI with SS.
2. Use Direct Mode 1.
   This requires using I/O_5, MOD pin, and dedicated MCU firmware for data encode and decode.
3. Use Direct Mode 0.
   This requires using MOD pin and dedicated MCU firmware.

Device#B03 *NFC-F Peer-to-Peer Mode Preamble*

Expected Behavior For some standards, the preamble is defined to be exactly 48 bits long.

Issue ECMA-340 and ISO/IEC 18092 defines the preamble for initiator and target in the start of the polling or response frame, or after the delay between consecutive frames. A minimum of 48 bits of Manchester-encoded logical zeros is defined.

The Sony FeliCa Card and NFC Forum documents based on JIS X 6319-4 show this preamble to be exactly 48 bits long.

The TRF7970A was designed to transmit a 56-bit preamble.

Condition The device is in Peer-to-Peer mode. The behavior is not dependent on any particular physical condition.

Implications The device fully supports the communication to Sony FeliCa Cards and hence to NFC-F products based on JIS X 6319-4. The 56-bit preamble does not allow compliance to the latest NFC-FeliCa definition due to the later extension of the standard.

Workaround There is no workaround identified.

Device#B04 *TX FIFO water level IRQ in ISO14443A Card Emulation Mode*

Expected Behavior FIFO water level IRQ signals the FIFO data string status in transmit and receive mode.

Issue The FIFO water level IRQ does not work in transmit mode, but it does work in receive mode. If a long data string (more than 127 byte) needs to be transmitted, the FIFO water level IRQ does not provide the intended warning to reload the FIFO.

Condition The device is in NFC-A Card Emulation Mode. The behavior is not dependent on any particular physical condition.

Implications The device FIFO water level IRQ does not provide the intended warning to reload the FIFO. For long data strings, the FIFO reload procedure cannot use the device IRQ signal.

Workaround For long data strings, the host CPU needs to read out the FIFO level regularly. Dedicated host software is needed to continuously fill up the FIFO.

Device#B05 *NFC A Card Emulation Mode Auto SDD (SAK Response)*

Expected Behavior SAK response should set NFC compliant bit in the device to be compliant with the latest NFC standard.

Issue SAK command response is not able to set NFC compliant bit.

Condition The device is in NFC-A Card Emulation Mode. The behavior is not dependent on any particular physical condition.

Implications The device is ISO14443A compliant, however, no dedicated bit to signal NFC compliance exists due to the later extension of the ISO standard.

Workaround Operate the device in Direct Mode and implement anti-collision for ISO14443A in firmware.

Device#B06 *Parity error indication in IRQ status register (0x0C) Bit 3*

Expected Behavior	When parity error is sent back as part of an ISO14443A or NFC-A transponder response, Bit 3 in register 0x0Ch should be set.
Issue	The device is supposed to indicate a parity error by setting bit 3 of the IRQ status register when operating as a reader/writer or initiator. Instead, a parity error is indicated as a CRC error (bit 4 in the IRQ status register 0x0Ch).
Condition	The behavior is not dependent on any particular device condition.
Implications	No parity error indication during EMVCoL1 Digital or NFC Wave1 compliance testing.
Workaround	Use the device in Direct Mode 0. This requires using the MOD pin and dedicated MCU firmware.

Device#B07 *RX FIFO overflow error indication in FIFO Status register (0x1C) Bit 7*

Expected Behavior	When the FIFO has more than 127 bytes stored in it, Bit 7 in register 0x1C should be set.
Issue	The device is supposed to indicate a FIFO overflow error by setting bit 7 of the FIFO status register when the FIFO is filled with more than 127 bytes when receiving a message from another transceiver. If the FIFO is read out by from the MCU while the FIFO is being filled with another transceiver's command which is larger than 127 bytes, Bit 7 of the FIFO Status Register might be set.
Condition	The TRF7970A's FIFO is being written with a command with size larger than 127 bytes, from another transceiver. The behavior is not dependent on any particular physical condition.
Implications	Erroneous software behavior not receiving commands completely.
Workaround	The firmware must mask Bit 7, when reading the FIFO Status Register (0x1C) and validate the command size in firmware based on the specification used.

Device#B08 *NFC Target Detection Level Register (0x18) has nonzero value at power up*

Expected Behavior	At power up, register 0x18 should have a default value 0x00.
Issue	The device is supposed to have a default value of 0x00, but certain cases may cause a nonzero value to be loaded. In the case where a different value is loaded, the TRF7970A or TRF7964A device will indicate 0 bytes in the FIFO Status Register(0x1C) after the RX complete interrupt (after completing a transmit command cycle).
Condition	The device can randomly exhibit this issue directly after power up while other times working properly at power up.
Implications	Erroneous behavior which results in not receiving data in the FIFO.
Workaround	The firmware must write register 0x18 with a value of 0x00 at power up as part of the firmware initialization procedure to avoid issues.

Device#B09 *RF Collision Avoidance Direct Commands do not behave as expected*

Expected Behavior

The RF collision avoidance direct commands (listed below) should be able to be used to reliably detect any active 13.56-MHz RF fields within proximity of the TRF7970A.

- 0x04 Perform RF Collision Avoidance
- 0x05 Perform Response RF Collision Avoidance
- 0x06 Perform Response RF Collision Avoidance (n = 0)

Issue

The RF collision avoidance direct commands (0x04 to 0x06) are not compliant with the ISO specifications.

Condition

When issuing the RF collision avoidance direct commands (0x04 to 0x06), they do not properly transmit the expected packets.

Implications

The RF collision avoidance direct commands cannot be relied on to complete RF collision avoidance before enabling the TRF7970A RF field.

Workaround

Perform RF collision avoidance by using the RSSI measurement features of the TRF7970A. The steps to do this are:

1. Write a 0x02 (3-VDC operation) or 0x03 (5-VDC operation) to the Chip Status Control register (0x00) to disable the transmitter and enable the receiver.
2. Send a Test External RF direct command (0x19).
3. Delay 50 µs to allow the transceiver to measure the field strength and latch the value into the RSSI register.
4. Read the RSSI Levels and Oscillator Status register (0x0F).
5. If the active channel RSSI value (bits 2:0) is greater than 0, remain in target mode for a predetermined time (number of milliseconds).
6. If the active channel RSSI value (bits 2:0) is equal to 0, enter initiator or target mode for active or passive communication.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from April 16, 2015 to December 16, 2016	Page
• Added Device#B09	5

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