APPLICATION NOTE

THE UC3823A,B AND UC3825A,B ENHANCED GENERATION OF PWM CONTROLLERS

BILL ANDREYCAK

ABSTRACT

This application note will highlight the enhancements incorporated in four new PWM control ICs, the UC3823A, UC3823B, UC3825A and UC3825B devices. Based upon the industry standard UC3823 and UC3825 controllers, this advanced generation features several key improvements in protection and performance over their predecessors. Newly developed techniques such as leading edge blanking of the current sense input and full cycle soft start protection following a fault have been incorporated into the design. Numerous enhancements to existing standard functions and features have also been made.

INTRODUCTION

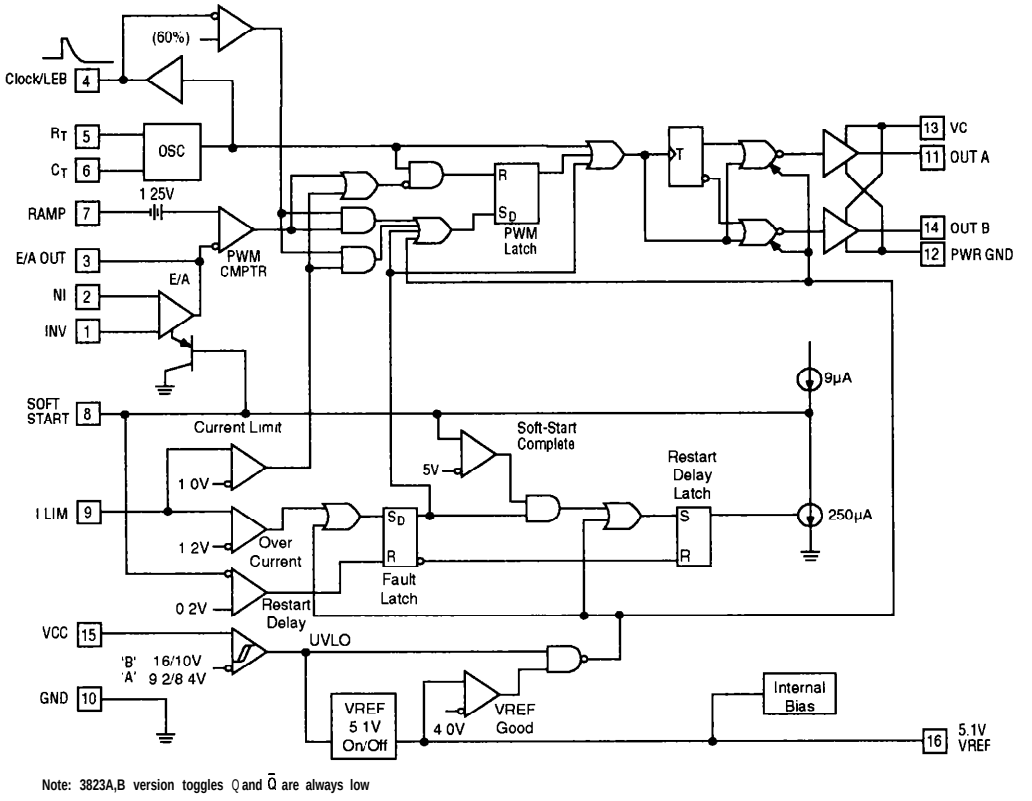
Higher degrees of integrated functions within PWM IC controllers are necessary to remain in pace with todays advancing power supply technology Many external features, used almost universally by designers, have been built into this new generation of UC3823A,B and UC3825A,B PWM controllers. These control enhancements can be classified as either a performance or protection improvement, and an itemized description of each will be presented. The new features are:

PERFORMANCE IMPROVEMENTS

- Lower startup current
- Accurate oscillator frequency
- Leading Edge Blanking
- Higher current totempole outputs
- Higher G.B.W. Error Amplifier

PROTECTION ENHANCEMENTS

- Active Low outputs during UVLO
- Advanced undervoltage lockout
- Latched fault logic
- Full-cycle soft start
- Restart delay after fault



Note: 3823A,B version toggles Q and $\bar{Q}$ are always low

Figure 1- UC3823A,B and UC3825A,B Block Diagram

UC3823A,B AND UC3825A,B FEATURES PREVIEW AND APPLICATIONS GUIDE

In most applications, the UC3823A and UC3825A devices are enhanced drop-in replacements for the UC3823 and UC3825 high speed PWMs. The "A" suffix versions (UC3823A and UC3825A) feature similar undervoltage lockout (UVLO) thresholds to the preceding generation which turn on at 9.2 volts and turn off at 8.4 volts. Off-line power supplies can benefit from the wider UVLO hysteresis of the "B" version devices (UC3823B and UC3825B) which turn on at 16 volts and off at 10 volts. This, in conjunction with the lower startup current of 100 microamps can streamline the IC's power supply and minimize startup circuitry power loss.

One significant difference will be found on the UC3823A and UC3823B controllers. Formerly, the UC3823 (non A or B version) provided access to the current limit comparator's threshold at pin 11. This could be accurately set by the user within the range of 1.0 to 1.25 volts with an external reference voltage. The UC3823A and UC3823B devices use pin 11 as a high current totempole output, identical to that found on pin 14. These outputs can be paralleled - effectively doubling the peak output current capability to 4 amps. No access to the previous current limit reference (I LIM REF) comparator is provided as this threshold is internally set to 1.0 volts with a +/- 5% accuracy over all operating conditions. Existing applications can incorporate the UC3823A or UC3823B devices by simply removing any of the former external biasing components to pin 11.

One other major difference to the prior generation of PWMs is the reduced maximum operating supply (Vcc) and collector supply (Vc) voltages of 22 volts versus 30 volts. This characteristic is a principal consideration when determining the IC power supply, as nearly all applications utilize a supply voltage between 10 and 15 volts. Typical supply current is higher; 28 mA versus the former 22 mA, however the maximum Icc is unchanged at 33 mA.

Since many of the enhancements in this new family of PWMs are executed using internal circuitry, most applications require no additional components externally to realize a performance or protection advantage. The list of improvements which includes latched fault protection and full cycle soft start should not require any PC board changes. The leading edge blanking feature, however, will require one capacitor from the CLOCK/LEB (pin4) to ground to facilitate programming.

The improved oscillator section can be optimally programmed for the correct frequency and maximum duty cycle combination. No changes to the timing component values of Rt and Ct are necessary. Additionally, high frequency current mode applications can benefit from the high gain bandwidth error amplifier (12 MHz). Unity gain bandwidth is also up from 5.5 MHz to 9 MHz. This should not require changes to the PC board layout unless the compensation circuit design relied upon the older 5.5 MHz UGBW for high frequency roll-off.

STARTUP FEATURES

Since a majority of PWM applications are off-line converters, a low startup current is desirable. This attribute minimizes the complexity and power loss of the startup power supply once normal operation is attained. Every milliamp of additional startup current drawn by the controller results in a power loss of approximately 385 milliwatts in a power factor corrected application. Heat, PC board real estate and additional cost are unnecessary extras which can be eliminated with a lower startup current controller.

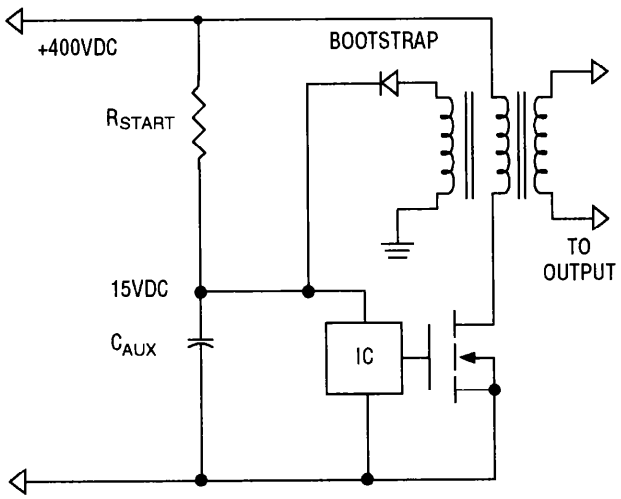


Figure 2 - Startup/Bootstrap Circuit

This new generation of UC3823A,B and UC3825A,B control ICs minimizes the startup current to 100uA typically. Once the IC crosses its undervoltage lockout threshold, the current drawn will increase to the typical running current.

In an off-line converter, two things are necessary to get the main converter up and running when the control IC turns on. First, the IC should contain wide undervoltage lockout hysteresis. Second, the bootstrap supply should come up and into regulation very quickly before the auxiliary capacitor voltage drops below the ICs lower (turn-off) undervoltage lockout threshold.

Undervoltage lockout thresholds are primarily determined by the allowable MOSFET gate voltage range. Operation with gate-to-source voltages above sixteen volts can cause over-stress to the device, and voltages lower than about nine volts can cause linear FET operation. The "B" suffix designator (UC3823B and UC3825B) is used to define devices which exhibit typical undervoltage lockout thresholds of

16V (turn-on) and 10V (turn-off) for off-line applications. The "A" suffix parts (UC3823A and UC3825A) incorporate 9.2V (turn-on) and 8.4V (turn-off) thresholds for DC to DC converter applications, and are compatible with existing UC3823 and UC3825 (non A,B) UVLO thresholds.

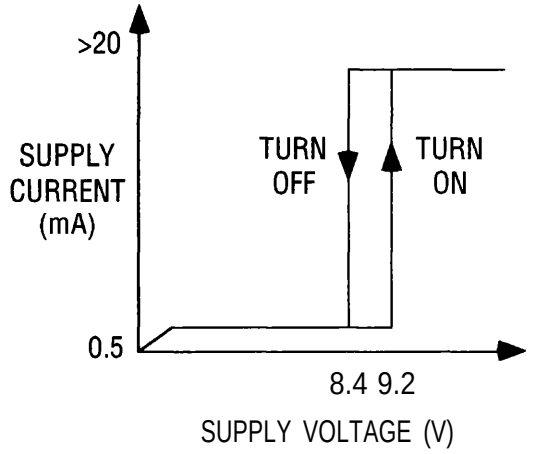


Figure **3** *- 9.2/8.4V UVLO Thresholds-DC/DC Converters*

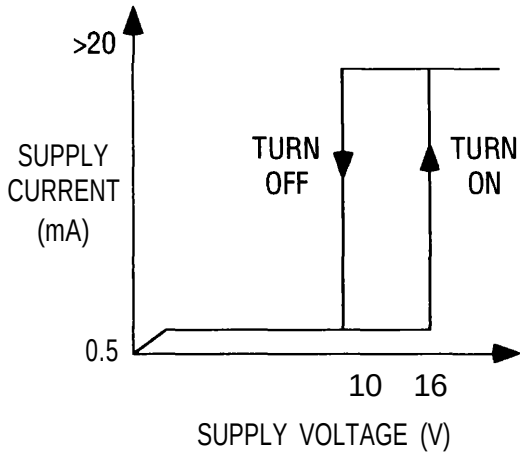


Figure 4 - 16/10V UVLO Thresholds-Off Line Power Supplies

SELF BIASING, ACTIVE LOW OUTPUTS DURING UV LOCKOUT

Another enhancement to the new UC3823A,B and UC3825A,B controllers is found in the output stages. During undervoltage lockout almost all internal functions of the control IC are disabled, primarily to obtain a low startup current. Generally, this would result in little or no available bias to actively keep the outputs low during this power-up condition, when it's needed the most. Outputs are in a high impedance state which is typically about 1 megohm. As the DC (bulk) high voltage rises, a capacitive divider is formed at the MOSFET switch between the drain-to-gate and the gate-to-source capacitances. A quickly rising bulk supply can couple a problematic gate drive command to any FET driven without a gate pull down circuit. Since the control IC is below its turn on threshold, the unbiased output drivers of older PWMs cannot prevent the switch from turning on under these circumstances.

One solution to prevent this parasitic turn-on during undervoltage lockout is to incorporate an active low, self biasing totem-pole design in the driver output. As shown in figure 5, a PNP drive transistor (Q2) is connected between the output pin of the IC and the lower NPN output transistor (Q3). As the output voltage rises, transistor Q1 is biased on through the 50K ohm resistance. This causes the base of Q2 to go low, turning Q2 on. The output pin supplies drive bias to the main totem-pole transistor, Q3, directly through the saturated PNP. Increasing voltage on the output pin provides more drive to transistors Q1, Q2 and Q3. The saturation voltage of this circuit at moderate currents (10mA) is well below the turn on thresholds of the power switching MOSFETs. This circuit is removed from operation once the undervoltage lockout requirements have been satisfied. Transistor Q4 is turned on with a valid UVLO which voids the possibility of transistor Q1 from ever turning on during normal operation. Additionally, a 250 microamp current source from Vcc keeps the PNP predriver (Q2) off after UVLO.

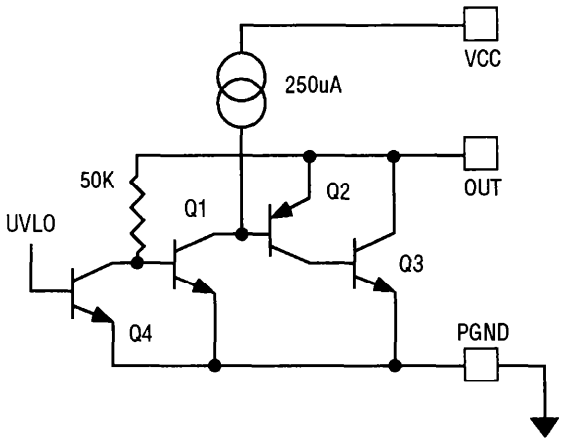


Figure 5 - UVLO Self Biasing Outputs

Another benefit of this technique is obtained during power down. As the IC crosses below its lower UVLO threshold, the self biasing circuitry is enabled. Any residual voltage on the output will similarly turn the totempole stage on which actively pulls the output low. This feature insures correct gate drive operation regardless of the turn off sequence.

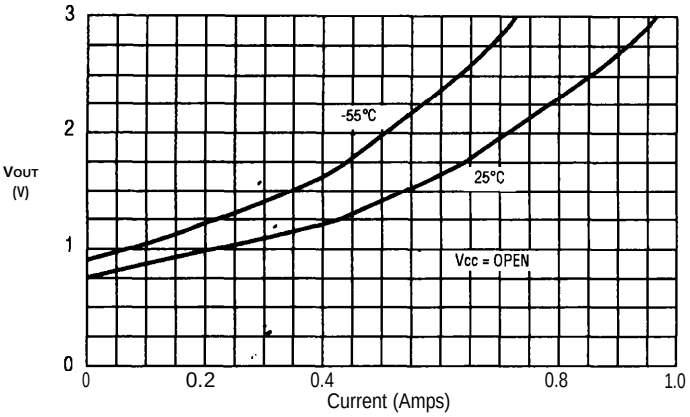


Figure 6 - Output V and I During UVLO

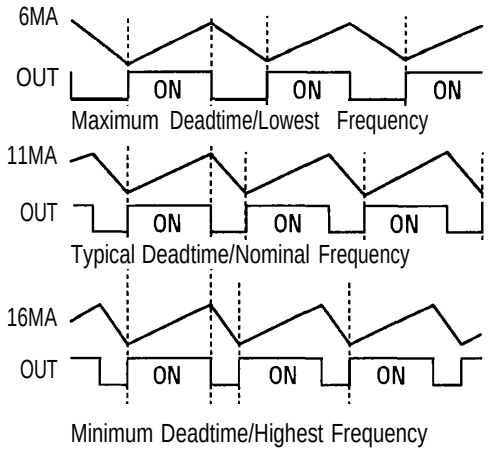


Figure 7 - Frequency and Deadtime Variations vs. Discharge Current Tolerances

OSCILLATOR ACCURACY

Fundamental to the design of any switchmode converter is maintaining an accurate switching frequency. The UC3823A/B and UC3825A/B ICs utilize two pins for the sawtooth oscillator; one each for the timing resistor (Rt) and timing capacitor (Ct). The resistor programs the charging current to the timing capacitor via an internal current mirror with high accuracy. Maximum switch on-time is determined by the rising capacitor voltage whereas deadtime, the programmed switch off time is determined by the timing capacitors discharge.

Considerable improvement has been made to the accuracy of the oscillator discharge current. The previous generation of UC3823/25 devices endured variations of plus or minus forty percent (+/- 40%) over the full military temperature range and production tolerances. This new generation of UC3823A/B and UC3825A/B PWM controllers features a well controlled oscillator discharge current which is "trimmed" at wafer probe testing to +/- 1 milliamp. Oscillator initial accuracy (400 KHz nominal) has been tightened to 375 KHz minimum and 425 KHz maximum. Total variation over all line and temperature ranges is limited to 350 and 450 KHz. A new specification for 1 MHz accuracy has been added, demonstrating a plus or minus fifteen percent total frequency variation at high frequency.

CLOCK OUTPUT

The UC3823A,B and UC3825A,B controllers also feature a TTL/CMOS compatible CLOCK output pin. Specified amplitudes are 3.7 volts in the high (off) state and 0.2 volts during its low state. Additionally, this pin is also used for programming of the leading edge blanking function. Notice that unlike their non A,B predecessors, these enhanced versions cannot be externally synchronized by an input to the clock pin. Synchronization is obtained by forcing a SYNC pulse across a resistor in series with the timing capacitor.

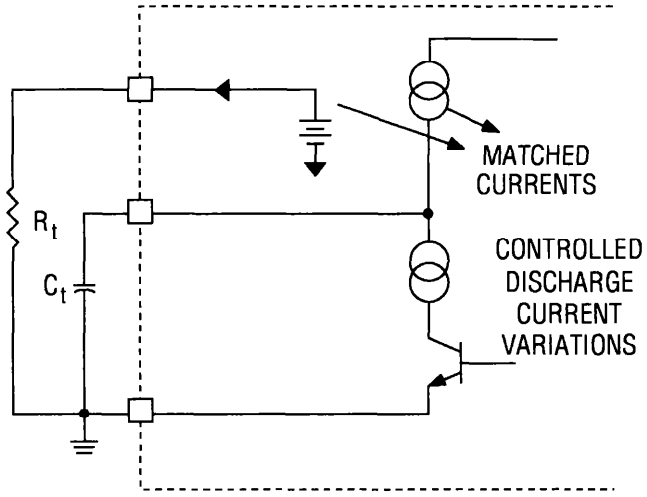


Figure 8 - Controlled Discharge Current

LEADING EDGE NOISE IN THE CURRENT SENSING CIRCUIT

One of the most difficult tasks with peak current mode control is sensing the inductor current. Instead, switch current is generally sensed by means of either a series resistor or current sense transformer. There is some difficulty with using this technique accurately, especially at light current levels. As the switch turns on, circuit parasitics in the power stage, output rectifier reverse recovery characteristics and high current gate drive pulses can create significant noise pulses on the leading edge of the current sense signal. Traditionally, this problem has been overcome by adding a small R-C noise filter between the current sense resistor and the PWM controllers current sense input. At low operating frequencies and high output current levels this R/C filtering technique will generally deliver satisfactory results. However, at higher switching frequencies, and almost always at lighter load currents the leading edge spike amplitude can greatly exceed the peak current sense signal.

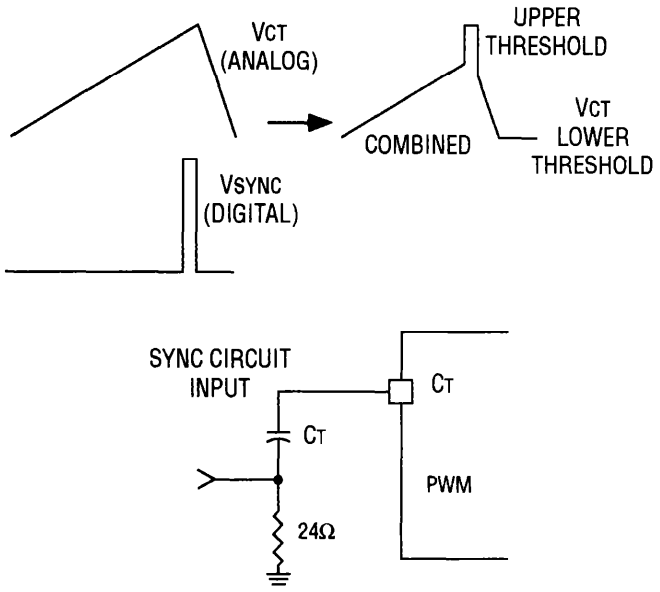


Figure 9 - Synchronization

The leading edge current sense noise shown in figure 10 will cause a premature, false triggering of the pulse width modulator. Additionally, this will lead to instability of the converter by causing the voltage loop to oscillate at light loads. When the PWM is triggered by the noise spike instead of the true current signal - a smaller (minimum) pulse width is delivered to the main switch. The power supply's output voltage subsequently falls which causes the voltage amplifier to command for a higher inductor (switch) current. Eventually this continues until the amplitude is sufficient to rise above the leading edge noise spike.

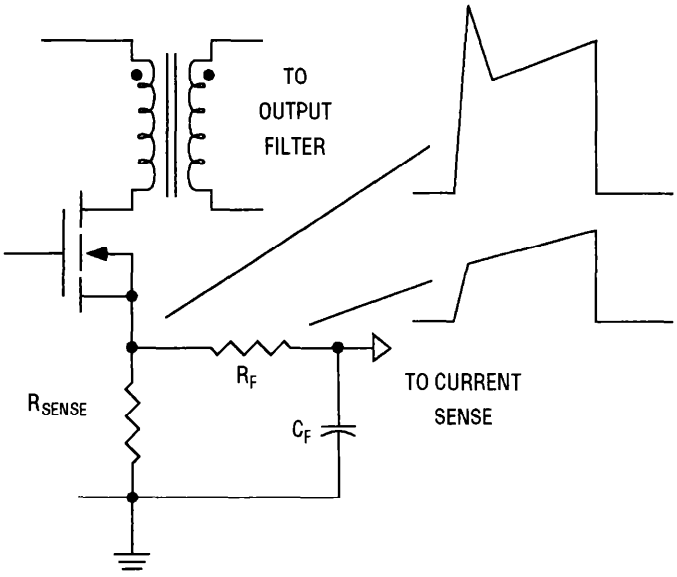


Figure 10 - Current Sensing Technique

Pulse widths too wide for proper operation are now delivered and the output voltage climbs until the voltage amplifier commands less current. This oscillatory process continues at a rate determined by several factors. Noteworthy is that this has nothing at all to do with the instability caused by inadequate slope compensation, or peak-to-average current error. The cause is leading edge noise, and even optimal loop compensation cannot protect against this problem.

LEADING EDGE BLANKING

The RC filter shown in figure 10 can be tailored to work well over a limited range of applications and power levels. Another technique, known as Leading Edge Blanking (LEB) essentially blindfolds (blanks) the PWM comparator for a specific amount of time during the beginning of the cycle. The blanking duration is user programmable and should correspond to the width of the leading edge noise spike. This eliminates the need for filtering of the current sense signal in peak current mode controlled circuits.

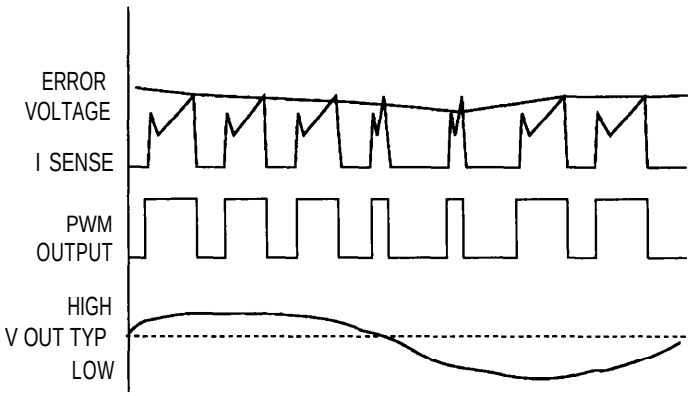


Figure 11- Instablity Caused By Leading Edge Noise Triggering

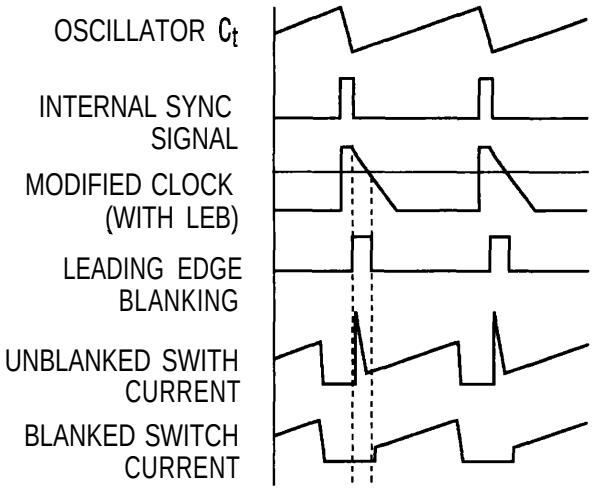


Figure 12 - Leading Edge Blanking Operational Waveforms

LEB IMPLEMENTATION

The focal point of any fixed frequency PWM controller is its clock. Used to accurately program the switching frequency and maximum duty cycle, the clock serves as the trigger source for the leading edge blanking circuitry. A digital representation of the timing capacitor charge/discharge status is developed by internal logic. This is made available at the PWMs CLOCK pin for external purposes. The UC3823A,B and UC3825A,B all use a high output to indicate the OFF period of the switching cycle, and a low to indicate the maximum ON time. These levels will be incorporated into the design of the leading edge blanking circuitry.

The clock output of the UC3823A,B and UC3825A,B is pulled high during the oscillator deadtime to approximately 4 volts. A capacitor added to the CLOCK output pin programs the leading edge blanking duration. An internal comparator with an accurate threshold set at 60% of the peak clock amplitude has been added. The LEB programming capacitor is discharged by an internal 10K ohm resistance to ground. The LEB interval is defined by the time required for the capacitance to discharge from 4 volts to the 60% threshold. Once the LEB capacitor discharges below this threshold, the PWM operates normally without any blanking. Programming should accommodate the worst case of leading edge noise. With no programming capacitor added, the ICs function similarly to their predecessors and provide no blanking.

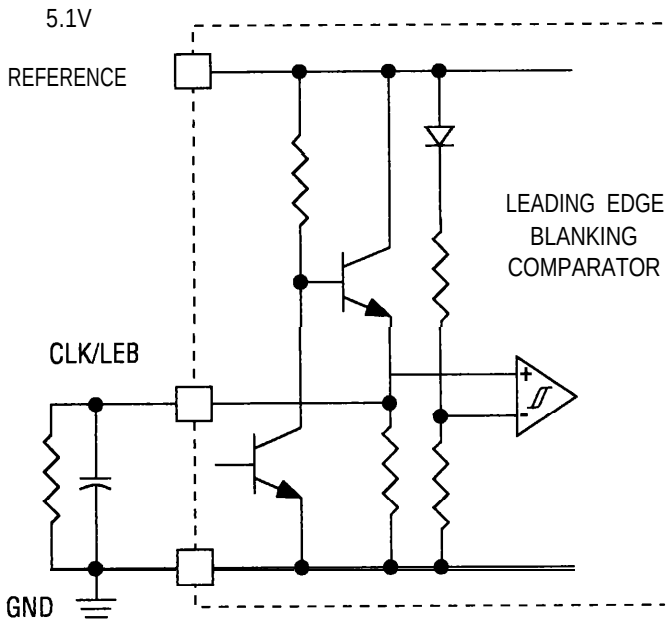


Figure 13 - LEB Circuitry

Because of the leading edge blanking, the PWM outputs will exhibit a minimum ON time in normal operation. The duration corresponds directly to that of the LEB programming, so a minimum duty cycle has also been established. Resolution between zero duty cycle and this minimum duty cycle cannot be obtained - which should also be taken into account when programming the LEB circuitry.

Zero duty cycle is a valid operating condition which can be achieved by one of two methods. The most obvious technique is to bias the error amplifier such that its output is driven below the PWM zero duty cycle threshold of 1.1V. The ICs error amplifier can easily accomplish this while sinking current up to 1 mA, worst case. The second technique utilizes the current limiting feature (ILIM) at pin 9. An ILIM input held above the 1.2V (typ) FAULT threshold will force the PWM's on-time and duty cycle to zero. More details of the interface between the PWM and fault circuitry will be found in the following fault protection section.

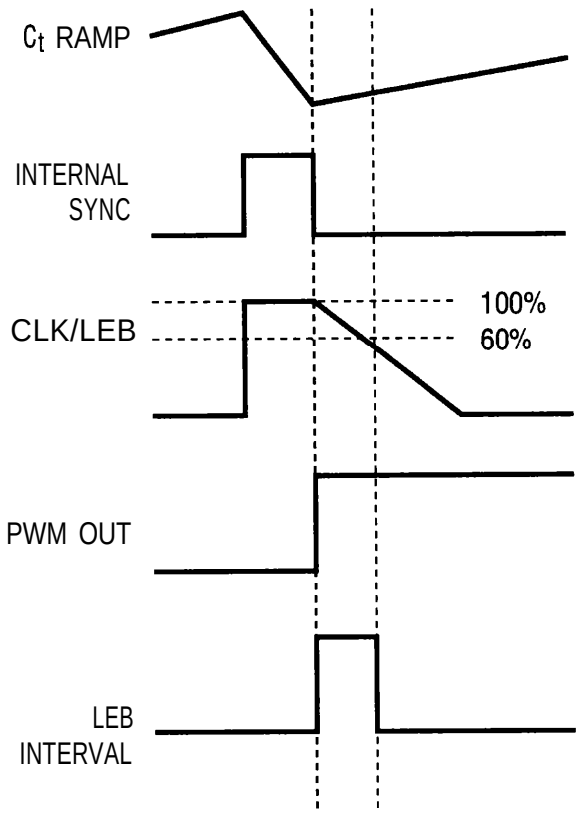


Figure 14 - Blanking Waveforms

LATCHED FAULT PROTECTION

While the previous generation of control ICs offered fault protection circuitry, they did not feature a fully latched shutdown after detecting a fault. The unlatched technique only

discharges the soft start capacitor during the duration of the fault - a duration which can be very brief with a high speed controller. As a result, the duty cycle is not significantly reduced, and the IC continues delivering output pulses at the the switching frequency. Typically, the switching components can easily be dangerously overstressed while also dissipating a significant amount of power.

The new UC3823A,B and UC3825A,B controllers feature a latched fault protection circuit as shown in figure 15. Two comparators are used to offer two stage protection - depending on the amplitude of the fault. The first comparator has a one volt threshold for cycle-by-cycle current limiting. In normal operation this terminates the immediate switch drive pulse but does not trigger the latching fault logic. One volt has been selected as the peak amplitude of the current sense signal for normal operation and slight overloads to accommodate transients.

The second comparator has a slightly higher threshold of 1.20 volts, indicative of a twenty percent overload or fault. When this comparator is tripped, the fault latch is turned on and the soft start capacitor begins discharging. The present output pulse had already been terminated by the one volt comparator circuity while the signal was rising to cross the 1.20 volt level. The over- current latch insures that the PWM latch is held off for an extended period of time, approximately equal to the soft start time constant.

Once this overcurrent latch is set, a second “restart” latch is triggered which insures the proper restart of the control logic. First, a current sink (typically 200 uA) is turned on by the restart latch output which overpowers the 9 uA charging current source and begins discharging the soft start capacitor. The capacitor voltage is monitored by a restart comparator, looking for a decay to the threshold level of 0.2 volts. Once this occurs, the restart comparator resets the overcurrent comparator which sequentially resets the restart latch.

The restart latch can only be set with the right set of conditions as shown in the block diagram. First, undervoltage lockout must be satisfied to insure proper operation during initial power-up. Secondly, the overcurrent (1.2 V) comparator must be triggered, indicative of a valid fault. Last, and most important, is that a full soft start cycle must be completed before the restart latch can be retriggered. A fourth comparator insures that the soft start capacitor voltage has charged to a 5 volt threshold. This indicates that a complete discharge followed by a complete charge has occurred.

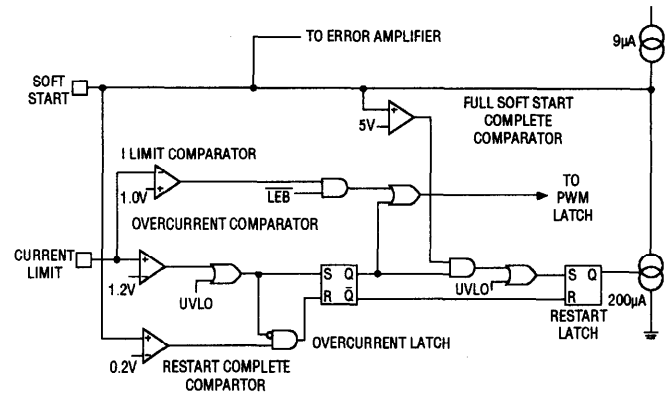


Figure 15 - Latched Fault And Full Cycle Soft Start Protection Circuitry

FULL CYCLE / CONTINUOUS FAULTS

During a fault, many designers prefer to reduce the repetition rate at which the switch is driven rather than to continue at the normal switching frequency. Often called “hiccup”, this delayed restart will significantly reduce the overstress and power dissipated during abnormal conditions. Implementation of the latched fault technology results in significantly lower power dissipation during a continuous fault or shorted output stage. Instead of delivering minimum duty cycle pulses at the oscillator frequency, the retry sequence occurs at a repetition rate approximately equal to the soft start period with a continuous fault.

In the worst case, two PWM outputs can occur in a time less than the soft start time constant, but this happens only once with a ‘true” fault input (>1.2 V). For example, assume that the converter is in normal operation when a fault is detected. The first valid fault immediately turns off the output and triggers the latching overcurrent circuitry. Since the soft start capacitor was fully charged (above 5 volts), the “full soft start complete” comparator allows the overcurrent latch to set the restart latch. Discharge begins and continues until the restart complete comparator is tripped at a soft start capacitor voltage of 0.2 volts. The restart latch is reset, and the soft start capacitor begins charging.

Note that a well defined time is required between this instant and the time when the first output pulse can next occur. The capacitor begins at 0.2 volts and the error amplifier output is internally clamped to the soft start capacitor voltage. Back at the PWM comparator, however, there is a 1.25 volt offset on the ramp pin to facilitate zero duty cycle. Therefore, the soft start capacitor must charge from 0.2 volts to 1.25 volts before the PWM comparator is active.

This provides a slight interval between the worst case of successive output pulses into a shorted load. From this point on, the soft start capacitor must fully charge up to the five volt threshold of the “full soft start complete” comparator. Once in this mode, only one PWM output per soft start period can be obtained into a fault as shown in figure 16.

LEB AND FAULT DETECTION

The leading edge blanking circuitry is interfaced to also blank some of the fault detection circuitry. While numerous arrangements are possible, only one configuration offers a reasonable compromise between quick response and noise immunity. As demonstrated in figure 12, leading edge blanking does inhibit the one volt, cycle-by-cycle current limit comparator during the programmed interval. However, the blanking does not disable the 1.2 volt overcurrent comparator and fault logic. This adaptation will accommodate a moderate amount of leading edge noise without having to significantly filter the current sense, and fault signals. Even if a moderate amount of filtering is required, the latched full cycle shutdown protection minimizes the power dissipation.

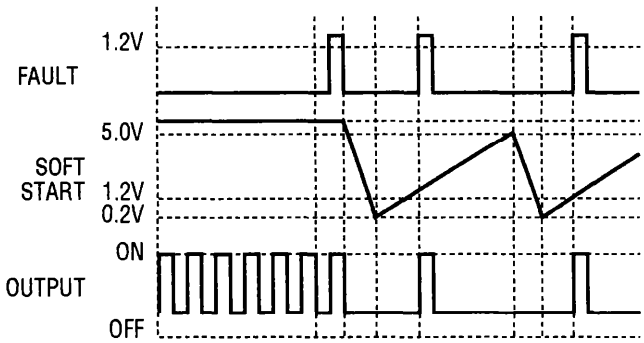


Figure 16 - Full Cycle Soft Start - Operational Waveforms

TIGHTER FAULT THRESHOLDS

This latest generation of IC controllers utilizes a thin film resistor process which provides improved control of the tolerance. These resistors are used to generate accurate voltage thresholds by dividing down the IC’s reference voltage internally. Both of the current limiting comparator thresholds have been tightened in the “A” and “B” versions of controllers. The cycle-by-cycle current limit threshold range has been tightened to +/- 5% from its previous +/- 10% specification. The new limits are 0.95V minimum, 1.05V maximum with the center remaining at the previous 1.0 volts.

The overcurrent (fault) threshold, however, has been centered at 1.2 volts instead of the 1.4 volt midpoint of the non A,B versions. The new specifications are 1.14 volts minimum to 1.26 volts maximum. Applications converting to the newer controllers may need to adjust the current sense resistor value accordingly. Typical propagation delay is unchanged at 50 ns typical, and 80 ns maximum.

HIGHER GAIN BANDWIDTH ERROR AMPLIFIER

Many of the critical UC3823/25 error amplifier specifications have been improved. The characteristics which significantly differ are: input offset voltage - reduced from 10 to 7 mV, unity gain bandwidth - increased from 5.5 MHz to 9 MHz, typical slew rate - reduced from 12 to 9 V/us. Notice that the minimum slew rate is unchanged at 6 V/us.

HIGH POWER OUTPUTS

The industry need for higher switching frequencies and improved efficiency has directly effected the design of the totem-pole output drivers. Many of the capacitive loads (MOSFETS) placed directly on the PWM outputs require high peak currents to obtain adequate switching transitions. The high speed UC3823A,B and UC3825A,B controllers feature peak current ratings of 2 amps, and are capable of slewing 15 volts in 35 nanoseconds into 1000pF Separate collector supply (Vc) and power ground connections (PGND) help decouple the analog circuitry from the high power gate drive noise.

TYPICAL APPLICATION

The 1.5 MHz, 50 Watt push-pull converter detailed in Application Note U-110 was redesigned to accept the UC3825”B” device. The basic power stage remained similar while an emphasis was placed on control circuit improvements. These enhancements included Leading Edge Blanking of the current sense signal and Restart Delay following a fault. Also, a current sense transformer was installed which not only reduced losses but allowed amplification of the current sense signal to approximately 2.5 volts, thus enhancing noise immunity.

Improvements to the power section of the converter include the use of larger MOSFETS (IRF640’s) and the addition of a bootstrap winding for the auxiliary bias supply. The startup resistor from the input supply was increased since the UC3825”B” device features a wide UVLO hysterisis of six volts.

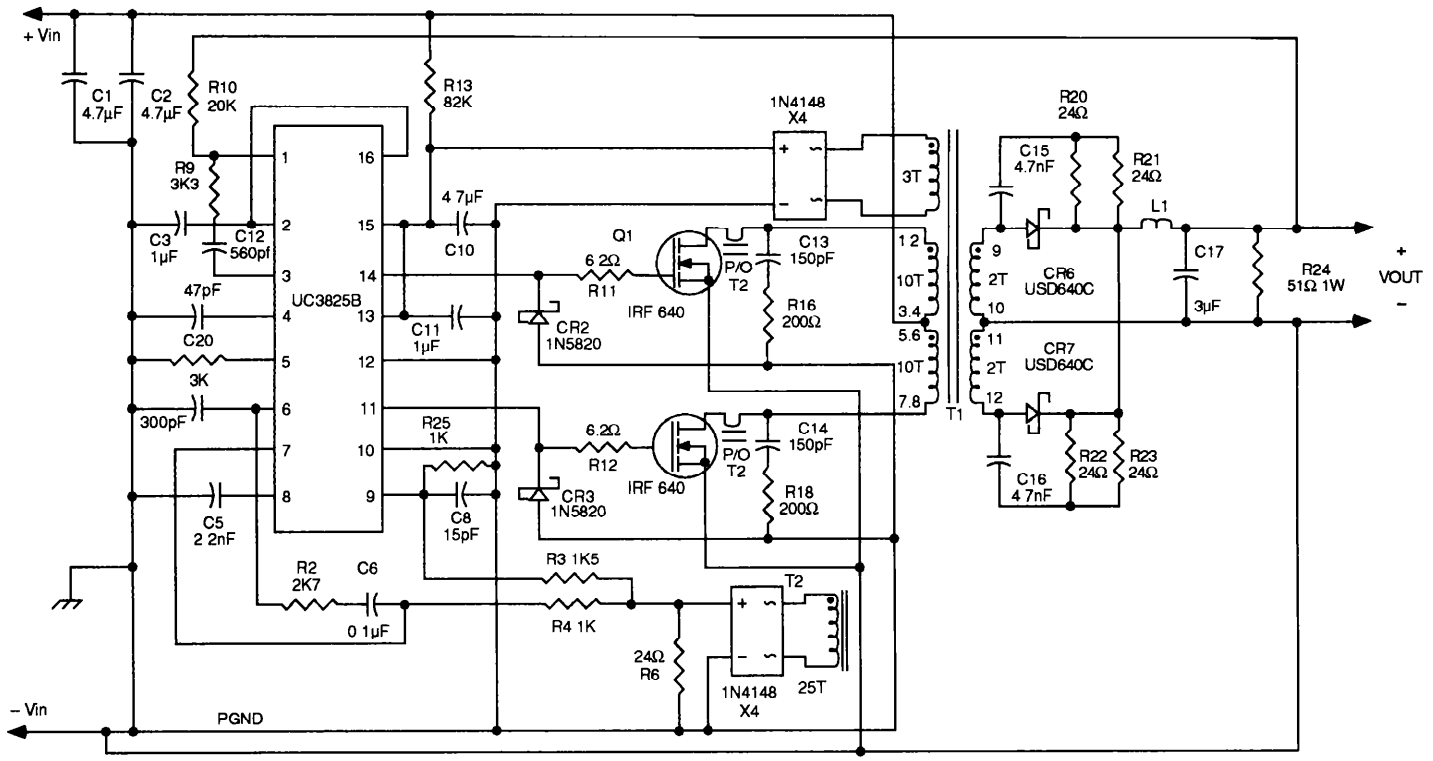


Figure 17 UC3825B Controlled 1.5 MHz Push Pull Converter

CONVERTER PERFORMANCE

The redesigned converter exhibited similar line, load and transient response to the original converter, which was excellent due to the high conversion frequency. A significant improvement was made in the short circuit performance by comparison. While operating into a continuous short circuited output, the UC3825"B" controlled version reduced the converter input power (and dissipation) to approximately one-hundredth of the original design. Featuring the programmable Restart Delay circuitry, the redesigned 50 Watt converter draws only one-quarter of a Watt (1/4 W) of input power with a shorted circuited output.

SUMMARY

This new generation of UC3823A,B and UC3825A,B PWM controllers features a multitude of performance advantages over its predecessors. Higher precision, increased protection and programmable new functions are just a few of the benefits obtainable with these enhanced versions of PWMs. And as the level of sophistication in todays power supplies increases, so too must that of its components - especially control ICs. Containing an expanded list of integrated features, this new era of enhanced UC3823A,B and UC3825A,B controllers overcomes the challenges of the power supply industry for higher levels of power, protection and performance.

ADDITIONAL INFORMATION AND REFERENCES

1. New Pulse Width Modulator Chip Controls 1 MHz Switchers; UNITRODE Application Note # U-107
2. 1.5 MegaHertz Current Mode IC Controlled 50 Watt Power Supply; UNITRODE IC Databook, Application Note # U-110
3. "Practical Considerations in Current Mode Power Supplies"; UNITRODE IC Databook, Application Note # U-111

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

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