BQ79606A-Q1 Design Recommendation

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ABSTRACT

The BQ79606A-Q1 is an AEC-Q100 automotive qualified part that monitors between 3 and 6 cells. It can be used in automotive vehicles as well as in industrial applications. There are many aspects to this device such as voltage and temperature monitoring, cell balancing, daisy chain communication, and NTC readings that need to be considered when designing a board layout. This applications note contains specific designs recommendations for the implementation of this battery monitor that should be observed for best performance.

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Trademarks

1 Power Supplies (BAT, LDOIN)

The BQ79606A-Q1 is powered through the BAT and LDOIN pins from the cells it is monitoring. They internally regulate and provide power to operate the part. Power reference is to the bottom of the connected cells through several VSS pins. Each VSS pin must be connected to the bottom cell of the module (refer to the Layout Considerations for specific recommendations).

The BAT and LDOIN pins should be filtered separately from the top cell. This is to protect against hotplug, in-rush current, and other relevant noise. Recommended filter resistors are 100 Ω for the BAT pin and a 40.2 Ω for the LDOIN pin (47 Ω is more common and close enough to the desired value). Each pin should use a 0.33 µF /50 V capacitor. Figure 1 shows the typical circuit. When less than 6 cells are used, the power filters should be connected to the top cell.

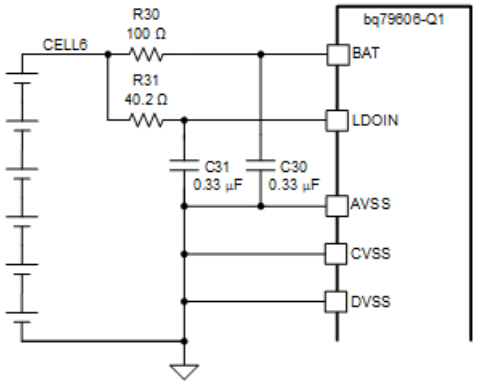


Figure 1. Power Supply Schematic

The filter resistors in Figure 1 serve several purposes. The main purpose is to limit the current into the pins in the event of a fault. Another is to provide some power dissipation away from the IC and onto the resistor.

Design Summary

- 47 Ω resistor and 0.33 µF/ 50 V capacitor on the LDOIN pin
- 100 Ω resistor and 0.33 µF/ 50 V capacitor on the BAT pin
- All VSS pins must be connected to the negative terminal of the bottom cell

2 AVDD, DVDD, VLDO and REF1 outputs, CVDD and VIO Inputs

AVDD, DVDD, and VLDO are regulated outputs derived from the LDOIN input. Each of these regulator outputs should have a bypass capacitor to avoid noise, but the capacitors should not be larger than 2.2 µF with a 10% tolerance due to the fact that larger capacitance will slow startup. REF 1 is an internal voltage reference, CVDD the power supply for Daisy Chain communication and VIO is the I/O voltage supply.

Each regulator provides power for delicate internal subsystems. Do not connect external circuitry or additional loads to these regulators beyond those described in the datasheet. There are special considerations for configuration depending on if the device is the base or a stack.

Base Device

AVDD is a 5 V regulated output which supplies internal circuits. AVDD should be bypassed to AVSS with a 2.2 µF/ 16 V capacitor. **Do not** connect any additional loads to AVDD.

DVDD is a 1.8 V regulator output that is used to power the digital logic inside the chip. Do not connect any additional loads to DVDD other than VIO which should be limited to a maximum of 8 mA.

REF1 is an internal voltage reference used for very sensitive internal circuits and **should not** be used to supply external circuits. A 2.2 µF/ 16 V bypass capacitor should be connected from REF1 to AVSS for proper operation of the part as seen in Figure 2.

CVDD is a supply input for the stack communication circuitry and must be connected to the VLDO output and CVSS as shown in Figure 2. CVDD should always be on and therefore should be connected to the VLDO output, which should always output 5 V. CVDD and VLDO should have a 2.2 µF/ 16 V bypass capacitor. This configuration is only for a system supply between 5.5 V and 33 V. Voltages between 4.75 V and 5.5 V should connect CVDD directly to LDOIN. This configuration is described in more detail in Section 7

VIO is a supply input for the digital signaling pins and should have a decoupling capacitor. Connect the input to the supply rail with a 2.2 µF/ 16 V capacitor as seen in Figure 2. This will bypass VIO to AVSS. There are two different configurations for VIO depending on if the BQ79606A-Q1 is a base or stack device. Proper configuration for this pin is important because the WAKEUP, RX, TX, and GPIO's use VIO as a reference.

For a device communicating to a host microcontroller, VIO can be connected to the host system's supply rail if it is in the range is between 1.8 V and 5.25 V as seen in Figure 2 .

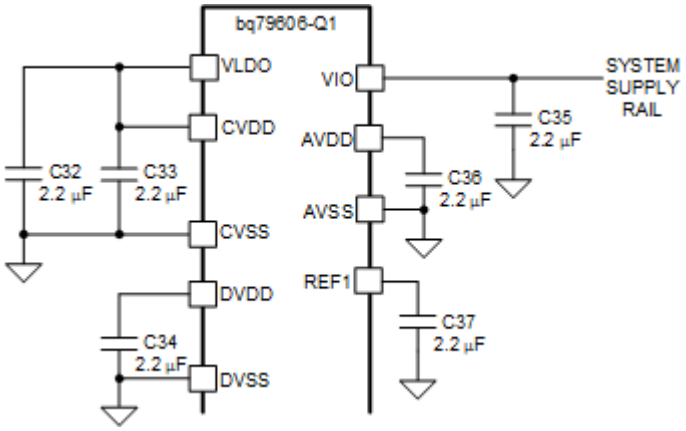


Figure 2. Regulator Connection for Base Device

Stack Device

Stack devices have the same configuration as the bases devices described except VIO is powered from VLDO. When connected to VLDO the bypass capacitors for the VLDO output and VIO input should both be 2.2 µF/ 16 V capacitor. Figure 3 shows this connection.

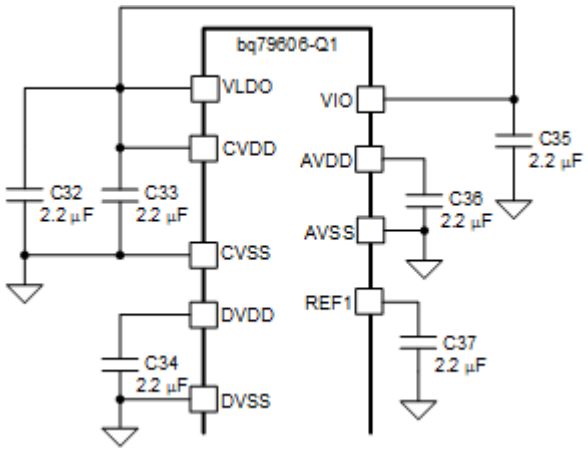


Figure 3. Regulator Connection for Stack Device

Design Summary

- REF1 is used for very sensitive internal circuits and **should not** be used to supply external circuits.
- Decouple a 2.2 µF/ 16 V capacitor on the each specified pin to the ground plane.

- **Put all the capacitor as close to pin as possible**.
- Connect CVDD to VLDO for cell stacks between 5.5 V and 33 V. Anything less will require a different connection.
- On the base device VIO should be tied to an external host system (typically a microcontroller) power rail between 1.8 V and 5.25 V
- On the stack device VIO should be tied to VLDO

3 VPROG Configuration for OTP Programming

The BQ79606A-Q1 has the ability to program the OTP memory via the VPROG pin. This pin has overvoltage and undervoltage monitoring along with other error check features which are outlined in the data sheet. While programming, the VPROG must have a 1 µF/ 16 V bypass capacitor to ground. When the pin is not in use then a pull down, 100 kΩ, resistor should be used. It is recommended that these two components be placed in parallel as shown in "A" of Figure 4. If VPROG is not being used then configuration "B" in Figure 4 should be used. **Do not leave VPROG floating.**

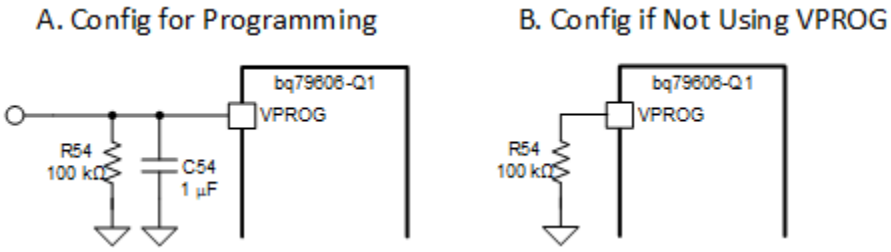


Figure 4. VPROG connection for OTP Programming

Design Summary

1. Place a 100 kΩ resistor and 1 µF/ 16 V capacitor in parallel at the VPROG pin

4 Cell Voltage Sense (VCn) and Cell Balancing (CBn)

Voltage monitoring is done though the VCn pins while cell balancing is done thought the CBn pins. Each of the VCn pins has their own delta sigma ADC to ensure the most accurate readings. Getting an accurate reading for these connections is critical to achieving maximum performance so the following design recommendations should be followed.

4.1 Cell Voltage Sense (VCn)

The VCn pins are the primary inputs for measuring the cell voltages. VC0 is the low side reference to the negative terminal of the bottom cell and VC6 is the high side reference to the positive terminal of the top cell. The BQ79606A-Q1 has internal zener diodes to limit the voltage between the inputs and internal anti-alias filters, however an additional external filter is still needed between each connection. When selecting the VCn-to-VCn+1 components is important to keep in mind that the BQ79606A-Q1 inputs are protected from ±33 V transients. Anything greater than that needs to be clamped to fall within that range.

The inputs should be connected to the cells using series resistors to limit current into the pins and protect the IC from system transients. Capacitors are also needed between the VCn inputs. Figure 5 illustrates the correct VCn-to-VCn+1 connections. When fewer than 6 cells are used on the BQ79606A-Q1, the lower cells must be used in order. The unused upper VCn inputs must be shorted to the highest used VCn input. An example of this can be seen in Figure 10.

The series resistor (R1 and R2 in Figure 5) serve several functions but the main function is that they protect the analog front end (AFE) inputs from in-rush current during hot plug. The series resistor on the VCn pins must be 4 times the value of the CBn series resistor for the best hot plug performance (Equation 1).

$$R_{VCn} = (4)(R_{CBn}) \quad (1)$$

This 4:1 ratio with the resistors will allow for short detection should such an event occur. It is recommended that the CBn series resistor be calculated first then multiplied to get the VCn value. How to perform these calculations can be found in Section 4.2. The recommended 40.2 Ω is an odd value for a resistor so a 47 Ω resistor will also work (and is the value used in the datasheet).

For applications that require a very low filter cutoff frequency, connect a differential capacitor between the VC lines to provide the bulk of the AFE input filtering. The bias voltage on these differential capacitors are the same (or very close), therefore, anti-aliasing is improved. A 0.1 µF capacitor is recommended.

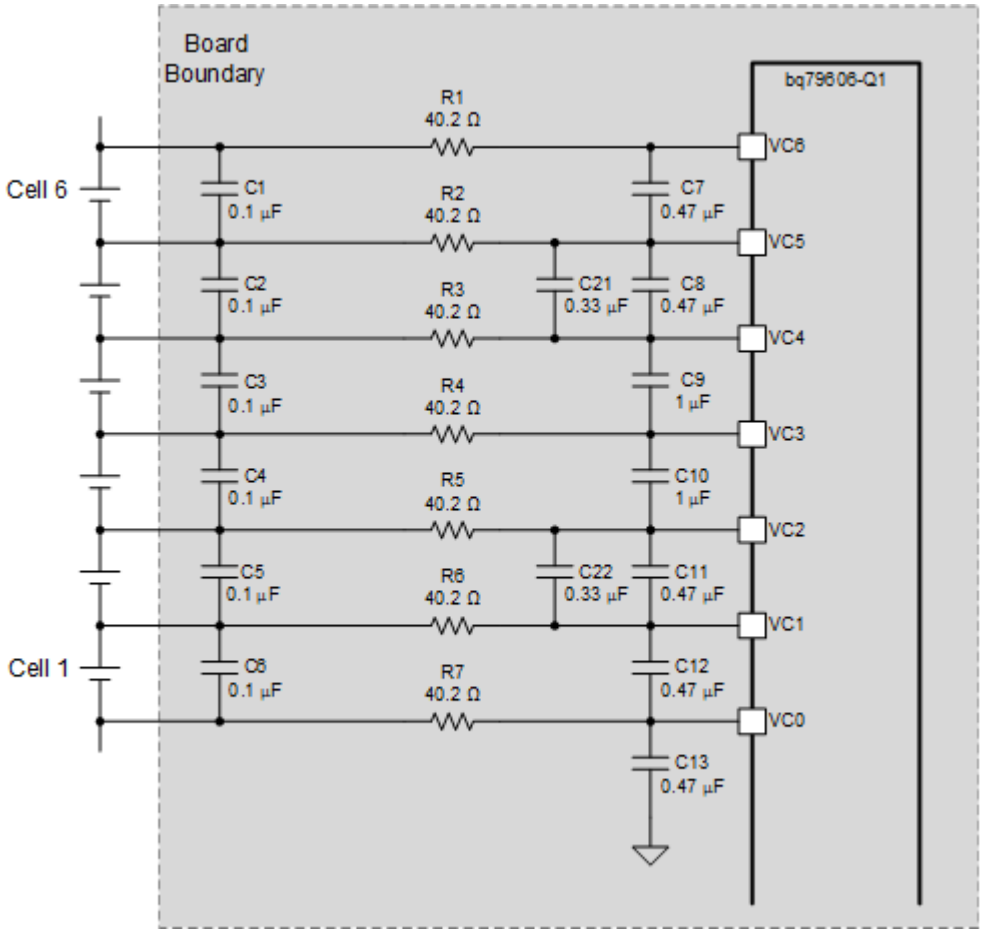


Figure 5. Cell Voltage Monitoring

4.2 Cell Balancing (CBn)

The CBn pins are the inputs for cell balancing with CB0 for the low side of the bottom cell and CB6 the connection for the high side of the top cell. The BQ79606A-Q1 has internal FET's that control the current for cell balancing and is set with an external resistor. Additional components are also needed to protect these inputs during hotplug and provide extra filtering. Any transients greater than 16 V need to be clamped.

Figure 6 illustrates the correct CBn-to-CBn+1 connections. The capacitor values are staggered in the figure to keep a similar cutoff frequency across the cells. The same value capacitor can be used for all inputs as shown in the data sheet, but the cutoff frequency will vary between cells. CBn inputs used must correspond to the VCn used. Unused CBn inputs are left unconnected as shown in Figure 10

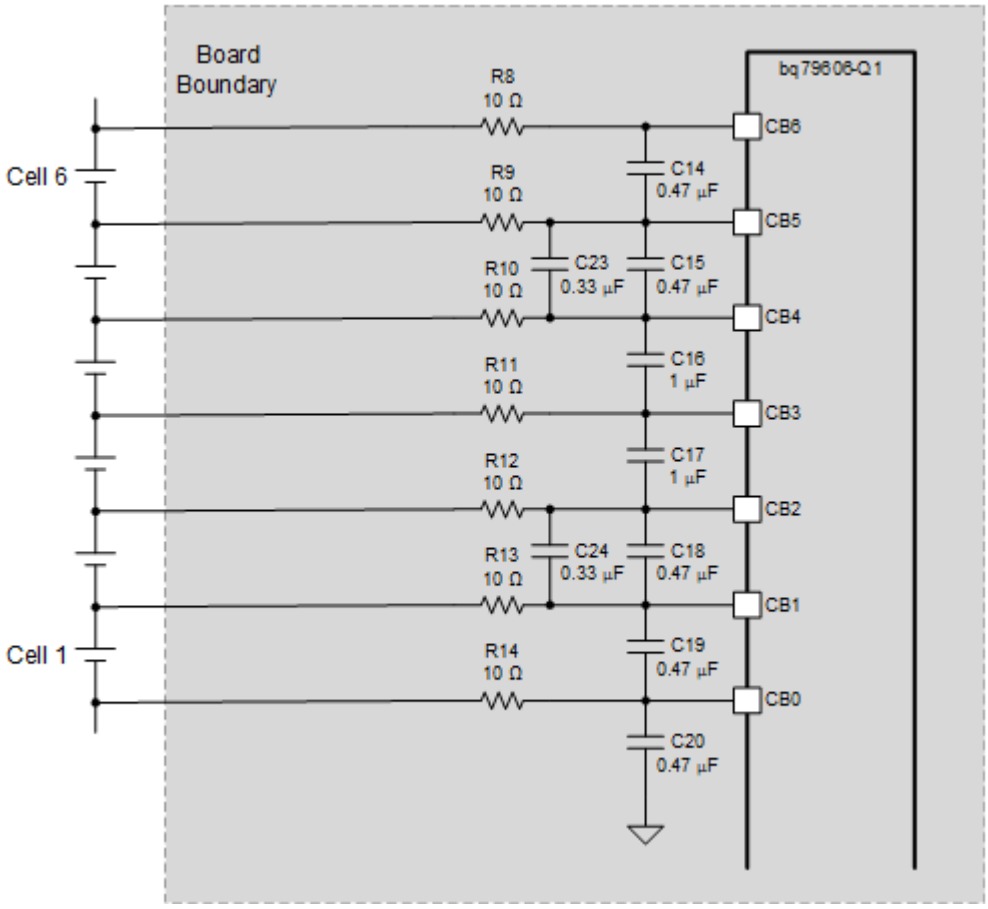


Figure 6. Cell Balancing

Cell Balancing current, I_{EQ}, is set with the series resistor, R_{EQ} (R8 in Figure 6). This resistor value is calculated using Equation 2. Where V_{BAT} is the voltage of the battery cell, I_{EQ} is the desired balancing current, and $R_{DS(ON)}$ is the resistance of the internal FET when it's on, that value can be found in the data sheet. Example calculations can be seen in Figure 7. Once this resistance has been calculated use it to set the series resistor on the VCn pins using Equation 1. If possible keep these resistance values as small as possible because a larger resistance will introduce more error into the signal.

$$R_{EQ} = \frac{1}{2}\left(\frac{V_{BAT}}{I_{EQ}} - R_{DS(ON)}\right) \quad (2)$$

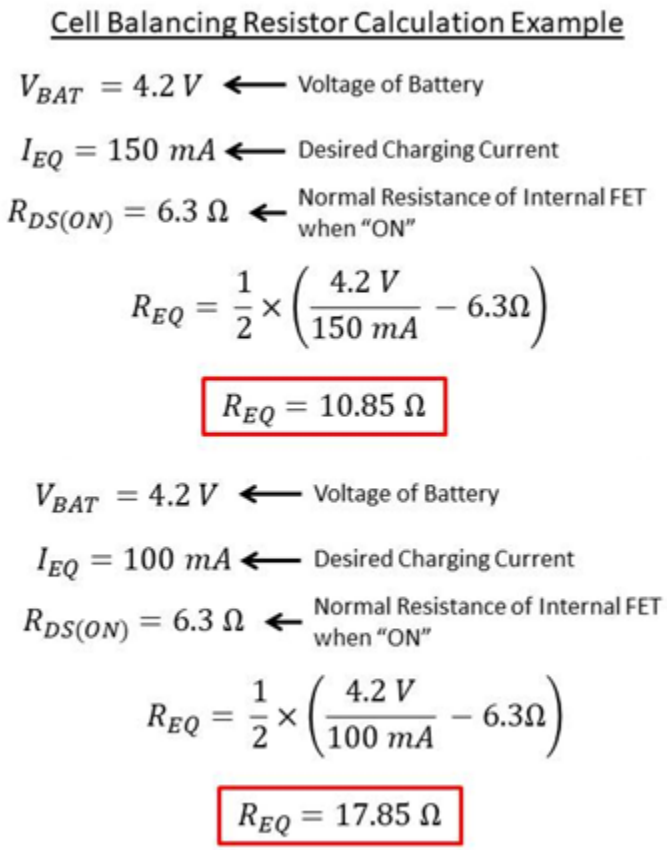


Figure 7. Cell Balancing Resistor Example Calculation

The BQ79606A-Q1 can handle 150 mA max for cell balancing current which means the series resistance value can be between 10 Ω to 500 Ω. Should more current be needed the cell balancing pins are able to support an external FET as shown in Figure 8. Details for that configuration can be found in the BQ79606A-Q1 data sheet.

Some quick notes about the external balancing before moving one. First is that the series resistors between the FET and pin are there to protect the pins during hot plug and the 1 nF capacitor is there to ensure that the FET does not turn on during hot plug. Also be aware of the following conditions that should be considered when selecting the FET.

1. The VDS must be selected based on derating requirements determined by the stack voltage.
2. The VGS threshold must be low enough to turn on with the lowest battery voltage planned for balancing. The gate of the MOSFET sees half of the battery voltage, so the VGS of the MOSFET must be selected to provide sufficiently low RDSON at half of the lowest battery voltage.

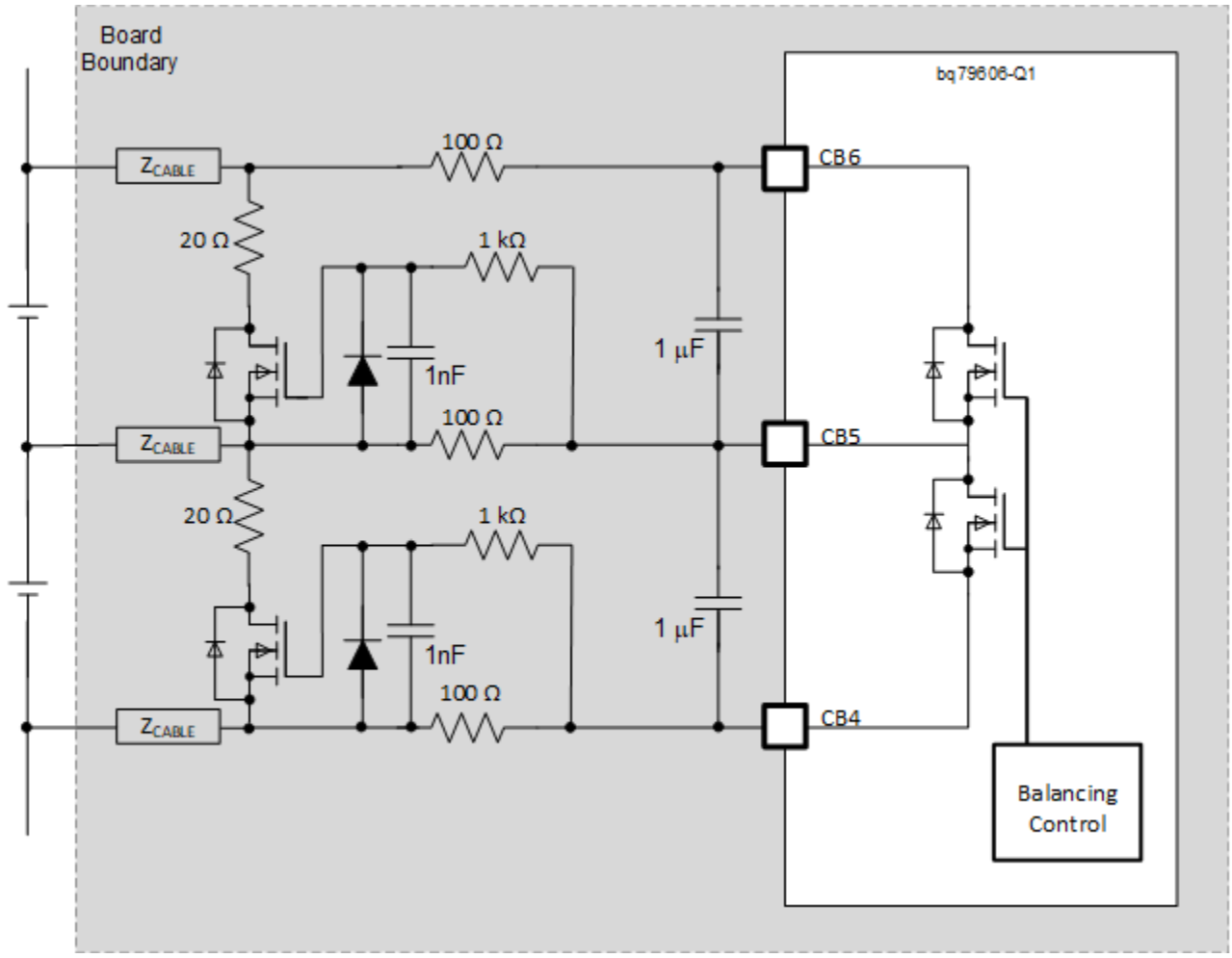


Figure 8. External FET Cell Balancing

Figure 9 shows a diagram of how the voltage connections and cell balancing connections would look together.

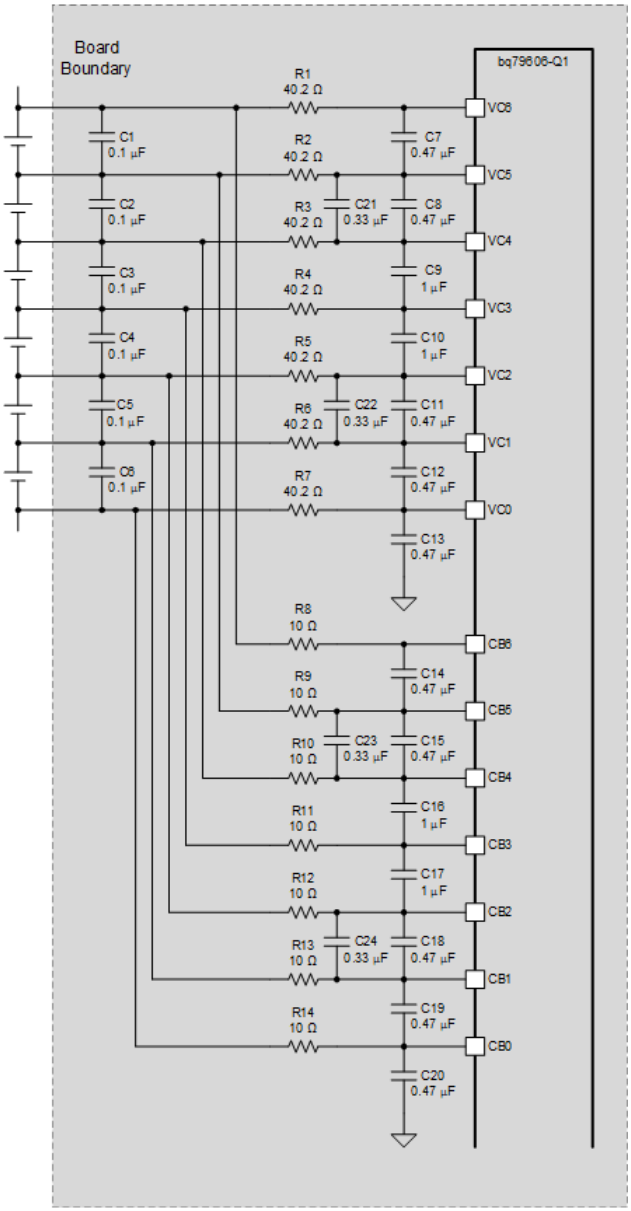


Figure 9. Cell Voltage Sense and Cell Balancing

4.3 Using Fewer than 6 Cells

As stated earlier, the BQ79606A-Q1 can support between 3 and 6 cells. The VCn inputs must be used in ascending order starting with VC0. Any unused upper connections should be tied to the highest connection as shown in Figure 10. CBn inputs must correlate to the VCn inputs. Any unused CBn connections are to be left unconnected.

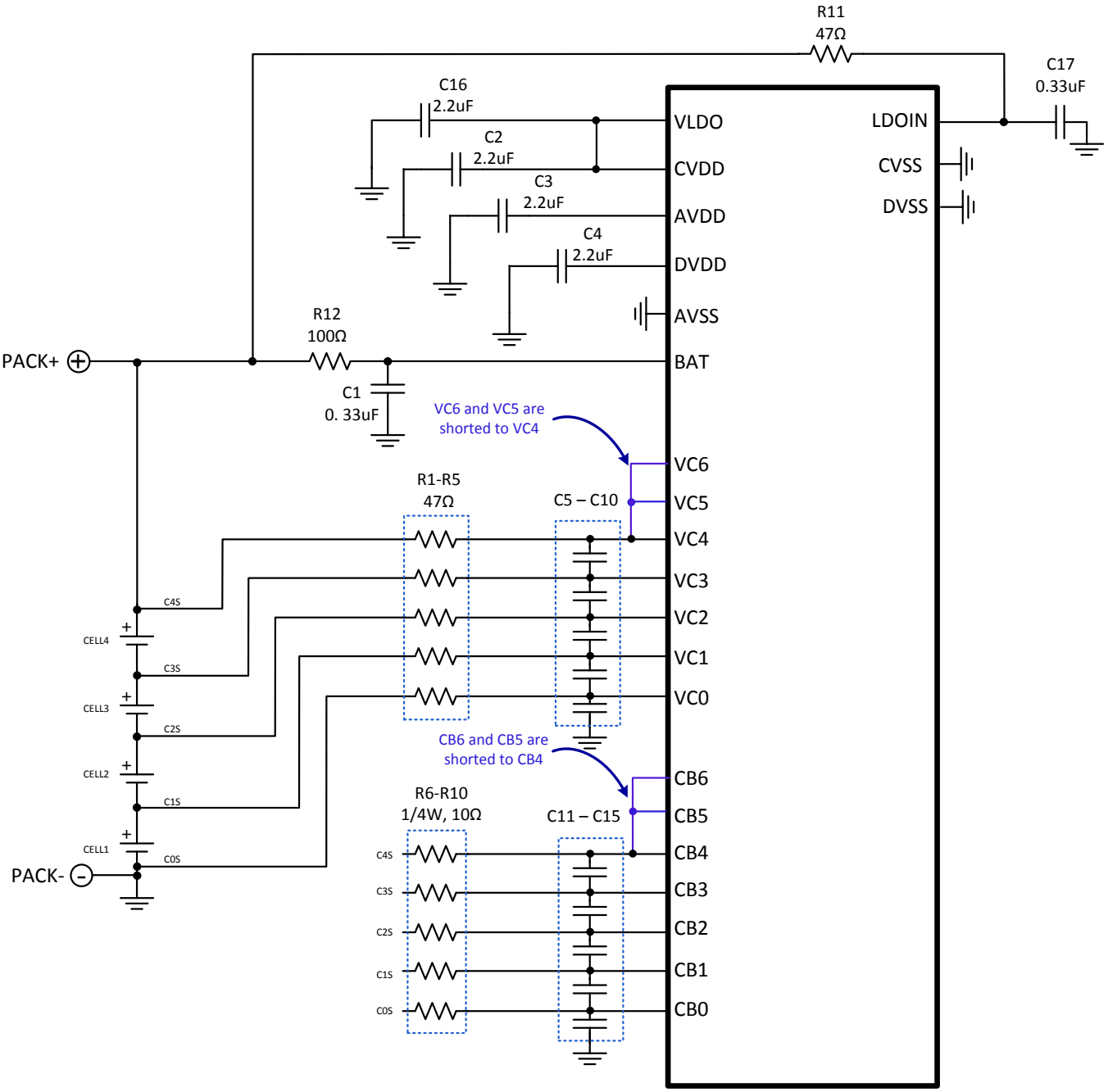


Figure 10. Connecting Fewer than 6 Cells

Design Summary:

- Capacitor values are staggered to keep a similar cutoff frequency across the cell on both the VCn and CBn lines.
- 0.1 µF differential capacitor between each VC line as close the to board edge as possible to provide additional filtering.
- Cell balancing current is set with the CBn series resistor.
- The CBn series resistor can range anywhere between 10 Ω to 500 Ω but use the formula in Equation 2 to calculate the correct resistance for the desired balancing current.
- The series resistor on the VCn pins should be 4 times the value of the CBn series resistor for the best hot plug performance. Calculate the CBn resistor value first. Try to keep both resistor values as low as

possible for better accuracy in cell voltage readings.

- VCn input connections must start with the lowest input, VC0, and then be connected in ascending order. Tie any unused upper VCn pins to the highest VCn input.
- CBn inputs used must correspond to the VCn used. Unused CBn inputs are left unconnected.
- For more than 150 mA of charging current use an external FET. Details can be found in the BQ79606A datasheet.

5 TSREF

TSREF is a reference output for temperature sensing and should be bypassed to AVSS with a 2.2 µF / 10 V capacitor. When thermistors are used for temperature measurements connect TSREF to the top of the resistor divider network as described in Section 6.1. TSREF should not connect to other pins for power. See Figure 11 for TSREF connection. Leave TSREF unconnected if not in use.

6 General Purpose Input-Output (GPIO) Configurations

There are six GPIO pins available in the BQ79606A-Q1. These pins may be used for temperature measurement, measurement of DC analog signals, digital input or output, and SPI. The behavior of the pins may be selected in the non-volatile RAM as described in the data sheet. If the signal goes off the board the input should be protected using a zener diode at the pin.

Unused GPIO pins should have an external 10 kΩ pulldown resistor to AVSS.

6.1 Ratiometric Voltage Measurement

Ratiometric voltage measurement is most commonly used for external temperature sensing. To measure an external temperature sensor, the GPIO connections must have a resistor divider from TSREF to AVSS with the GPIO connected to the center tap. The NTC can then be connected from TSREF to GPIO or from GPIO to AVSS (see Figure 11). The input should be filtered using a low-pass filter to reduce high frequency noise. A 1 kΩ resistor and 1 µF capacitor are common but the filter may be adjusted to the requirements of the application. This setup provides a ratiometric measurement of the GPIO, and linearizes the NTC curve.

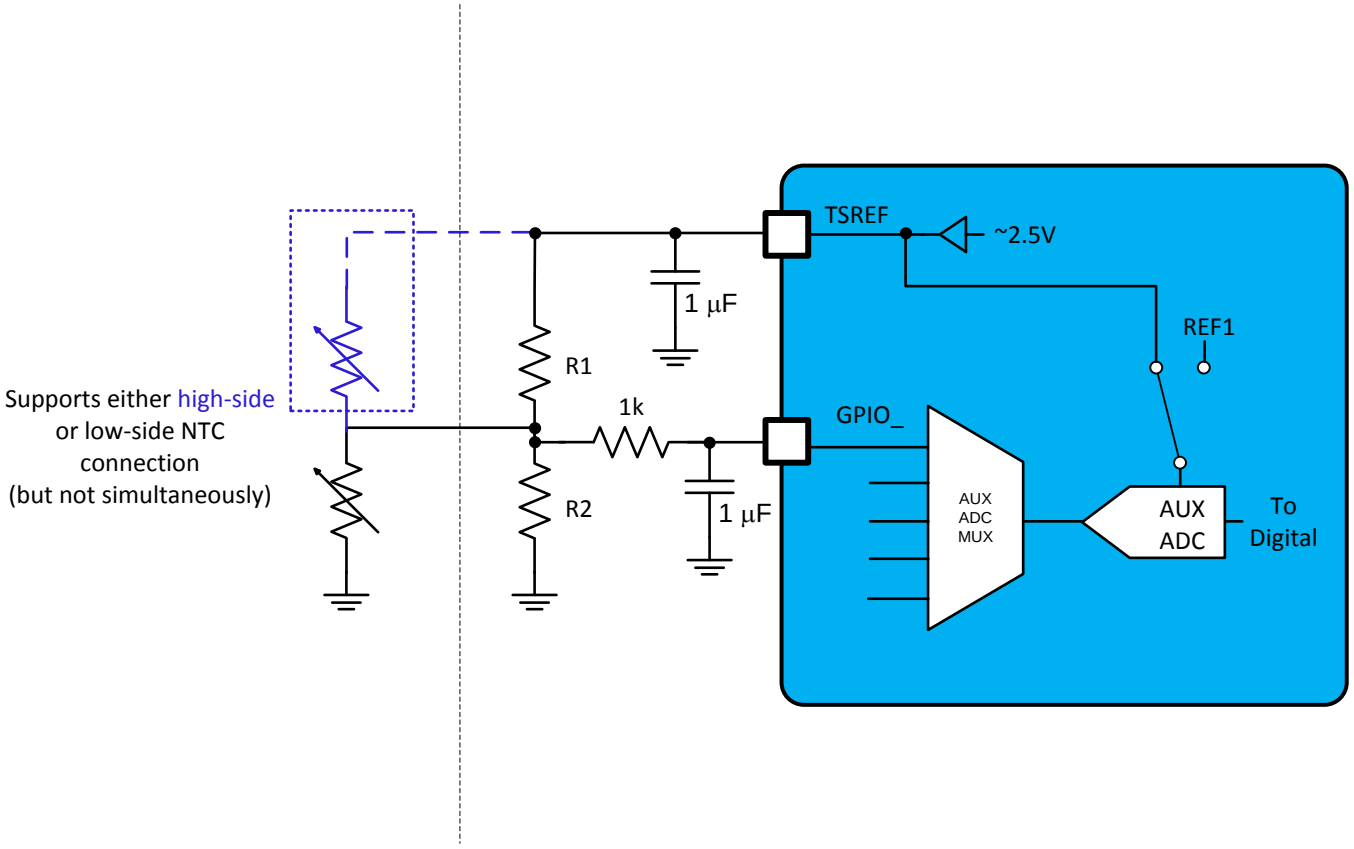


Figure 11. GPIO Ratiometric Measurement

In order to select the appropriate values for R1 and R2, please refer to the "GPIO* Inputs" section of the datasheet for formulas and best practices.

When configured for temperature measurement, the BQ79606A will adjust the AUX ADC to use the TSREF for measurement and provide a ratiometric value.

6.2 Absolute Voltage Measurement

When measuring analog signals a resistor and capacitor are recommended to filter out transient noise. When configured as an analog input, the AUX ADC uses the REF1 reference rather than the TSREF so the data is a DC value and not ratiometric.Figure 12 shows an example of a GPIO used for absolute measurement of an on-board signal. When configured for analog input the GPIO pin should not be left floating.

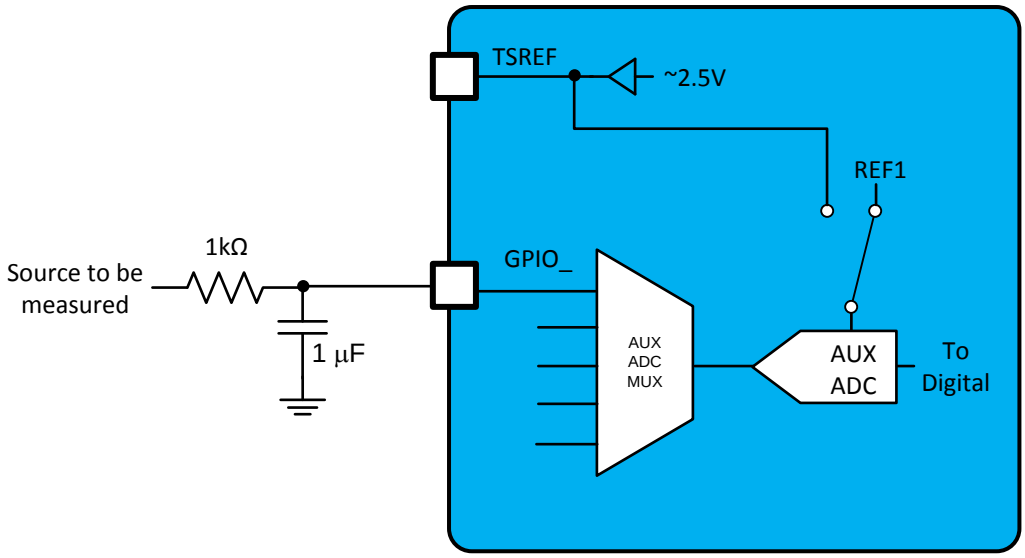


Figure 12. GPIO Absolute Voltage Measurement

6.3 SPI Mode

One use of GPIO[6:3] is as a SPI master. Connection of the pins in SPI mode is the same as general digital connections, but SPI configuration replaces the GPIO pin configuration. Figure 13 shows an example connection of GPIO[6:3] for digital signaling or SPI mode.

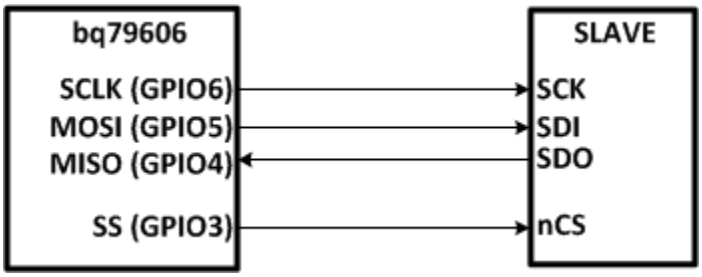


Figure 13. Example SPI Master Connections

Unused GPIO pins should be tied to AVSS through a 10-kΩ pull down resistor. By default the GPIO pins are configured internally as an input with a weak pull-down resistor, so program the GPIO configuration appropriately to avoid leakage current.

Design Summary:

- Connect external temperature sensor to GPIO's using a voltage divider network.
- GPIO pins used for temperature measurement should have a pull up resistor to TSREF equivalent to the resistance of the NTC at nominal temperature. Each input should also have a 1 kΩ resistor and 1 µF capacitor.
- GPIO pins with signals connecting from off-board should use a zener diode clamp.
- DC voltage readings need a 1 kΩ resistor and 1 µF capacitor.
- To use GPIO's in SPI mode, use GPIO3 - GPIO6. Unused GPIOs should be pulled high to VIO or low to GND.
- GPIO pins are all programmed as inputs with a weak pulldown, leaving the inputs floating. The pins should not be allowed to remain as floating inputs. Reprogram the pins to become outputs or add a pulldown resistor.

7 Base Device Configuration

Single ended communication lines with the BQ79606A-Q1 normally refers to the base device in a stack that communicates with the host microcontroller though UART. There are two main ways to configure the base device. The first is using the BQ79606A-Q1 as a bridge device (Figure 14) and the second utilizes an isolation circuit (Figure 15). Even those two methods are different, setting up the base device remains the same.

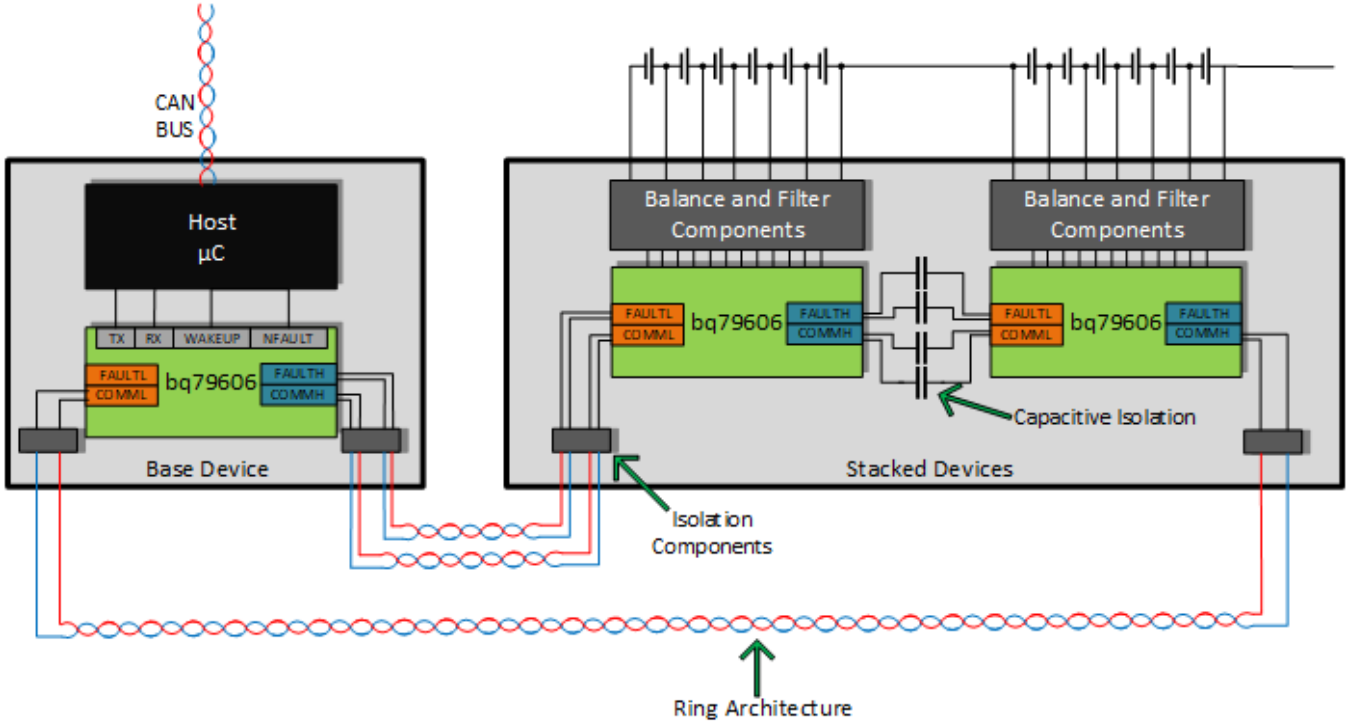


Figure 14. Using BQ79606A-Q1 as Bridge Device Block Diagram

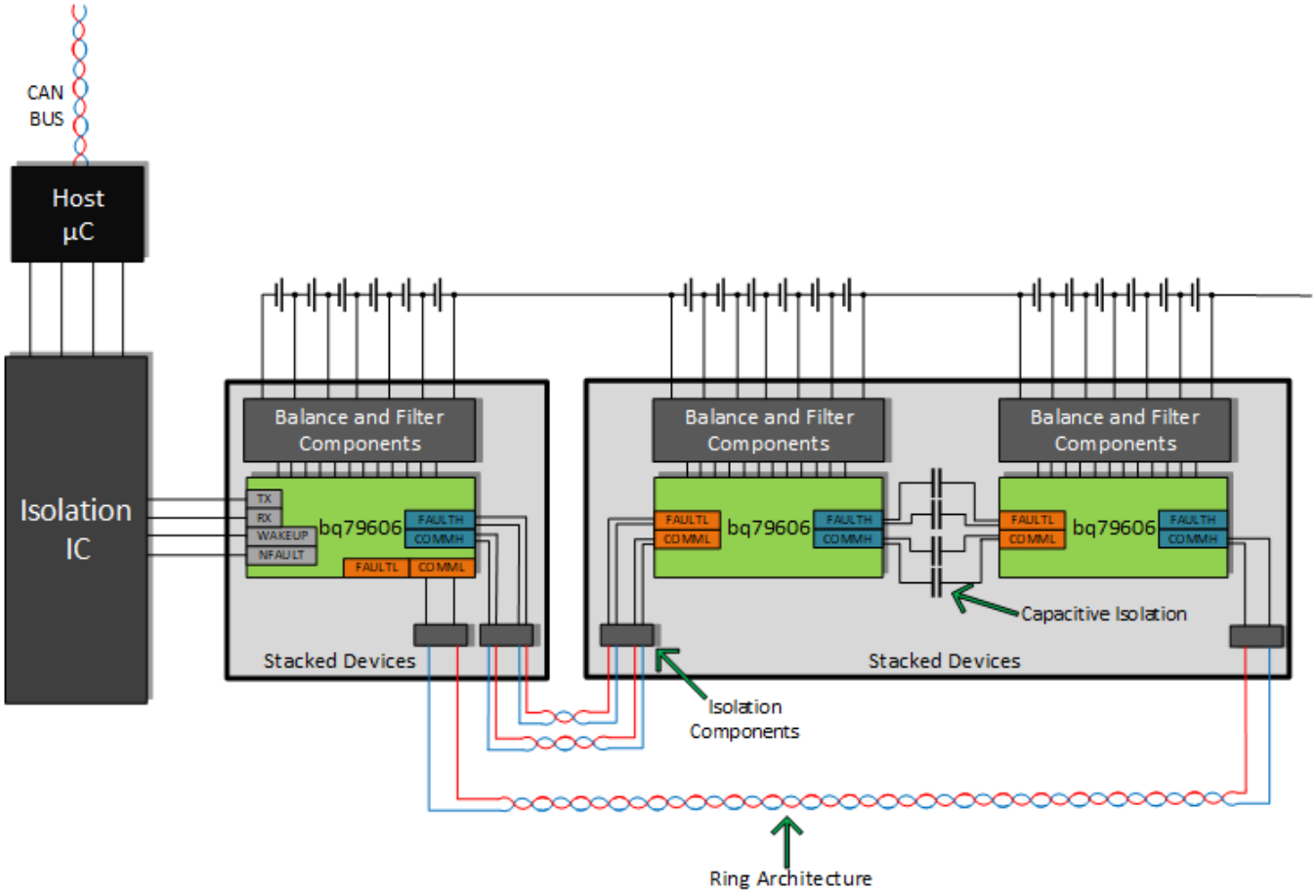


Figure 15. Using BQ79606A-Q1 with an Isolation Circuit Block Diagram

An overview of how a bridge device should be configured is shown in Figure 16. This configuration is for stacks that are between 5.5 V and 33 V. If a lower voltage is used than connect CVDD to LDOIN as shown in Figure 17.

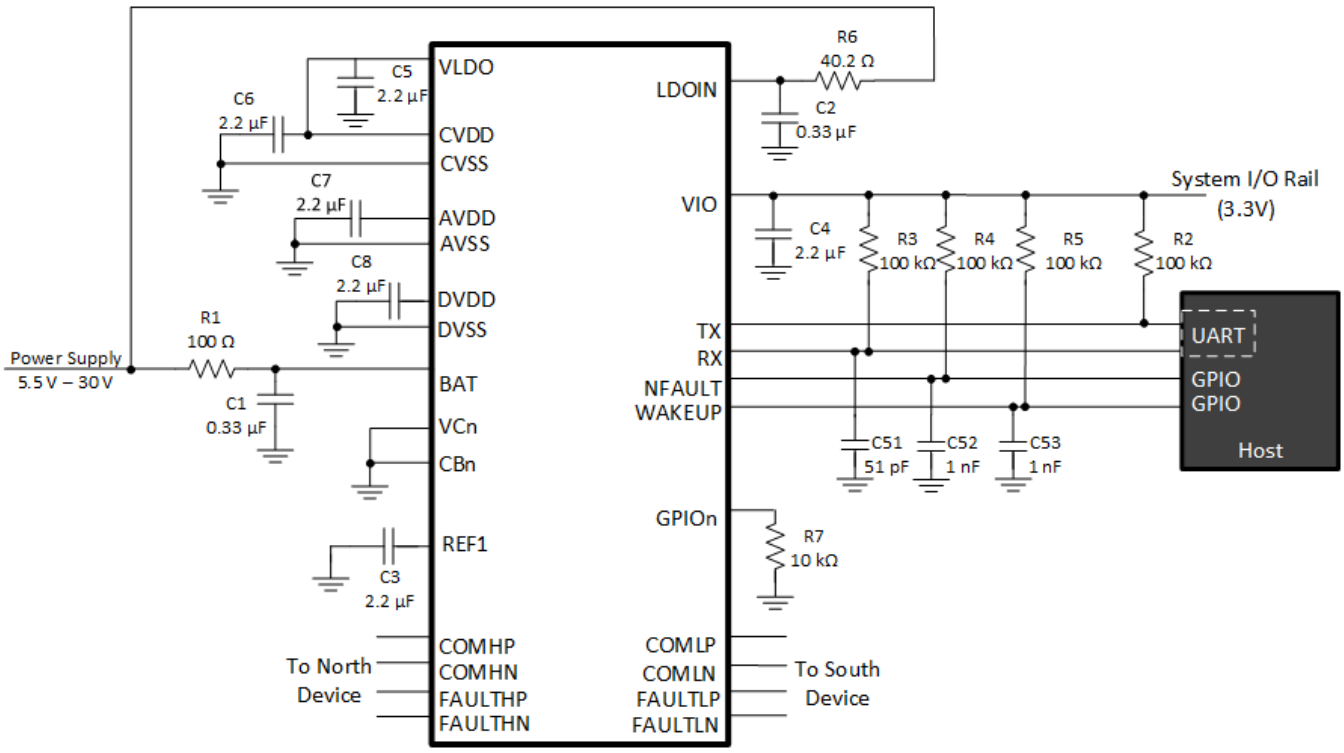


Figure 16. Bridge Device Schematic for 5.5 V - 33 V

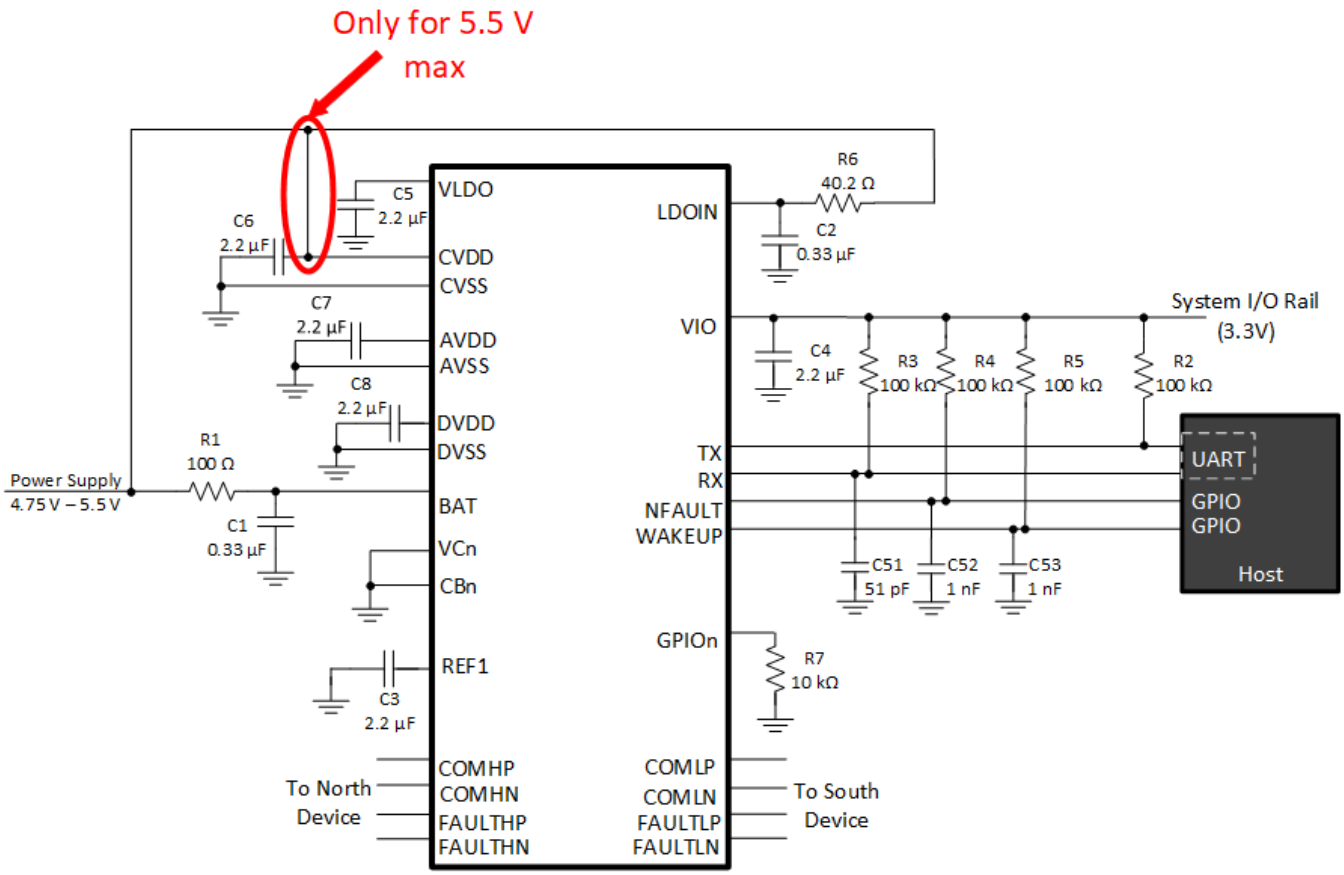


Figure 17. Bridge Device Schematic for 4.75 V to 5.5 V

7.1 WAKEUP

Base Device

A base device is awakened from SHUTDOWN mode by sending a WAKE TONE signal on the WAKEUP pin. For the base device, the WAKEUP pin should be pulled up to VIO. Wakeup must transition low for the prescribed time and back high to wake the device. Operation is unpredictable if the WAKEUP pin floats, ensure the WAKEUP pin is kept in a defined state. Figure 18 shows example connections of WAKEUP. Additional signal conditioning may be desired if WAKEUP comes from a cable. The device may be sent to SHUTDOWN mode by sending a prescribed pulse, but setting the WAKEUP pin low does not put the device into SHUTDOWN mode.

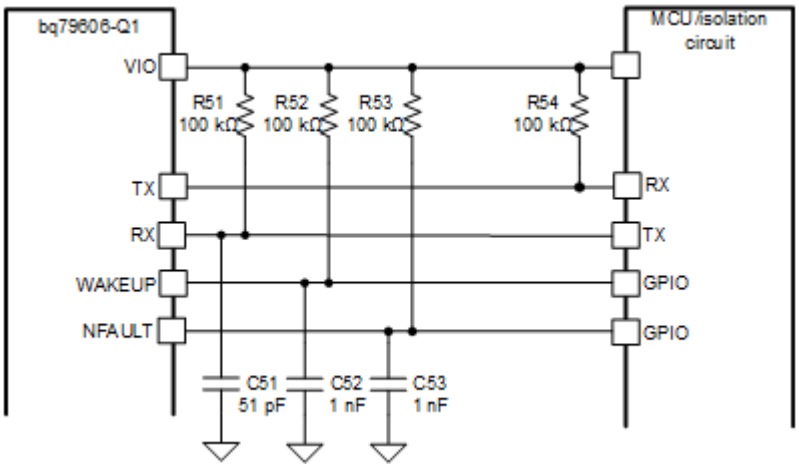


Figure 18. Connecting WAKEUP and Communication for Bottom Device

Stack Device

For stacked devices WAKEUP should be tied to AVSS. The wakeup signal for stack devices comes through the daisy-chain communication interface. Figure 19 shows the WAKEUP configuration for a stack device.

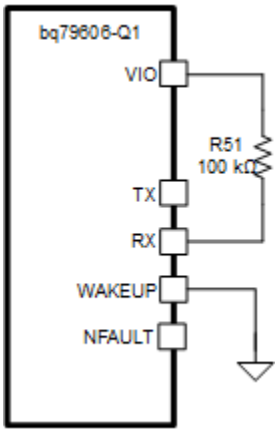


Figure 19. Connecting WAKEUP and Communication for Stacked Device

7.2 Single-Ended Communication

Communication with the BQ79606A-Q1 from a host controller is performed utilizing UART communication protocol. The UART interface connections are shown in Figure 18. Here the TX and RX are being used and will be connected to the host microcontroller or to an isolation circuit. The RX should be pulled high on the BQ79606A-Q1 side with a 10 kΩ - 100 kΩ resistor to VIO. TX should be pulled high on the host side.

NFAULT is an active low fault indicator that, in the event of a fault, will pull low to signal the host that a fault has occurred. Due to this fact the NFAULT pin should have a 100 kΩ pullup resistor to VIO. If the device is a stack device then NFAULT can be left unconnected.

Design Considerations

- For the base device, provide a 100 kΩ pull up resistor to VIO for WAKEUP, NFAULT, and RX on the device side. Pull TX high on the host side.
- For base devices RX is pulled-up to VIO through a 10 kΩ - 100 kΩ resistor. **Do not leave RX unconnected.**When using a serial cable to connect to the host controller, connect the TX pullup on the host side and the RX pullup on the BQ79606A-Q1 side.

- For stacked devices tie WAKEUP toAVSS ground
- For stacked devices leave NFAULTand TX floating
- For stacked devices tie RX to VIO with a 100 kΩ resistor

8 Daisy-Chain Stack Configuration

In the stacked configuration, the main microcontroller first communicates through a BQ79606A-Q1 base device using the UART communications interface. Communication is then relayed up the chain of connected slave BQ79606A-Q1 devices using a proprietary differential communications protocol over AC-coupled differential links interconnected by the COMMH± and COMML± pins. A high level diagram of this can be seen in Figure 14 or Figure 15.

8.1 Communication Line Isolation

Many applications requires multiple, daisy-chained BQ79606A-Q1 devices that are separated by cables or located on the same PCB. The cables can introduce additional challenges and additional components are needed for noisy environments. There are 3 different solutions to this noise problem, capacitor only isolation, capacitor and choke isolation, and transformer isolation. Each of these solutions will be discussed in the following sections

Same PCB

The first solution, capacitor isolation, is best suited for reducing noise and providing voltage isolation for IC's that are located on the same PCB. Figure 20 shows how this configuration would look for two IC's connected on the same PCB. A 10 kΩ termination resistor should be added at the high and low sides. In addition a 49 Ω resistor and 51 pF capacitor should be added on each line on both the high and low side to proved additional filtering. The capacitor should be 2200 pF with a voltage rating twice that of the local cell stack. For example, for a 400 V system, a 800 V capacitor is needed. This configuration should be done on both the COMM± and FAULT± lines.

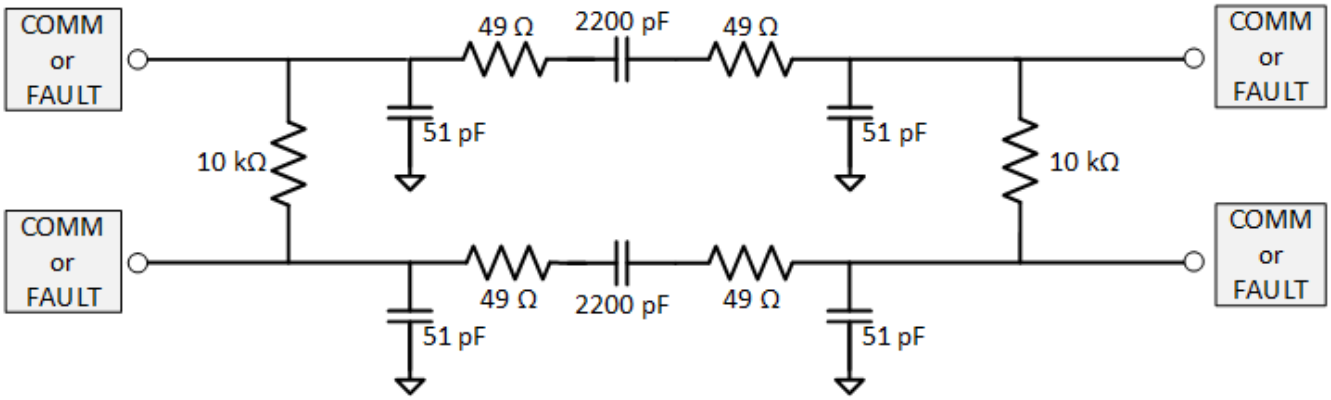


Figure 20. Noise Isolation for Devices on Same PCB

Devices Separated by a Cable (Different PCB's)

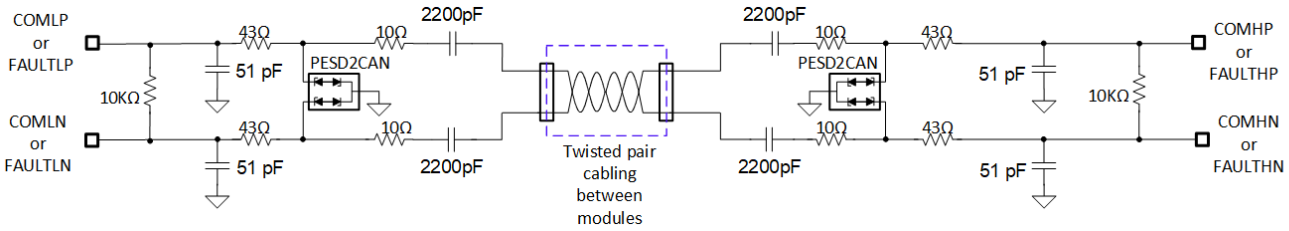
Devices that are separated by a cable (i.e. on different PCB's) require different filtering because the cable introduces new challenges. The first option is capacitive coupling isolation. The second is the implementation of a capacitor and choke. These two options can be seen in Figure 21. The third option is the use of a transformer, seen in Figure 22. In all of these situations the recommendation is based off how long the cable between boards is, and in all cases, twisted pair cabling is used between modules. The main purpose of these noise isolation methods is to remove common mode noise from the signal. More detail can be read in Section 15.

It is recommended that with any design that is chosen that additional ESD protection be added. The PESD2CAN is shown in the following sections to proved ESD isolation on the communication lines.

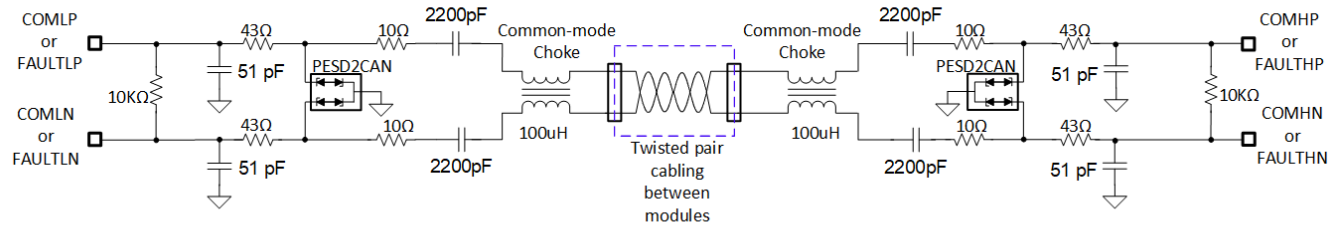
Capacitor & Capacitor/Choke

For capacitor only isolation follow the design in Figure 21 part A. The capacitor should be 2200 pF with a voltage range twice that of the local cell stack. One capacitor is sufficient but if additional safety is needed then two may be used, one at each end of the cable. In this case a 4700 pF capacitor should be used. Capacitance has a direct effect on performance so all intended and parasitic capacitance should be taken into account when choosing components.

If the cable length is greater than 2 m, it is not recommended that capacitor only isolation be implemented. Instead a common mode choke should be added. A single or duel choke can be used. In the dual common-mode filter then a 100 µH and 470 µH should be used. In a single filter mode then the line should have TDK 51 µH 2.8 kΩ choke (part number ACT45B-510-2P-TL003).



A. Components Required for Capacitive Coupled Daisy Chain with Cabling < 2m



B. Components Required for Capacitive Coupled Daisy Chain with Cabling > 2m

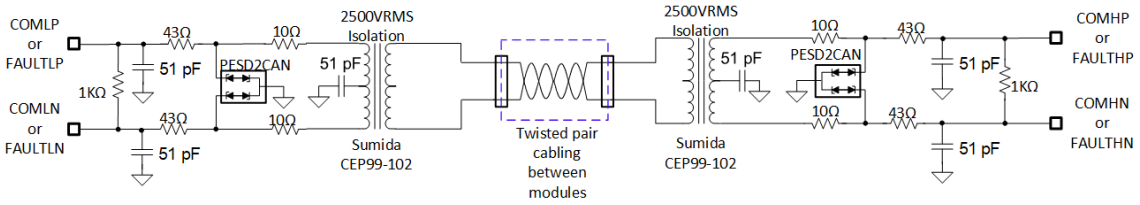
Figure 21. Capacitor Isolation for Devices Separated by Cabling

Transformer Isolation

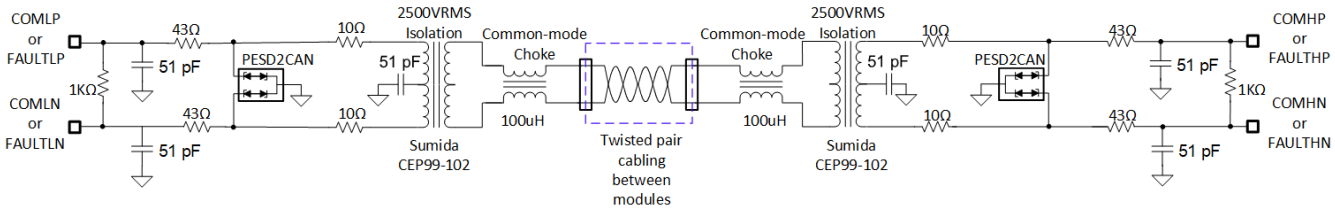
Transformer isolation is the most effective method for removing common mode noise from the system. The two options for this implementation can be seen in Figure 22. The following parameters are recommended for the transformer selection:

- Inductance = 618 µH
- Leakage Inductance = 28.6 µH
- DCR = 1.34 Ω
- Current = 310 mA
- Isolation Voltage = 2500 V, AC

The CDEP99-102 transformer is recommended and needs to be center tapped with a 51 pF capacitor. The transformer can be used on its own or in combination with a choke. Refer to the previous section for choke selection.



A. Components Required for Transformer Coupled Daisy Chain with Cabling < 2m



B. Components Required for Transformer Coupled Daisy Chain with Cabling > 2m

Figure 22. Transformer Isolation for Devices Separated by Cabling

Regardless of which isolation method is chosen, there are a few things that are common among all of them. First is the 51 pF capacitor and 43 Ω resistor before the ESD isolation on both the high and low side on both the positive and negative lines. Second is the 10 Ω resistor on the right side of the ESD isolation on each line.

Finally each design has a termination resistor. The purpose of this resistor is to prevent reflected signals from interfering in the communication. It is recommend that a 10 kΩ be used with capacitor and cap/choke isolation. For transformer isolation is should be 1 kΩ.

8.1 Design Summary

- Follow Table 1 for all communication pins
- For devices located on the same PCB there should be a 2200 pF isolation capacitor on each COMM± and FAULT± line with a voltage rating twice that the cell stack
- In addition to the isolation method there should be a termination resistor at each end of the connection for devices located on the same PCB and for between PCB's.
- There are three types of noise isolation methods that can be employed when communicating via a cable:
  1. Capacitor Only Isolation
     a. Only recommended for cables less than 2 m
  2. Capacitor and Choke Isolation
     a. Cables longer than 2 m
     b. Part number: **ACT45B-510-2P-TL003** for single mode choke
  3. Transformer Isolation
     a. **CDEP99-102** transformer is recommended
- **PESD2CAN** recommended between communication lines to add ESD isolation
- *Any* capacitance present on the communication line will have an effect on the performance. All intentional and parasitic capacitance should be calculated and taken into effect.

8.2 Ring Architecture

The ring architecture of the BQ79606A-Q1 provides another level of safety to the system. If a break were to occur between modules, the host microcontroller would still be able to communicate with those devices that come after the break by switching the communication direction. The COMMH± at the top of stack device needs to be connected to the COMML± of the base device as seen in Figure 14 or Figure 15.

If a response is not received for a pre-determined amount of time then the host needs to perform the follow actions in the order that they are presented

1. Configure the Base Device
   a. Disable High TX and RX
      i. DAISY_CHAIN_CTRL[COMHRX_EN] = 0
      ii. DAISY_CHAIN_CTRL[COMHTX_EN] = 0
   b. Enable Low TX and RX
      i. DAISY_CHAIN_CTRL[COMHRX_EN] = 1
      ii. DAISY_CHAIN_CTRL[COMHTX_EN] = 1
   c. Set the COMMH/COMML and TX/RX functions to be controlled by the DAISY_CHAIN_CTRL register
      i. CONTROL2[DAISY_CHAIN_CTRL_EN] = 1
   d. Reverse the direction of the base and next subsequent commands to go low side
      i. CONTROL1[DIR_SEL] = 1
2. Send a broadcast "Write Reverse Direction" command frame to all devices to switch their direction.
3. Send a broadcast command to clear the CONFIG register of all the devices. This is to clear the CONFIG[TOP_STACK] register.
4. Perform auto addressing
   a. CONTROL1[ADD_WRITE_EN] = 1 (send in a broadcast command)
5. Broadcast address of each device
   a. DEVADD_USR
6. Set the "Top of Stack"
   a. CONFIG[TOP_STACK] = 1 (on top device)

8.3 Re-Clocking

Another BQ79606A-Q1 feature that needs to be highlighted is re-clocking. This means that the BQ79606A-Q1 regenerates each communication signal before it sends it on to the next device. This feature is to prevent compression of a signal as it moves up the stack. Re-clocking generates the ideal waveform but also adds about 3 µs of delay.

Figure 23 shows screen captures from an experiment in which 18 BQ79606A-Q1 EVM's were daisy chained together to observe the bit compression. As it can be seen there is almost no difference in the bit-width between the base and top of stack board. This is due to the re-clocking feature. Re-clocking allows for a longer daisy chain cable between board and also increased the number of stackable devices in the system.

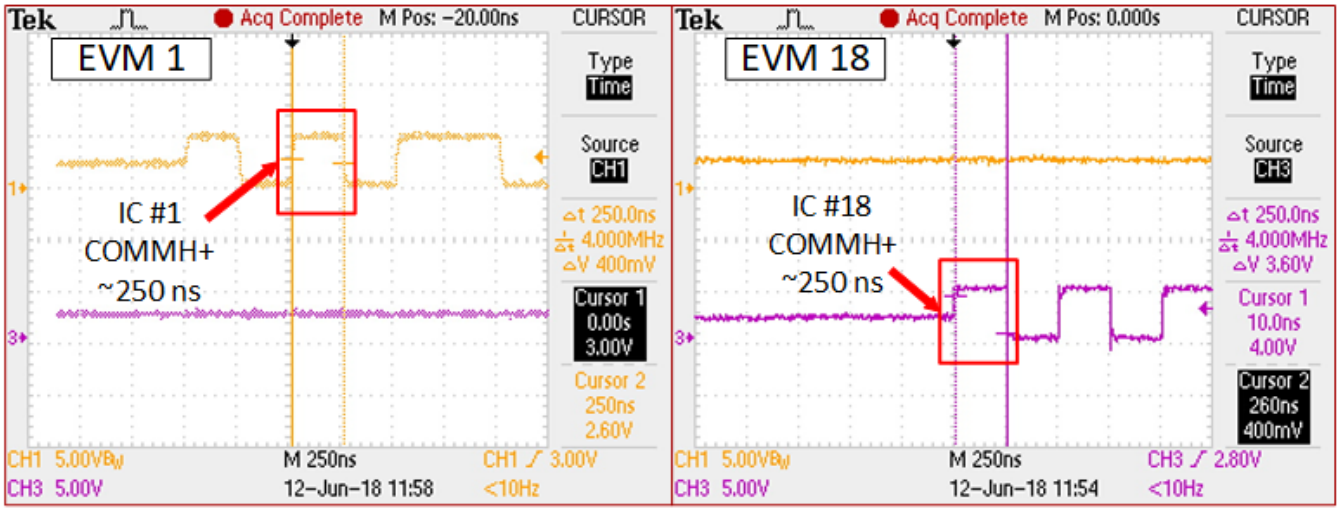


Figure 23. Re-Clocking Bit Compression Example

Design Summary

- Ring architecture allows for the host to continue communication to all devices in the event of a break.
- Re-clocking the communication signals preserves the signal integrity but adds delay into the design.

Table 1. Stack and Single-Ended Communication Check List

List	Pin	Base Device	Stacked Devices	Top of Stack Device
1	RX	10 - 100 kΩ pullup to VIO, 51 pF to GND	10- 100 kΩ pullup to VIO	10- 100 kΩ pullup to VIO
2	TX	10 - 100 kΩPull up on Host side	Float	Float
3	COMML+	COMMH+ of Top of Stack	COMMH+ of lower device	COMMH+ of lower device
4	COMML–	COMMH+ of Top of Stack	COMMH– of lower device	COMMH– of lower device
5	COMMH+	COMML+ of upper device	COMML+ of upper device	COMML+ of Base Device
6	COMMH–	COMML– of upper device	COMML– of upper device	COMML- of Base Device
7	FAULTH+	FAULTL+ of upper device	FAULTL+ of upper device	Float
8	FAULTH–	FAULTL - of upper device	FAULTL- of upper device	Float
9	FAULTL+	Float	FAULTH+ of lower device	FAULTH + of lower device
10	FAULTL-	Float	FAULTH– of lower device	FAULTH– of lower device
11	NFAULT	100 kΩ pullup to VIO, 1 nF to GND	Float	Float
12	WAKEUP	100 kΩ pullup to VIO, 1 nF to GND	Tied to GND	Tied to GND

9 Multi-drop Configuration

An alternative to the daisy-chain configuration is multi-drop. Here all the BQ79606A-Q1 devices are seen as base devices and connected in parallel. This configuration does not support auto-addressing. Figure 24 shows a high level representation of this set up. For more information please refer to the BQ79606A-Q1 data sheet.

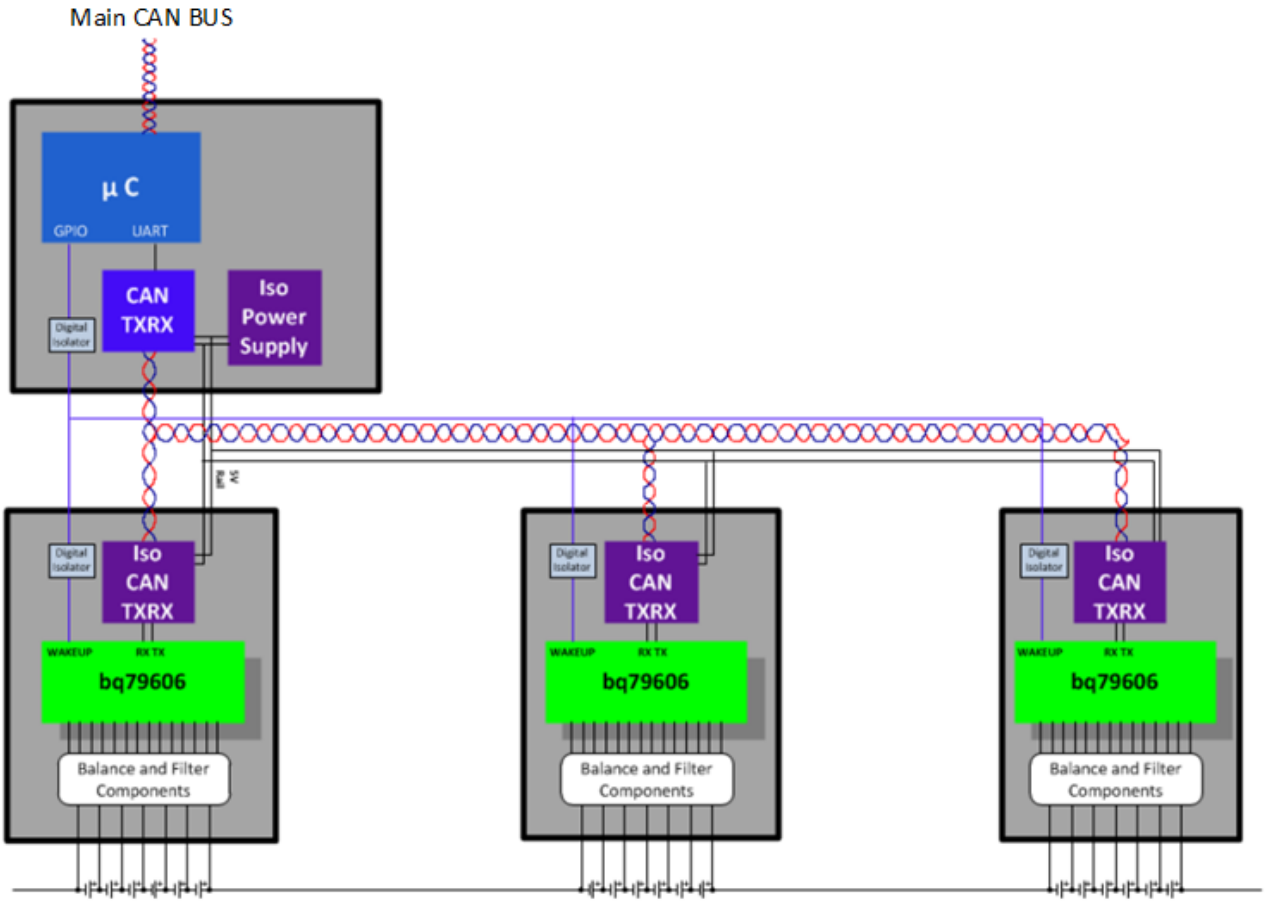


Figure 24. Multi-Drop Configuration

10 Decimation Ratio

The decimation ratio, DR, is directly related to how quickly a conversion result is available. There are 4 different values available and the selection of this value is dependent on conversion time, and effective number of bits (ENOB) as shown in Table 2. This value can be set for the cell or AUX ADC's.

Table 2. DR Conversion Times

CELL_ADC_CONF1[DR] or AUX_ADC_CONF[DR]	Decimation Ratio	Typical ADC Conversion Time (µs)	ENOB
00	32	214 µs	9
10	64	311 µs	11
10	128	503 µs	13
11	256	887 µs	16

The DR works together with the 3rd order SINC filter to produce the voltage signal that will be stored in the register. The DR defines how many samples will be taken and the SINC^3 filter will take the number of samples three times. A high level overview of how this filtering works can be seen in Figure 25.

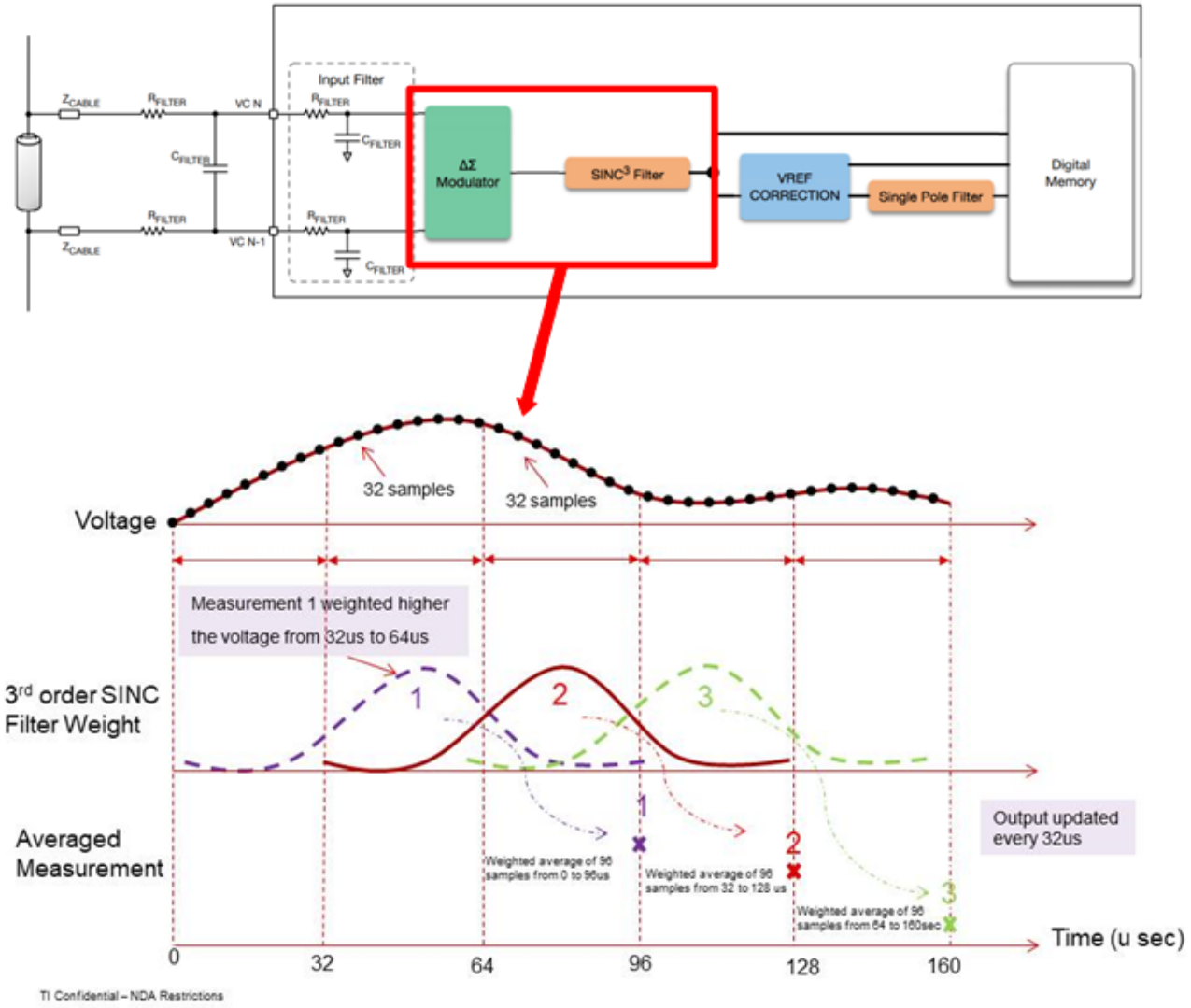


Figure 25. Simplified Signal and Weighting of SINC^3 Filter with DR = 32

11 Digital Low Pass Filter

11.1 Overview

The BQ79606A-Q1 has integrated a digital low pass filter to allow the filtering of much lower frequencies on the cell voltage signal. This filter is a simple, first-order, single pile filter, with a response is similar to that of a regular RC filter. The corrected VREF value is fed into this filter and stored in a register. Figure 26 shows a high level representation of how this LPF works with the rest of the cell voltage process.

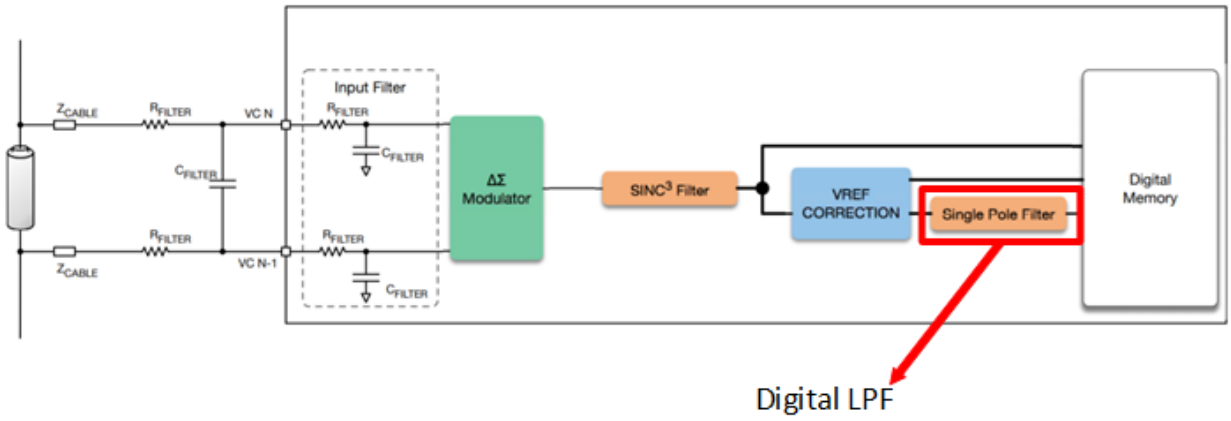


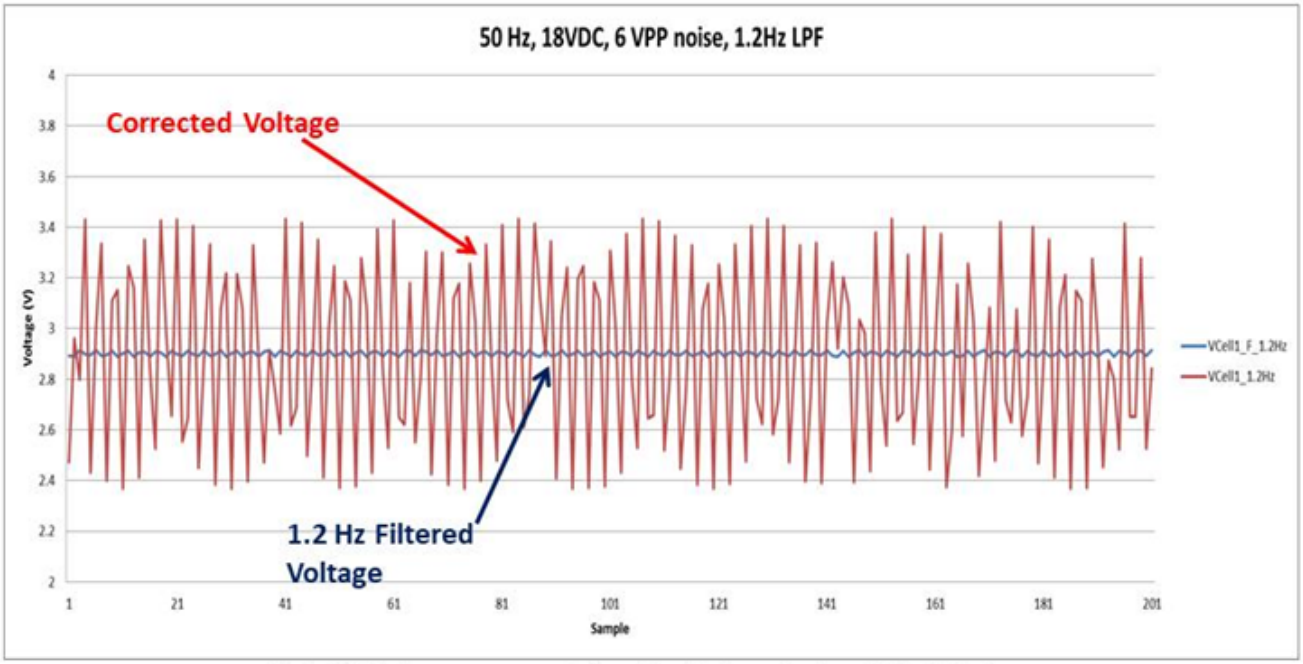
Figure 26. Battery Voltage Signal Chain

The selection of the corner frequency happens by writing a hex value to the CELL_ADC_CONF1[FILSHIFT] register bits. The possible frequencies are listed in Table 3.

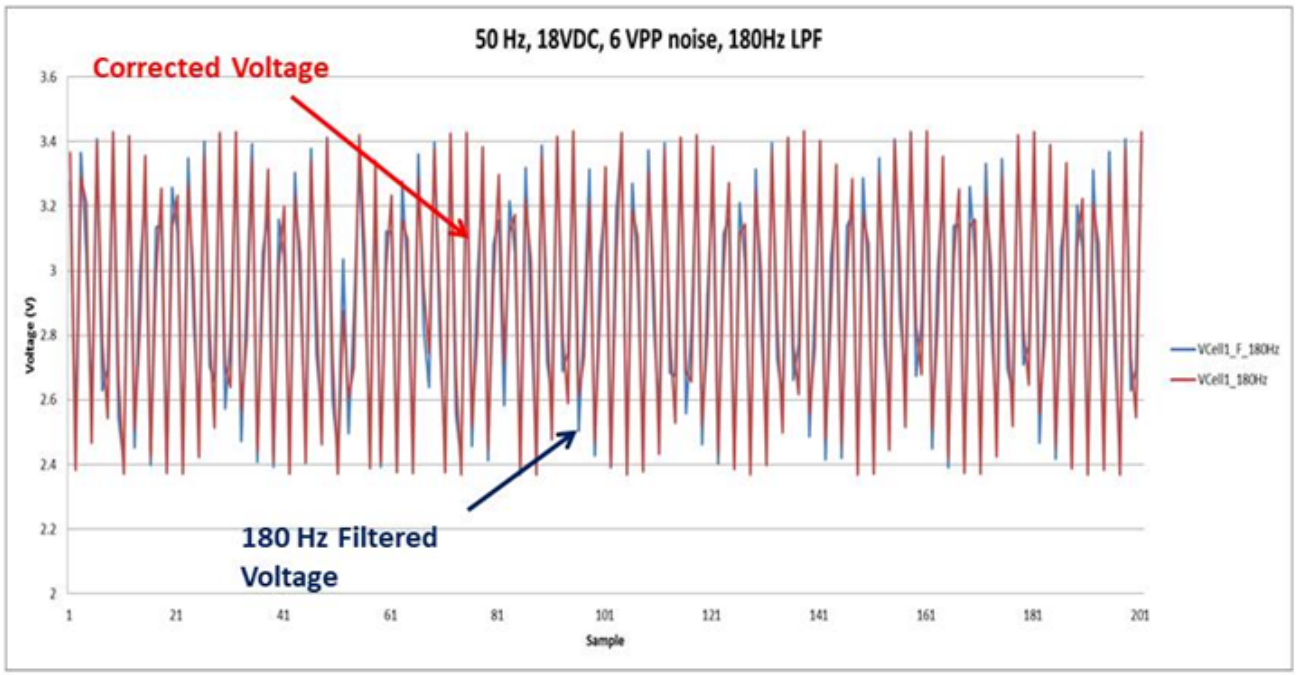
Table 3. Digital Low Pass Filter Corner Frequencies

CELL_ADC_CONF1[FILSHIFT]	Typical Corner Frequency (Hz)
0b000	180.1
0b001	83.1
0b010	40.1
0b011	19.7
0b100	9.8
0b101	4.9
0b110	2.4
0b111	1.2

The implementation of this filter should be highly considered because it allows for the most accurate voltage reading. Figure 27 shows two examples of LPF implementation with a 1.2 Hz and 180 Hz corner frequency. As it can be seen this filter significantly helps in reducing noise and produces a cleaner signal. This experiment was setup by applying a 18 V DC source, and 50 Hz 6 Vpp wave across a resistor ladder network and capturing the LPF data though the GUI.



Note: Cell1 shown as representative data. All channels show similar behavior



Note: Cell1 shown as representative data. All channels show similar behavior

Figure 27. Digital Low Pass Filter Example Plots

ADC Setup for Digital LPF

If using the digital low pass filter then the ADC's need to be set to continuous conversions. To do this the following registers need to be configured.

- CELL_ADC_CTRL (0x109)
  - Set B0 - B5 to 1 to enable each of cells ADC

- CELL_ADC_CONF2 (0x25)
  - Set B3 ([CELL_CONT]) to a 1, enabling continuous ADC Conversion
  - B2, B1, and B0 ([CELL_INT]) set the time interval for the conversions. See Table 4 for the time selection.

Table 4. Continuous ADC Conversion Time Intervals

CELL_ACD_CONF2[CELL_INT]	
000	Minimum timing (starts directly after registers update)
001	1 ms
010	5 ms
011	10 ms
100	50 ms
101	100 ms
110	500 ms
111	1 s

- CONTROL2[CELL_ADC_GO] (0x106)
  - Set B0 to a 1 to start the cell ADC conversions

NOTE The digital low pass filter and the DR are not completely independent of each other. The frequencies stated in Table 3 can only happen if a DR of 256 is chosen. If any other DR is selected then the actual corner frequency will be different. Follow the formula in Equation 3 for calculation of the actual corner frequency. Where the desired frequency is the one found in Table 3 and DR is the selected decimation ratio from Table 2.

$$Corner\ \ Frequency\ \ = \ \ (Desired\ \ Frequency) \ \ \times \ \ \left(\frac{256}{DR}\right) \tag{3}$$

12 ADC Post Calibration

The delta sigma ADC accuracy can shift during soldering/baking. Therefore post-manufacturing calibration might be necessary . The gain and offset of each cell ADC can be programmed with the steps outlined in this section. The gain can be adjusted ±19.4 mV while the offset can be adjusted ± 24.2 mV. This correction does not apply to the GPIO channels.

Before performing any calibration, take note of the following:

- Perform correction at room temperature
- Use a stable, high-accuracy DC source and/or voltmeter
- The registers contain signed 2's complement values
  - VIN1 and VIN2 are the two measurement points taken during correction
  - 0 in either register = no correction

12.1 Gain Error Correction

For a 5 V cell voltage,±19.4 mV in 255 steps (8 bits) in the CELL*_GAIN registers (one per channel) Procedure:

1. Set the CELL ADC to 1 MHz frequency, 256 Decimation Ration, Corner frequency to 1.2 Hz for best results
2. Apply voltage VIN1, read back from ADC VOUT1 in the VCELL*_LF, VCELL*_HF registers, and record both.
3. Apply voltage VIN2, read back from ADC VOUT2 in the VCELL*_LF, VCELL*_HF registers, and record both.
4. Find the gain error correction (GEC) at 5 V (5 V is used regardless of VINx value) and write the 8-bit value to the CELL*_GAIN register with the following steps
   a. Calculate slope m with Equation 4. Where VOUT are from steps 2 and 3.

$$m = \frac{(VOUT2 - VOUT1)}{(VIN2 - VIN1)} \quad (4)$$

b. The gain error is calculated at 5 V with Equation 5

$$Gain\ Error = (5V \times m) - 5V \quad (5)$$

c. The Gain Shift value is 0.15 mV.

$$Gain\ Shift = \frac{19.4\ mV \times 2}{255} = 0.15\ mV \quad (6)$$

d. Take the negative of the gain and divide it by the gain shift to find bit shift needed with Equation 7.

$$Bit\ Shift = \frac{-Gain\ Error}{Gain\ Shift} \quad (7)$$

e. Convert bit shift to a two's complement hex value

f. Make sure that if the bit shift is greater than "127", the hex value will be "7F".

g. Make sure that if the bit shift is less than "-128", the hex value will be "80".

h. Finally enter the calculated Hex value to CELL*_Gain

5. Repeat steps 1-3 on each cell voltage
6. Perform the steps in Offset Error Correction (Section 12.2)

12.2 Offset Error

Offset Error Correction: ± 24.2 mV in 255 steps (8 bits) in the CELL*_OFF registers (one per channel) Use recorded, VIN1, and VOUT1 from the Gain Error Correction procedure. Procedure:

1. Find the offset value based on the VIN1 and VOUT1 value with Equation 8

$$Offset = \frac{VIN1 - VOUT1}{190.7348\ \mu V} \quad (8)$$

2. Convert to a two's complement hex value
3. Make sure that if the offset is greater than "127", the hex value will be "7F"
4. Make sure that if the offset is less than "-128", the hex value will be "80"
5. Write the 8-bit values to the Cell*_OFF register
6. Repeat steps 1 - 5 on each cell voltage
7. Save the new values to OTP by following the NVM programming procedure (found in the BQ79606A-Q1 data sheet)
8. The OTP CRC must be re-calculated and saved due to this change

13 Layout Considerations

Since the BQ79606A-Q1 measures small changes in voltage, care must be taken in the layout of signals to and from the device to avoid coupling noise onto sensitive inputs. The layout of ground and power connections, as well as communication signals should also be made carefully. Designing a good layout is critical to achieving the best ADC accuracy, thermal performance, EMI performance and so on. In this section the layout of ground, power and communication signals are discussed.

The isolation caps must be placed close to the edge of the board. The Common Mode Chokes must be close to the daisy-chain cable connector to provide a high-impedance path to common-mode noise as it enters the board. Place the series resistors and TVS diodes next to the BQ79606A-Q1.

Ground and VSS

The BQ79606A-Q1 has 4 device grounds, AVSS (pin 15 and 45), CVSS (pin 26), and DVSS (pin35) and creation of a good ground plane in the layout is critical to getting optimal performance. All these, including PAD, should connect to the ground plane with the shortest track sections possible. This is to reduce the impact of stray inductance on the system. A good ground plane on a dedicated layer will improve measurement accuracy, reduce noise, and provide the necessary ESD, EMI, and EMC performance.

There is a strong recommendation to have a minimum of four layers in the PCB, with one fully dedicated as an unbroken VSS plane (except thermal reliefs). Avoid placing tracks on this layer to maintain the unbroken integrity of the plane structure. Figure 28 shows a high level depiction of what the layout should look like.

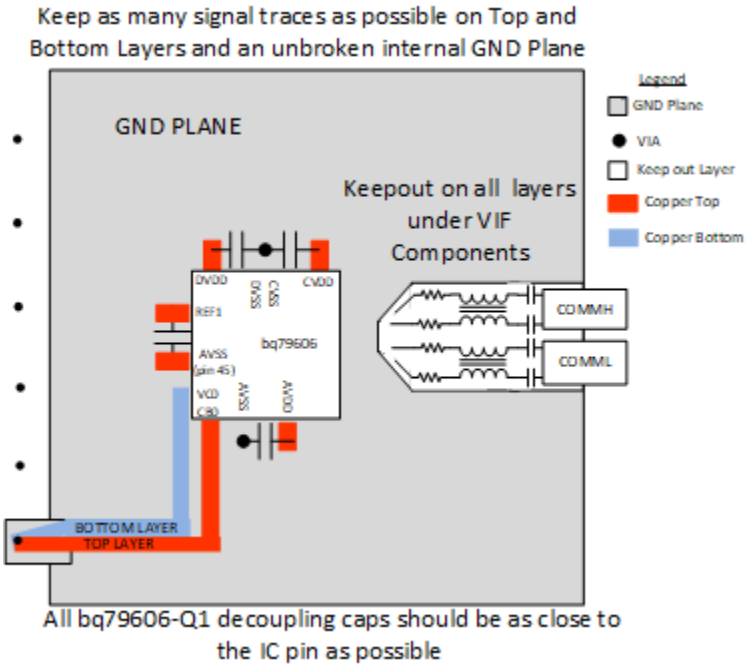


Figure 28. Simplified Layout Guidelines

Differential Communication

Maintaining signal integrity while in a stacked configuration is critical to the success of this part. In order to maximize immunity to interfering signals there are a couple design choices that need to be made. For transformer based communication, be sure to select a transformer that provides isolation appropriate for the specific application so ignore point number 5.

1. Keep wires and PCB traces as short as possible. Do not exceed datasheet recommendations.
2. For any single-signal pair between two nodes (ICs), individual wires and traces should have the same length.
3. Unshielded, twisted-pair wiring is required for any cable runs.
4. Run PCB traces in parallel, on the same layer, without any other traces or planes in between. Long runs should avoid noisy traces and/or be stitched at intervals similar to twisted-pair wire.
5. Use high-quality capacitors for voltage isolation between ICs and place in close physical proximity to each other as part of the parallel-track layout

Power Supplies and References

There are three more pins that need to be address specifically, REF1 (pin 46), TSREF (pin 43), and VLDO (pin 39). All of these pins are used as a reference point for some other function in the system and therefore it is critical that bypass capacitors be placed as close to the pins as possible, as described in Section 2.

The REF1 bypass capacitor needs to be placed as close as possible to the REF1 and AVSS pin 45 to ensure the trace is noise free.

Cell Balancing Connections

To achieve the best thermal performance with the BQ79606A-Q1 in regards to the cell balancing connections, it is important to ensure proper trace width based on the desired balancing current. When designing the layout for this section, please determine the thickness of the trace based on both balancing current and thermal performance.

Bypass Capacitors

Through this document there was mention of bypass capacitors on several pins. **These capacitors need to be placed as close to the pin as possible in order to reduce stray inductance and allow them to be as effective as possible.**

14 BCI Performance

Bulk Current Injection (BCI) was performed according to the ISO 11452-4 standard. The cable length was 1.7 m with a baud rate of 1 Mbps. The BCI noise was injected on the communication lines. There where 3 different isolation methods that were tested: capacitive only, cap & choke, and transformer.

Figure 29 shows the results from using capacitive only isolation on the communication lines. Figure 30 shows the corresponding schematic to achieve these results.

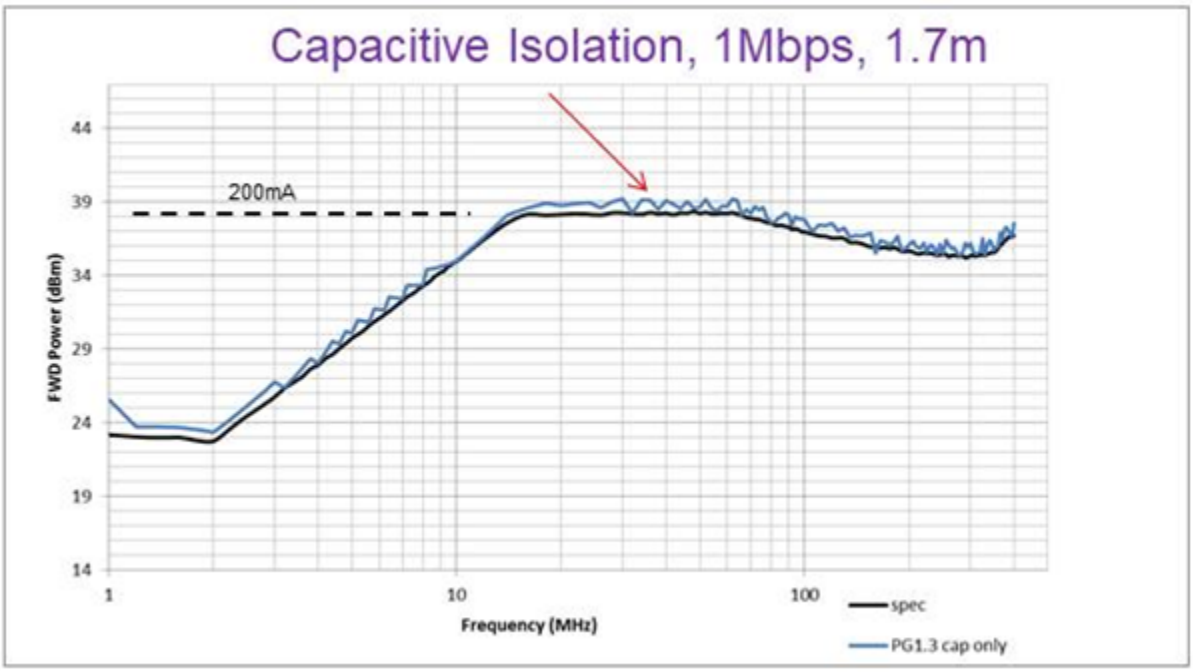


Figure 29. Capacitive Isolation BCI Plot

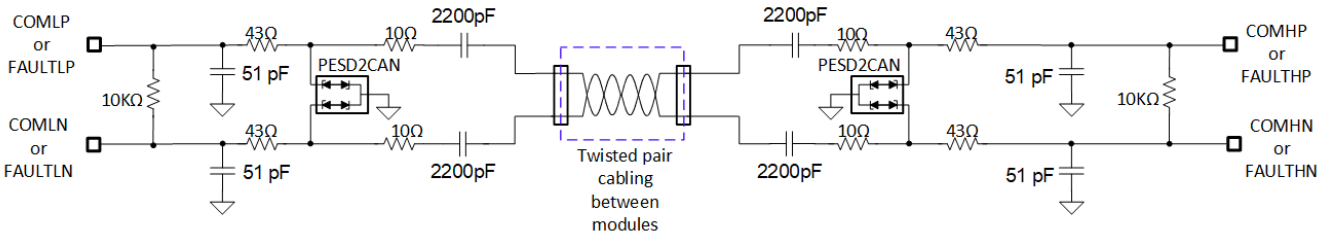


Figure 30. Capacitive Only Isolation Schematic

This second graph shown in Figure 31 is the comparison between Cap & Choke and Transformer Isolation. Already these two methods are much better than capacitive only isolation. The ISO standard have been added to better view where these methods stand. If the Cap & Choke is what will be used then follow the schematic for component selection (see Figure 32). If transformer isolation is desired then follow the schematic shown in Figure 33.

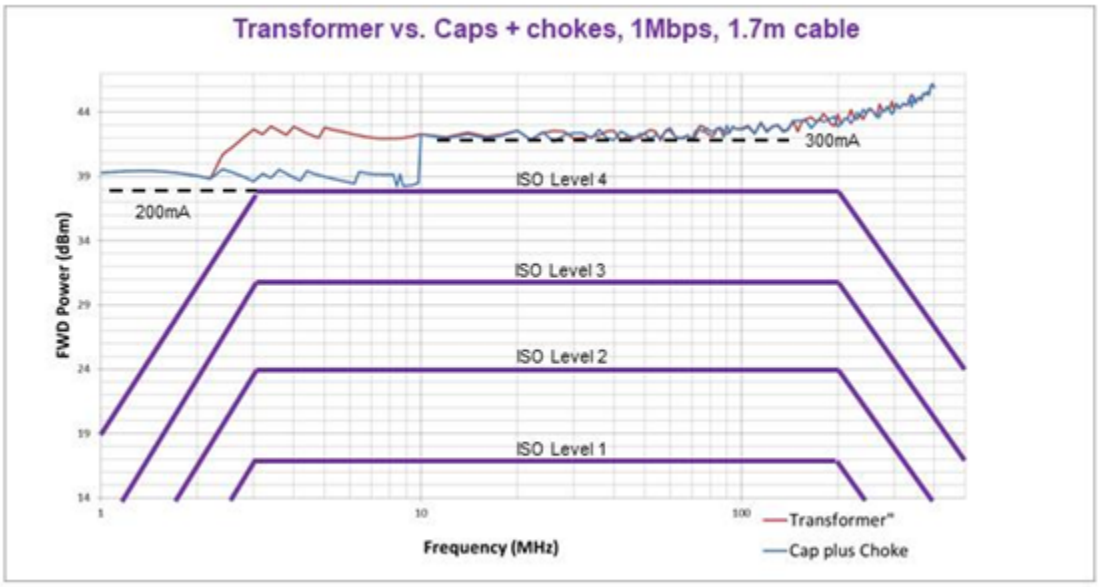


Figure 31. Transformer vs Cap & Choke BCI Plot

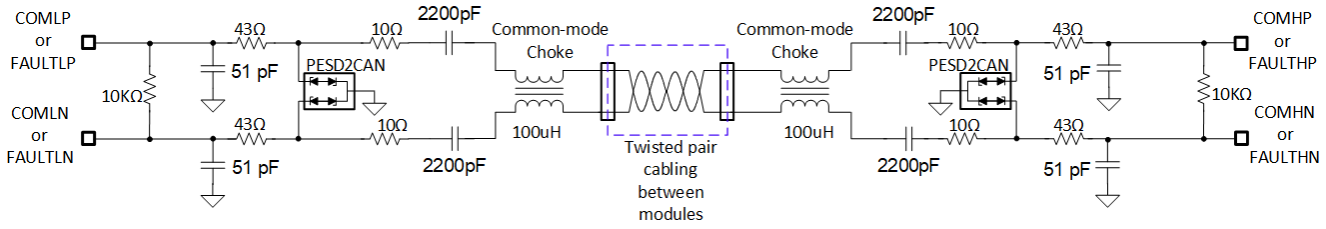


Figure 32. Cap & Choke Isolation Schematic

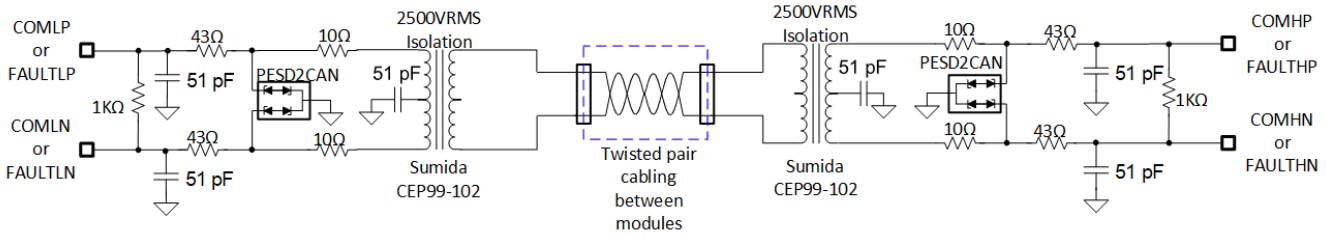


Figure 33. Transformer Isolation Schematic

15 Common and Differential Mode Noises

X-Y caps are commonly used and may be required for extremely noisy environments

- Differential mode noise goes out one wire and returns back on another wire. An X capacitor is placed between two lines to suppress the noise.
- Common mode noise goes out from both wires and returns back to the chassis through stray capacitance to ground. A Y capacitor is placed between the chassis as Figure 34 illustrates.

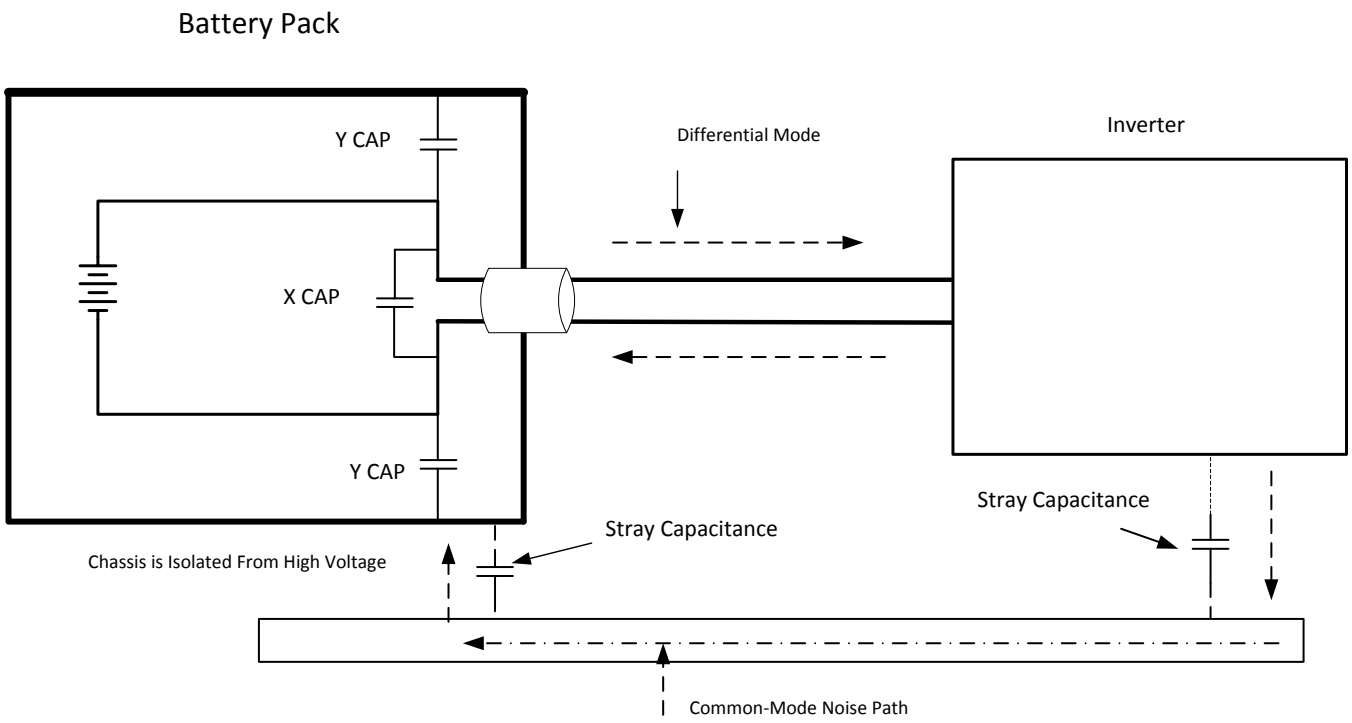


Figure 34. XY Caps

Design Considerations

- Device placement is important. Daisy-chain cable should not be resting on bus-bar or mental enclosure surface.

16 EMC Susceptibility on Cell Inputs

Additional components may be necessary to improve EMC performance of the BQ79606A-Q1 in automotive applications with electrically noisy environments.

- Use ferrite beads or small inductors in series with the cell inputs between the cell output and the series resistor to the VCn input. The bead and small capacitor must be located near each other.
- Add a 0.0033-µF capacitor from each cell input to the battery pack (BAT0 in Figure 35). Adjust the value of capacitance to satisfy the PCB layout and field conditions for the application.

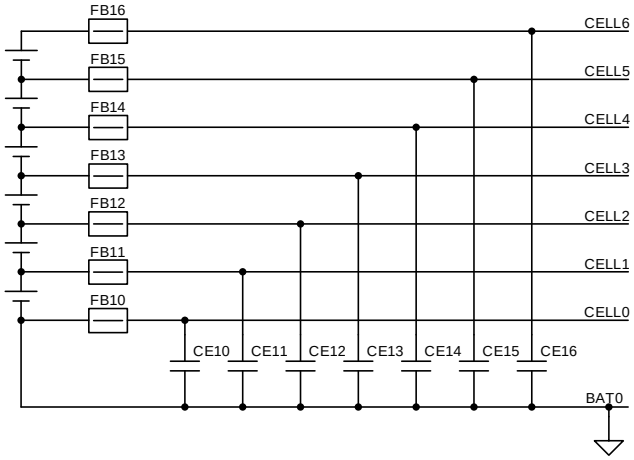


Figure 35. EMC Filter

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (December 2018) to C Revision	Page
• Changed all instances of BQ79606/BQ79606-Q1 to BQ79606A/Bq79606-Q1.	1

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