Application Report
SLUA966A–May 2019–Revised December 2019

Migrating to UCC25640x from UCC25630x

ABSTRACT

The UCC25640x LLC controller family is tailored for applications requiring low standby power as well as low audible noise and is pin-to-pin compatible with the UCC25630x. This application report walks through key differences between the UCC25640x and UCC25630x LLC controller families.

Contents

List of Figures

List of Tables

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1 Introduction

The purpose of this document is to explain the differences between the UCC25640x and UCC25630x LLC controller families and demonstrate how to migrate the UCC256404 to an existing design. The naming convention of the UCC25640x matches that of the UCC25630x. The new device ending in UCC256403 has a similar feature set to UCC256303 as shown in Table 1. The same is true for the new UCC256402 and UCC256404 compared to the older UCC256302 and UCC256304. summarizes the key differences between the UCC25630x and UCC25640x device families

Table 1. Device Comparison Table

	UCC256302	UCC256303	UCC256304	UCC256402	UCC256403	UCC256404
Burst Mode Algorithm	15 pulses in each burst packet	15 pulses in each burst packet	15 pulses in each burst packet	• 16 pulses in each burst packet • No burst soft on/off • User option to disable burst mode • User adjustable burst mode hysteresis	• 40 pulses in each burst packet • Burst soft on/off • User option to disable burst mode • User adjustable burst mode hysteresis	• 40 pulses in each burst packet • Burst soft on/off • User option to disable burst mode • User adjustable burst mode hysteresis
HV Startup	Yes	No	Yes	Yes	No	Yes
X-Cap Discharge	No	No	Yes	No	No	Yes
Minimum Detectable Slew Rate	1 V/ns	1 V/ns	1 V/ns	0.1 V/ns	0.1 V/ns	0.1 V/ns
BLK Start Threshold	3 V	3 V	1 V	3 V	3 V	1 V
BLK Stop Threshold	2.2 V	2.2 V	0.9 V	2.2 V	2.2 V	0.9 V
RVCC Voltage	12 V	12 V	12 V	13 V	13 V	13 V
OCP2 Threshold	0.84 V	0.84 V	0.84 V	0.6 V	0.6 V	0.6 V
OCP3 Threshold	0.64 V	0.64 V	0.64 V	0.43 V	0.43 V	0.43 V
FB Pin Clamp	No	No	No	Yes	Yes	Yes

2 Burst Pattern

To satisfy standards such as CoC Tier 2 and DOE Level VI, good light-load efficiency is needed. This is especially challenging for LLC converters, which require a minimum amount of circulating resonant current to maintain regulation of the output voltage. The UCC25630x and UCC25640x address this with the inclusion of a burst mode function to reduce standby power and improve light-load efficiency. While this enables LLC designs to greatly improve standby power performance, this can lead to audible noise in some designs, depending on the transformer construction. The UCC25640x addresses this by using a tailored burst pattern to minimize audible noise where transformer current is slowly increased at the beginning of a burst packet and slowly decreased at the end of a burst packet. This burst algorithm avoids sharp changes in the LLC transformer current, which can lead to mechanical oscillation of the transformer and result in transformer “humming”.

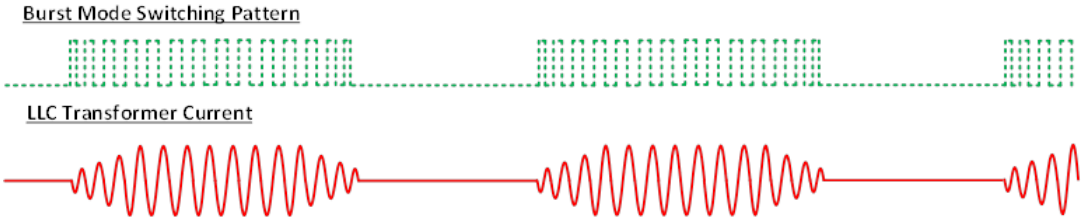

Figure 1. UCC256403/UCC256404 Burst Mode Pattern

In addition, the UCC256403 and UCC256404 has a larger minimum number of switching cycles within a burst packet compared to the UCC25630x. This allows for a much lower burst packet frequency at standby to further avoid the audible switching frequency range.

Table 2. Switching Packet Size Comparison

	UCC25630x	UCC256402	UCC256403/UCC256404
Minimum number of switching cycles per burst packet	15	16	40

3 Improved Adaptive Dead Time Control

The UCC25640x and UCC25630x use adaptive dead time control where the switch node is monitored to detect when the switch node is done “slewing” to either V_{IN} or ground before turning on the next MOSFET.

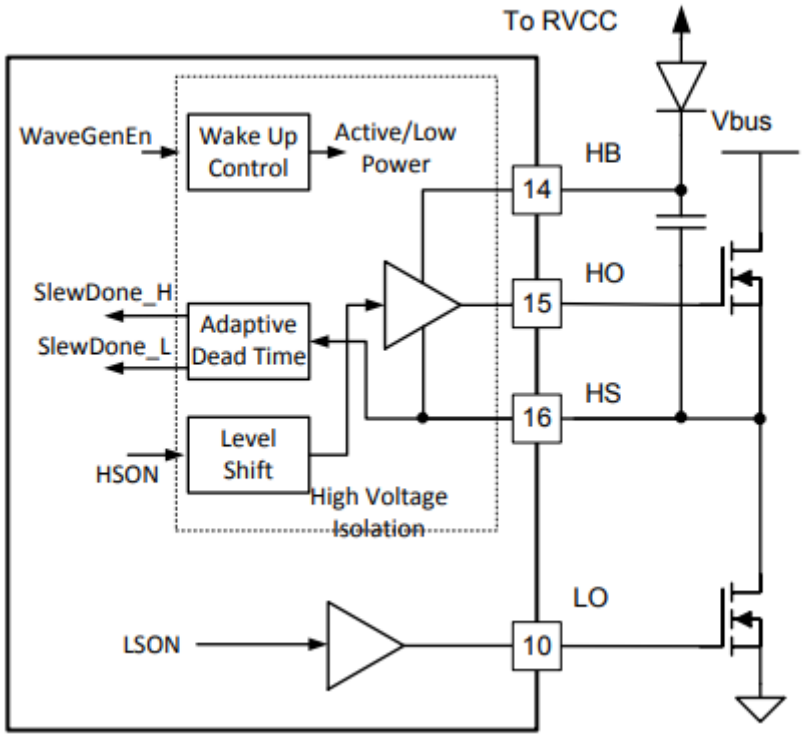

Figure 2. Adaptive Dead Time Control

While the UCC25630x is capable of detecting switch node slew rates as low as 1 V/ns, the UCC25640x is capable of detecting switch node slew rates down to 0.1 V/ns. A more sensitive slew rate detector provides numerous benefits. More capacitance on the switch node can be tolerated with a more sensitive slew rate detector, meaning MOSFETs with larger C_{OSS} can be used or larger switch node snubber capacitance can be used to meet EMI requirements. The slew rate detector is only used to determine the dead time between high side off – low side on. The UCC25640x includes a dead time copy feature to match the dead time between low side off – high side on and high side off – low side on. This feature ensures proper switching behavior and reliability.

4 Startup Configurability

The UCC25630x designs rely on the capacitance of the VCR pin to set the switching frequency profile during soft start. In addition, the initial soft start voltage in the UCC25630x is fixed at 0 V. For certain VCR configurations, this can lead to an initial switching frequency that is quite high. The UCC25640x adds the ability to program an initial voltage onto the soft-start pin to shift the initial switching frequency lower. The UCC25640x incorporates a programming period before the converter starts switching where the LL/SS voltage is allowed to charge up from RVCC. This charging period allows for a precharge voltage to develop on the soft-start capacitor which reduces the switching frequency profile during start-up. This configurability allows the designer a second degree of freedom to limit the maximum switching frequency during start-up to ensure zero voltage switching.

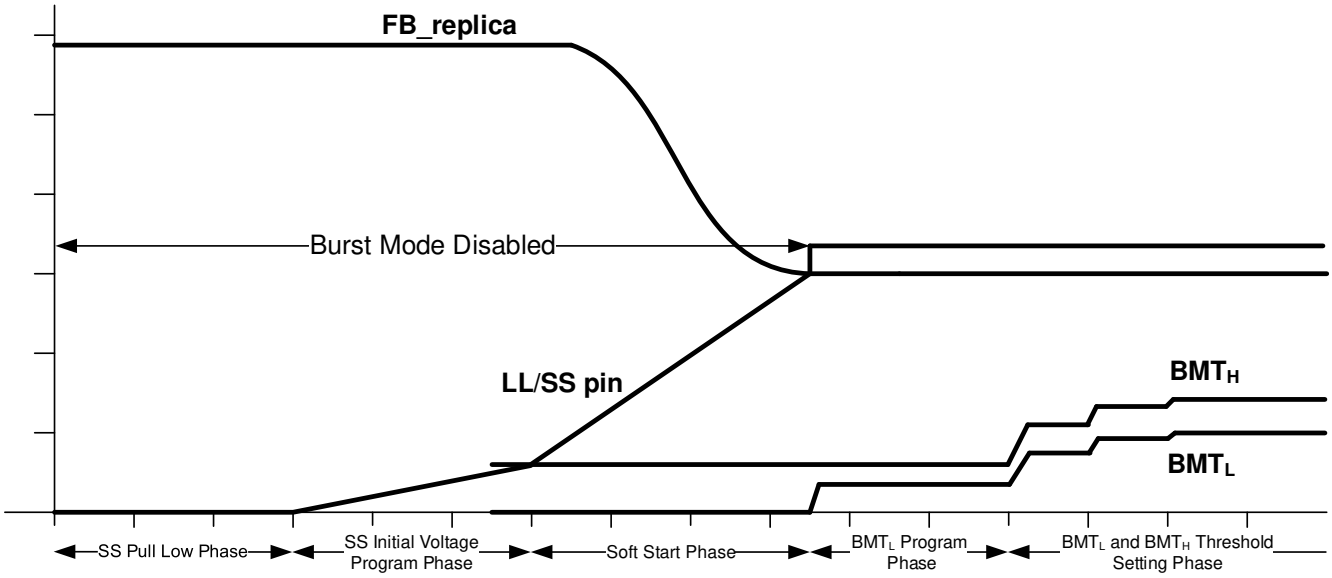

Figure 3. LL/SS Precharge

Unlike the UCC25630x, the BLK pin voltage is not buffered onto the LL/SS pin. Instead, a static 3.5 V is buffered onto the LL/SS pin for burst mode programming of the BMT_H threshold.

5 FB Pin Clamp

At very light loads, the opto-coupler can draw large current causing opto-coupler saturation. Once the opto-coupler is saturated, there is a delay to bring the opto-coupler out of saturation, which can lead to poor transient performance. For the UCC25630x, a resistor and Zener are typically added between RVCC and the FB pin to avoid opto-coupler saturation by sourcing more current to the opto-coupler when the FB pin voltage reduces. For the UCC256404, if the opto-coupler demands greater than I_{FB}, a secondary current source is enabled to supply more current to the opto and avoid saturation. This integrated clamp makes the external resistor and Zener unnecessary for most designs.

6 RVCC Voltage

While the RVCC voltage of the UCC25630x is 12 V, the RVCC voltage of the UCC25640x is increased to 13 V. This allows the UCC25640x controller family to power PFC controllers with slightly higher UVLO thresholds such as the UCC28180 directly from the RVCC pin.

7 Migrating from UCC25630x to UCC25640x

The UCC25630x and UCC25640x are pin-to-pin compatible and can be interchanged. This section describes how to migrate an existing design from the UCC25630x to UCC25640x.

7.1 ISNS Pin

While the OCP1 detection threshold of the UCC25630x and UCC25640x are the same, the OCP2 and OCP3 detection thresholds are reduced by approximately 40% in UCC25640x. The greater margin between OCP1 and OCP2 and OCP3 helps avoid overcurrent fault during full load start-up.

To accommodate the change in OCP2 and OCP3 thresholds, the ISNS resistor connected between ISNS and gnd should be reduced by 40%.

Table 3. OCP Thresholds

	UCC25630x	UCC25640x
OCP1 Detection Threshold	4 V	4 V
OCP2 Detection Threshold	0.84 V	0.6 V
OCP3 Detection Threshold	0.64 V	0.43 V

7.2 LL/SS Pin

For the UCC25640x, this pin is used to program two values: the initial soft-start voltage and the burst threshold, BMT_H. Programming an initial voltage onto the LL/SS pin provides a second degree of freedom to limit the maximum switching frequency during start-up. Both the precharge voltage and the burst mode threshold are programmed through an external resistor divider connected from RVCC to LL/SS.

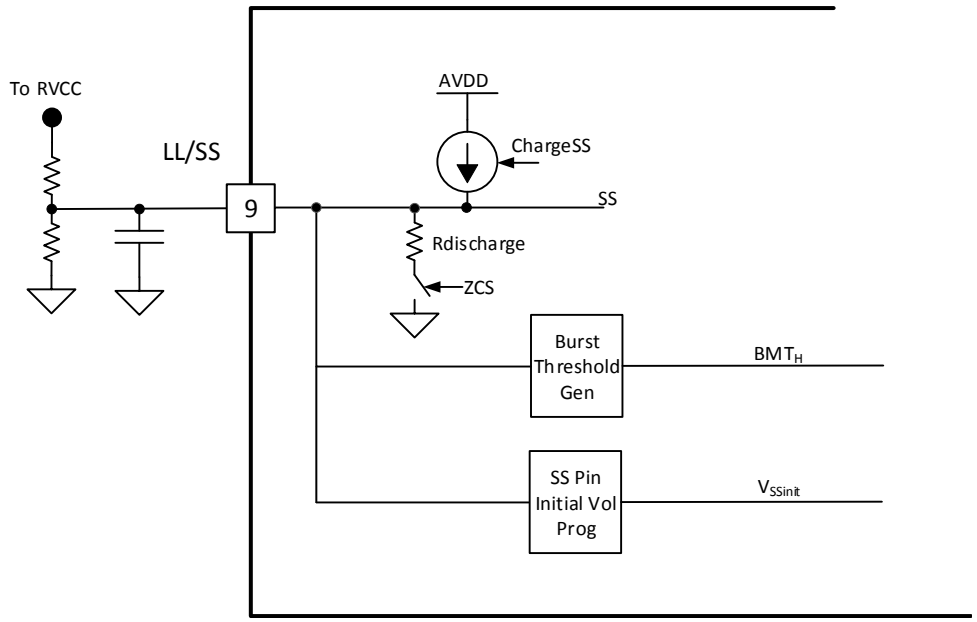

Figure 4. LL/SS Programming

The suggested ranges for LL/SS offset voltage and BMT_H burst threshold are the following:

$$0\ V < V_{ssinit} < 1\ V \quad (1)$$

$$0.2\ V < V_{BMT\_H} < 4\ V \quad (2)$$

To determine the LL/SS resistor values, first select a soft-start capacitance based on the required maximum start-up time. This can be estimated based on the expected maximum peak-to-peak voltage on VCR.

$$C_{SS} = I_{SS} \times \frac{T_{SS\_Max}}{V_{VCR(pk-pk)} - V_{ssinit}} = 37.5\mu A \times \frac{T_{SS\_Max}}{V_{VCR(pk-pk)} - V_{ssinit}} \quad (3)$$

After the soft-start capacitance has been selected, calculate the required programming current on the LL/SS pin to give the desired BMT_H burst mode threshold.

$$I_{BMT} = \frac{V_{BMT\_H}}{R_{LL}} = \frac{V_{BMT\_H}}{98k\Omega} \quad (4)$$

After the required programming current is determined, calculate the required equivalent voltage, V_{TH}, and equivalent resistance, R_{TH}, on the LL/SS pin that satisfies both the required precharge voltage on LL/SS and the required burst mode threshold.

$$V_{TH} = \frac{3.5\ V}{1 - \frac{I_{BMT}}{V_{ssinit}}\left(1.2k\Omega + \frac{t_{ssinitVolPrgm}}{C_{SS}}\right)} = \frac{3.5\ V}{1 - \frac{I_{BMT}}{V_{ssinit}}\left(1.2k\Omega + \frac{776\mu s}{C_{SS}}\right)} \quad (5)$$

$$R_{TH} = \frac{V_{TH} - 3.5V}{I_{BMT}} \quad (6)$$

After V_{TH} and R_{TH} have been found, the upper and lower resistance values on the LL/SS pin can be calculated.

$$R_{LL/SS\_Upper} = \frac{R_{TH} \times RVCC}{V_{TH}} = \frac{R_{TH} \times 13\ V}{V_{TH}} \quad (7)$$

$$R_{LL/SS\_Lower} = \frac{R_{TH} \times R_{LL/SS\_Upper}}{R_{LL/SS\_Upper} - R_{TH}} \quad (8)$$

Note that a UCC25640x design calculator is available to perform these calculations.

7.3 BW Pin

BW serves as a dual purpose pin for the UCC25640x functioning as an output overvoltage detection pin as well as programming the threshold between burst mode entry threshold and burst mode exit threshold. Figure 3 shows the timing of relevant signals used in BW programming.

The ratio between low frequency and high frequency burst is set by the equivalent resistance between the BW pin and ground. A 54-µA current source is fed to the pin and the resulting voltage programs the burst threshold ratio during the start-up phase.

$$R_{BWth} = \frac{R_{BWUpper} \times R_{BWLower}}{R_{BWUpper} + R_{BWLower}} \quad (9)$$

$$V_{BWconfig} = R_{BWth} \times I_{BWconfig} \quad (10)$$

Table 4. Burst Mode Threshold Configuration on the BW Pin

BMT CONFIGURATION NAME	BMT LOW/HIGH RATIO	BW PIN EQUIVALENT RESISTANCE (R_{BWth})
User Option 1	0.95	> 24 730 Ω
User Option 2	1	17 125 Ω – 19 976 Ω
User Option 3	0.9	12 562 Ω – 13 624 Ω
User Option 4	0.8	90 18 Ω – 9 813 Ω
User Option 5	0.6 (No Vssinit)	6 478 Ω – 6 849 Ω
User Option 6	0.6	4 450 Ω – 4 732 Ω
User Option 7	0.4 (Burst disabled)	2 422 Ω – 3 038 Ω

7.4 Using UCC256404 on UCC25630-1EVM-291

Despite the differences described above, the UCC25640x is pin-to-pin compatible with the UCC25630x. Any design with the old device can be modified with the new one. An example presented here shows how UCC25630-1EVM-291 is modified to work with UCC256404. The changes in Table 5 must be made to the UCC25630-1EVM-291. Changes can also be seen on the modified schematic in Figure 5.

Table 5. List of Changes on UCC25630-1EVM-291

COMPONENT	ORIGINAL VALUE	NEW VALUE	REASONS
R4	140 kΩ	41.2 kΩ	UCC256404 has a different BLK Start threshold than UCC256301. The recommended value is given in the design calculator.
R13	357 Ω	237 Ω	ISNS resistor must be reduced to account for smaller OCP2/OCP3 thresholds.
R14	732 kΩ	267 kΩ	LL/SS upper resistor value is determined by setting desired burst mode threshold for exit equal to 1.2 V in the design calculator.
R15	402 kΩ	147 kΩ	LL/SS lower resistor value is determined by setting desired burst mode threshold for exit equal to 1.2 V in the design calculator.
R17	42.2 kΩ	41.2 kΩ	BW upper resistor value is determined by setting the burst mode threshold entry and exit ratio to 0.6 (User Option 5) in the design calculator.
R18	10 kΩ	8.06 kΩ	BW lower resistor value is determined by setting the burst mode threshold entry and exit ratio to 0.6 (User Option 5) in the design calculator.
R20	6.04 kΩ	1 kΩ	R20 is decreased to prevent opto-coupler saturation and reduce gain to maintain stable compensation.
C28	0.047 µF	0.01 µF	Compensation adjustment to improve burst mode pattern
R22	10 kΩ	33.2 kΩ	Adjustment to keep compensation zero in the same location
C17	0.15 µF	0.056 µF	Decrease start-up time

7.4.1 Schematic

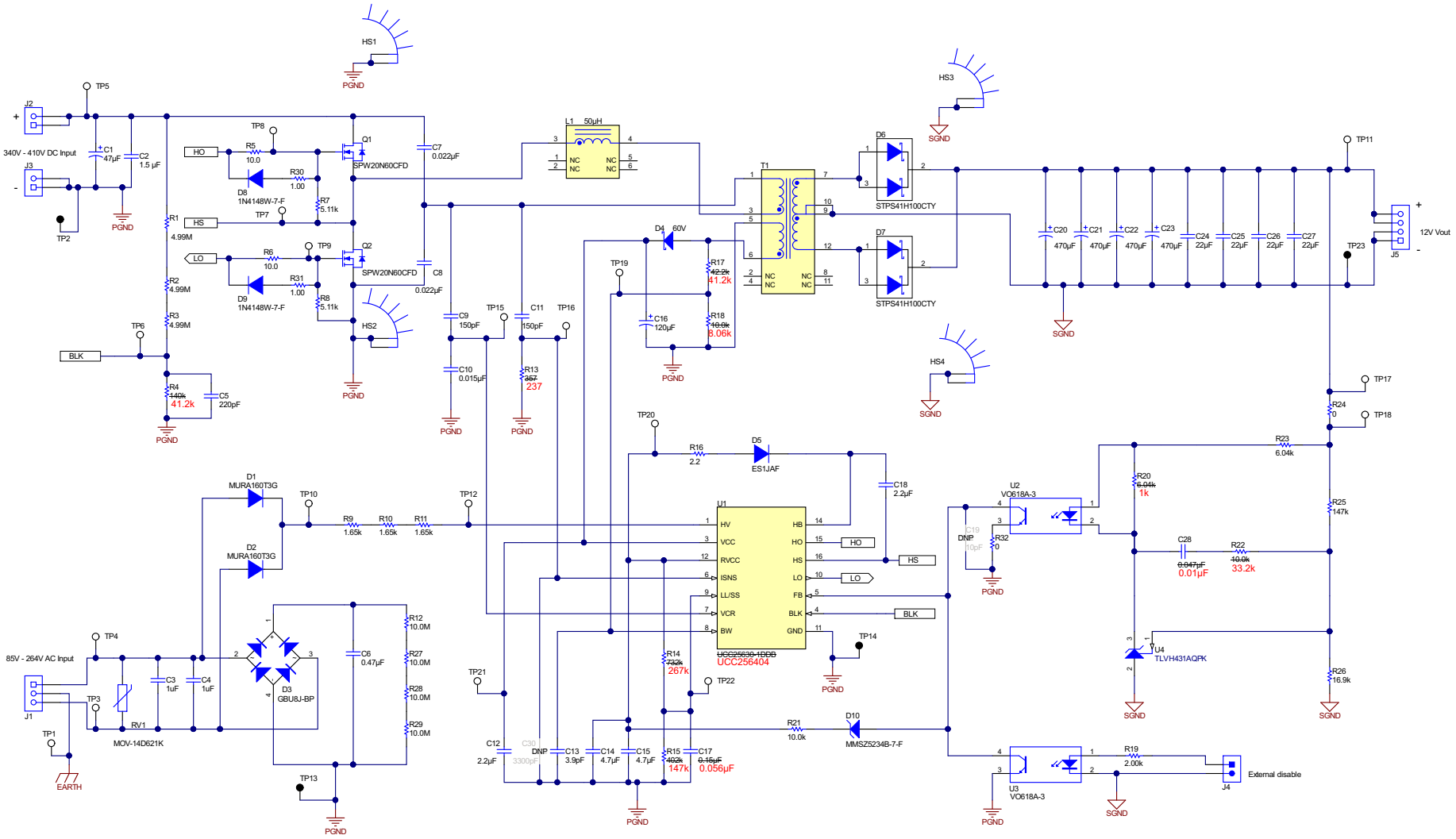

Figure 5. UCC25630-1EVM-291 Modified Schematic

7.5 Performance of UCC256404 on UCC25630-1EVM-291

Performance data is taken on UCC25630-1EVM-291 after implementing the changes from Section 7.4. The *UCC25630-1EVM-291 User's Guide* shows the baseline measurements for the UCC25630x on the original EVM.

7.5.1 Standby and Light Load Power

Table 6 lists the total standby power measurement for the standalone EVM. The average input power is measured over a two minute interval.

Table 6. Standby and Light Load Power

I_{OUT} (mA)	V_{OUT} (V)	P_{OUT} (mW)	V_{IN} (V)	I_{IN} (mA)	P_{IN} (mW)
0	12.06	0.0	389.82	0.137	53.31
10.97	12.06	132.30	389.82	0.570	222.21
20.97	12.06	252.90	389.82	0.970	378.01
50.95	12.05	613.95	389.81	2.177	848.61
100.90	12.05	1215.85	389.79	4.168	1624.75

7.5.2 Efficiency

Figure 6 illustrates the EVM efficiency graph.

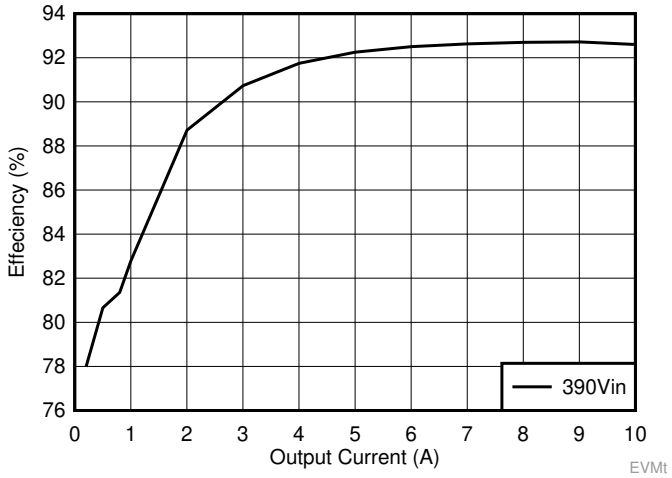

Figure 6. Efficiency

7.5.3 Audible Noise

Figure 7 and Figure 8 show the audible noise measurements during burst mode operation. The measurements are performed in a soundproof container with the microphone 5 mm above the transformer.

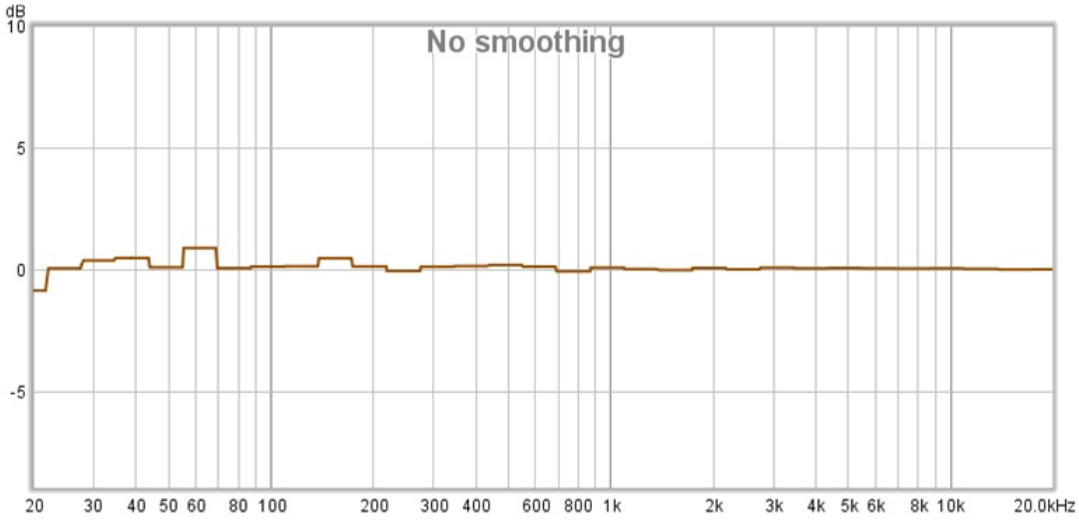

Figure 7. Audible Noise Measurement at 10 mA Load

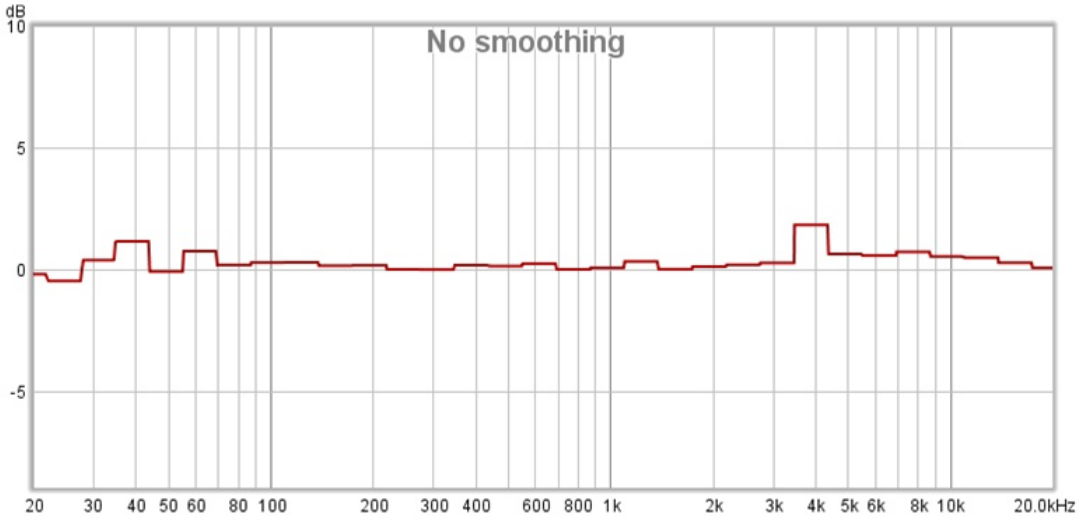

Figure 8. Audible Noise Measurement at 500 mA Load

7.5.4 Steady State

The following waveforms show the resonant capacitor voltage (VCR) and low-side gate voltage (LO) with 115 VAC, 60 Hz applied to the AC input, and 390 VDC applied to the DC input. Figure 9 and Figure 10 show the waveforms during burst mode.

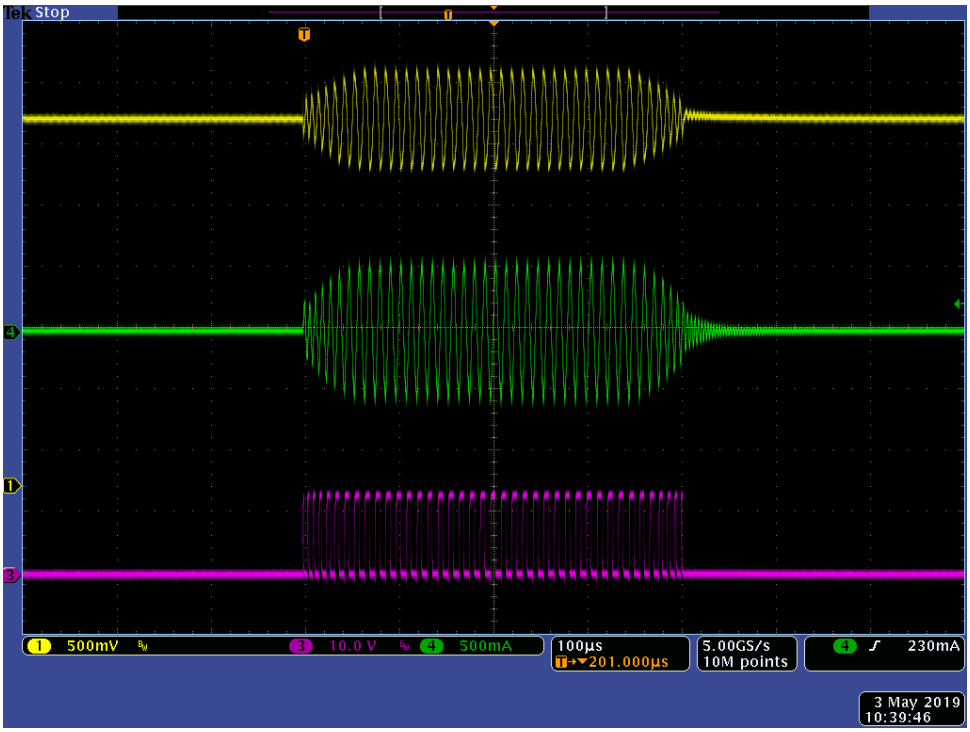

Figure 9. Steady State Waveforms at 10 mA Load (Ch1 = VCR; Ch3 = LO)

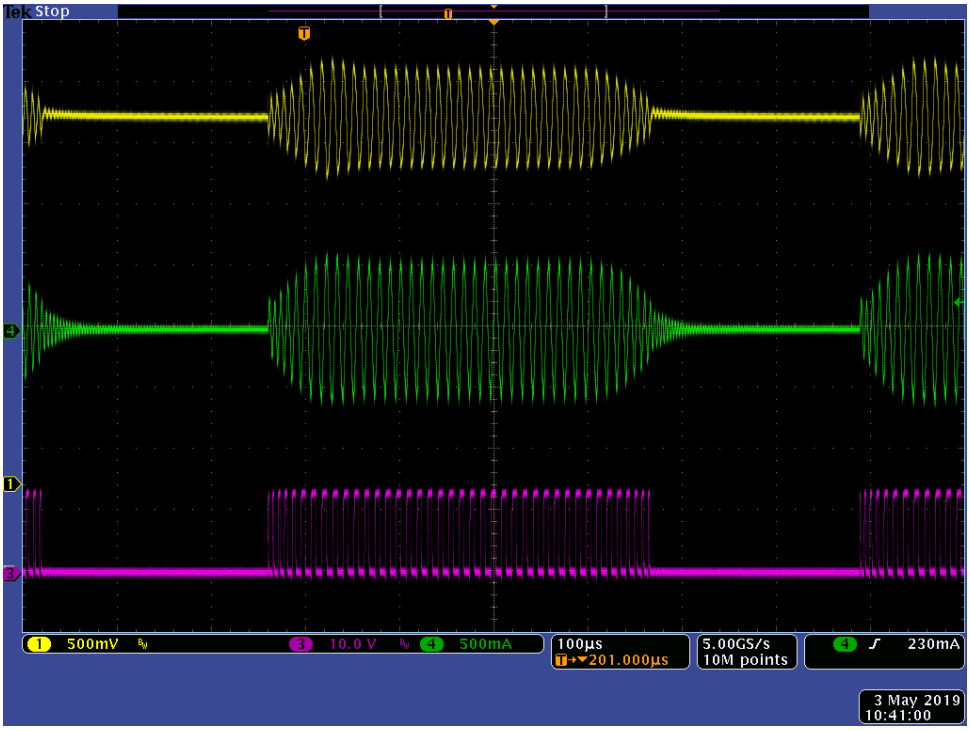

Figure 10. Steady State Waveforms at 500 mA Load (Ch1 = VCR; Ch3 = LO)

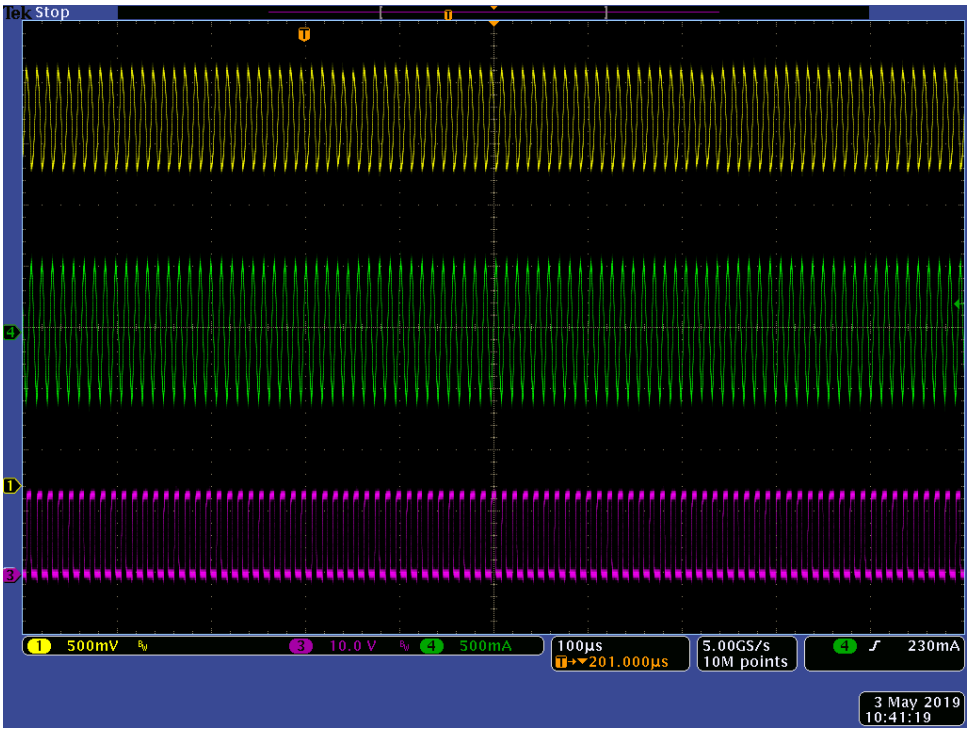

Figure 11. Steady State Waveforms at 1 A Load (Ch1 = VCR; Ch3 = LO)

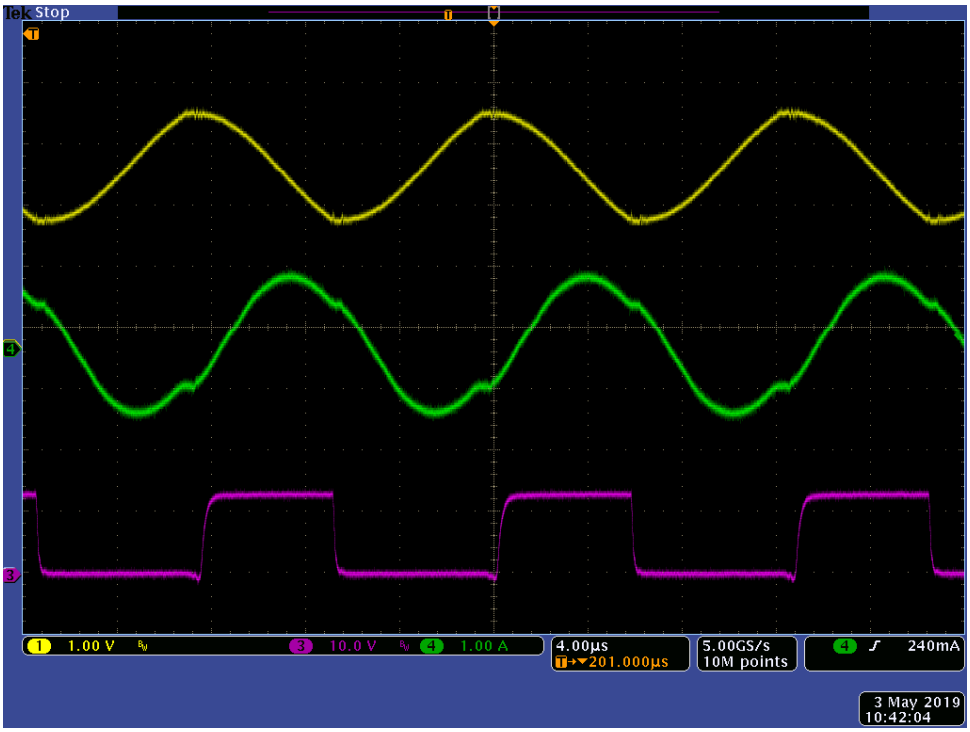

Figure 12. Steady State Waveforms at 10 A Load (Ch1 = VCR; Ch3 = LO)

7.5.5 Load Transient

The following waveforms show the output voltage with 115 VAC, 60 Hz applied to the AC input, and 390 VDC applied to the DC input.

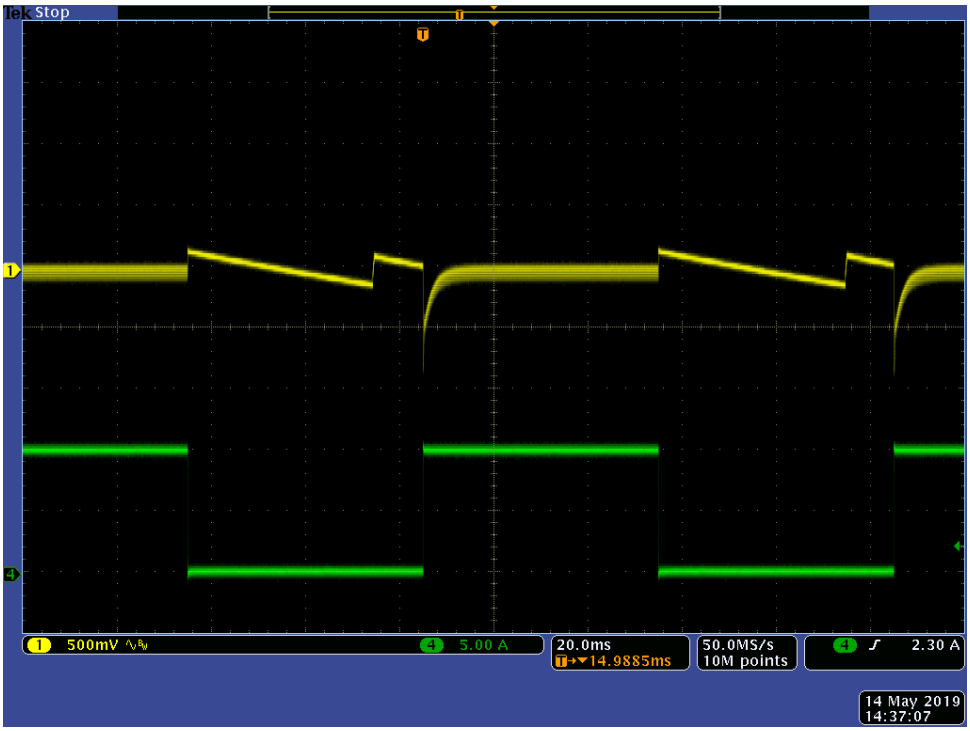

Figure 13. 10 mA to 10 A Transient (Ch1=V_{OUT}; Ch4 = I_{OUT})

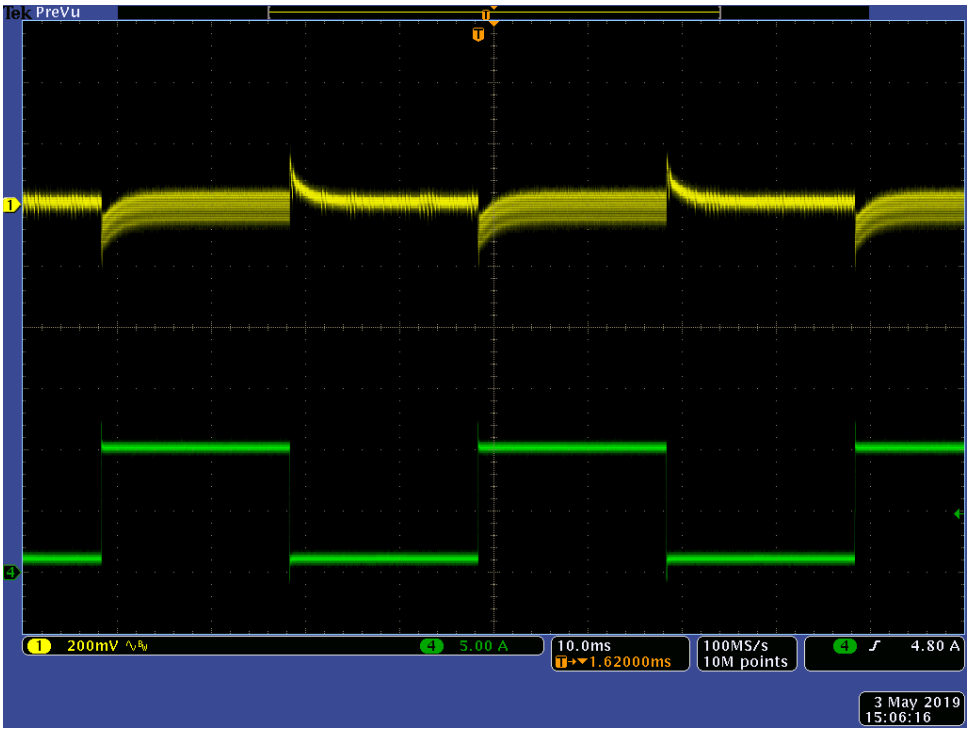

Figure 14. 1 A to 10 A Transient (Ch1=V_{OUT}; Ch4 = I_{OUT})

7.5.6 Loop Response

Figure 15 shows the loop response with 115 VAC, 60 Hz applied to the AC input, and 390 VDC applied to the DC input.

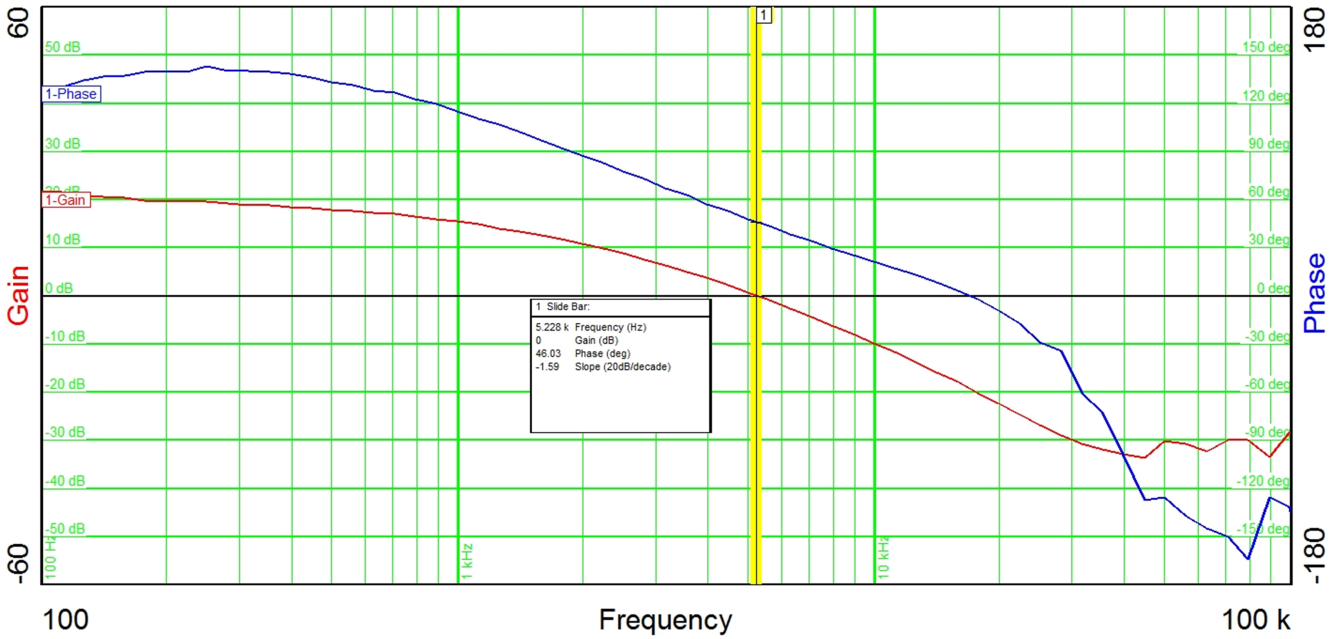

Figure 15. Bode Plot at 10 A Load

8 Summary

The UCC25630x and UCC25640x are both LLC controller families offering excellent standby power and transient response performance with a rich feature set. The UCC25640x includes additional features to allow for greater flexibility in the LLC converter design as well as features to mitigate audible noise without sacrificing standby power performance. The additional features of UCC25640x allow for reduction in BOM count and superior system performance.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2019) to A Revision	Page
• Edited application report for clarity	1
• Added the UCC256402 to Table 1	2
• Added the UCC256402 to Table 2	3
• Changed LL/SS Resistor Equations to reflect updated programming method in *Section 7.2*	6
• Changed Table 4 to match the latest silicon burst mode threshold user options	7

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