Application Note

MOSFET Selection with the TPS53211

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ABSTRACT

Proper MOSFET Selection for Integrated Driver BUCK switching regulator controllers like the TPS53211 is a critical element of voltage regulator design. However, in addition to selecting MOSFETs for efficient voltage conversion, proper operation of the TPS53211 requires designers to consider some additional MOSFET parameters such as the total gate drive current and gate charge of the low-side MOFET. With these constraints in mind, the TPS53211 controller can provide efficient and effective regulation of low voltage rails up to 20 A of load current.

Table of Contents

1 Introduction....2
2 MOSFET Selection for TPS53211 Synchronous BUCK controller....2
3 Summary....3
4 References....4

Trademarks

1 Introduction

The TPS53211 1.5-V to 19-V, single phase PWM buck controller with light load efficiency provides the control of a high-efficiency switch-mode buck voltage regulator. The TPS53211 uses external enhancement mode N-channel MOSFET switches to convert the input voltage to a regulated output voltage. In this applications note, we will review TI's guidelines and recommendations for selection of the MOSFETs for use with the TPS53211. Following these guidelines will simplify the design process and provide cost effective, efficient conversion while avoiding potential design issues that can be associated with inappropriate MOSFET selections.

2 MOSFET Selection for TPS53211 Synchronous BUCK controller

Efficiency of energy conversion, useful output power divided by total input power, is one of the fundamental performance metrics of a voltage regulator. With BUCK regulator controllers like the TPS53211, selection of the power stage, especially the power MOSFETS, is critical to optimizing the performance of the converter.

Maximizing efficiency is most effectively seen as minimizing loss factors, such as RDSON conduction losses, switch transition losses and gate drive losses for the external power FETs. Since larger MOSFETs with lower RDSON typically have higher gate charge and thus gate drive and switching losses, minimizing loss and maximizing efficiency is best considered as a balance between these loss factors. Minimum loss and thus maximum efficiency occurs when gate-charge driven losses, such as switch transition and gate drive losses, and RDSON driven conduction losses are equal. Further reducing one increases the other more than the prior is reduced.

One method for selecting MOSFETs with the optimum RDSON versus Gate Charge ratio is called the J/K method. In this method, J represents the MOSFET gate-charge related switching and gate drive losses while K represents the RDSON conduction related losses.

Control (High-side) MOSFET

$$J = 10^{-9}\left(\frac{V_{IN} \times I_{OUT}}{I_{DRIVE}} + \frac{Q_G}{Q_{SW}} \times V_{DRIVE}\right) f_{SW} \left(W/nC\right) \quad (1)$$

$$K = 10^{-3}\left({I_{OUT}}^2 + 1/12 {I_{pp}}^2\right) \times \frac{V_{OUT}}{V_{IN}} \left(W/m\Omega\right) \quad (2)$$

Rectifying (Low-side) MOSFET

$$J = 10^{-9}\left(\frac{V_{fd} \times I_{OUT}}{I_{DRIVE}} + \frac{Q_G}{Q_{SW}} \times V_{DRIVE}\right) f_{SW} \left(W/nC\right) \quad (3)$$

$$K = 10^{-3}\left({I_{OUT}}^2 + 1/12 {I_{pp}}^2\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \left(W/m\Omega\right) \quad (4)$$

With the optimum MOSFET at the operating condition of V_{IN} to V_{OUT} @ I_{OUT} having the $R_{DS(ON)}$ / Q_{sw} = J / K.

For more about optimized MOSFET selection and balancing gate-charge and conduction losses using the J/K Method see – The J/K Method: A Technique for Selecting the Optimal MOSFET.

1. Limit total gate drive current to less than 50 mA to avoid overloading the internal VCCDR regulator.
   a. When VCCDR is not powered by an external supply, VCCDR is powered by an internal 6.5-V linear regulator powered from VCC. The VCCDR regulator's current limit can be as low as 50 mA, so the total gate charge of all high-side and low-side MOSFETs times the switching frequency should be less than 50 mA. For example, with a 500 kHz switching frequency, the combined gate charge of all MOSFETs should be less than 100 nC.
2. Limit Low-side FET gate charge to less than 55 nC
   a. During the turn-off of the low-side MOSFET, the low-side FET gate charge is discharged through LGATE to the GND pin. The high current and duration of this discharge can disrupt the GND pin when the total low-side FET gate charge is greater than 55 nC
   b. If low-side MOSFETs with total gate charge greater than 55 nC must be used, 1-Ω-2.2-Ω series resistors need to be added between LGATE and the MOSEFT gate pins to limit the discharge current.
3. If multiple MOSFETs are used in parallel, each needs to use its own series gate resistor

a. While multiple MOSFETs are unusual for the TPS53211 controller, given the limited gate-drive current and low-side FET gate charge, if multiple MOSFETs are used, each MOSFET have a separate gate resistor.
b. Since each MOSFET will have a slightly different gate threshold voltage, using separate resistors allows parallel MOSFETs maintain separate gate-source voltages during their switch transition, balancing their switching losses.

Within these limitations, the TPS53211 can drive a wide range of Power MOSFETs and meet the efficiency requirements of most applications. To reduce switching and gate-driver losses at currents below critical conduction mode, the TPS53211 includes an “auto-skip” function that switches to discontinuous conduction mode with diode emulation of the low-side FET and reduced the switching frequency with Pulse Frequency Modulation when the load current is less than ½ of the continuous conduction peak to peak inductor ripple current.

3 Summary

The TPS53211 Synchronous BUCK controller uses external MOSFETs. The selection of the MOSFETs used with the TPS53211 will determine the power conversion efficiency. Designers need to use a MOSFET selection optimization technique such as the J/K method for selecting MOSFETs that provide the best performance within the cost and size constraints of the design.

While rare, if designers choose to use parallel MOSFETs for the High-Side or Low-Side MOSFETs, separate series resistor need to be used for each parallel MOSFET.

In addition, designers need to limit the total gate drive current to less than 50 mA and the total low-side FET gate capacitance at Vgs = 6.5 V to less than 55 nC.

4 References

- The J/K Method: A Technique for Selecting the Optimal MOSFET
- Texas Instruments, *TPS53211 1.5-V to 19-V, Single Phase PWM Buck Controller with Light-Load Efficiency* product folder
- *Single-Phase PWM Controller with Light-Load Efficiency Optimization* data sheet

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