Functional Safety Information

UCC28C4x-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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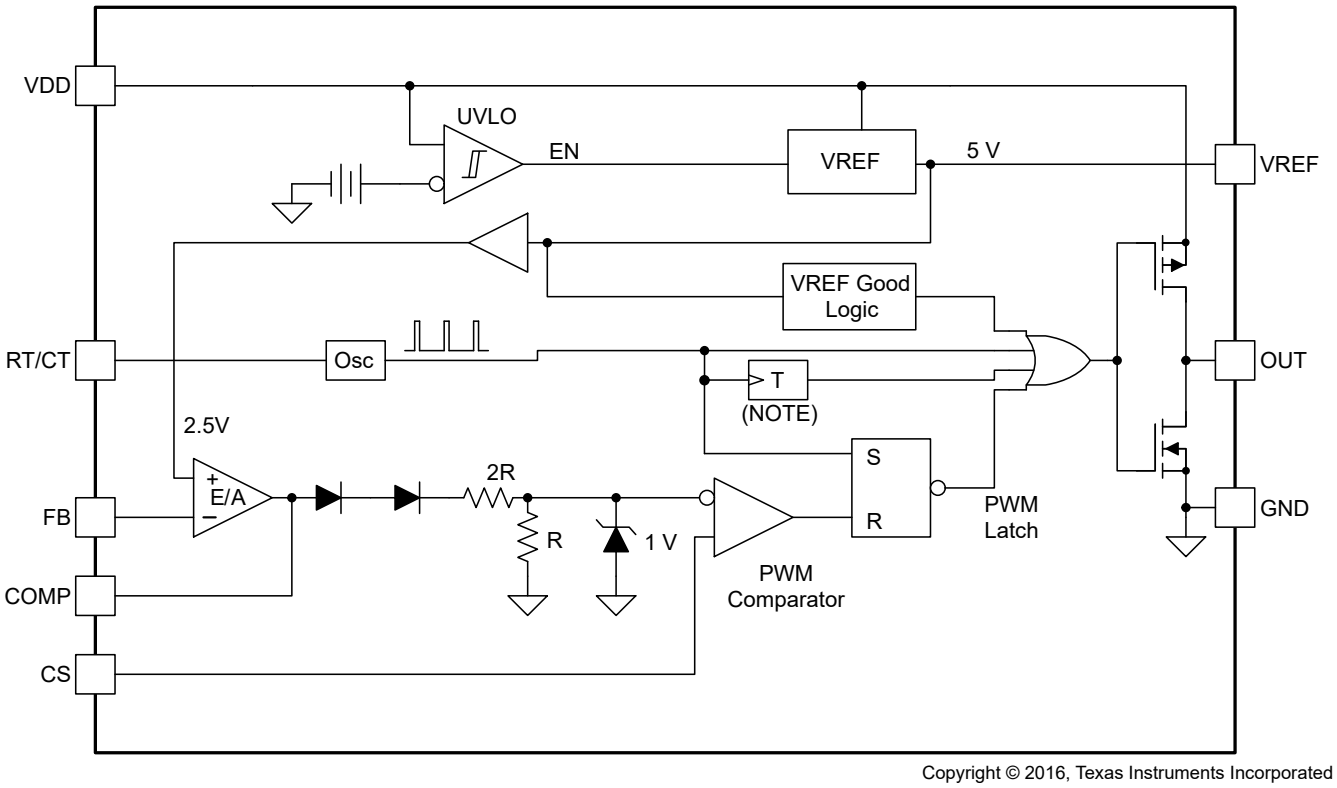
1 Overview

This document contains information for UCC28C4x-Q1(UCC28C40-Q1, UCC28C41-Q1, UCC28C42-Q1, UCC28C43-Q1, UCC28C44-Q1, and UCC28C45-Q1) (SOIC (8) package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1shows the device functional block diagram for reference.



Note

Toggle flip-flop used only in UCC28C41-Q1, UCC28C44-Q1, and UCC28C45-Q1

Figure 1-1. Functional Block Diagram

UCC28C4x-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

Table 1-1. Device Comparison Table

UVLO			MAXIMUM DUTY CYCLE	TEMPERATURE (T_A)
TURN ON AT 14.5 V TURN OFF AT 9 V SUITABLE FOR OFF-LINE APPLICATIONS	TURN ON AT 8.4 V TURN OFF AT 7.6 V SUITABLE FOR DC/DC APPLICATIONS	TURN ON AT 7 V TURN OFF AT 6.6 V SUITABLE FOR BATTERY APPLICATIONS		
UCC28C42QDRQ1	UCC28C43QDRQ1	UCC28C40QDRQ1	100%	–40°C to 125°C
UCC28C44QDRQ1	UCC28C45QDRQ1	UCC28C41QDRQ1	50%	

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOIC (8) Package

This section provides Functional Safety Failure In Time (FIT) rates for SOIC (8) package of UCC28C4x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate (71.6 mW, 150 mW, 300 mW)	10, 11, 15
Die FIT Rate (71.6 mW, 150 mW, 300 mW)	3, 4, 7
Package FIT Rate (71.6 mW, 150 mW, 300 mW)	7, 7, 8

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 71.6 mW, 150mW, 300mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC28C4x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT stuck low	34
OUT pulse width not as expected	19
OUT stuck high	14
System is unstable	11
No effect	22

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the UCC28C4x-Q1 (SOIC (8) package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- IC is connected based on the typical application design schematic in UCC28C4x-Q1 datasheet Figure 30

4.1 SOIC (8) Package

Figure 4-1 shows the UCC28C4x-Q1 pin diagram for the SOIC (8) package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC28C4x-Q1 data sheet.

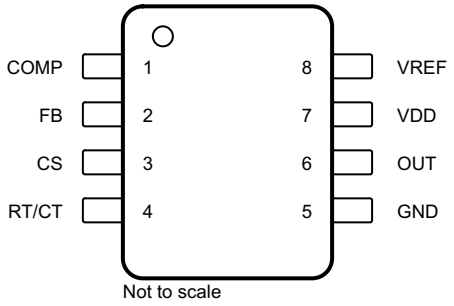


Figure 4-1. Pin Diagram SOIC (8) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	OUT zero duty cycle, output loss of regulation. Possible IC damage	B
FB	2	COMP pin go high, OUT excessive duty-cycle, output loss of regulation.	B
CS	3	Maximum OUT duty-cycle, loss of regulation, likely damage to power switch	B
RT/CT	4	Oscillator stops, OUT zero duty cycle, output loss of regulation	B
GND	5	N/A	D
OUT	6	OUT remains low, zero duty cycle. Likely IC damage	A
VDD	7	IC not biased, OUT zero duty cycle, output loss of regulation	B
VREF	8	OUT zero duty cycle, output loss of regulation, possible IC damage	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	Regulation loop becomes unstable, oscillation may result	C
FB	2	COMP stays high, OUT excessive duty-cycle, output loss of regulation	B
CS	3	CS pin stays high, OUT zero duty cycle, output loss of regulation	B
RT/CT	4	Oscillator stops, OUT zero duty cycle, output loss of regulation	B
GND	5	Internal GND pulled up to 0.65 V, IC behavior unpredictable	B
OUT	6	OUT at maximum duty cycle, output loss of regulation	B
VDD	7	IC not biased, OUT at zero duty cycle, output loss of regulation	B
VREF	8	VREF reglator unstable and oscillates, output oscillates	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	FB	COMP at VREF level, OUT excessive duty cycle, output loss of regulation	B
FB	2	CS	COMP stays at high, OUT excessive duty cycle, output loss of regulation	B
CS	3	RT/CT	Oscillator stops, OUT zero duty cycle, output loss of regulation	B
RT/CT	4	N/A		D
GND	5	OUT	OUT stays low, OUT zero duty cycle, output loss of regulation, likely IC damage	A
OUT	6	VDD	OUT stays high, 100% duty cycle, likely IC and power supply damage	A
VDD	7	VREF	VREF excess Abs max rating, IC damage, output loss of regulation	A
VREF	8	N/A		D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	Possible IC damange. OUT excessive duty cycle, output loss of regulation	A
FB	2	Excess Abs. Max rating, IC damage. OUT excessive duty cycle, output loss of regulation	A
CS	3	Excess Abs. Max rating, IC damage, OUT zero duty cycle, output loss of regulation	A
RT/CT	4	Excess Abs. Max rating, IC damage, OUT zero duty cycle, output loss of regulation	A
GND	5	IC is not biased. OUT zero duty cycle, output loss of regulation	B
OUT	6	OUT stays high, 100% duty cycle, likely IC and power supply damage	A
VDD	7	N/A	D
VREF	8	VREF excess Abs max rating, IC damage, output loss of regulation	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2020) to Revision A (September 2022)	Page
• Updated the Functional Block Diagram	2
• Updated Table 2-2	3
• Updated Table 3-1	4

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