EVM User's Guide: UCC21551CQEVM-079

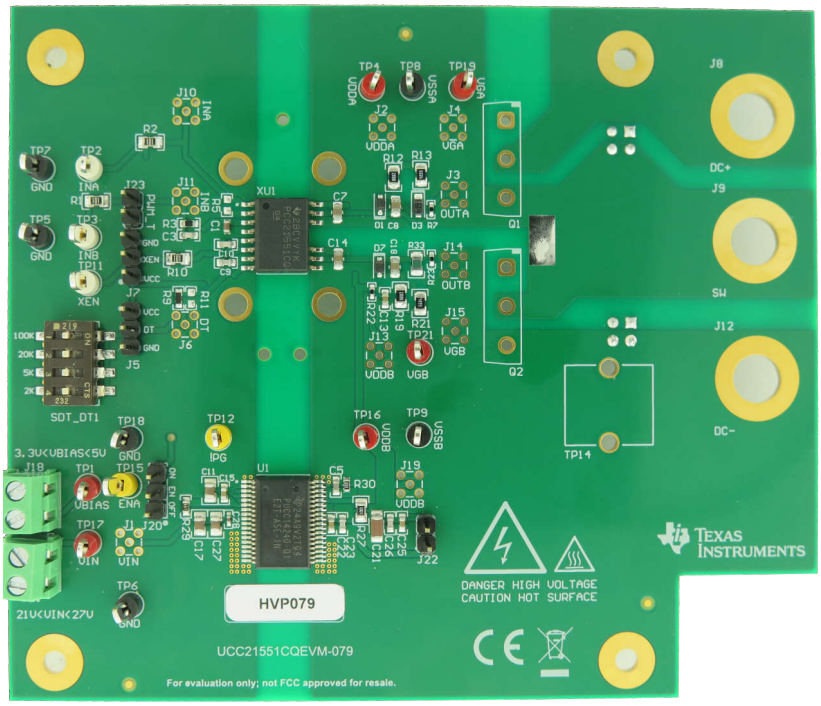
UCC21551CQEVM-079 Evaluation Module

Description

The UCC21551CQEVM-079 is a two copper layer PCB containing multiple test points and jumpers to fully evaluate the functionality of the UCC21551 gate driver. The EVM features PWM input control, onboard adjustable power supply, sockets for discrete FETs, external active clamp for low side protection, bootstrapped high side power supply, negative gate voltage capability, configurable deadtime switches, EN/DIS jumpers, and socket for Wolfspeed XM3 SiC-based half bridge power modules. The layout has been optimized to minimize gate loop area for each channel and placement of bypass capacitors allow for clean and sharp signal reading with minimal noise interference.

Features

- Variety of test points to help evaluate all of the gate driver functions
- Onboard isolated adjustable bias supply configured for 20 V
- Selectable dead time modes: overlap, interlock, programmable
- Low side external active clamping circuit
- 16 V/-3V Zener negative voltage pulldown circuit for SiC FETs
- Socket for Wolfspeed XM3 module



PCB Top Side

1 Evaluation Module Overview

1.1 Introduction

The UCC21551CQEVM evaluation module is designed for evaluating TI's UCC2155XX family of gate drivers. The UCC2155XX is a 5.7-kVrms isolated dual-channel gate driver with 4-A source and 6-A sink peak current for driving Si MOSFETs, IGBTs and WBG devices such as SiC and GaN transistors. This guide provides a complete EVM schematic diagram, printed circuit board layout, bill of materials, test setup, and feature descriptions for the UCC21551C. To evaluate other Iso-Drivers in the UCC2155XX family, TI recommends that the user read the data sheet thoroughly before switching the part in the EVM covered by this user guide.

CAUTION		
	**Caution**	**Read the user's guide before use.**

CAUTION		
	**Caution**	**Hot surface. Contact can cause burns. Do not touch!**

WARNING		
	**Danger**	**Do not use EVM to test isolation above V_{IOWM} = 1414 V_{DC}. High voltage.**

1.2 Kit Contents

- UCC21551CQEVM-079 two layer PCB

1.3 Specification

UCC21551CQEVM-079 primary function is to evaluate the UCC2155xx dual channel gate driver family. Multiple test points enable monitoring of the different input and outputs of the gate driver for thorough performance evaluation. The gate driver output can be configured to drive a capacitive loads for low voltage testing as well as discrete MOSFETs in a halfbridge configuration.

1.4 Device Information

The UCC21551x-Q1 is an isolated dual channel gate driver family with programmable dead time and wide temperature range. The device is designed with 4-A peak- source and 6-A peak-sink current to drive power MOSFET, SiC, and IGBT transistors.

The UCC21551x-Q1 can be configured as two low- side drivers, two high-side drivers, or a half-bridge driver. The input side is isolated from the two output drivers by a 5-kVRMS isolation barrier, with a minimum of 125-V/ns common-mode transient immunity (CMTI).

Protection features include: resistor programmable dead time, disable feature to shut down both outputs simultaneously, and integrated de-glitch filter that rejects input transients shorter than 5 ns. All supplies have UVLO protection.

With all these advanced features, the UCC21551x- Q1 device enables high efficiency, high power density, and robustness in a wide variety of power applications.

1.5 General TI High Voltage Evaluation User Safety Guidelines

Always follow TI's set-up and application instructions, including use of all interface components within the recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and the safety of those working around you. Contact TI's Product Information Center http://support/ti./com for further information.

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions can result in personal injury, property damage, or death due to electrical shock and/or burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise, and knowledge of electrical safety risks in development and application of high-voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments. If you are not suitably qualified, you must immediately stop from further use of the HV EVM.

- **Work Area Safety:**
  - Maintain a clean and orderly work area .
  - Qualified observers must be present anytime circuits are energized.
  - Effective barriers and signage must be present in the area where the TI HV EVM and the interface electronics are energized, indicating operation of accessible high voltages can be present, for the purpose of protecting inadvertent access.
  - All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50 V_{RMS}/75 VDC must be electrically located within a protected Emergency Power Off (EPO) protected power strip.
  - Use a stable and non-conductive work surface.
  - Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
- **Electrical Safety:**

  As a precautionary measure, a good engineering practice is to assume that the entire EVM can have fully accessible and active high voltages.

  - De-energize the TI HV EVM and all the inputs, outputs, and electrical loads before performing any electrical or other diagnostic measurements. Confirm that TI HV EVM power has been safely de-energized.
  - With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
  - When EVM readiness is complete, energize the EVM as intended.

  WARNING

  WARNING: While the EVM is energized, never touch the EVM or the electrical circuits as the EVM or electrical circuits can be at high voltages capable of causing electrical shock hazard.
- **Personal Safety:**
  - Wear personal protective equipment, for example, latex gloves and/or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.
- **Limitation for Safe Use:**
  - EVMs are not to be used as all or part of a production unit.

The EVM is designed for professionals who have received the appropriate technical training, and is designed to operate from an AC power supply or a high-voltage DC supply. Please read this user guide and the safety-related documents that come with the EVM package before operating this EVM.

CAUTION

Do not leave the EVM powered when unattended.

WARNING

High Voltage! Electric shock is possible when connecting board to live wire. Board must be handled with care by a professional.

For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

2 Hardware

2.1 Power Requirements

Table 2-1. UCC21551CQEVM-079 Electrical Specifications

	Description	Min	Typ	Max	Units
VIN	Enable for UCC21551 and UCC14240	3.3	5	5	V
VBIAS	Primary side input voltage UCC14240	21	24	27	V
VDDB VDDA	UCC21551C output bias supply voltage See data sheet for UCC2155XX variants	13.5		25	V
Fs	Switching frequency	0		500	KHz
DC	Voltage on DC+ for half bridge application	0		800	V
Tj	Operating junction temperature	-40		150	°C

2.2 Header Information

Table 2-2. Headers Description

Header Marker	Description
J5	Dead time setting
J7	Gate driver enable/disable
J20	Bias supply enable/disable
J22	Unused
J23	PWM mode toggle

2.3 Jumper Information

Table 2-3. Jumper Configurations

Header	Jumper Settings	Default
J5	VCC1-DT DT-GND Unconnected	DT-GND: enables gate driver interlock mode
J7	XEN-GND XEN-VCC1	XEN-VCC1: connects VCC1 to UCC21551 EN pin, enabling gate driver
J20	VCC1-ENA ENA-GND	VCC1-ENA: enables UCC14240 bias supply
J23	Connected Unconnected	Unconnected: disables single input PWM mode

2.4 Connectors Information

Table 2-4. Connectors Description

Connector	Description
J18	VCC1 Input for UCC14240 3.3-5V
J21	VIN Input for UCC14240 21-27V

2.5 Interfaces Information

Table 2-5. Interfaces Description

Interface	Description
J8	DC+
J9	Switch node
J12	DC-
J16A	XM3 Wolfspeed Socket CHA Gate

Table 2-5. Interfaces Description (continued)

Interface	Description
J16B	XM3 Wolfspeed Socket CHA VSSA
J17A	XM3 Wolfspeed Socket CHB Gate
J17B	XM3 Wolfspeed Socket CHB VSSB
Q1	Socket for discrete FET1
Q2	Socket for discrete FET2

2.6 Test Points

Table 2-6. Test Point Description

Test Point	Test Point Board Marker	Description
TP1	VBIAS/VCC1	EN for UCC14240
TP2	INA	Input for channel A
TP3	INB	Input for channel B
TP4	VDDA	Output side channel A supply
TP5	GND	Input side ground
TP6	GND	Input side ground
TP7	GND	Input side ground
TP8	VSSA	Output side channel A ground
TP9	VSSB	Output side channel B ground
TP11	XEN	Test point to apply an external enable signal
TP12	PG	Fault pin for detecting fault status for UCC14240
TP15	ENA	Test point for measuring UCC14240 enable signal
TP16	VDDB	Output side channel B supply
TP17	VIN	Test point for primary supply for UCC14240 (21V-27V)
TP18	GND	Input side ground
TP19	VGA	Q1 FET gate
TP21	VGB	Q2 FET gate
J1	VIN	MMCX pad for primary supply for UCC14240 (21V-27V)
J2	VDDA	MMCX pad for output side channel A supply
J3	OUTA	MMCX pad for channel A output
J4	VGA	MMCX pad for Q1 gate
J6	DT	MMCX pad for Deadtime pin
J10	INA	MMCX pad for input to channel A
J11	INB	MMCX pad for input to channel B
J13	VDDB	MMCX pad for output side channel B supply
J14	OUTB	MMCX pad for channel B output
J15	VGB	MMCX pad for Q2 gate
J19	VDDB	MMCX pad for output low side supply

3 Implementation Results

3.1 Evaluation Setup

This section describes the default EVM configurations and recommended test set up for the UCC21551-Q1 EVM.

Equipment

The following equipment is recommended for testing the EVM:

- One DC supply capable of 5 V/0.5A, for example: Keysight E3634A.
- One DC supply capable of 24 V/0.5A, for example: Keysight E3634A.
- One Arbitrary Function Generator, dual channel, for example: Tektronix AFG3102A
- One Oscilloscope, at least 3 channels, bandwidth 200 MHz or above, for example, Tektronix MDO3054 or TDS3054C.
- Three passive oscilloscope probes, bandwidth 200 MHz or above. For example, TPP1000 like probe with a ground spring.
- 4X BNC to Grabber Cables for input and supply connections.
- Banana plug connector.

Equipment Configurations

- **DC Power Supply Settings**
  - **DC Supply 1:**
    - Voltage setting: 5 V
    - Current limit: 0.5A
  - **DC Supply 2:**
    - Voltage setting: 24 V
    - Current limit: 0.5A
- **Function Generator Settings**
  - **Function:** Pulse
  - **CH1:** High: 5 V, Low: 0 V
  - **CH2:** High: 5 V, Low: 0 V
- **Oscilloscope Settings**
  - **CH1-CH3:**
    - DC coupling
    - Highest bandwidth setting available
    - Termination 1M or automatic
    - Probe scale: 10X or auto

Equipment Setup

- **Jumper Connections**
  - **J7:** Shunt XEN to VCC
  - **J20:** Shunt ON to EN
  - **J5:** Shunt DT to GND
  - **SDT_DT1:** All switches in the left most position
- **Oscilloscope Connections**
  - **CH1:** VGA to VSSA
  - **CH2:** VGB to VSSB
  - **CH3:** VDDB to VSSB
- **Function Generator**
  - **CH1:** INB to GND
  - **CH2:** INA to GND
- **Power Supply**
  - **DC Supply 1:** J18
  - **DC Supply 2:** J21

If testing the EVM with FETs, then populate Q1 and Q2 or the XM3 connector. If testing the EVM without FETs, then place a banana plug connector between SW and DC-. See Figure 3-1 for a visual of the default test connections.

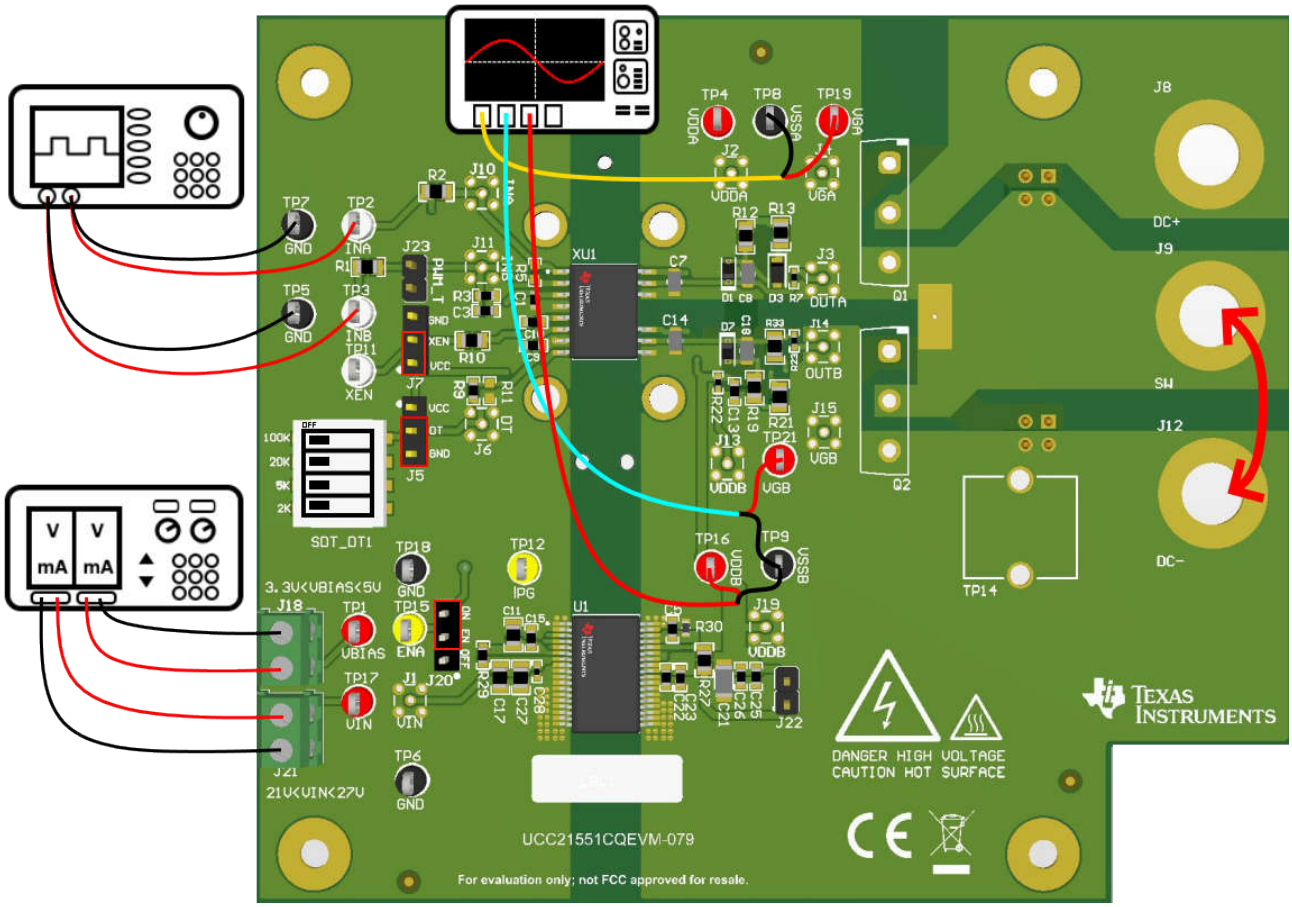


Figure 3-1. Default Connections Without Load

3.2 Performance Data and Results

Test Procedure

- **Power Up**
  1. Before proceeding make sure the EVM and all equipment is setup as described in section Equipment Configurations and Equipment Setup.
  2. Turn on the 5 V and 24 V power supply. Probing VDDB(TP16)-VSSB(TP9) measures 20 V. Probing VCC1(TP1)-GND(TP6) measures 5 V.
  3. Turn on both channels of the function generator.
  4. Use any probe of choice to verify that there is a 5 KHz, 5 V, pulse on INA and INB each with respect to GND.
  5. Probing VGA-VSSA and VGB-VSSB shows a PWM output signal from the gate driver going up to +16V when HIGH and -3V when LOW as shown in Figure 3-2.

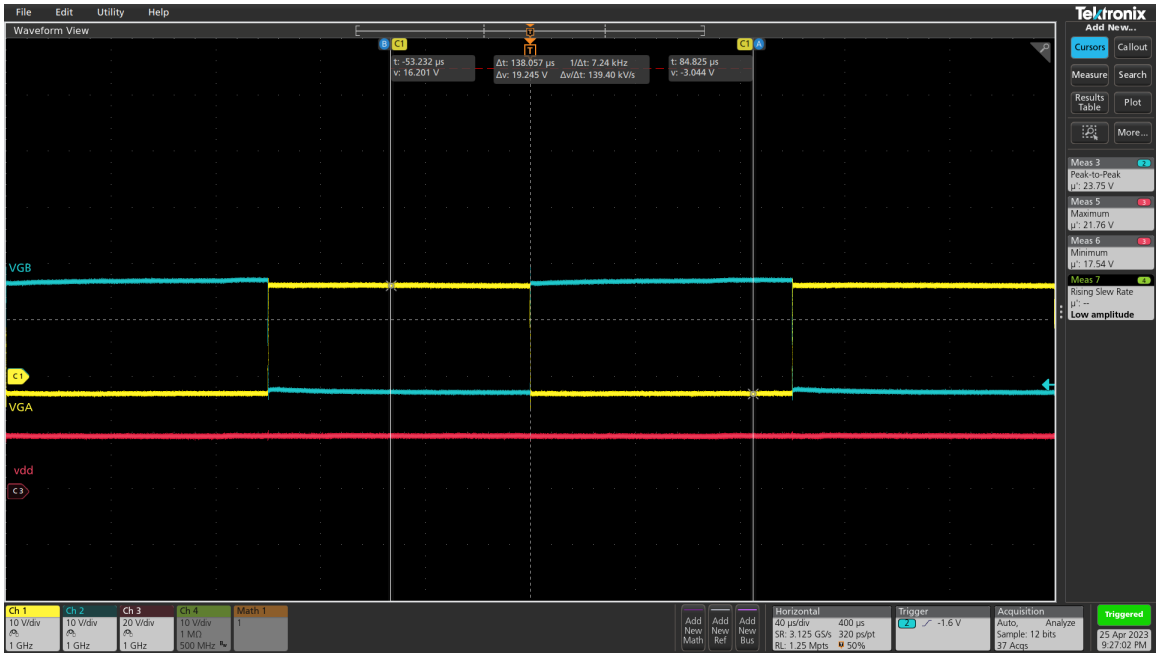


Figure 3-2. Power-up Test: Switching at 5 kHz

Deadtime Configuration

The UCC21551 has 3 dead time modes that are selectable with the UCC21551CQEVM. Those modes are Interlock, Programmable, and Overlap.

- **Interlock Mode:** Interlock mode sets a minimum delay of approximately 5 ns between gate driver outputs to prevent the channels from overlapping. This mode is initiated when the dead time pin is grounded (Shunting J5 to DT-GND). The dead time is defined as the delay between 90% of the falling edge of the first output and 10% of the rising edge of the second output. Timing is illustrated in Figure 3-3. See Figure 3-4for an example of Interlock mode.

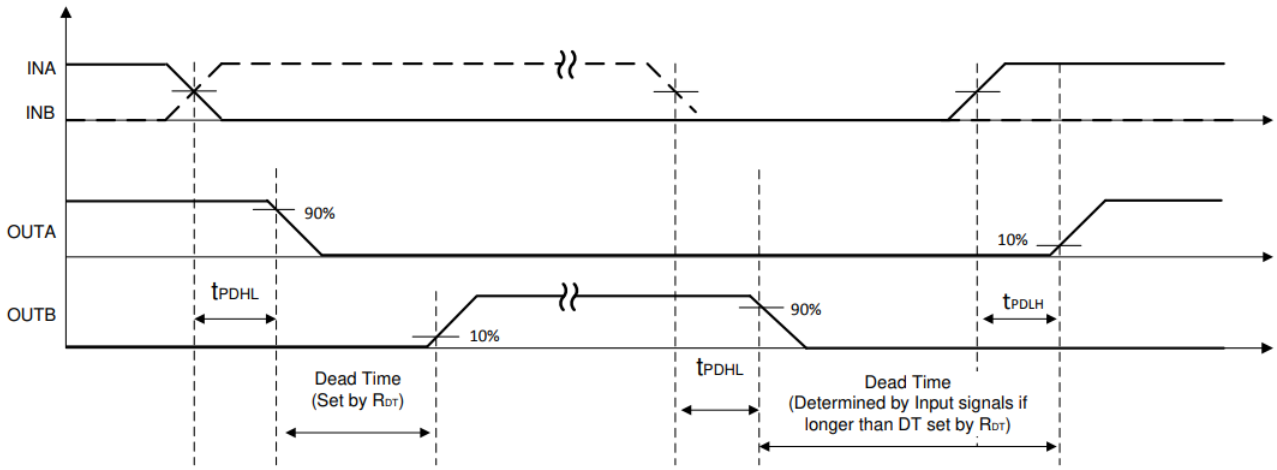


Figure 3-3. Timing Diagram

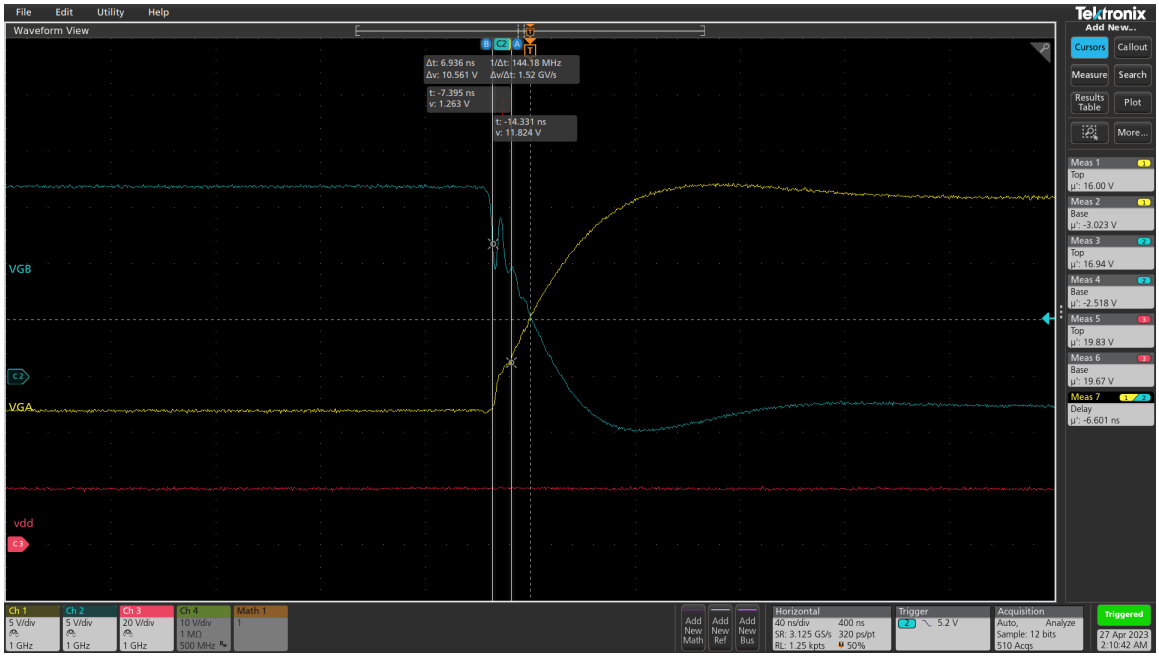


Figure 3-4. Interlock Mode

- **Programmable Mode**: Programmable dead time mode is activated when the dead time pin is connected to a resistor between 1.7K-100K Ohms to ground. To activate this mode on the EVM, leave jumper J5 unconnected. To adjust the deadtime, use the switches on SDT_DT1. By default, switch the switches to the left. To program the dead time, move the switch to the right. The available resistors allow for various dead time settings. Additional values can be created by toggling multiple switches at the same time, which has the effect of paralleling the resistors. Figure 3-5 is an example output waveform with 5 kΩ resistance.

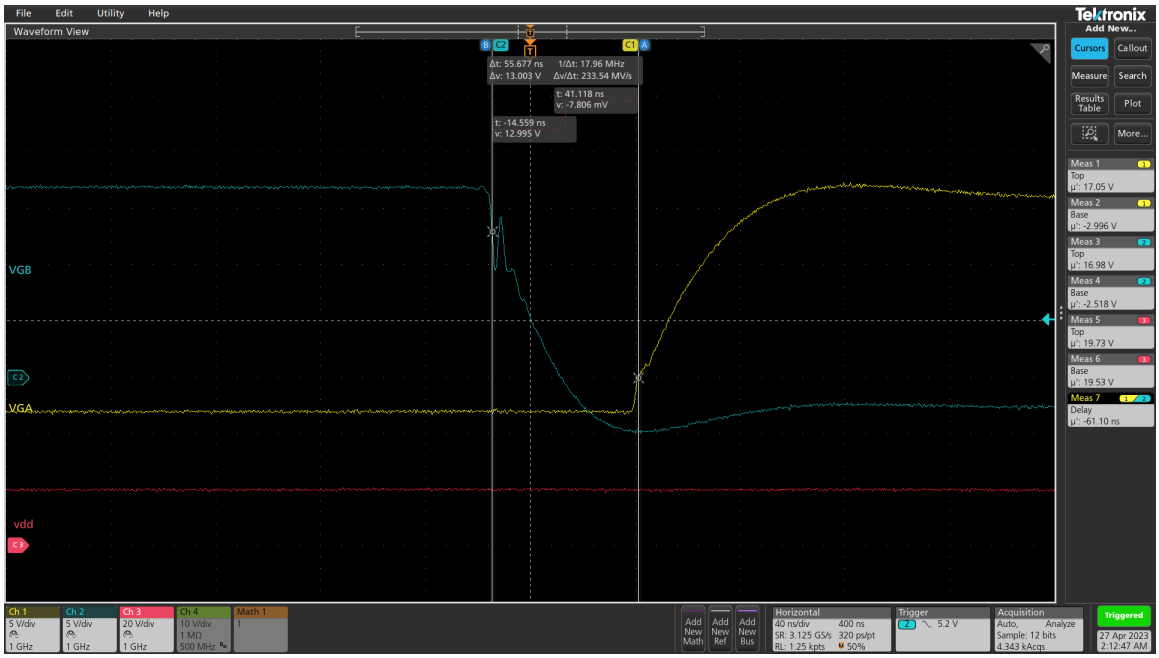


Figure 3-5. Programmable Mode: 5 kΩ RDT Resistor Selection

- **Overlap Mode**: Overlap mode disables the deadtime circuitry to allow the outputs to overlap. To select this mode, shunt jumper J5 to VCC-DT. An example of overlap mode is depicted in Figure 3-6.

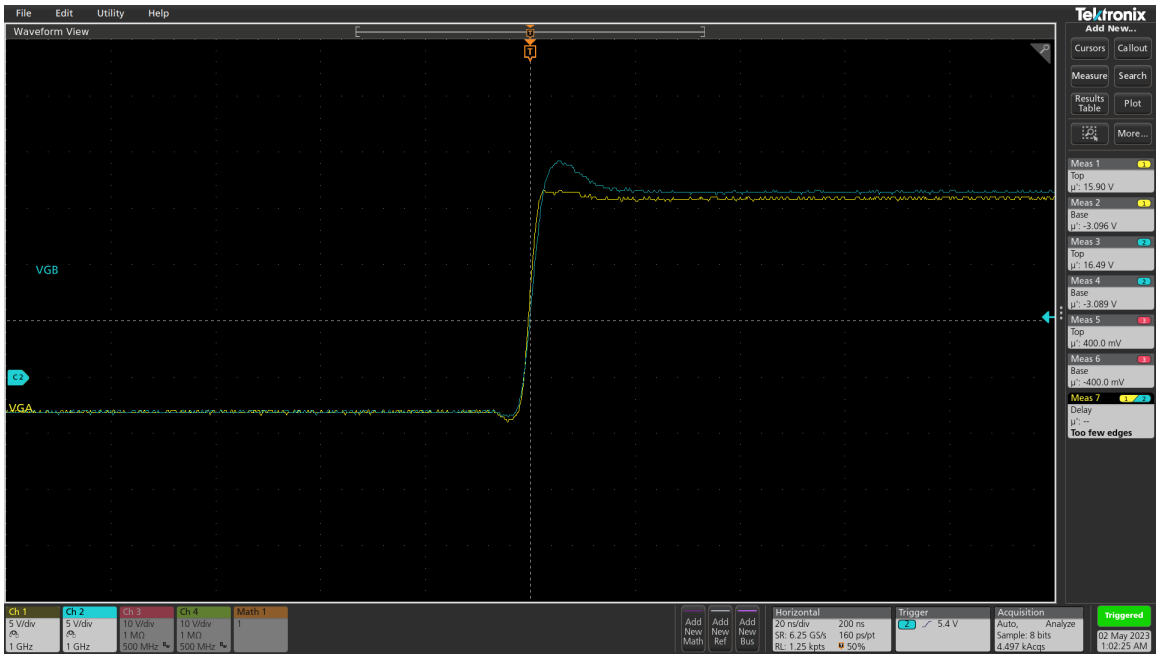


Figure 3-6. Overlap Mode

Single Input PWM

Single input PWM allows the user to control channel A and B with a single PWM signal. On the EVM, this is accomplished with a BJT inverter circuit that takes the incoming channel A signal inverts and forwards to the input pin of channel B. To enable this mode, shunt jumper 23. Note that in this mode, there is an unavoidable intrinsic dead time of 1us imposed by the BJT switching delay. This only occurs between the falling edge of VGA and the rising edge of VGB. If the deadtime circuit of the UCC21551 is enabled, then the interlock and programmable deadtime modes only affects the rising edge of VGA and the falling edge of VGB. This is because the 1us deadtime caused by the BJT is happening in parallel with the gate driver deadtime instead of adding. In Figure 3-7 and Figure 3-8, the driver is in interlock mode and both channels are switching at the same frequency. As the frequency increases, the output pulses eventually become smaller than the 1us delay. Figure 3-8 is depicting switching at 200 kHz, at which about half of INB's signal is lost.

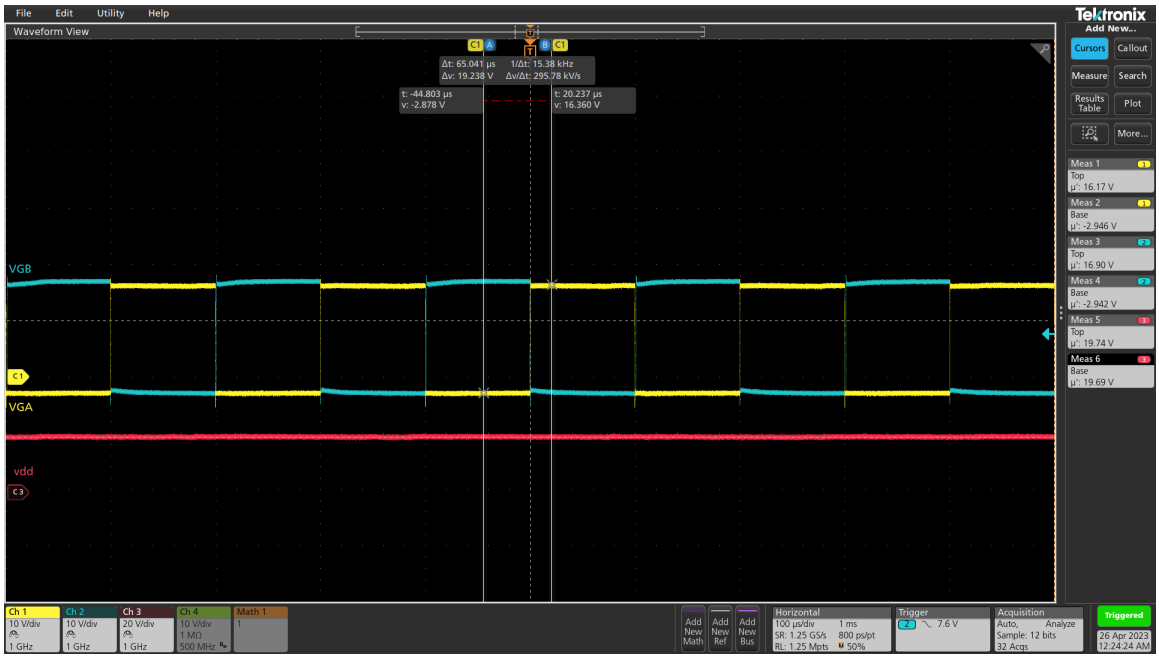


Figure 3-7. Switching at 5 kHz

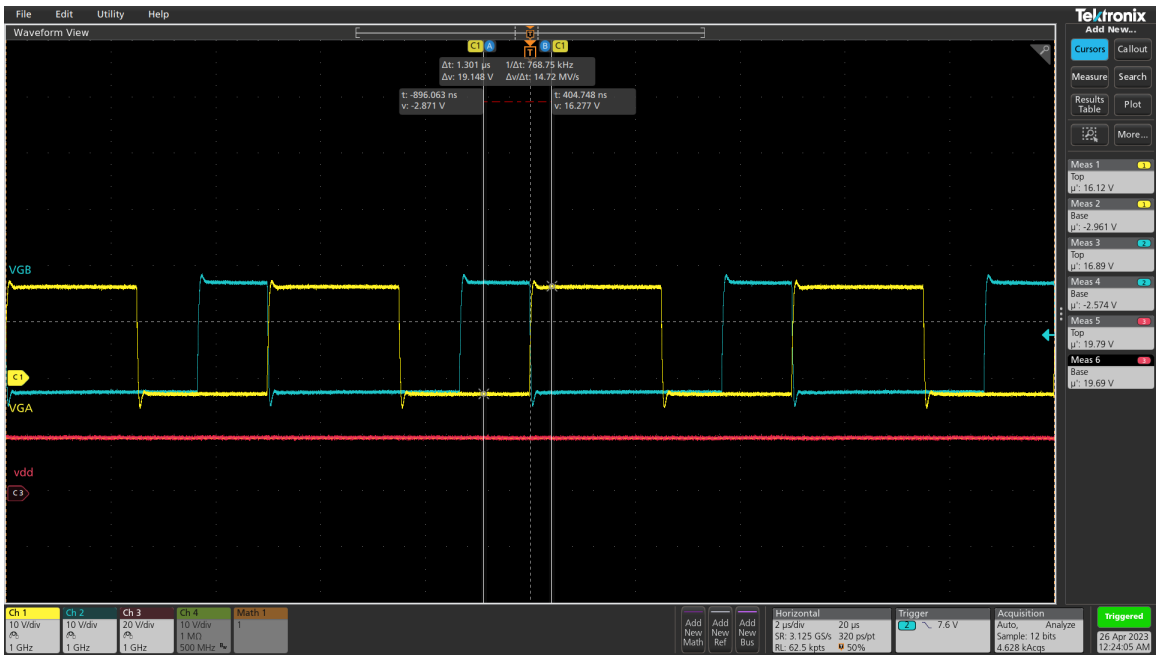


Figure 3-8. Switching at 200 kHz

Active Clamp

The Active clamp is a protection circuit added to channel B of the UCC21551CQEVM. This circuit helps keep the gate low when the driver is not powered or if there is an unintended voltage rise coupling to VGB. If there is a rise in the voltage on VGB greater than the voltage on OUTB, then the PNP BJT turns on and provides a path for current to flow to ground instead of into the FET gate, which can turn the FET on. The active clamp clamps voltage transients on VGB to approximately 1.2V. This is shown in Figure 3-9.

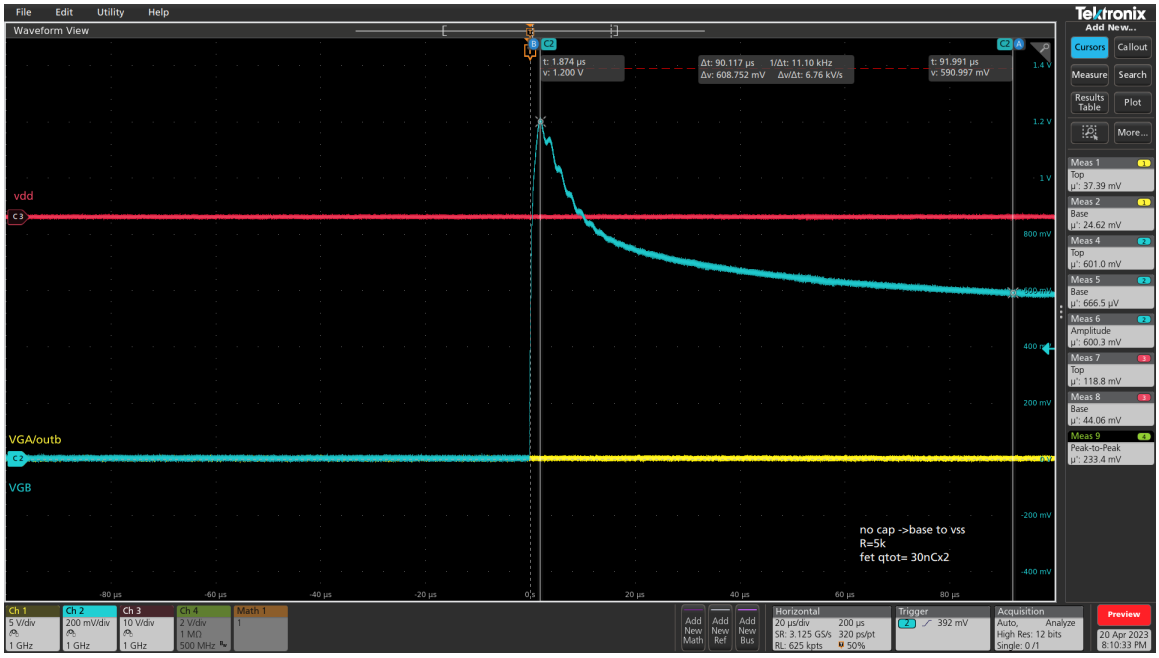


Figure 3-9. Active Clamp Clamping an Unintended Rise on VGB

Onboard Adjustable Bias Supply (UCC14240)

The UCC14240 is a 1.5W isolated adjustable bias supply configured to supply 20 V to the low side (channel B) of the gate driver. The user can change this output voltage to accommodate different versions of UCC2155XX drivers by changing resistor R28. For more information on how to adjust the output voltages, refer to the UCC14240-Q1 Component Calculator and the application note *UCC14240-Q1 Simplifies HEV, EV, Bias Supply Design for Isolated Gate Drivers*.

Negative Bias Supply Generation

The UCC21551CQEVM is equipped with a zener diode circuit on both gate driver output channels. This takes the 20 V VDD supply and splits into +16/-3V. Applying a negative bias to the gate of MOSFET mitigates the system from having unintentional turn on of the MOSFET caused by current flowing through the miller capacitor during high dv/dt switching. The negative pulldown circuit needs multiple cycles to reach steady state. Not all tests, such as a double pulse test, feature a negative voltage on the gate when performed.

High Voltage Double Pulse Test

This UCC21551CQEVM-079 was designed to work with voltages of up to 800 V. A low side double pulse test was performed to test the high voltage capability of the EVM. This test consisted of a Wolfspeed XM3 evaluation board which includes a SiC FET module and DC bus capacitor. The inductor is connected across the high side FET so the body diode can free-wheel the inductor current while the low side FET switches.

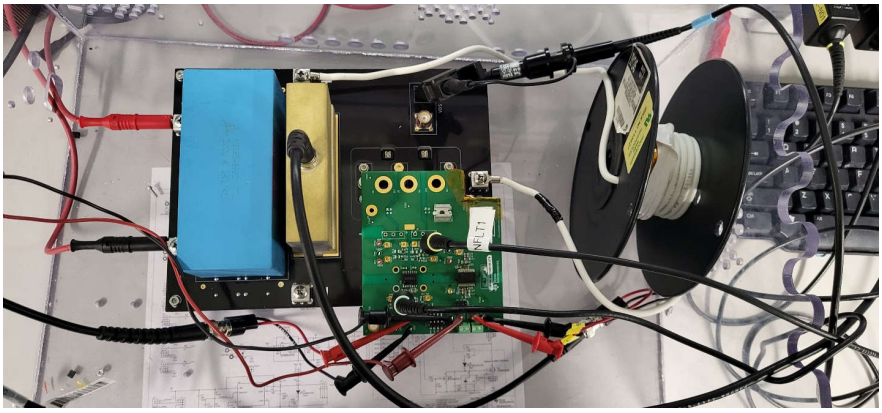


Figure 3-10. UCC21551CQEVM-079 Connected to SiC Wolfspeed XM3 Module

If the Wolfspeed XM3 evaluation board is not in use, then the user has the capability of connecting DC bus link capacitors to the board by using connectors J8 (DC+) and J12 (DC-).

Figure 3-11 shows the waveforms taken of an 800 V double pulse test. The signals are described below:

- Red: ID, inductor current
- Blue: Vds, drain to source voltage of the low side FET switching
- Yellow: Vg, gate voltage of the low side FET
- Green: Vin, channel B input pulse signal

The peak current measured during this test measured 522 amps and the peak voltage across the low side fet measured 977 volts.

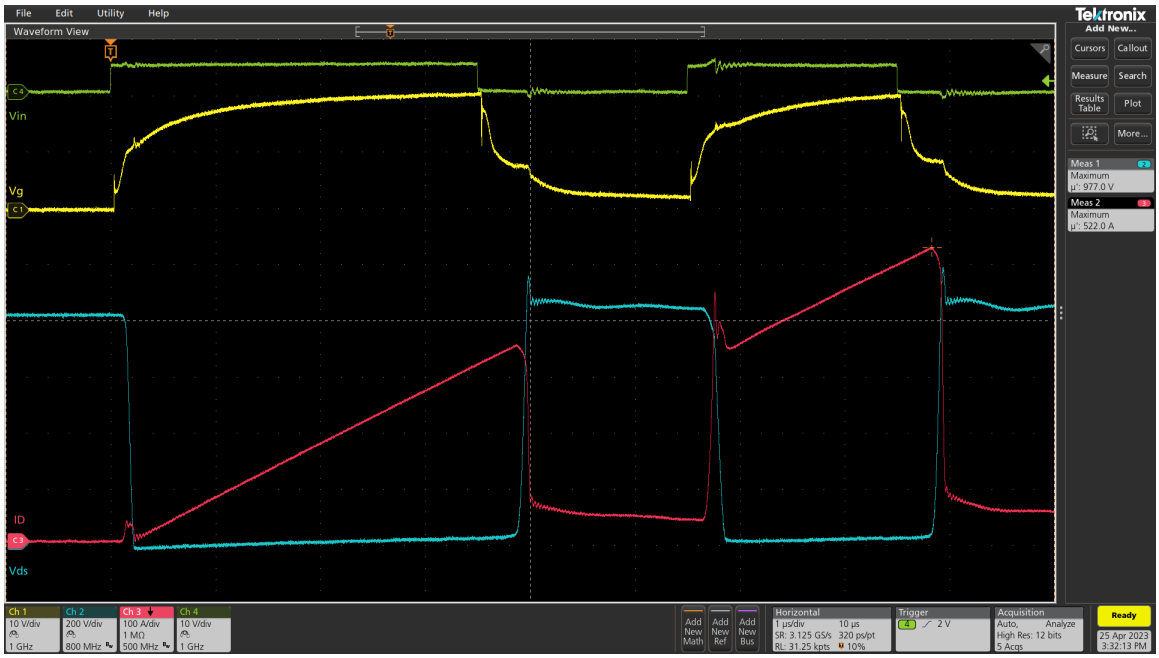


Figure 3-11. Double Pulse Test Results at 800 V

4 Hardware Design Files

4.1 Schematics

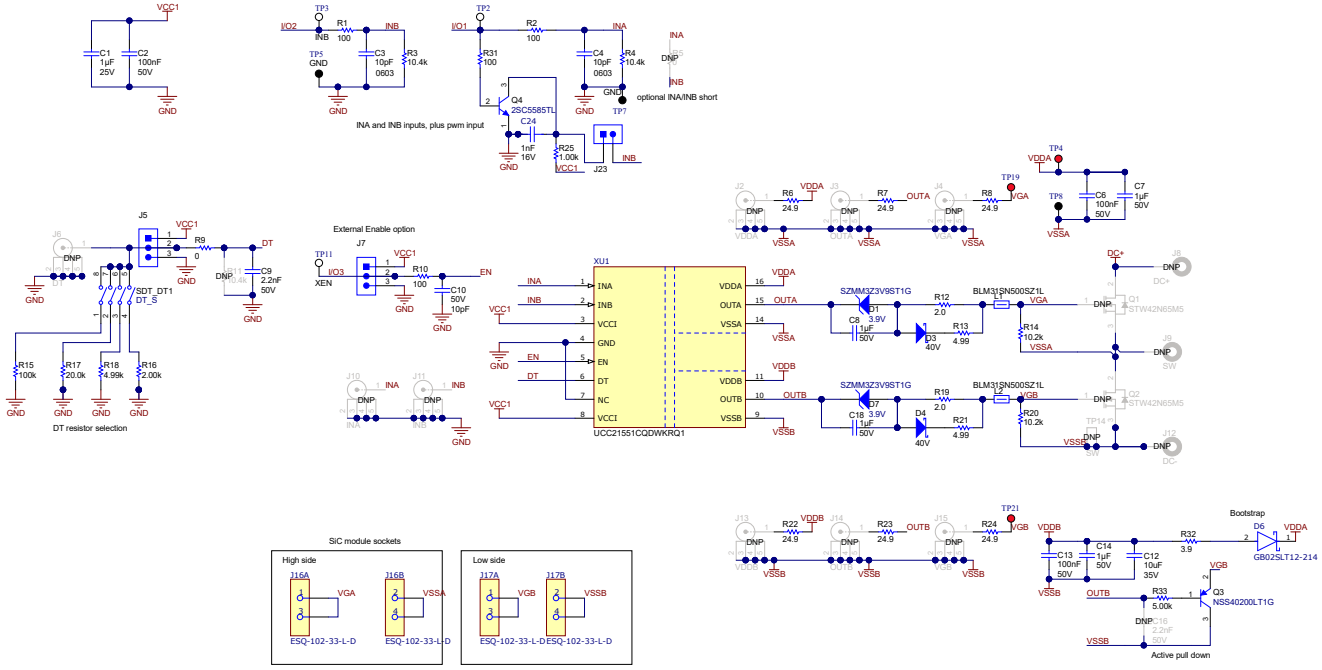


Figure 4-1. UCC21551C Schematic

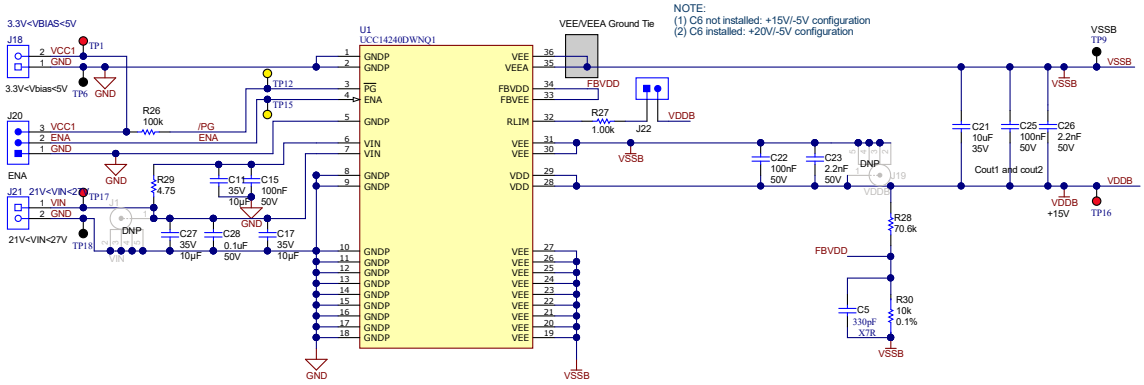


Figure 4-2. UCC14240 Schematic

4.2 PCB Layouts

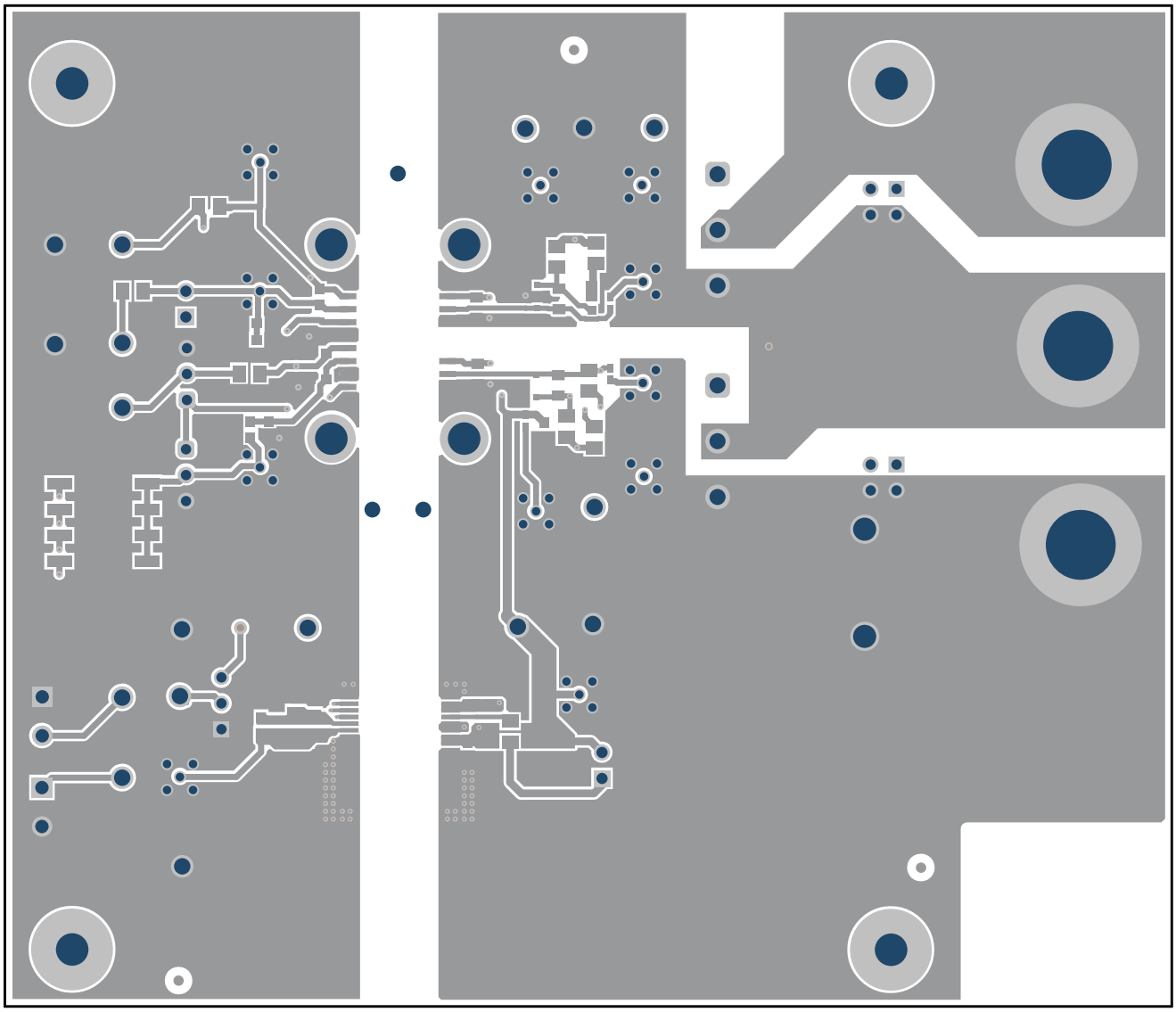


Figure 4-3. PCB Top Layer

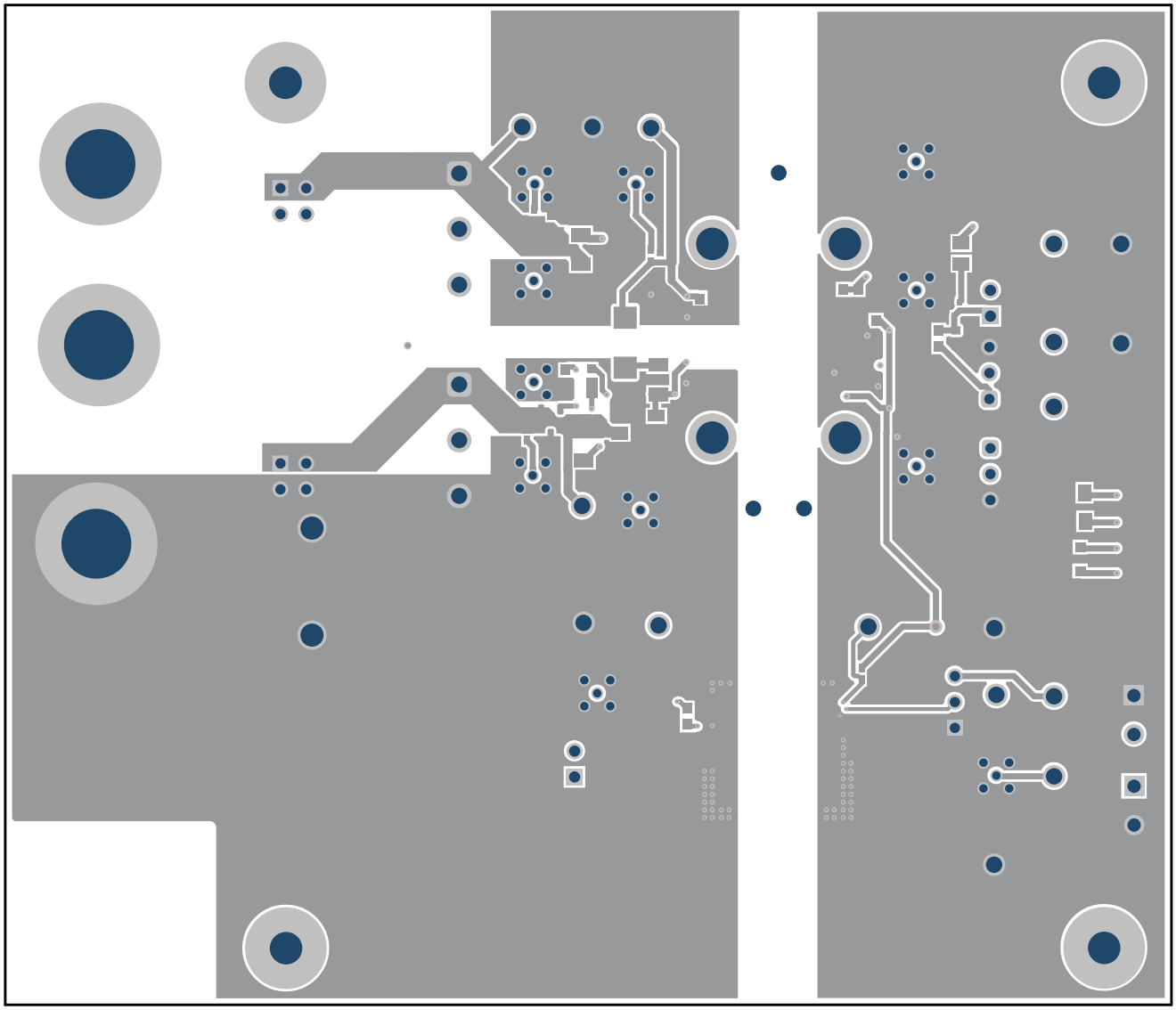


Figure 4-4. PCB Bottom Layer

4.3 Bill of Materials (BOM)

Table 4-1. Bill of Materials

Designator	Qty	Description	Part Number	Manufacturer
C1	1	CAP, CERM, 1 µF, 25 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	CGA3E1X7R1E105K080AC	TDK
C2, C6, C13, C15, C22, C25	6	CAP, CERM, 0.1 uF, 50 V, +/- 5%, X7R, 0603	C0603C104J5RACTU	Kemet
C3, C4, C10	3	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0603	GRM1885C1H100JA01D	MuRata
C5	1	CAP, CERM, 330 pF, 100 V, +/- 10%, X7R, 0603	GRM188R72A331KA01D	MuRata
C7, C8, C14, C18	4	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0805	C2012X7R1H105K085AC	TDK
C9, C23, C26	3	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0603	C0603C222K5RACTU	Kemet
C11, C17, C27	3	CAP, CERM, 10 µF, 35 V,+/- 10%, X5R, 0805	GMK212BBJ106KG-T	Taiyo Yuden
C12, C21	2	CAP, CERM, 10 uF, 35 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206_190	CGA5L1X7R1V106K160AC	TDK
C24	1	1000 pF ±10% 16 V Ceramic Capacitor X7R 0603 (1608 Metric)	CC0603KRX7R7BB102	YAGEO
C28	1	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71H104KE02D	MuRata
D1, D7	2	Diode, Zener, 3.9 V, 300 mW, AEC-Q101, SOD-323	SZMM3Z3V9ST1G	ON Semiconductor
D3, D4	2	Diode, Schottky, 40 V, 1 A, MicroSMP	MSS1P4-M3/89A	Vishay-Siliconix
D6	1	Diode Silicon Carbide Schottky 1200 V 2 A (DC) Surface Mount DO-214AA	GB02SLT12-214	GeneSiC Semiconductor
FID1, FID2, FID3	3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
J5, J7	2	Header, 100mil, 3x1, Gold, TH	TSW-103-07-G-S	Samtec
J16, J17	2	4 Position Elevated Socket Connector Through Hole	ESQ-102-33-L-D	Samtec
J18, J21	2	Terminal Block, 2x1, 3.81mm, 24-16 AWG, 10 A, 300VAC, TH	691214310002	Wurth Elektronik
J20	1	Header, 100mil, 3x1, Tin, TH	PEC03SAAN	Sullins Connector Solutions
J22, J23	2	Header, 2.54mm, 2x1, TH	961102-6404-AR	3M
L1, L2	2	Ferrite Bead, 50 ohm @ 100 MHz, 12 A, 1206	BLM31SN500SZ1L	MuRata
LBL1	1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady
Q3	1	Transistor, PNP, 40 V, 2 A, AEC-Q101, SOT-23	NSS40200LT1G	ON Semiconductor
Q4	1	Transistor, NPN, 12 V, 0.5 A, SOT-416	2SC5585TL	Rohm
R1, R2, R10, R31	4	RES, 100, 0.5%, 0.1 W, 0805	RR1220P-101-D	Susumu Co Ltd
R3, R4	2	RES, 10.4 k, 0.5%, 0.1 W, 0603	RT0603DRE0710K4L	Yageo America

Table 4-1. Bill of Materials (continued)

Designator	Qty	Description	Part Number	Manufacturer
R6, R7, R8, R22, R23, R24	6	RES, 24.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040224R9FKED	Vishay-Dale
R9	1	RES, 0, 0%, 0.25 W, AEC-Q200 Grade 0, 0603	PMR03EZPJ000	Rohm
R12	1	RES, 2.0, 5%, 0.125 W, 0805	CRCW08052R00JNEA	Vishay-Dale
R13, R21	2	RES, 4.99, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	CRCW08054R99FKEA	Vishay-Dale
R14, R20	2	RES, 10.2 k, 0.5%, 0.1 W, 0805	RR1220P-1022-D-M	Susumu Co Ltd
R15	1	RES, 100 k, 1%, 0.125 W, 0805	CRG0805F100K	TE Connectivity
R16	1	RES, 2.00 k, 0.01%, 0.1 W, 0603	Y16362K00000T9W	Vishay Foil Resistors
R17	1	RES, 20.0 k, 0.5%, 0.1 W, 0805	RR1220P-203-D	Susumu Co Ltd
R18	1	RES, 4.99 k, 1%, 0.1 W, 0603	CRCW06034K99FKEAC	Vishay-Dale
R19	1	RES, 2.0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	CRCW08052R00JNEA	Vishay-Dale
R25	1	RES, 1.00 k, 0.1%, 0.1 W, 0603	RT0603BRD071KL	Yageo America
R26	1	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	ERJ-2GEJ104X	Panasonic
R27	1	RES, 1.00 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	ERJ-6ENF1001V	Panasonic
R28	1	RES, 70.6 k, 0.5%, 0.1 W, 0603	RT0603DRE0770K6L	Yageo America
R29	1	RES, 4.75, 0.5%, 0.1 W, 0603	RT0603DRE074R75L	Yageo America
R30	1	Res Thin Film 0603 10K Ohm 0.1% 1/10W ±10ppm/°C Molded SMD SMD Punched Carrier T/R	ERA-3ARB103V	Panasonic
R32	1	RES, 3.9, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	CRCW12063R90JNEA	Vishay-Dale
R33	1	RES, 5.00 k, 0.1%, 0.2 W, 0805	PNM0805E5001BST5	Vishay Thin Film
SDT_DT1	1	Switch, SPST, Slide, Off-On, 4 Pos, 0.1A, 20 V, SMD	219-4MST	CTS Electrocomponents
TP1, TP4, TP16, TP17, TP19, TP21	6	Test Point, Multipurpose, Red, TH	5010	Keystone Electronics
TP2, TP3, TP11	3	Test Point, Multipurpose, White, TH	5012	Keystone Electronics
TP5, TP6, TP7, TP8, TP9, TP18	6	Test Point, Multipurpose, Black, TH	5011	Keystone Electronics
TP12, TP15	2	Test Point, Multipurpose, Yellow, TH	5014	Keystone Electronics
U1	1	2W, 24V-Vin, 25V-Vout, High-Efficiency, >2. 5 kVRMS Isolated DC-DC Converter	UCC14240DWNQ1	Texas Instruments
XU1	1	Automotive 4-A, 6-A, Reinforced Isolation Dual-Channel Gate Driver	UCC21551CQDWKRQ1	Texas Instruments
C16	0	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0603	C0603C222K5RACTU	Kemet
H1, H2, H3, H4	0	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	0	Standoff, Hex, 0.5"L #4-40 Nylon	1902C	Keystone

Table 4-1. Bill of Materials (continued)

Designator	Qty	Description	Part Number	Manufacturer
J1, J2, J3, J4, J6, J10, J11, J13, J14, J15, J19	0	Connector, MMCX 50 ohm, TH	MMCX-J-P-H-ST-TH1	Samtec
J8, J9, J12	0	Standard Banana Jack, Uninsulated, 15 A	108-0740-001	Cinch Connectivity
Q1, Q2	0	MOSFET, N-CH, 650 V, 33 A, TO-247	STW42N65M5	STMicroelectronics
R5	0	RES, 0, 0%, 0.25 W, AEC-Q200 Grade 0, 0603	PMR03EZPJ000	Rohm
R11	0	RES, 10.4 k, 0.5%, 0.1 W, 0603	RT0603DRE0710K4L	Yageo America
TP14	0	Fuse Holder, 5AG, TH	3566	Keystone

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

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9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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