

PSE Solution Delivers High Power-Over-Ethernet to 25-W PD Over Two Pairs

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ABSTRACT

This application report discusses a solution to the additional power required in those PoE applications that exceed the power requirements defined in the current IEEE802.3af standard.

Contents

1	Introduction	1
2	Recommended Characteristics	2
3	Simple High Power PSE Solution	2
4	Analysis of the Current Booster Circuit	4
5	Test of Current Booster Circuit	5
6	Thermal Considerations	5
7	Required High-Power Components	6
8	Conclusion	7
9	References	7

List of Figures

1	Typical PoE Application Diagram.....	2
2	Diagram of Two-Pairs Solution for 25-W PD, Minimum Worst Case	3
3	A Possible PoE Transformer Topology	6

1 Introduction

The Power-over-Ethernet (PoE) technology provides electrical power via standard Cat-5 Ethernet cables, thereby eliminating the need for wall adapters or other external power sources for equipment connected in an Ethernet network. The two major components in a PoE system are the power sourcing equipment (PSE), that provides the power, and the powered device (PD), that receives and uses this power (see [Figure 1](#)).

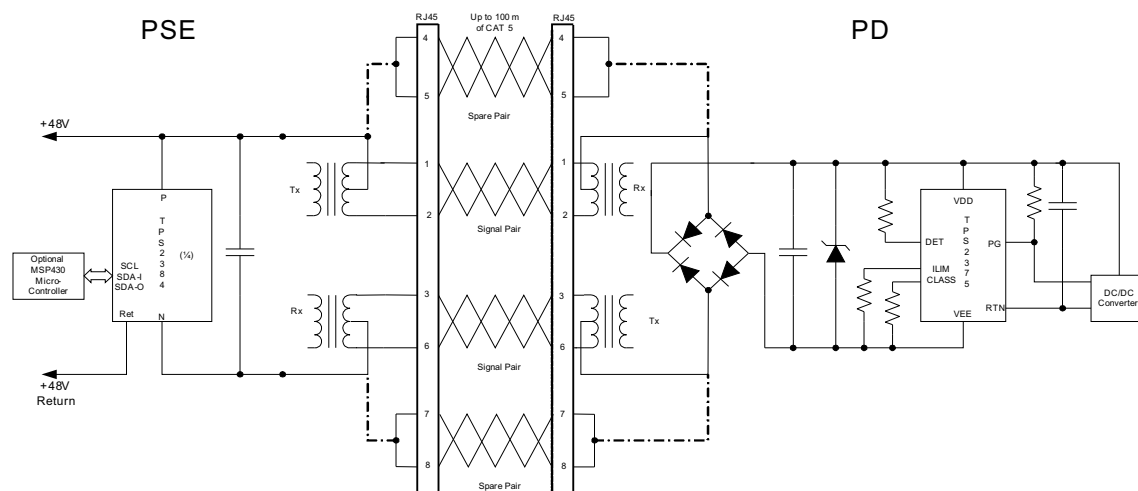


Figure 1. Typical PoE Application Diagram

Recently, practical applications using PoE have been developed. Many of these new applications require more power than the power limit defined in the current 802.3af standard (approximately 13 W at the PD end). For example, a sophisticated security system with motor-controlled cameras would benefit from high-power PoE.

2 Recommended Characteristics

Any high-power solution must meet the following basic criteria:

- Must avoid overheating the Ethernet cables
- Must not result in an imbalance of current within a pair of wires, thereby avoiding saturating Ethernet transformers
- Must be useable with the existing cabling system, based on Cat-5 cable type
- No overheating in the PSE nor in the PD
- Operating voltage within the 802.3af standard voltage range

Also, any solution for more than 18 W should provide (if possible) the following features:

- Power provided over two pairs only
- Compatibility with 802.3af standard PDs
- Power management capability
- Acceptable heating in PSE, in PD, or in between
- Minimum loss of efficiency of complete system

3 Simple High Power PSE Solution

The IEEE802.3af standard stipulates a PSE output voltage from 44 V to 57 V, with an I_{CUT} (represents a level beyond which power consumption is regarded as an overload) of 350 mA minimum and an I_{LIM} (represents the highest consumption level possible) of 400 mA minimum. Using 100 m of cable with a worst-case feed resistance of 20 Ω (from IEEE802.3af), this results in a limit of 12.95 W at the PD's input, when operating at the minimum allowed voltage.

Integrated power controllers like the TPS2384 are factory-set to meet this requirement. The TPS2384 is capable of delivering 425 mA (I_{LIM}) nominally to the port for a short time. Also, if the port current exceeds 375 mA (I_{CUT}) for more than 62 ms ($T_{OVL D}$), the TPS2384 turns off the port.

The high-power solution proposed in this document, using the TPS2384, involves operating at higher bus voltage and then adding a simple current booster circuit. Currently, Cat-5 communications wiring is the recognized minimum for broadband services. Its specific standard designation is EIA/TIA-568; it is built with 24 AWG conductors which results in worst-case feed resistance of 12.5 Ω, which is considerably less than 20 Ω. It is assumed in the following demonstration that such cable is used.

The minimum operating voltage must rise up to 53 V, with 55 V nominal and 57 V maximum. This results in more power available for an unchanged current limit.

The current booster provides additional current beyond that available through the TPS2384 (see Figure 2).

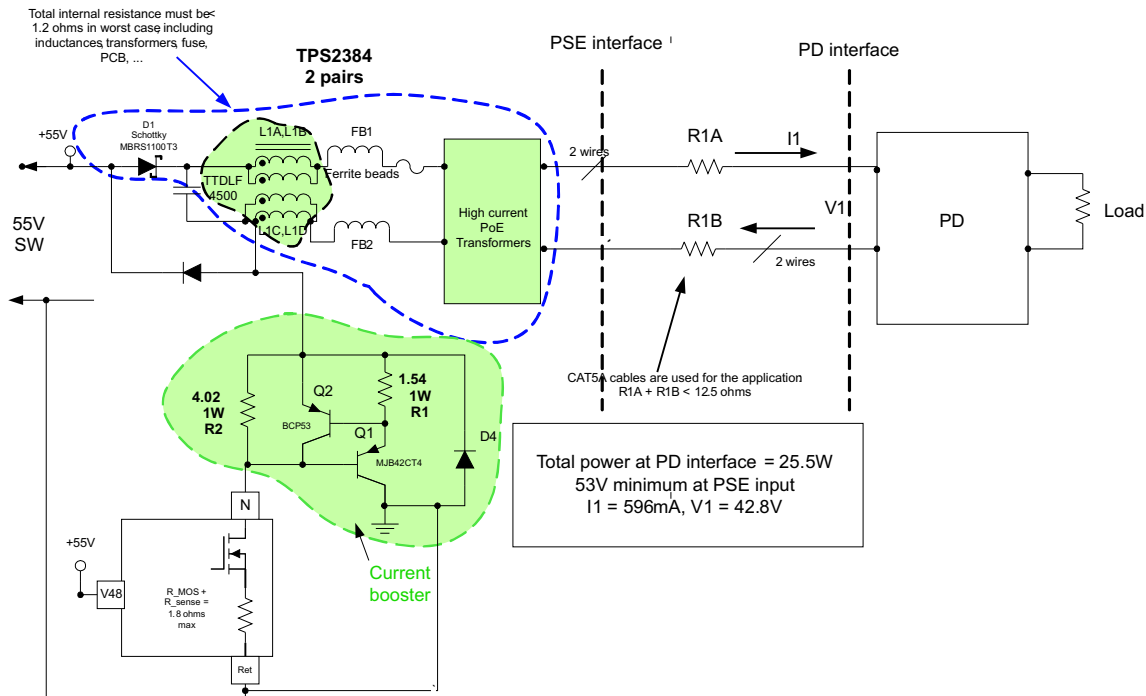


Figure 2. Diagram of Two-Pairs Solution for 25-W PD, Minimum Worst Case

As can be seen, if the port current is greater than $V_{be_Q1}/R2$, then the voltage drop on R2 is high enough to allow Q1 to turn on and additional current flows through Q1, with some limitation imposed by Q2. The feedback through Q2 helps to improve the thermal behavior of the circuit. Then, the total current in the port is limited to the TPS2384 maximum allowed current plus the current in Q1:

$$I_{max} = I_{Lim_TPS2384} + V_{be_Q2}/R1$$

$$I_{cut} = I_{Cut_TPS2384} + V_{be_Q2}/R1$$

Analysis and simulations indicate that this circuit provides a minimum guaranteed current greater than 600 mA. In so doing, and considering the losses in Cat-5 cable and the PSE, the minimum power available at the PD's input increases substantially from 13 W to 25.5 W.

The benefits of such a solution include:

- Power provided at PD input increases by 96% versus a standard PoE system
- Operating voltage of 53 V to 57 V is within the 802.3af standard voltage range of 44 V to 57 V.
- Power provided over two pairs only
- Existing Cat-5 cable installations are still useable, but care must be taken to ensure that the maximum-rated cable temperature is not exceeded; this includes the ambient temperature along with the cable temperature rise due to dissipation in the wires. Also, connectors must be selected according not only to their current-carrying capability, but also their mating/unmating resilience (capacitive and inductive loads).

The characteristics of such a system are:

- Limited power management is achievable with the MSP430 microcontroller (there is no provision for precise port voltage/current measurement).
- Limited compatibility with the 802.3af standard PDs. PD detection capability.
- High-current capability magnetic components are necessary.
- In PoE applications, good design rules must be followed in order to ensure current balancing between wires within each pair, especially important at this current level. In some cases, resistor-capacitor ballast networks must be installed. Additionally, imbalance may arise due to a faulty wire connection on the cable.
- The minimum worst-case I_{CUT} level is specified to be no less than 600 mA.
- This extra power is based on the fact that the PD input current limit is not below 600 mA.
- Requires a tight-tolerance ($\pm 3.5\%$), 55-V power supply for this solution to work

Because the operating voltage is high, the 55-V overvoltage protection (OVP) function must be disabled by the MSP430 software. The TPS2384 allows disabling both the OVP and the Port Under Voltage Protection on all four ports simultaneously. The 55-V power supply must incorporate OVP to ensure that any power supply failure does not propagate to the PSE, the loads, or the end-users (as in any standard PoE application).

4 Analysis of the Current Booster Circuit

As previously noted, this circuit provides extra current in addition to what is available through the TPS2384.

Analysis indicates that the circuit is thermally stable. This is because when the temperature of Q1 increases, the reaction could be that V_{be_Q1} decreases, which could result in more voltage in R1 and hence more current. However, if Q2 is thermally matched with Q1, its V_{be} also decreases, reducing the voltage across R1 so that the current and dissipation on R1, R2, and Q1 also decrease. The result is that the dissipation of the booster circuit (R1, R2, Q1, Q2) decreases as temperature increases; this is opposite to the TPS2384 power switch which dissipates more at higher temperatures.

The BCP53 transistor was used for the analysis. Its characteristics are: 1.5 A, 80 V, and SOT223 with metal tab.

The analysis was done by assuming the worse-case power switch resistance of the TPS2384 (1.8 Ω). Note that because of high instantaneous power during a short-circuit condition at port output or during an inrush on a large capacitor, a high-power package like the D2PAK is highly recommended for Q1. An example is the MJB42CT4, rated at 6 A and 100 V, and can handle high instantaneous power.

Using the BCP53 model and values (see [Figure 2](#)), Pspice analysis indicates:

- At hot temperature ($T_{j_BCP53} = 110^{\circ}\text{C}$): I_{cut} total of 650 mA if $I_{cut_2384} = 350$ mA
- At hot temperature: I_{cut} total of 695 mA if $I_{cut_2384} = 400$ mA
- At cold temperature (-40°C): I_{cut} total of 720 mA if $I_{cut_2384} = 350$ mA
- At cold temperature (-40°C): I_{cut} total of 860 mA if $I_{cut_2384} = 400$ mA

The simulation indicates that the dissipation is maximum at cold temperature. The variations in current limit behavior can be explained by the V_{be} change with temperature and collector current and by the I_{cut_2384} variations.

At hot temperature, the dissipation is minimum, calculated as follows: when $I_{cut_2384} = 400$ mA, then dissipation is 0.243 W on R2, 0.148 W on R1, 0.35 W on Q1, and 0.153 W on Q2, for a total of 0.894 W. However, it is assumed that Q1 and Q2 are assembled in close proximity to enhance thermal coupling between these two transistors.

At ambient temperature and TPS2384 power switch resistance of 1.2 Ω and $I_{cut_2384} = 380$ mA, dissipation is 0.4 W on R2, 0.23 W on R1, 0.44 W on Q1, and 0.076 W on Q2, for a total of 1.15 W. The total I_{cut} is then 771 mA. These values are used later for laboratory measurement comparisons. Also, $V_{be_Q1} = 0.675$ V and $V_{be_Q2} = 0.605$ V. Note that under the same conditions but at high temperature, these values change to 0.144 W, 0.233 W, 0.34 W, and 0.13 W, respectively, for a total of 0.847 W.

Similar analytical results have been obtained using the MJB42CT4 model for Q1.

5 Test of Current Booster Circuit

The assembly of the booster circuit provided enough copper surface for the dissipative components.⁽¹⁾ Three regions, each approximately 1.2 square inches, were used for that purpose. For these tests, the BCP53 was used for Q1, but no short-circuit test was performed.

At room temperature, the following results were obtained:

- Total current limit: 750 mA
- I_{R2} = 351 mA, P_{R2} = 0.35 W
- I_{R1} = 373 mA, P_{R1} = 0.21 W
- V_{ce_Q1} = 1.28 V, P_{Q1} = 0.48 W
- I_{limit} of TPS2384 of ~380 mA
- Ron of TPS2384 switch of ~ 1.23 Ω
- P_{Q2} = 41 mW
- V_{be_Q1} = 0.807 V
- V_{be_Q2} = 0.566 V
- Total additional dissipation: 1.08 W

These results compare favorably with the predictions.

Simple temperature tests also were performed. At hot temperatures, it was possible to lower the limit to approximately 726 mA, whereas at cold temperatures, it was increased to approximately 780 mA.

⁽¹⁾ Note: For this test, R2 = 3.9 Ω.

6 Thermal Considerations

In implementing this solution, some basic rules must be followed. First, sufficient copper surface is required for the dissipative components, particularly the TPS2384. If many of the TPS2384 ports are configured for high power, then a multilayer board is required with dissipative planes and good thermal contact to them with thermal vias. Appropriate use of the PowerPAD™ package of the TPS2384 is then necessary.

Also, Q1 (D2PAK) and Q2 must be physically located close together, and the trace layout must result in a good thermal matching between the two in order to facilitate V_{be} temperature tracking.

Finally, the layout must facilitate heat spreading on the PC board without neglecting other key constraints like ESD/EFT/surges immunity, EMC, safety, electrical performance, etc. Temperature measurements are also recommended to validate the thermal design.

7 Required High-Power Components

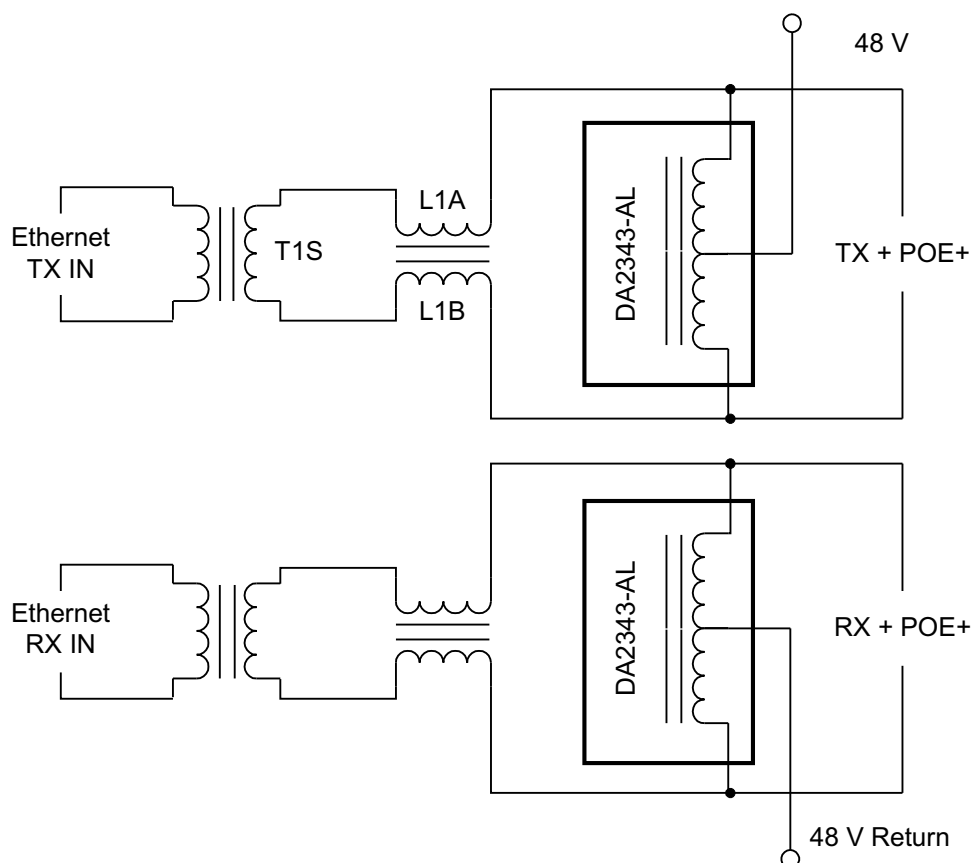


Figure 3. A Possible PoE Transformer Topology

For this high-current application, the following component changes are required versus the basic TPS2384 schematic (HPA109).

Ethernet Transformer Assembly. It is important that this assembly be compatible with the IEEE802.3af standard. It must be usable at 700 mA DC and be able to tolerate at least 20 mA (30 mA better) of imbalance without altering the Ethernet signals. Preferably, the topology chosen must be compatible with any Bob Smith terminations, or equivalent, between signal pairs. A few topologies are possible; one of these is illustrated in [Figure 3](#). In this example, the Coilcraft part DA2343-AL is used.

In this particular case, the DC bias current in the secondary of the Ethernet transformer is a specific percentage of the DC imbalance in DA2343-AL. This percentage is the ratio of one-half (0.08 Ω) of DA2343-AL total resistance over the total secondary resistance of each Ethernet transformer (through L1A, T1S, and L1B, for example). In order to keep the DC bias current acceptably low for the transformer (usually non-PoE must handle at least 6 mA but that includes the data pattern asymmetry), that ratio has to be low enough.

PSE Common Mode Choke. Use the TTDLF4500 as indicated in [Figure 2](#).

Schottky Diode D1. MBRS1100T3 or similar

Fuse of Appropriate Current Rating.

RJ45 Connector. Examples are the SS-6488S-A-PG4-BA-50 (one port) and the SS-73100-047 (16 ports) from Bell Stewart.

Transistors Q1 and Q2. Q1 must be a 100-V transistor capable of handling 600 mA and able to withstand port ESD stress. Current gain is not important. Q2 must be capable of a 600-mA current. An MJB42CT4 transistor could be used for Q1, and a BCP53 transistor could be used for Q2.

Diode D4. This diode must be ultrafast (e.g., 1-ns forward recovery time) with 100-V capability and 30-A, 8/20- μ s surge capability. Its forward voltage drop must be <3 V at that current. For example, a Schottky diode, like the MBRS1100T3, could be used.

8 Conclusion

For higher power close to 25 W on two pairs (Cat-5 cable), a simple solution based on the combination of a close-tolerance power supply with a current booster is possible, by using the TPS2384. Available power then can be increased by 96%.

9 References

1. *TPS2384 User's Guide* ([SLVU126](#))
2. *High-Power PoE PD Using TPS2375/77-1* application report ([SLVA225](#))
3. *Power over Ethernet Requirements and Limitations due to the Cabling System*, J. H. Walling, Ph.D., walling_1_0905.pdf presented to IEEE802.3af, September 2005.

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