# TMS320DM335/DM355 DSP Power Reference Design PR742

## 1 Features

- Provides sequenced core and input/output voltages from 2-V to 5.5-V input voltages
- Suitable for Li-ion and 3 AA battery inputs
- $\overline{\text{RESET}}$ delay fixed at 20 ms, but can be adjusted
- Optimized for cost and efficiency

## 2 Introduction

This reference design is for the TMS320DM335/DM355 digital signal processor (DSP) and accounts for voltage, current, and sequencing requirements. The operating input voltage ranges from 2 V to 5.5 V for Li-ion batteries and 3 AA batteries. This design also can work with 2 AA batteries with some limitations. The design is optimized for efficiency over the full range of operation and low overall cost.

## 3 Requirements

The TMS320DM335/DM355 DSP requires three input rails, which are outlined in Table 1.

**Table 1. Voltage Input Requirements**

| Power Rail | Voltage (V) | Current (mA) | Power-up Sequence | Power-down Sequence |
|---|---|---|---|---|
| Vout 1 | 1.3 | 210 | First | Second or third |
| Vout 2 | 1.8 | 30 | Second | Second |
| Vout 3 | 3.3 | 95 | Second or third | First |

To avoid corrupting data or damaging the DSP, the rails must power up and power down in the proper order. On power up, the 1.3 V comes up first, then 1.8 V and 3.3 V together, or 1.8 V, then 3.3 V. Power down is the exact opposite sequence. The 1.8 V and 3.3 V come down together, then 1.3 V, or in the order 3.3 V, 1.8 V, and then 1.3 V.

## 4 Implementation

This design achieves the three voltages needed to power the TMS320DM335/DM355 with the correct sequencing using two switching converters (TPS62240 and TPS63001), one low dropout (LDO) linear regulator (TPS72118), and two supply voltage supervisors (SVS) (TPS3808-01 and TPS3808G33). The block diagram of the design is shown in Figure 1. See the schematic for further detail.

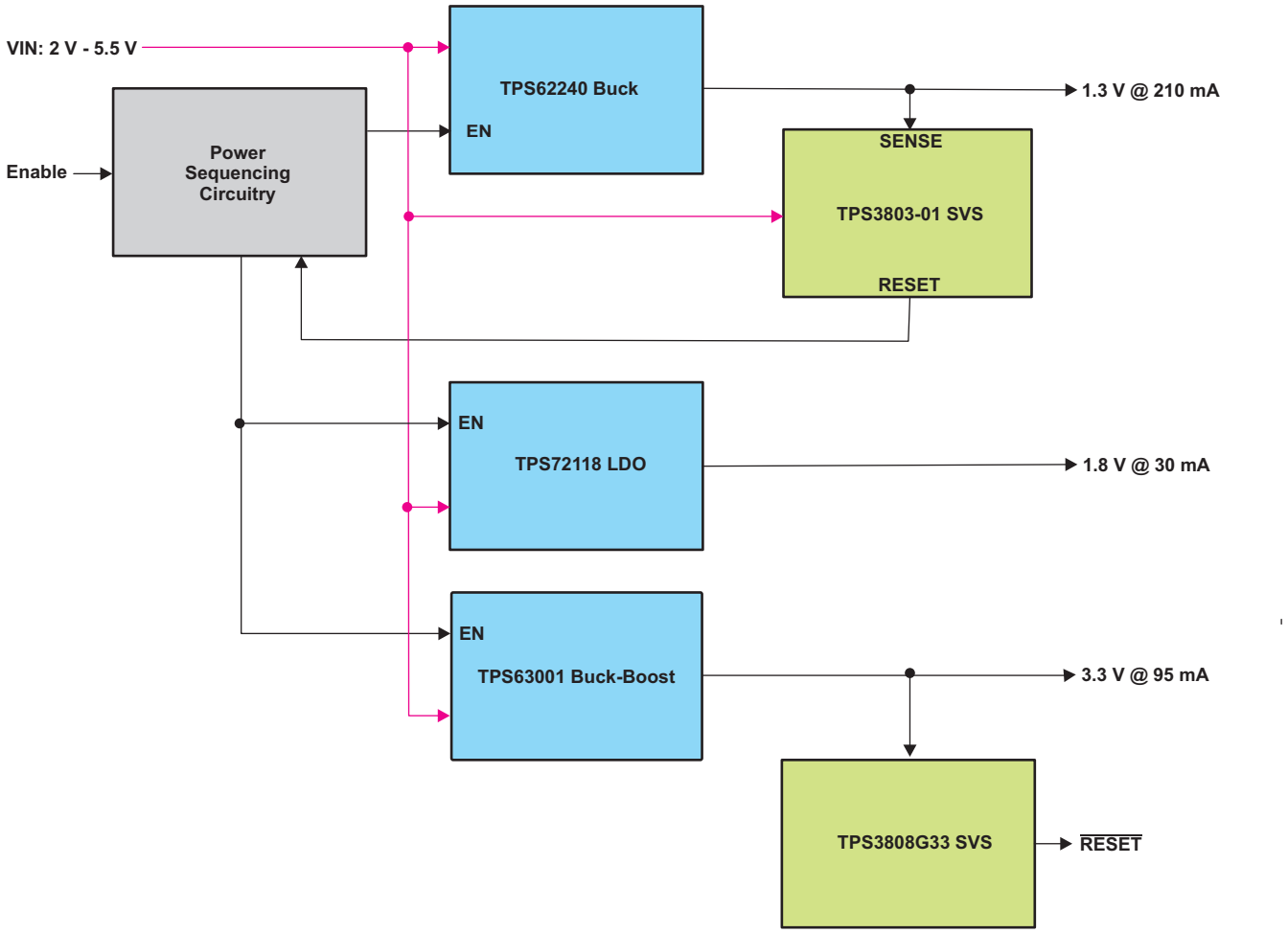


**Figure 1. Block Diagram of Power Design**

## 4.1 Power Up

When ENABLE goes high (high is considered 1 V to VIN), the TPS62240 is enabled first and the 1.3-V rail comes up. Once the 1.3 V goes above the 1.226-V voltage threshold of the TPS3808-01 SVS, the open-drain RESET pin is pulled up to VIN. This pulls the ENABLE pins high on the TPS72448 and TPS63001. The 1.8-V rail comes up first and then the 3.3-V rail. The TPS2808G33 SVS is placed on the 3.3-V rail because it is the last rail to come up. The threshold voltage for the TPS2808G33 is 3.07 V, and the delay is set to 20 ms in this design.

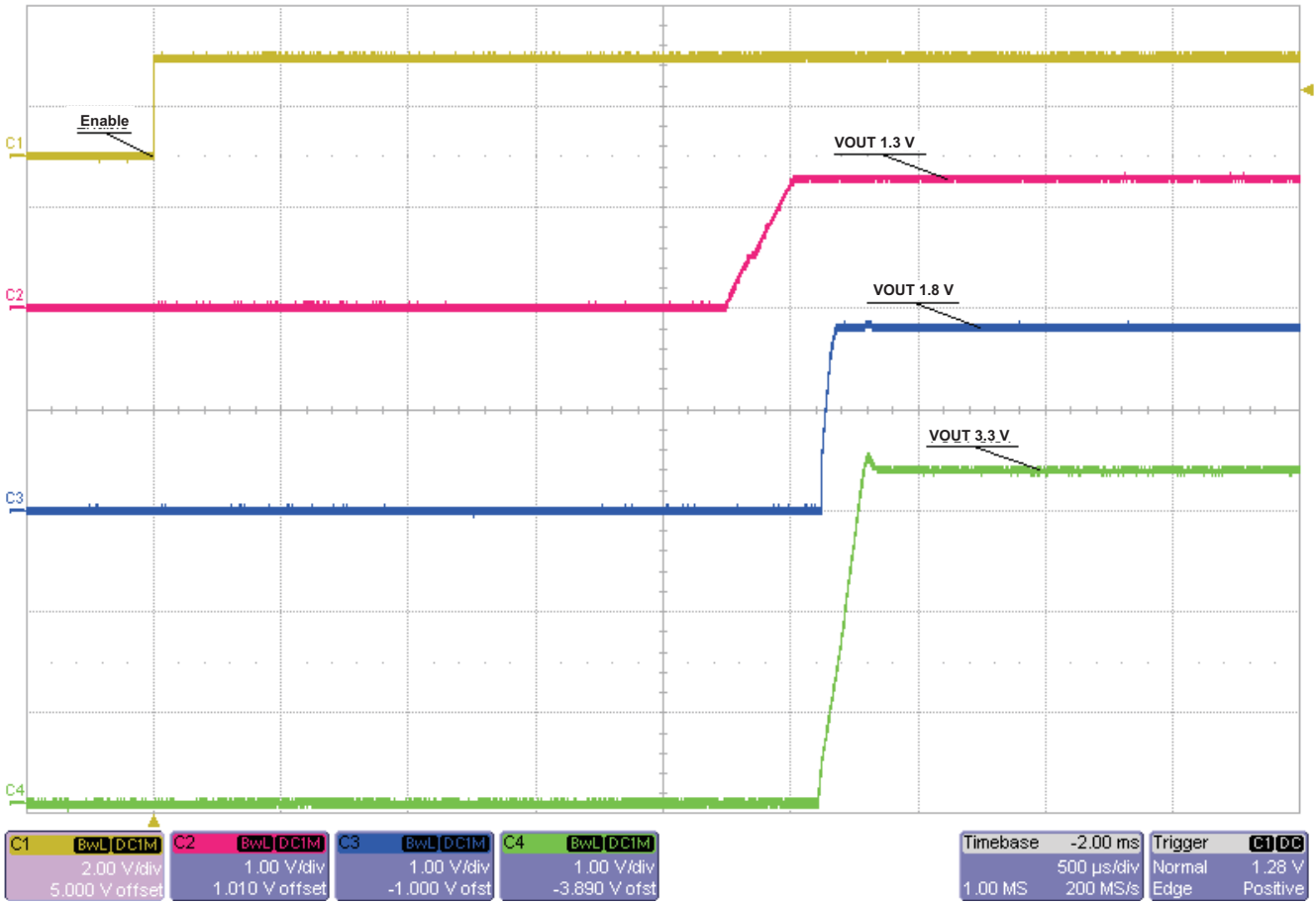


**Figure 2. Power Up With 2-V Input and ENABLE Voltage**

Once ENABLE is pulled high, the 1.3-V rail comes up and the 1.8 V and 3.3 V come up together 200 s later.

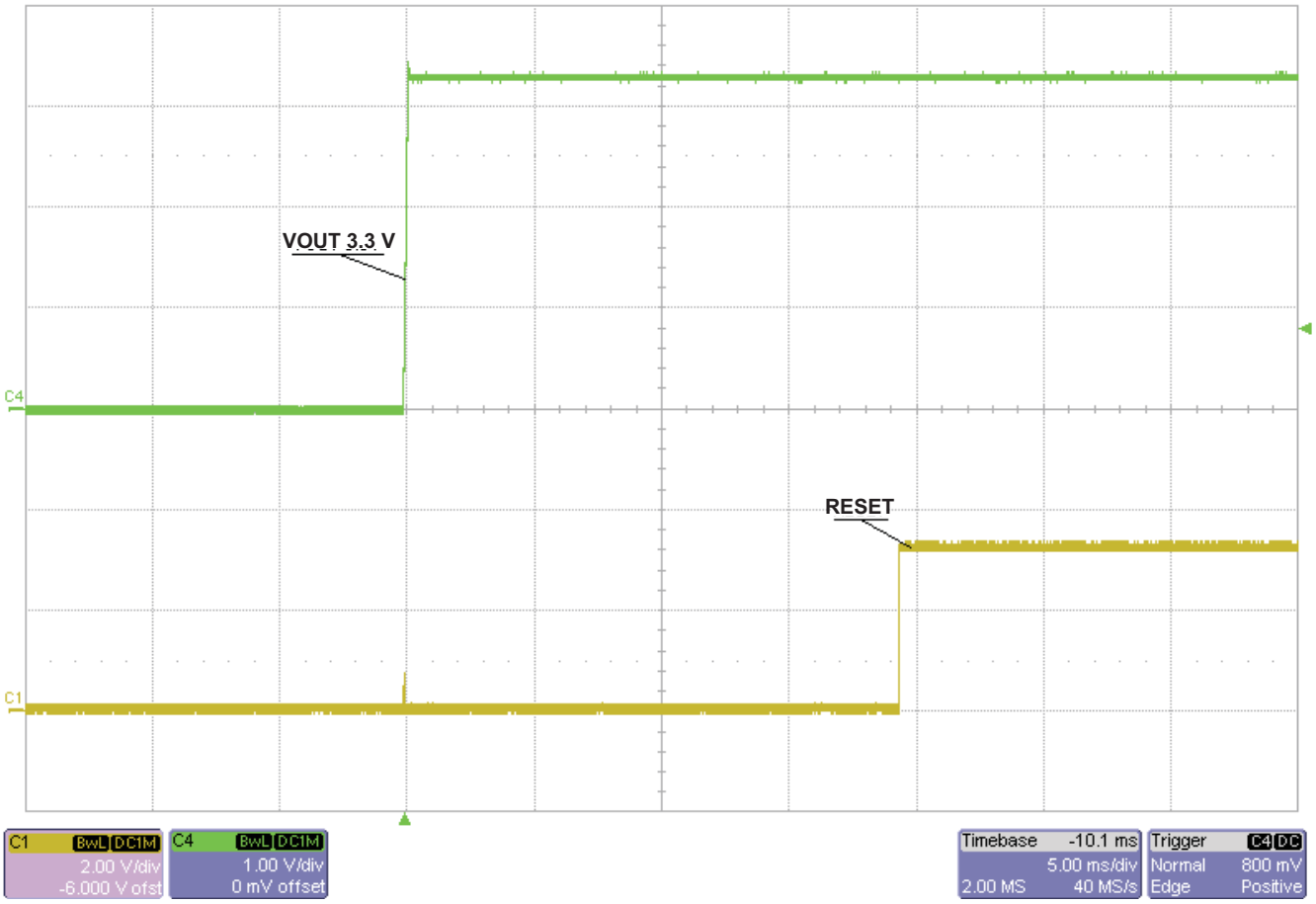


**Figure 3. $\overline{\text{RESET}}$ Pin of TPS3808G33 Pulled High**

The $\overline{\text{RESET}}$ pin of TPS3808G33 that supervises the 3.3-V rail is pulled high about 20 ms after the 3.3-V rail is up. Input and ENABLE voltages are 2 V.

## 4.2 Power Down

When ENABLE is pulled low (low is considered 0 V to 0.4 V), the ENABLE pins on the TPS72118 and TPS63001 are pulled low immediately, letting the 1.8-V and 3.3-V rails fall first. An RC circuit with a 5-ms time constant on the ENABLE of the TPS62240 keeps the 1.3-V rail up longer. The delay between ENABLE going low and the 1.3-V rail falling depends on the ENABLE voltage. With the ENABLE voltage between 1 V and 5.5 V, it is 513 ms.

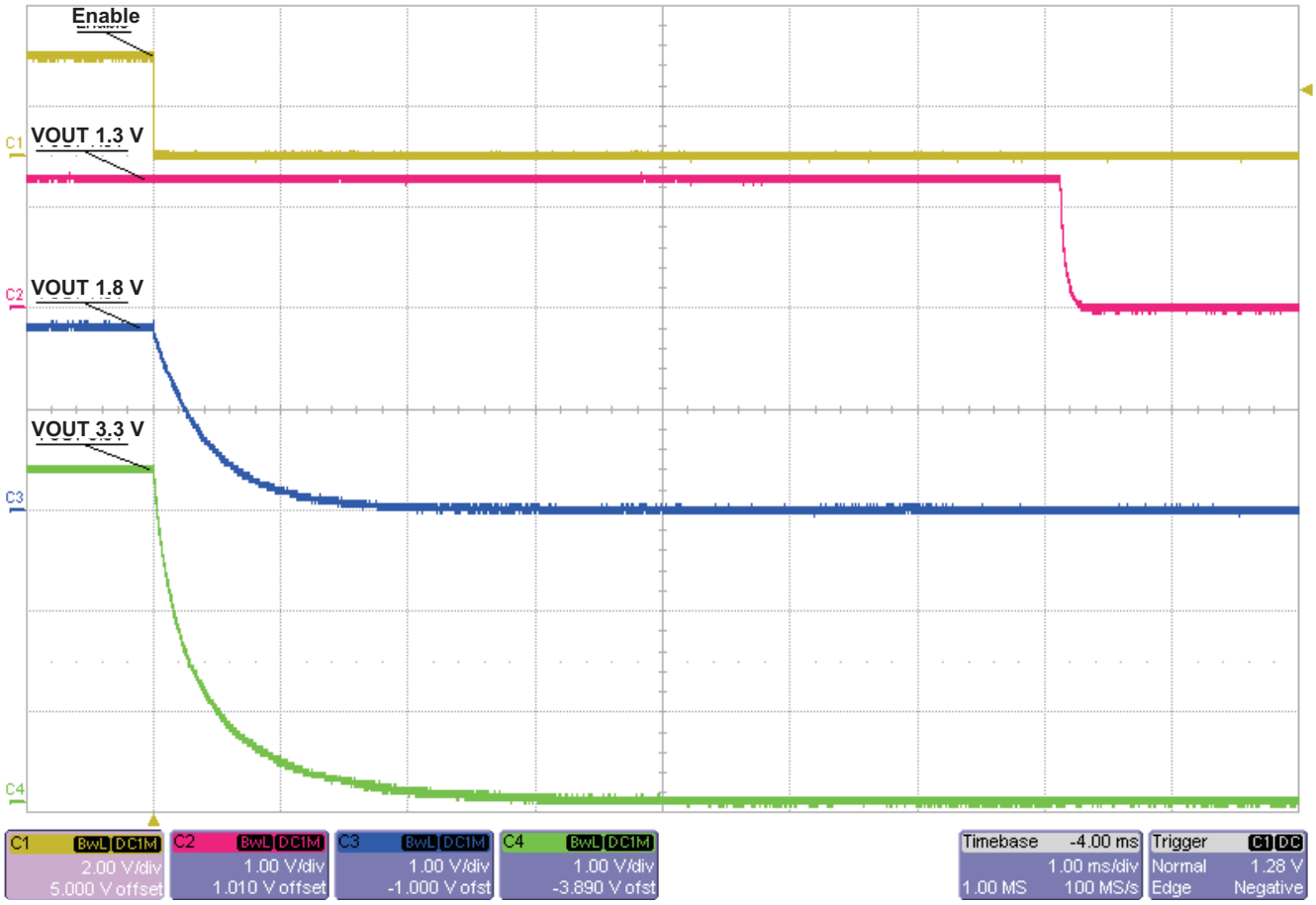


**Figure 4. Power Down With 2-V Input and ENABLE Voltage**

Once ENABLE is pulled low, the 1.8 V and 3.3 V come down together and the 1.3-V rail comes down 7 ms later.

## 4.3 Output Current

Depending on the DSP and application needs, you may need more or less current than the values given in the requirements. The maximum output currents for each rail are shown in Table 2.

**Table 2. Maximum Output Current**

| Output Voltage (V) | System Input Voltage (V) | Maximum Output Current (mA) |
|---|---|---|
| 1.3 | 2 - 2.3 | 150 |
| | 2.3 - 5.5 | 300 |
| 1.8 | 2 - 5.5 | 150 |
| 3.3 | 2 - 3.3 | 800 |
| | 3.3 - 5.5 | 1200 |

Note that with VIN between 2 V and 2.3 V, only 150 mA can be attained from the 1.3-V source. However, tests at VIN = 2 V met the current and sequencing requirements outlined in the requirements section. If you plan to run the system off 2 AA batteries (1.8-V to 3-V range), consider using 3 AAA batteries (2.7-V to 4.5-V range) or Li-ion batteries (3-V to 4.2-V range). Otherwise, additional testing will be required.

### 4.4 Reset Delay Time

The reset delay time in this design is set to 20 ms, but the TPS3808G33 has a programmable delay time that can be programmed anywhere between 1.25 ms and 10 s. See the *TPS3808G33* data sheet for a detailed explanation.

## 5 Additional Waveforms

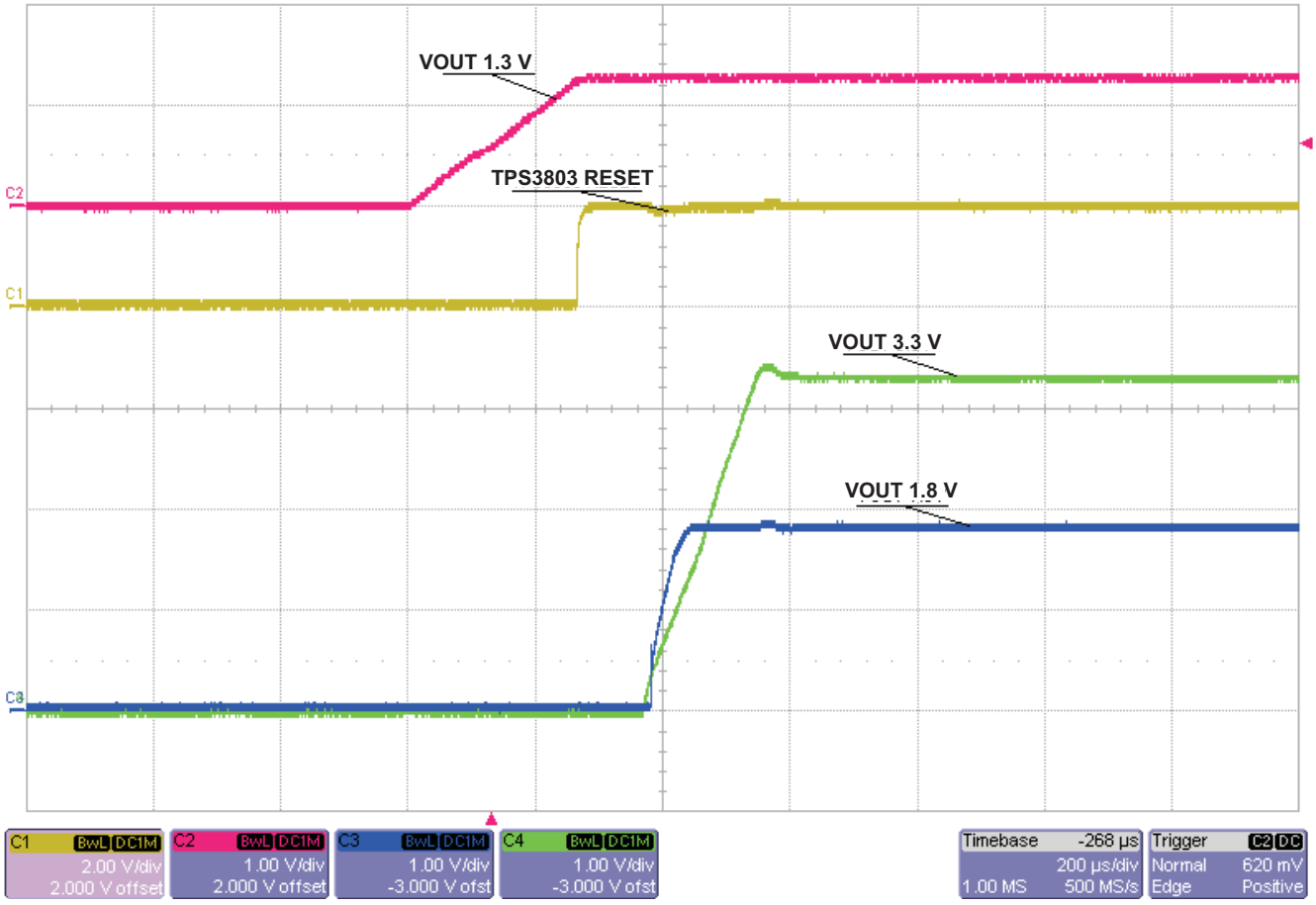


**Figure 5. Power-Up Sequence Showing TPS3803-01 RESET Signal**

In the power-up sequence of Figure 5, the TPS380-01 RESET signal enables the 1.8-V and 3.3-V rails. The input and ENABLE voltages are 2 V.

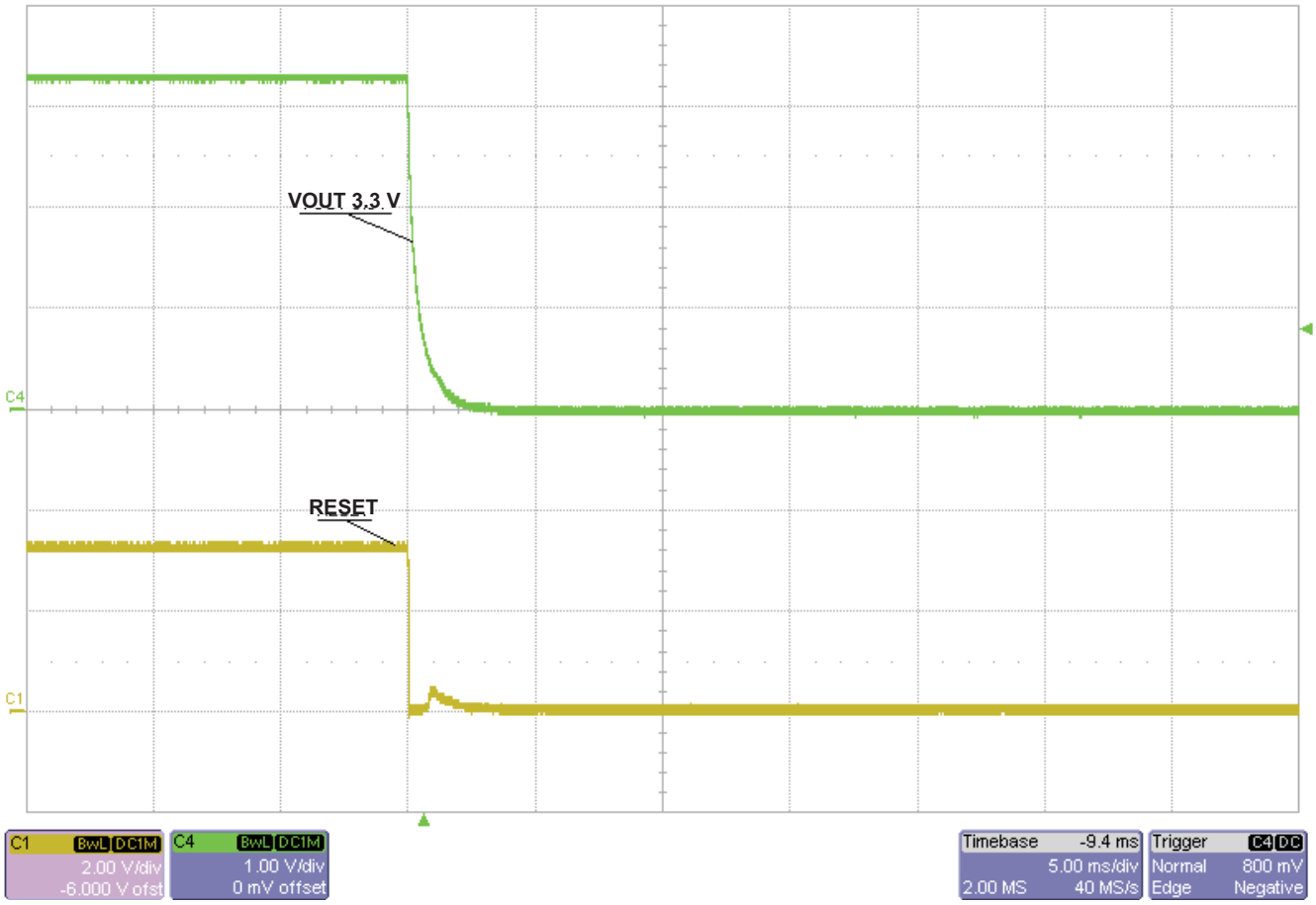


**Figure 6. Power-Down Sequence Showing TPS3808G33 $\overline{\text{RESET}}$ Pin Signal**

In Figure 6, the input and ENABLE voltages are 2 V.

## 6 Data Sheet Web Links

| Part Number | Datasheet Web Link |
|---|---|
| TPS62240 | http://www.ti.com/lit/gpn/tps62240 |
| TPS3803-01 | http://www.ti.com/lit/gpn/tps3803-01 |
| TPS72118 | http://www.ti.com/lit/gpn/tps72118 |
| TPS63001 | http://www.ti.com/lit/gpn/tps63001 |
| TPS3808G33 | http://www.ti.com/lit/gpn/tps3808g33 |

# 7 Schematic and Bill of Materials

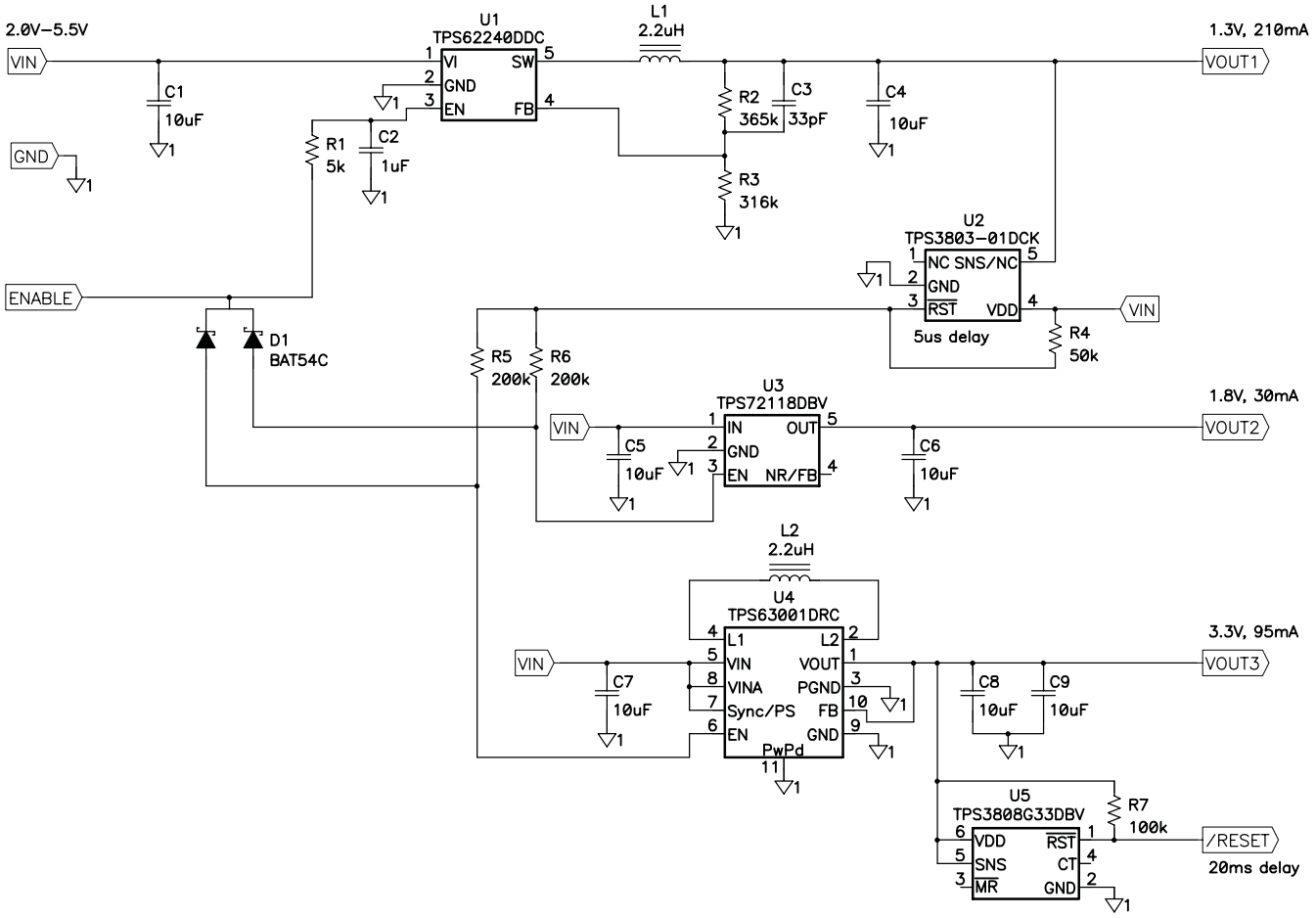


**Figure 7. Schematic**

**Table 3. Bill of Materials**

| Count | RefDes | Value | Description | Size | Part Number | MFR |
|---|---|---|---|---|---|---|
| 7 | C1, C4C9 | 10 F | Capacitor, Ceramic, 6.3V, X5R, 20% | 0603 | GRM188R60J106ME47D | Murata |
| 1 | C2 | 1 F | Capacitor, Ceramic, 50V, C0G, 5% | 0603 | C1608C0G1H220J | TDK |
| 1 | C3 | 33 pF | Capacitor, Ceramic, 50V, C0G, 5% | 0603 | C1608C0G1H220J | TDK |
| 1 | D1 | | Diode, Dual Schottky, 200-mA, 30-V | SOT23 | BAT54C | Vishay-Liteon |
| 2 | L1, L2 | 2.2 H | Inductor, SMT, 1.5A, 110 milliohm | 0.118 0.118 | LPS3015-222ML | Coilcraft |
| 1 | R1 | 5k | Resistor, Chip, 1.16W, 1% | 0603 | Std | Std |
| 1 | R2 | 365k | Resistor, Chip, 1.16W, 1% | 0603 | Std | Std |
| 1 | R3 | 316k | Resistor, Chip, 1.16W, 1% | 0603 | Std | Std |
| 1 | R4 | 50k | Resistor, Chip, 1.16W, 1% | 0603 | Std | Std |
| 2 | R5, R6 | 200k | Resistor, Chip, 1.16W, 1% | 0603 | Std | Std |
| 1 | R7 | 100k | Resistor, Chip, 1.16W, 1% | 0603 | Std | Std |
| 1 | U1 | | IC, 2.25 MHz, 600 mA Step-Down Converter | SOT23-5 | TPS62240DDC | TI |
| 1 | U2 | | IC, Voltage Detector | SOP-5 (DCK) | TPS3803-01DCK | TI |
| 1 | U3 | | IC, 150mA, Low Iq, Wide Bandwidth, LDO Linear Regulators | SC70 | TPS71718DBV | TI |
| 1 | U4 | | IC, High Efficiency Single Inductor Buck-Boost Converter with 1.2A Switches | QFN10 | TPS63000DRC | TI |
| 1 | U5 | | IC, Low Quiescent Current, Programmable vv-V, Delay Time: 1.25ms to 10s | SOT23-6 | TPS3808G33DBV | TI |

**Table 3. Bill of Materials (continued)**

| Count | RefDes | Value | Description | Size | Part Number | MFR |
|---|---|---|---|---|---|---|
| Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed. | | | | | | |
| 2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable. | | | | | | |
| 3. These assemblies must comply with workmanship standards IPC-A-610 Class 2. | | | | | | |
| 4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components. | | | | | | |

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